

TOSHIBA Multichip Discrete Device

HN7G01FE

Power Management Switch Applications

Driver Circuit Applications

Interface Circuit Applications

- Q1 (transistor): 2SA1955 equivalent
- Q2 (MOSFET): SSM3K03FE equivalent

Q1 (Transistor) Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	-15	V
Collector-emitter voltage	V_{CEO}	-12	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-400	mA
Base current	I_B	-50	mA

Q2 (MOSFET) Maximum Ratings (Ta = 25°C)

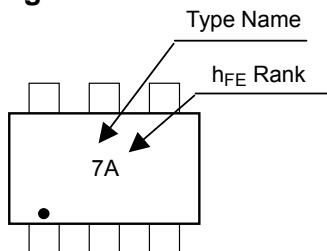
Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GSS}	10	V
Drain current	I_D	50	mA

Q1, Q2 Common Ratings (Ta = 25°C)

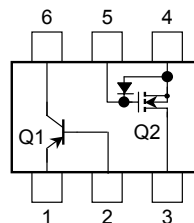
Characteristic	Symbol	Rating	Unit
Power dissipation	P (Note 1)	100	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	-55~125	°C

Note 1: Total rating

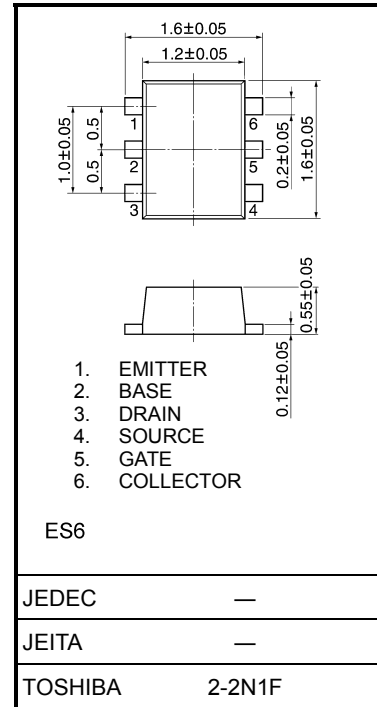
Marking



Pin Assignment (top view)



Unit: mm



Weight: 0.003 g (typ.)

Q1 (Transistor) Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cutoff current	I_{CBO}	$V_{CB} = -15\text{ V}, I_E = 0$	—	—	-0.1	μA
Emitter cutoff current	I_{EBO}	$V_{EB} = -5\text{ V}, I_C = 0$	—	—	-0.1	μA
DC current gain	h_{FE} (Note 2)	$V_{CE} = -2\text{ V}, I_C = -10\text{ mA}$	300	—	1000	
Collector-emitter saturation voltage	$V_{CE(sat)}(1)$	$I_C = -10\text{ mA}, I_B = -0.5\text{ mA}$	—	-15	-30	mV
	$V_{CE(sat)}(2)$	$I_C = -200\text{ mA}, I_B = -10\text{ mA}$	—	-110	-250	
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = -200\text{ mA}, I_B = -10\text{ mA}$	—	-0.87	-1.2	V

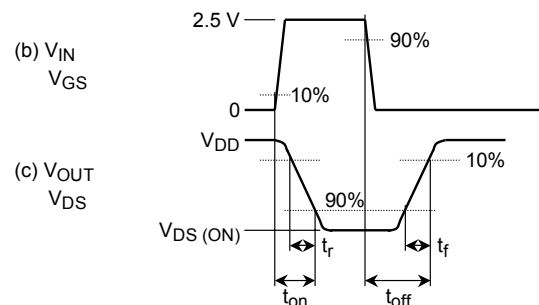
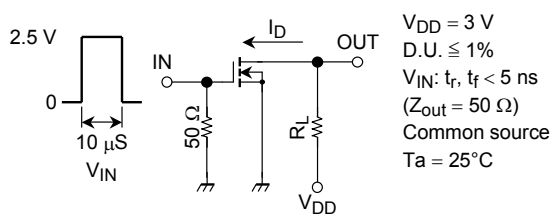
Note 2: h_{FE} classification A: 300~600, B: 500~1000

Q2 (MOSFET) Electrical Characteristics (Ta = 25°C)

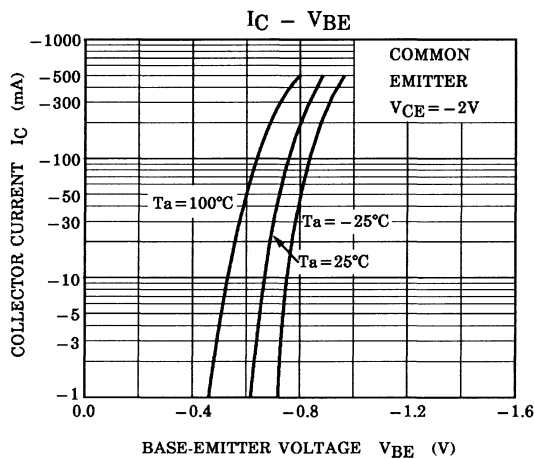
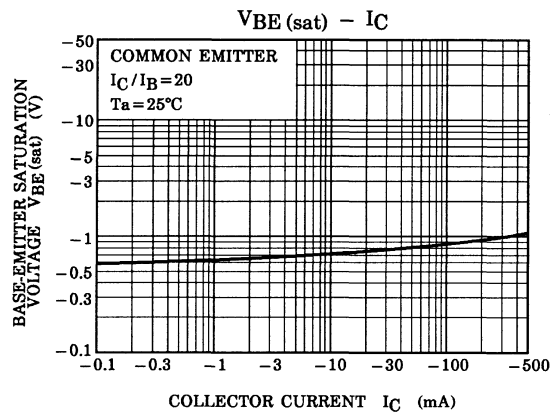
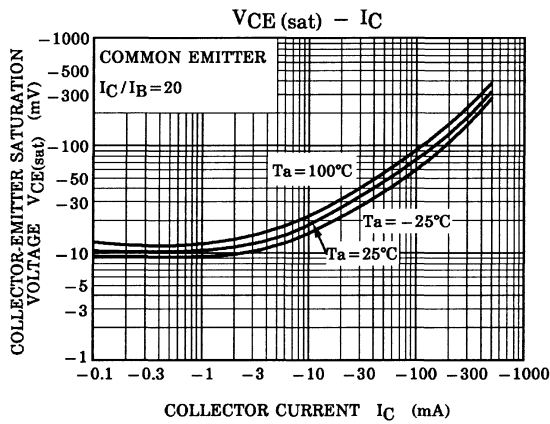
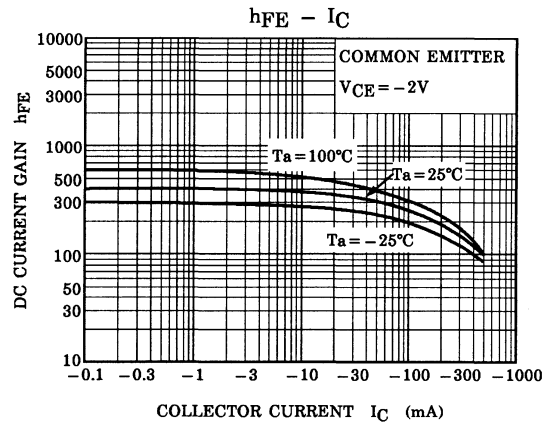
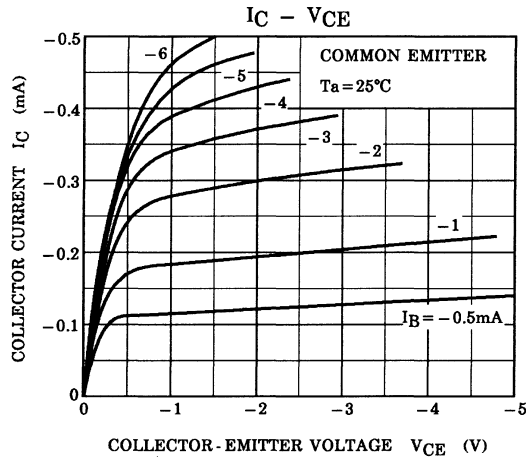
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	I_{GSS}	$V_{GS} = 10\text{ V}, V_{DS} = 0$	—	—	1	μA	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 100\text{ }\mu\text{A}, V_{GS} = 0$	20	—	—	V	
Drain cutoff current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0$	—	—	1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.7	—	1.3	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	25	50	—	mS	
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = 10\text{ mA}, V_{GS} = 2.5\text{ V}$	—	4	12	Ω	
Input capacitance	C_{iss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	11.0	—	pF	
Reverse transfer capacitance	C_{rss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	3.3	—	pF	
Output capacitance	C_{oss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	9.3	—	pF	
Switching time	Turn-on time	t_{on}	$V_{DD} = 3\text{ V}, I_D = 10\text{ mA}, V_{GS} = 0\sim 2.5\text{ V}$	—	0.16	—	μs
	Turn-off time	t_{off}	$V_{DD} = 3\text{ V}, I_D = 10\text{ mA}, V_{GS} = 0\sim 2.5\text{ V}$	—	0.19	—	

Switching Time Test Circuit

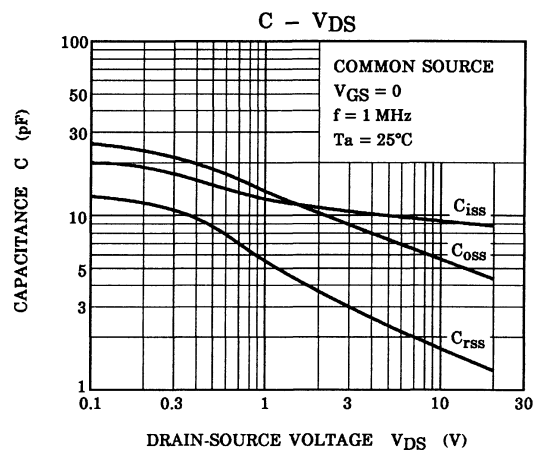
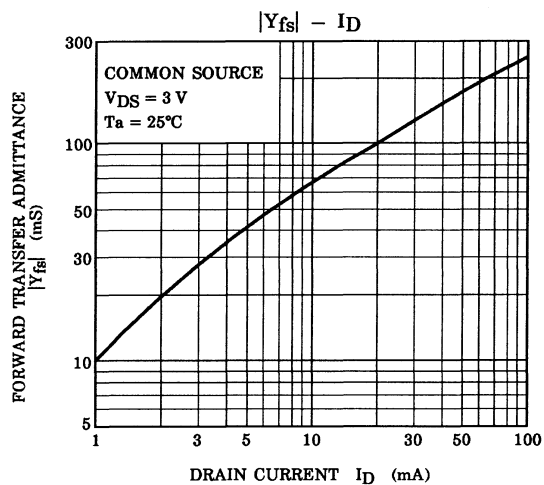
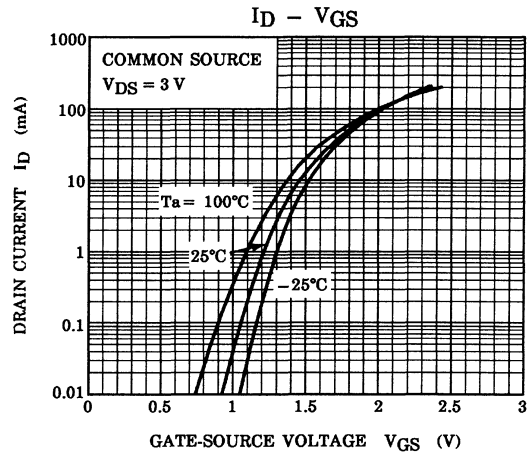
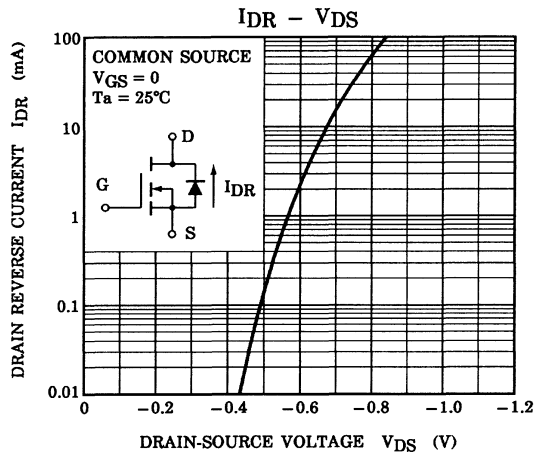
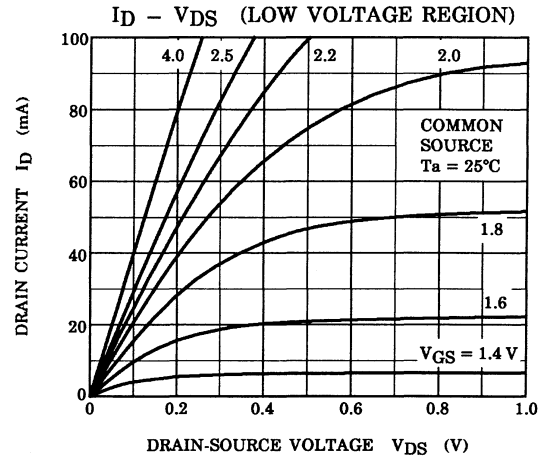
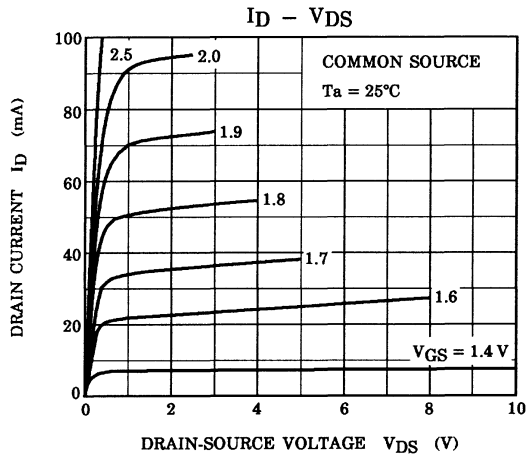
(a) Switching time test circuit



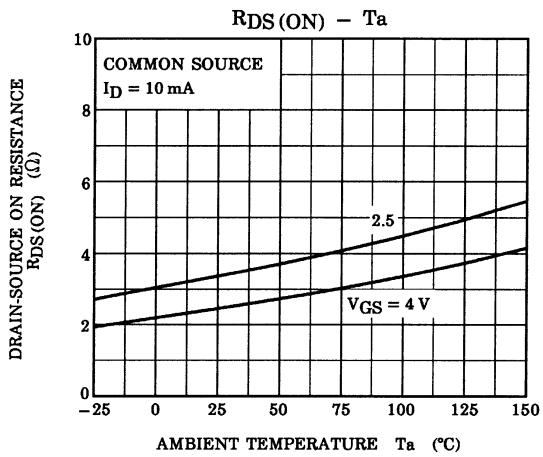
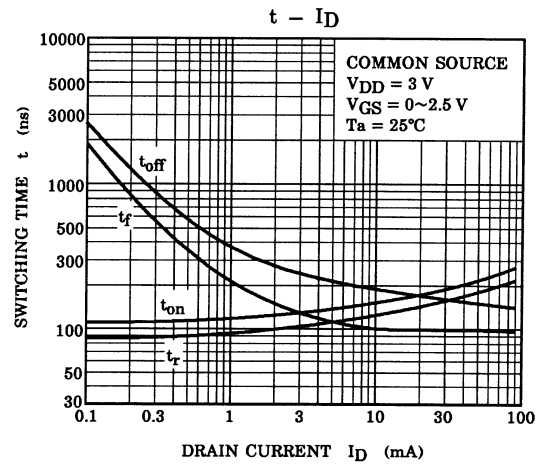
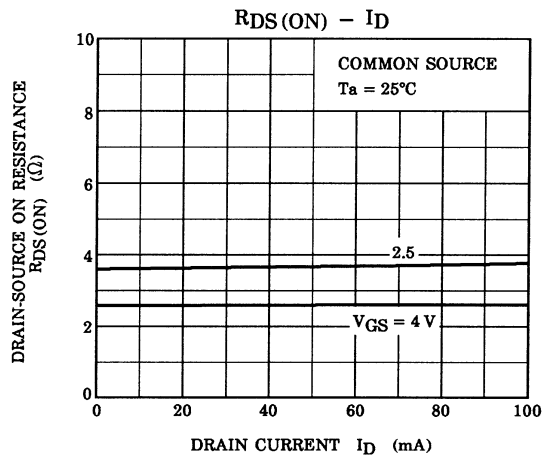
Q1 (Transistor)



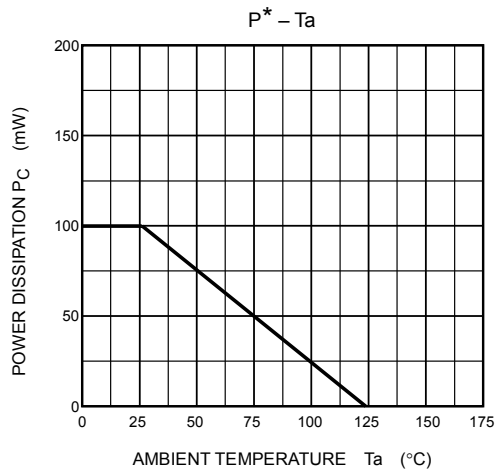
Q2 (S-MOS)



Q2 (S-MOS)



Q1, Q2 Common



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