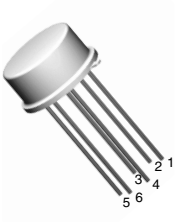
2N3810HR

Hi-Rel PNP dual matched bipolar transistor 60 V - 0.05 A

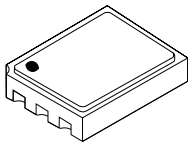
Features

BV_{CEO}	60 V
I_C (max)	0.05 A
H_{FE} at 10 V - 150 mA	> 150
Operating temperature range	-65°C to +200°C

- Hi-Rel PNP dual matched bipolar transistor
- Linear gain characteristics
- ESCC qualified
- European preferred part list - EPPL
- Radiation level: lot specific total dose contact marketing for specified level

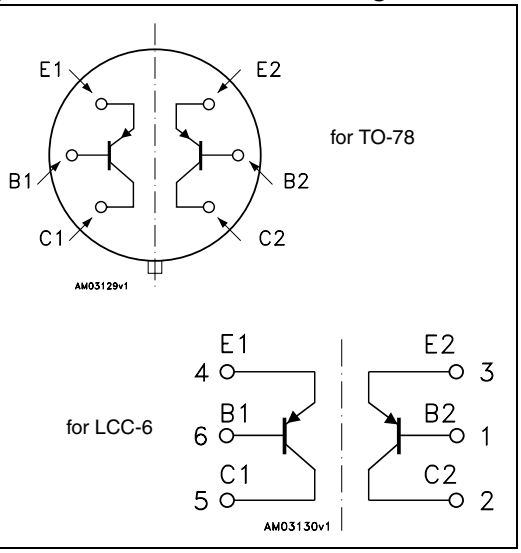


TO-78



LCC-6

Figure 1. Internal schematic diagram



Description

The 2N3810HR is a silicon planar epitaxial PNP transistor in TO-78 and LCC-6 packages. It is specifically designed for aerospace Hi-Rel applications and ESCC qualified according to the 5207-005 specification. In case of conflict between this datasheet and ESCC detailed specification, the latter prevails.

Table 1. Device summary

Order codes	Packages	Lead finish	Marking	Type	EPPL	Packaging
2N3810HR	TO-78	Gold Solder Dip	520700501 520700502	ESCC Flight		Strip pack
2N3810T1	TO-78	Gold	2N3810T1	Engineering model		Strip pack
SOC3810	LCC-6	Gold	SOC3810	Engineering model		Waffle pack
SOC3810HRB	LCC-6	Gold Solder Dip	520700507 520700509	ESCC Flight	Yes	Waffle pack

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage (I_E = 0)	-60	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	-60	V
V_{EBO}	Emitter-base voltage (I_C = 0)	-5	V
I_C	Collector current	-50	mA
P_{TOT}	Total dissipation at $T_{amb} \leq 25$ °C		
	for 2N3810HR (1)	0.5	W
	for 2N3810HR (2)	0.6	W
	for SOC3810HRB (1) (3)	0.6	W
	for SOC3810HRB (2) (3)	1.2	W
	Total dissipation at $T_c \leq 25$ °C		
	for 2N3810HR (1)	0.5	W
	for 2N3810HR (2)	0.6	W
T_{STG}	Storage temperature	-65 to 200	°C
T_J	Max. operating junction temperature	200	°C

1. One section.
2. Both sections.
3. When mounted on a 15 x 15 x 0.6 mm ceramic substrate.

Table 3. Thermal data for through-hole package

Symbol	Parameter		Value	Unit
R_{thJC}	Thermal resistance junction-case (1)	max	350	°C/W
	Thermal resistance junction-case (2)	max	292	°C/W
R_{thJA}	Thermal resistance junction-ambient (1)	max	350	°C/W
	Thermal resistance junction-ambient (2)	max	292	°C/W

1. One section.
2. Both sections.

Table 4. Thermal data for SMD package

Symbol	Parameter		Value	Unit
R_{thJA}	Thermal resistance junction-ambient (1)(3)	max	292	°C/W
	Thermal resistance junction-ambient (2)(3)	max	146	°C/W

1. One section.
2. Both sections.
3. When mounted on a 15 x 15 x 0.6 mm ceramic substrate.

2 Electrical characteristics

T_{case} = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector-base cut-off current (I_E = 0)	V_{CB} = -50 V V_{CB} = -50 V T_C = 150 °C			-10 -10	nA µA
I_{EBO}	Emitter-base cut-off current (I_C = 0)	V_{EB} = -4 V			-20	nA
$V_{(BR)CBO}$	Collector-base breakdown voltage (I_E = 0)	I_C = -10 µA	-60			V
$V_{(BR)CEO}$ (1)	Collector-emitter breakdown voltage (I_B = 0)	I_C = -10 mA	-60			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = -10 µA	-5			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = -100 µA I_B = -10 µA I_C = -1 mA I_B = -100 µA			-0.2 -0.25	V V
$V_{BE(sat)}$ (1)	Base-emitter saturation voltage	I_C = -100 µA I_B = -10 µA I_C = -1 mA I_B = -100 µA			-0.7 -0.8	V V
h_{FE} (1)	DC current gain	I_C = -10 µA V_{CE} = -5 V I_C = -100 µA V_{CE} = -5 V I_C = -500 µA V_{CE} = -5 V I_C = -1 mA V_{CE} = -5 V I_C = -10 mA V_{CE} = -5 V I_C = -100 µA V_{CE} = -5 V T_{amb} = -55 °C	100 150 150 150 125 60		 450 450 450 	
h_{FE2-1} / h_{FE2-2}	DC current ratio comparison	I_C = -100 µA V_{CE} = -5 V	0.91		1.1	
h_{FE2-1} / h_{FE2-2}	DC current ratio comparison	I_C = -100 µA V_{CE} = -5 V T_{amb} = -55 °C to +125 °C	0.85		1.18	
$\Delta \lvert V_{BE1} - V_{BE2} \rvert$	Base-emitter voltage differential	V_{CE} = -5 V I_C = -10 µA V_{CE} = -5 V I_C = -100 µA V_{CE} = -5 V I_C = -10 mA			5 3 5	mV mV mV
$\Delta \lvert V_{BE1} - V_{BE2} \rvert$	Base-emitter voltage differential	V_{CE} = -5 V I_C = -100 µA T_{amb} = -55 °C to +25 °C T_{amb} = +25 °C to +125 °C			 0.8 1	 mV mV
I_{Lk}	Leakage current between active devices	V = -50 V to E_2, B_2, C_2 V = 0 V to E_1, B_1, C_1			-5	µA
h_{fe}	Small signal current gain	V_{CE} = -5 V I_C = -10 mA f = 1 kHz	125			

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
h_{fe}	Small signal current gain	V_{CE} = -10 V I_C = -10 mA f = 1 kHz	150		600	
f_T	Transition frequency	I_C = -1 mA V_{CE} = -5 V	80		500	MHz
C_{obo}	Output capacitance (I_E = 0)	V_{CB} = -5 V 100 kHz ≤ f ≤ 1 MHz			6	pF
C_{ibo}	Input capacitance (I_C = 0)	V_{EB} = -0.5 V 100 kHz ≤ f ≤ 1 MHz			15	pF
h_{ie}	Input impedance	I_C = -1 mA V_{CE} = -10 V f = 1 kHz	3		30	kΩ
NF	Noise figure	V_{CE} = -5 V I_C = -200 µA R_S = 2 kΩ f = 100 Hz			7	dB
NF	Noise figure	V_{CE} = -5 V I_C = -200 µA R_S = 2 kΩ f = 1 kHz			3	dB
NF	Noise figure	V_{CE} = -5 V I_C = -200 µA R_S = 2 kΩ Bandwidth = 10 Hz to 15.7 kHz			3.5	dB

1. Pulsed duration = 300 µs, duty cycle ≤ 1.5%

3 Package mechanical data

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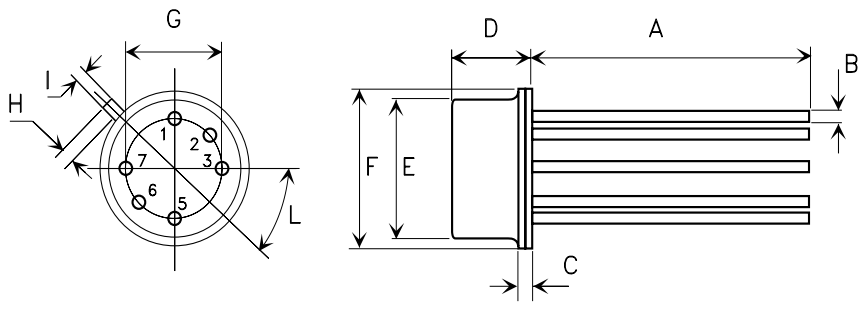
TO-78 mechanical data

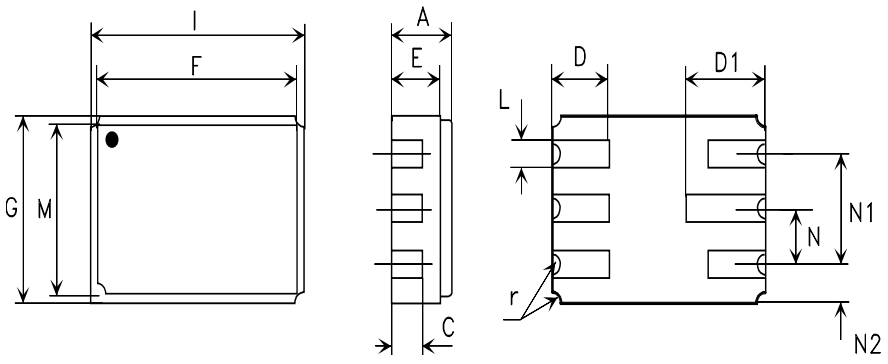
Dim.	mm		
	Min	Typ	Max
A	12.70		14.20
B			0.47
C	0.55		0.76
D			4.57
E			8.50
F			9.40
G		5.08	
H			0.86
I			1.00
L		45 °	



0015965E

Ceramic Leadless Chip Carrier 6 mechanical data

DIM.	mm.		
	MIN.	TYP	MAX.
A	1.53		1.96
C	0.78	0.89	0.99
D		1.65	
D1		2.28	
E		1.40	
F	5.75		5.95
G	4.15		4.50
I	6.05		6.30
L		0.63	
M	3.85		4.05
N		1.27	
N1		2.54	
N2		0.89	
r		0.23	



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4 Revision history

Table 6. Document revision history

Date	Revision	Changes
10-Dec-2008	1	Initial release
08-Jan-2010	2	Modified *Table 1 on page 1*

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