

Hi-Rel PNP bipolar transistor 60 V - 0.6 A

Features

BV_{CEO}	60 V
I_C (max)	0.6 A
H_{FE} at 10 V - 150 mA	> 100
Operating temperature range	-65°C to +200°C

- Hi-Rel PNP bipolar transistor
- Linear gain characteristics
- ESCC qualified
- European preferred part list - EPPL
- Radiation level: lot specific total dose contact marketing for specified level

Description

The 2N2907AHR is a silicon planar epitaxial PNP transistor in TO-18 and LCC-3 packages. It is specifically designed for aerospace Hi-Rel applications and ESCC qualified according to the 5202-001 specification. In case of conflict between this datasheet and ESCC detailed specification, the latter prevails.

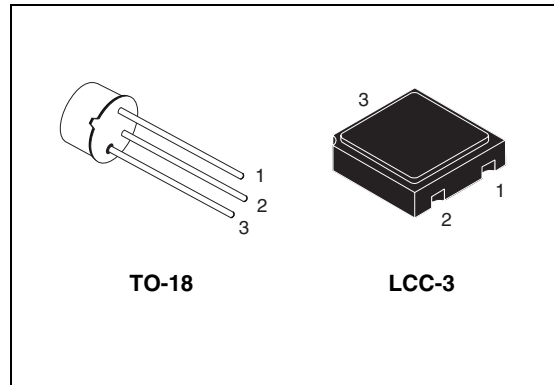


Figure 1. Internal schematic diagram

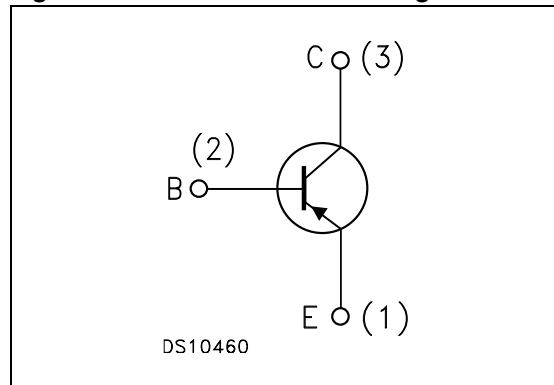


Table 1. Device summary

Order codes	Packages	Lead finish	Marking	Type	EPPL	Packaging
2N2907AHR	TO-18	Gold Solder Dip	520200101 520100102	ESCC Flight		Strip pack
2N2907AT1	TO-18	Gold	2N2907AT1	Engineering model		Strip pack
SOC2907A	LCC-3	Gold	SOC2907A	Engineering model		Waffle pack
SOC2907AHRB	LCC-3	Gold Solder Dip	520200104 520200105	ESCC Flight	Yes	Waffle pack

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage ($I_E = 0$)	-60	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	-60	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	-5	V
I_C	Collector current for 2N2907AHR for SOC2907AHRB	-0.6	A
		-0.5	A
P_{tot}	Total dissipation at $T_{amb} \leq 25\text{ °C}$ for 2N2907AHR	0.4	W
	for SOC2907AHRB	0.4	W
	for SOC2907AHRB ⁽¹⁾	0.73	W
	Total dissipation at $T_c \leq 25\text{ °C}$ for 2N2907AHR	1.8	W
T_{stg}	Storage temperature	-65 to 200	°C
T_J	Max. operating junction temperature	200	°C

1. When mounted on a 15 x 15 x 0.6 mm ceramic substrate.

Table 3. Thermal data for through-hole package

Symbol	Parameter	TO-18	Unit
R_{thJC}	Thermal resistance junction-case	max 97	°C/W
R_{thJA}	Thermal resistance junction-ambient	max 437	°C/W

Table 4. Thermal data for SMD package

Symbol	Parameter	SOC	Unit
R_{thJA}	Thermal resistance junction-ambient	max 437	°C/W
	Thermal resistance junction-ambient ⁽¹⁾	max 240	°C/W

1. When mounted on a 15 x 15 x 0.6 mm ceramic substrate.

2 Electrical characteristics

$T_{\text{case}} = 25\text{ °C}$ unless otherwise specified.

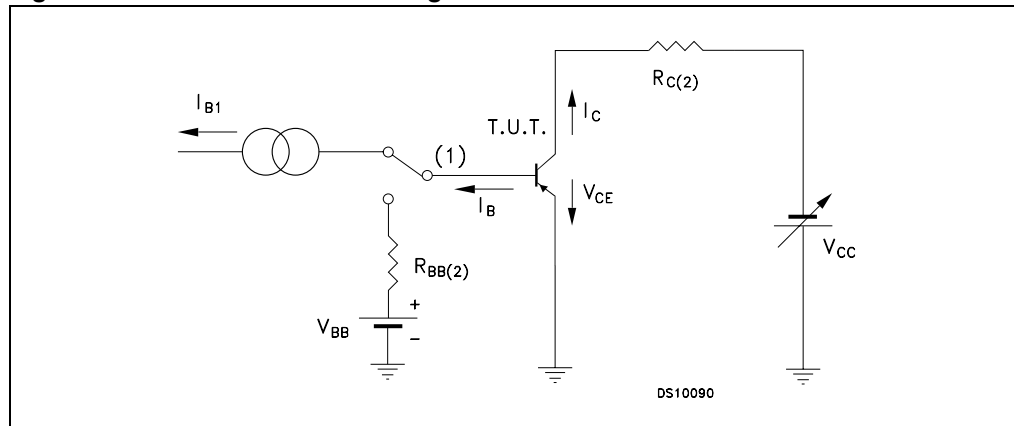
Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector-base cut-off current ($I_{\text{E}} = 0$)	$V_{\text{CB}} = -50\text{ V}$ $V_{\text{CB}} = -50\text{ V}$ $T_{\text{C}} = 150\text{ °C}$			-10 -10	nA μA
$V_{(\text{BR})\text{CBO}}$	Collector-base breakdown voltage ($I_{\text{E}} = 0$)	$I_{\text{C}} = -10\text{ }\mu\text{A}$	-60			V
$V_{(\text{BR})\text{CEO}}^{(1)}$	Collector-emitter breakdown voltage ($I_{\text{B}} = 0$)	$I_{\text{C}} = -10\text{ mA}$	-60			V
$V_{(\text{BR})\text{EBO}}$	Emitter-base breakdown voltage ($I_{\text{C}} = 0$)	$I_{\text{E}} = -10\text{ }\mu\text{A}$	-5			V
$V_{\text{CE}(\text{sat})}^{(1)}$	Collector-emitter saturation voltage	$I_{\text{C}} = -150\text{ mA}$ $I_{\text{B}} = -15\text{ mA}$			-0.4	V
$V_{\text{BE}(\text{sat})}^{(1)}$	Base-emitter saturation voltage	$I_{\text{C}} = -150\text{ mA}$ $I_{\text{B}} = -15\text{ mA}$			-1.3	V
$h_{\text{FE}}^{(1)}$	DC current gain	$I_{\text{C}} = -0.1\text{ mA}$ $V_{\text{CE}} = -10\text{ V}$ $I_{\text{C}} = -10\text{ mA}$ $V_{\text{CE}} = -10\text{ V}$ $I_{\text{C}} = -150\text{ mA}$ $V_{\text{CE}} = -10\text{ V}$ $I_{\text{C}} = -500\text{ mA}$ $V_{\text{CE}} = -10\text{ V}$	75 100 100 50		300	
h_{fe}	Small signal current gain	$V_{\text{CE}} = -20\text{ V}$ $I_{\text{C}} = -20\text{ mA}$ $f = 100\text{ MHz}$	2			
C_{CBO}	Output capacitance ($I_{\text{E}} = 0$)	$V_{\text{CB}} = -10\text{ V}$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$			8	pF
t_{on}	Turn-on time	$V_{\text{CC}} = -30\text{ V}$ $I_{\text{C}} = -150\text{ mA}$ $I_{\text{B1}} = -15\text{ mA}$			45	ns
t_{off}	Turn-off time	$V_{\text{CC}} = -30\text{ V}$ $I_{\text{C}} = -150\text{ mA}$ $I_{\text{B1}} = -I_{\text{B2}} = -15\text{ mA}$			300	ns

1. Pulsed duration = 300 μs , duty cycle $\leq 1.5\%$

2.1 Test circuit

Figure 2. Resistive load switching test circuit



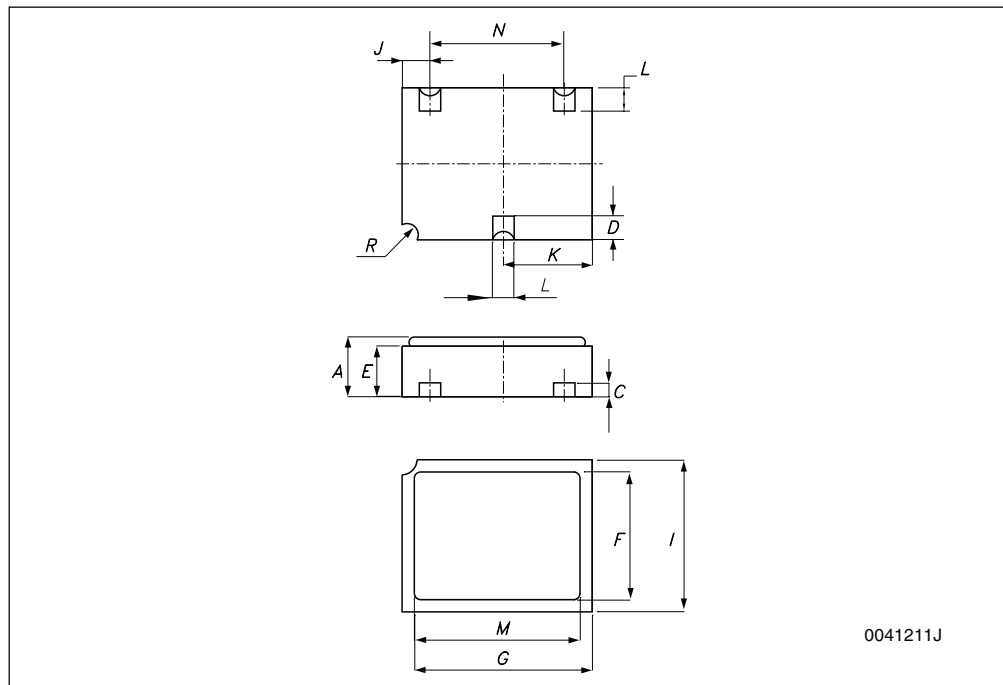
1. Fast electronic switch
2. Non-inductive resistor

3 Package mechanical data

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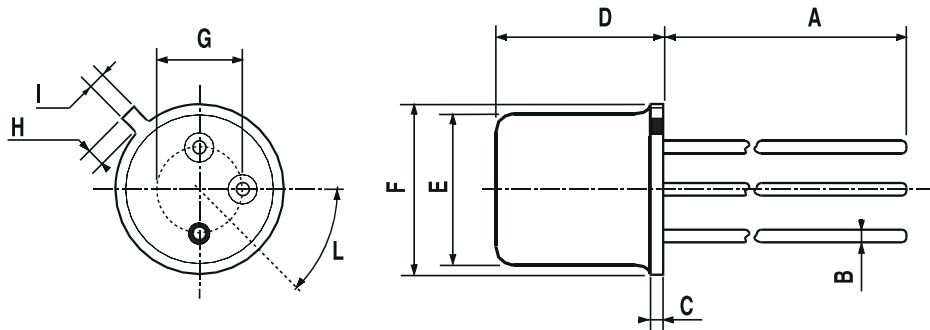
Ceramic Leadless Chip Carrier 3 mechanical data

DIM.	mm.		
	MIN.	TYP	MAX.
A	1.16		1.42
C	0.45	0.50	0.56
D		0.76	
E		1	
F	1.90		2.15
G	2.90		3.25
I	2.40		2.74
J	0.40	0.57	0.80
K	1.35	1.52	1.75
L		0.50	
M	2.40		2.65
N		1.90	
R		0.30	



TO-18 Mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		12.7			0.500	
B			0.49			0.019
D			5.3			0.208
E			4.9			0.193
F			5.8			0.228
G	2.54			0.100		
H			1.2			0.047
I			1.16			0.045
L	45°			45°		



0016043D

4 Revision history

Table 6. Document revision history

Date	Revision	Changes
09-Feb-2009	1	Initial release
05-Jan-2010	2	Modified Table 1 on page 1

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