Tsi564A™
Serial RapidIO Switch

Features

Serial RapidIO Interfaces

- Bandwidth of up to 40 Gbps
- Low latency with cut-through capability
- Individual port power down
- *RapidIO Interconnect Specification (Revision 1.2)* compliant

The Tsi564A enhances system scalability through device configuration and provides architects and designers with a solution for both throughput intensive and power sensitive applications.

- Port flexibility for multiple I/O bandwidth requirements:
  - Up to four 4x mode ports or eight 1x mode ports
  - Each 4x serial port can be configured as two 1x serial ports
- Integrated high-speed, full-duplex SerDes with 8b/10b encoding
- Advanced non-blocking internal switching fabric
  - Specifically designed for line rate termination and prevention of head-of-line blocking
  - Port SerDes frequency configuration to 1.25, 2.5, and 3.125 Gbits/s
- Look-up tables: Table-based packet routing

Other Device Capabilities

- I^2C Interface: Supports configuration through register initialization
- Hot Swappable ports: Enables use in field replaceable blade applications

Device Overview

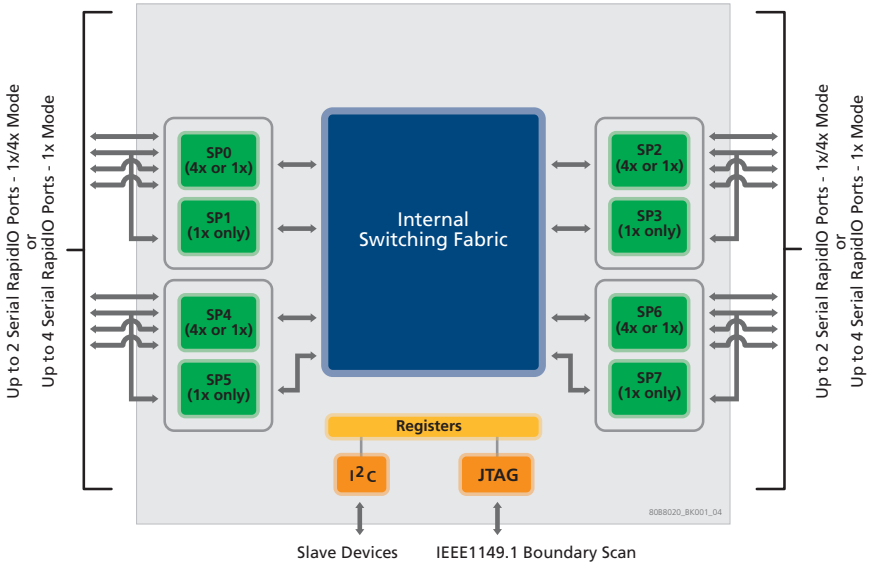
The IDT Tsi564A is an industry leading Serial RapidIO switch supporting 40 Gbps aggregate bandwidth. The Tsi564A is part of a family of switches that enable customers to develop systems with robust features and high performance at low cost.

The Tsi564A provides designers and architects with maximum scalability to design the device into a wide range of applications. Flexible port configurations can be selected through multiple port width and frequency options.

Based on the *Serial RapidIO Specification,* the Tsi564A incorporates SerDes functionality, error recovery, priority-based fabric routing, high payload efficiency, and table-based fabric packet routing. In addition, the Tsi564A supports RapidFabric extensions including data streaming packet switching for interworking and encapsulation.

The device goes beyond standard specification requirements to solve system level issues by optimizing performance, lowering power consumption, and supporting hot swappable I/Os. The extensive buffering and traffic management architecture is specifically designed for line rate termination and the prevention of head-of-line blocking.

Block Diagram



Benefits

- Scalability: device variations of port width and frequencies
- Performance: low latency and high protocol efficiency
- Power: low power implementation of integrated SerDes functionality
- Time-to-market: leverages open-standard technology

Specifications

- Technology: 0.13u
- Voltage: 1.2V, 3.3V
- Flexible power consumption
  - Highly configuration dependent with SerDes voltage range, baud rate, and port width impacting power consumption
- Package: 399 ball, 21mm x 21mm, 1mm ball pitch FCBGA

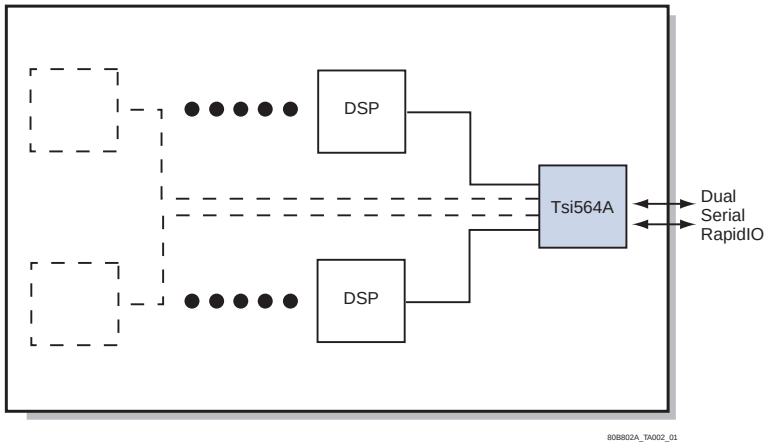
Target Markets

- Wireless Embedded Communications
  - Node B, Radio Network Controller, Media Gateway
- Access Embedded Communications
  - Multiservice WAN Switches, 1 to 10 Gbit Ethernet Switches, 1 to >10 Gbit Routers, DSLAMs
- Storage
  - Storage Area Networks, Network Attached Storage, High-Performance Work Stations
- Video and Imaging
  - Signal and image processing, and media processing applications

Typical Applications

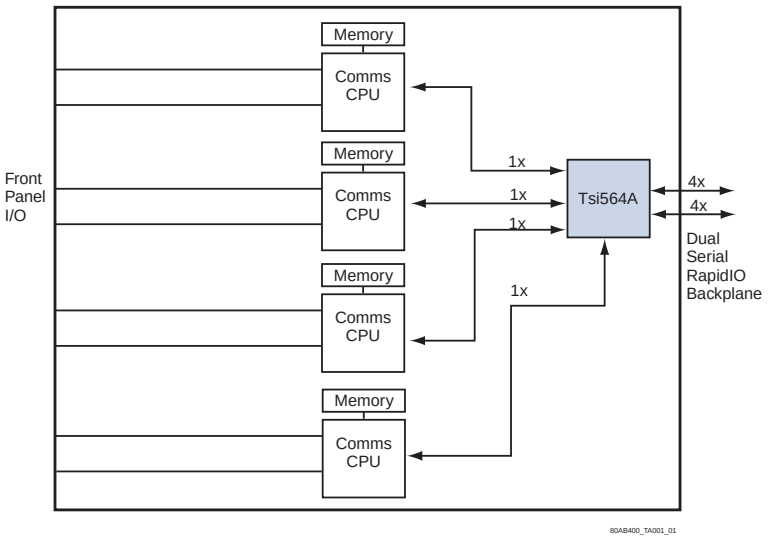
The Tsi564A can be used in many embedded communication applications. It provides chip-to-chip interconnect between I/O devices and can replace existing proprietary backplane fabrics for board-to-board interconnect which improves system cost and product time-to-market.

Processor Farm Mezzanine



The Tsi564A provides traffic aggregation through packet prioritization when it is used with RapidIO-enabled I/O devices. When it is in a system with multiple RapidIO-enabled processors it provides high performance peer-to-peer communication through its non-blocking switch fabric.

Distributed Processing Blade



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