240V, 12-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options	
		24 Lead SOW	Die
HV510	240V	HV510WG	HV510X

Features

- ❏ HVCMOS® technology
- ❏ Operating output voltage of 240V
- ❏ Low power level shifting from 5V to 240V
- ❏ Shift register speed 8MHz @ V_{DD} = 5V
- ❏ 12 latched data outputs
- ❏ Output polarity and blanking
- ❏ CMOS compatible inputs
- ❏ Forward and reverse shifting options

General Description

The HV510 is a low voltage serial to high voltage parallel converter with 12 high voltage push-pull outputs. This device has been designed to drive small capacitive loads such as piezo electric transducers. It can also be used in any application requiring multiple high voltage outputs, low current sourcing and sinking capabilities.

The device consists of a 12-bit shift register, 12 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, D_{IOA} is Data In and D_{IOB} is Data Out; data is shifted from $HV_{OUT}12$ to $HV_{OUT}1$. When DIR is at logic high, D_{IOB} is Data In and D_{IOA} is Data Out: data is then shifted from $HV_{OUT}1$ to $HV_{OUT}12$. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$, $\overline{BL}$, or the $\overline{POL}$ inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +6V
Supply voltage, V_{PP}	V_{DD} to 260V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[3]	0.3A
High voltage supply current[2]	0.25A
Continuous total power dissipation[3]	750mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 85°C at 12mW/°C.

Electrical Characteristics (for V_{DD} = 5V, V_{PP} = 240V, T_A = 25°C)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current				4	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} supply current				200	µA	All V_{IN} = 0V or V_{DD}
I_{PP}	High voltage supply current				0.25	mA	V_{PP} = 240V All outputs high
					0.25	mA	V_{PP} = 240V All outputs low
I_{IH}	High-level logic input current				10	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current				-10	µA	V_{IL} = 0V
V_{OH}	High-level output	HV_{OUT}	220			V	V_{PP} = 240V, IHV_{OUT} = -0.5mA
			175			V	V_{PP} = 200V, IHV_{OUT} = -0.5mA
		Data out	V_{DD} -1V			V	I_{DOUT} = -100µA
V_{OL}	Low-level output	HV_{OUT}			25	V	V_{DD} = 5V, IHV_{OUT} = 1mA
		Data out			1.0	V	I_{DOUT} = 100µA
V_{OC}	HV_{OUT} clamp voltage				V_{PP} +1.5	V	I_{OL} = 1mA
					-1.5	V	I_{OL} = -1mA
I_{OH}	Output Source Current		1.0			mA	V_{PP} = 240V
			0.8			mA	V_{PP} = 200V

AC Characteristics[1] (For V_{DD} = 5V, V_{PP} = 200V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency			8	MHz	
t_W	Clock width high and low	62			ns	
t_{SU}	Data setup time before clock rises	35			ns	
t_H	Data hold time after clock rises	30			ns	
t_{WLE}	Width of latch enable pulse	80			ns	
t_{DLE}	$\overline{LE}$ delay time after rising edge of clock	35			ns	
t_{SLE}	$\overline{LE}$ setup time before rising edge of clock	40			ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}			6.0	µs	C_L = 20pF
t_{DHL}	Delay time clock to data out high to low			125	ns	C_L = 20pF
t_{DLH}	Delay time clock to data out low to high			125	ns	C_L = 20pF
t_r, t_f	All logic inputs			5	ns	

Note:

1. Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V
V_{PP}	High voltage supply	60		240	V
V_{IH}	High-level input voltage	V_{DD} -0.9		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.9	V
T_A	Operating free-air temperature	-40		+85	°C

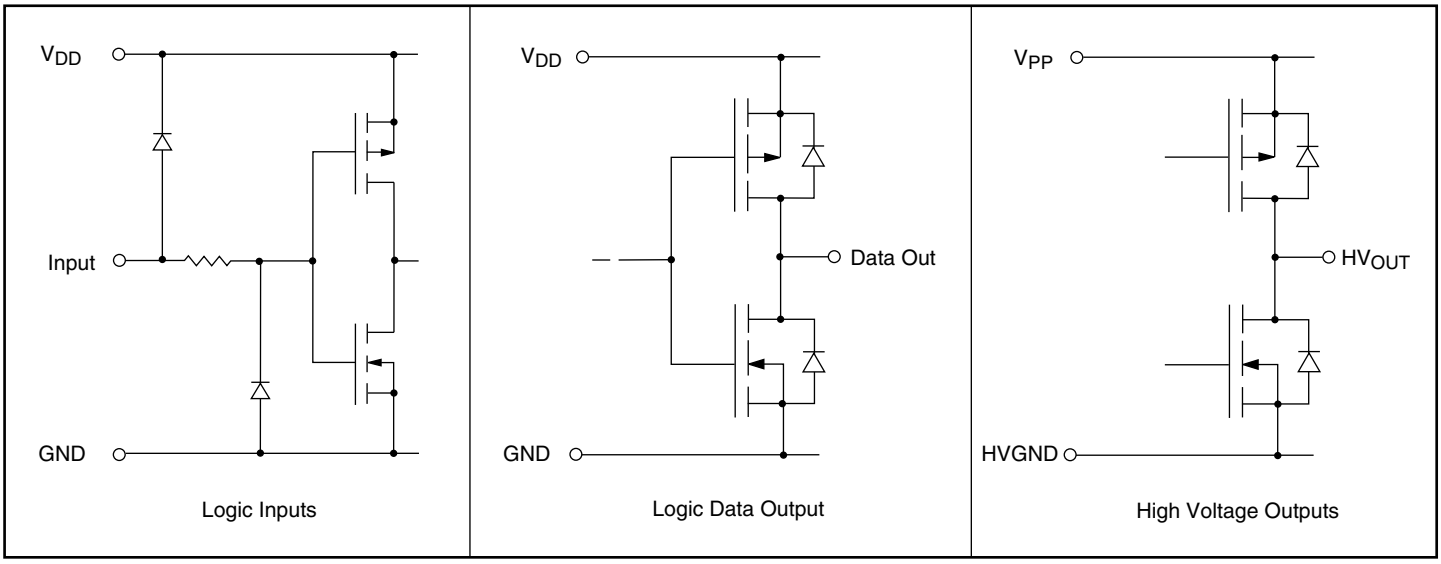
Notes:

Power-up sequence should be the following:

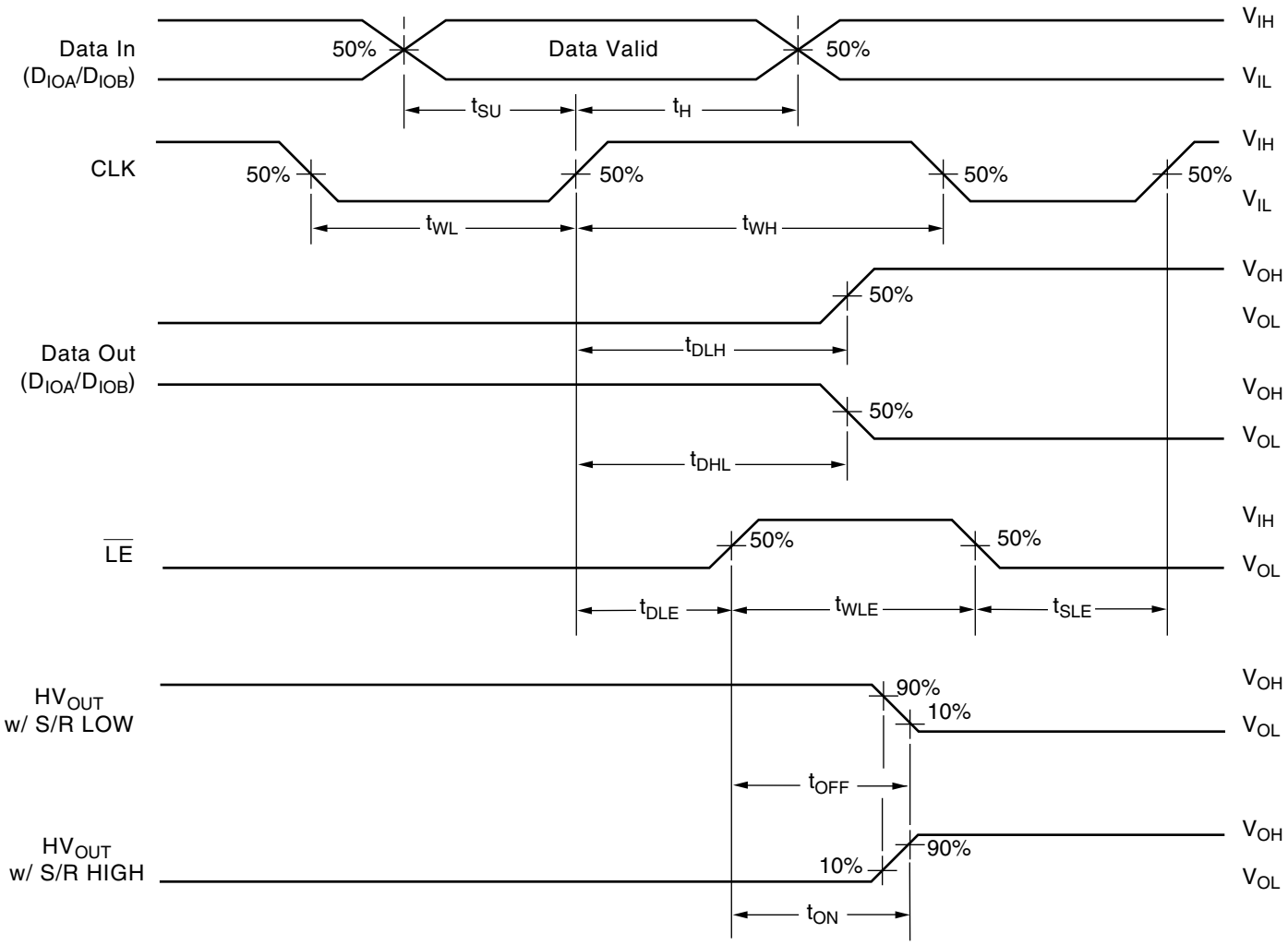
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

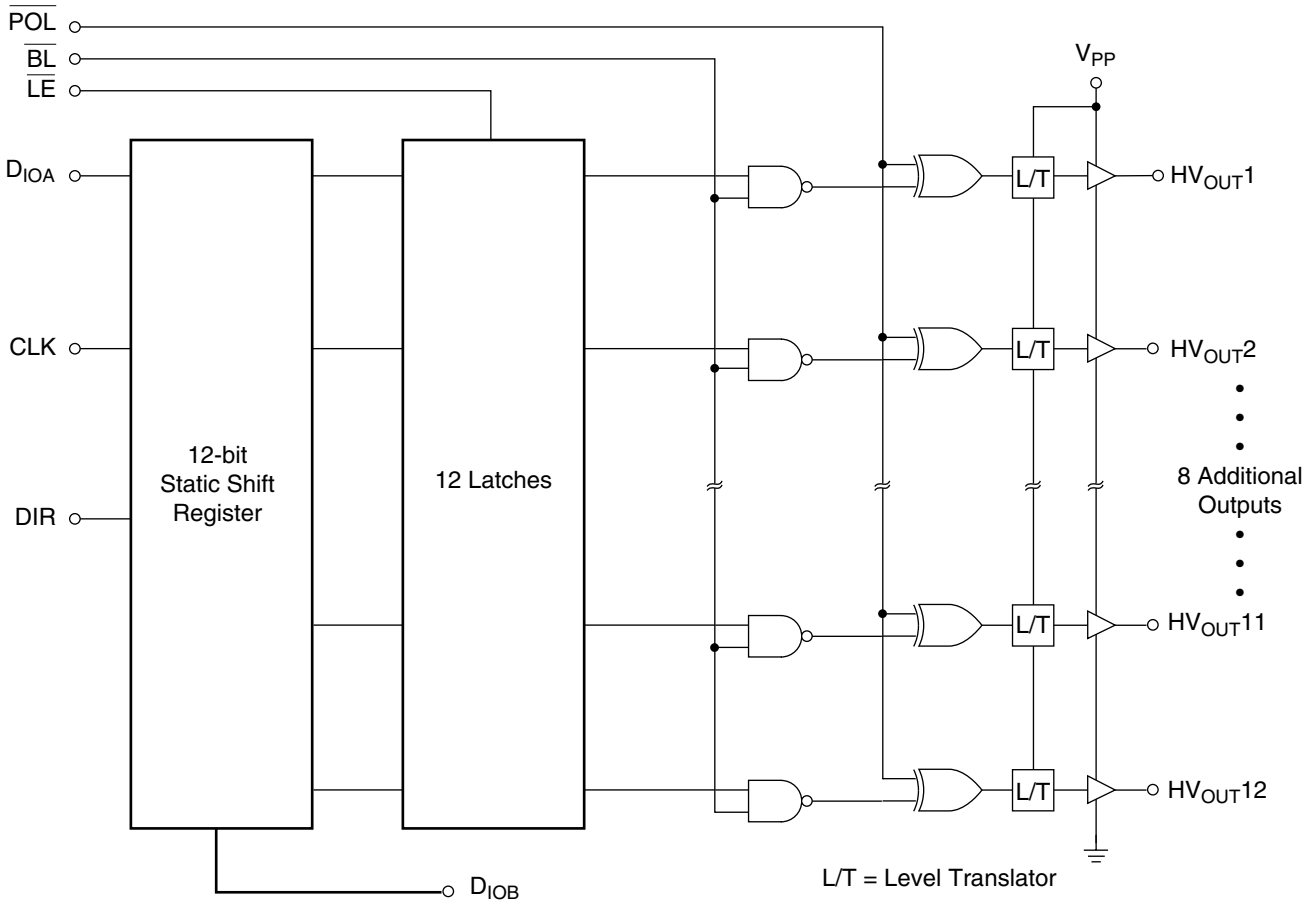
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1	Shift Reg 2…12	HV Outputs 1	HV Outputs 2…12	Data Out *
All on	X	X	X	L	L	X	*	*…*	H	H…H	*
All off	X	X	X	L	H	X	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*…*	*	*…*	*
Store data in latches	X	X	↓	H	H	X	*	*…*	*	*…*	*
	X	X	↓	H	L	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Transparent latch mode	L	↑	H	H	H	X	L	*…*	L	*…*	*
	H	↑	H	H	H	X	H	*…*	H	*…*	*
I/O relation	D_{IOA}	↑	X	X	X	L	$Q_n \rightarrow$	Q_{n-1}	—		D_{IOB}
	D_{IOB}	↑	X	X	X	H	$Q_n \rightarrow$	Q_{n+1}	—		D_{IOA}

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

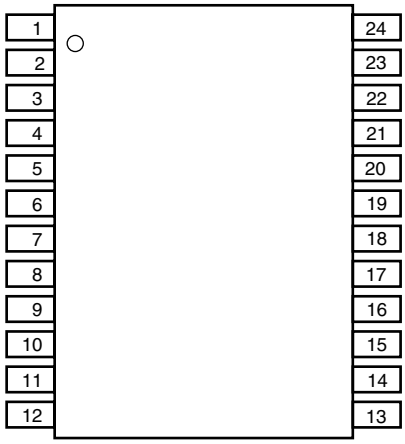
Pin Configurations

HV510
24 Pin SOW Package

Pin	Function
1	V_{PP}
2	D_{IOA}
3	$\overline{BL}$
4	$\overline{POL}$
5	V_{DD}
6	DIR
7	LGND
8	HVGND
9	CLK
10	$\overline{LE}$
11	D_{IOB}
12	V_{PP}
13	$HV_{OUT}12/1$
14	$HV_{OUT}11/2$
15	$HV_{OUT}10/3$
16	$HV_{OUT}9/4$
17	$HV_{OUT}8/5$
18	$HV_{OUT}7/6$
19	$HV_{OUT}6/7$
20	$HV_{OUT}5/8$
21	$HV_{OUT}4/9$
22	$HV_{OUT}3/10$
23	$HV_{OUT}2/11$
24	$HV_{OUT}1/12$

Note:
Pin designation for DIR = H/L
Example: for DIR = H, Pin 13 is $HV_{OUT}12$
for DIR = L, Pin 13 is $HV_{OUT}1$

Package Outline



top view
24-pin SOW