8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

Features

- ❏ HVCMOS, technology
- ❏ Operating output voltage of 250V
- ❏ Low power level shifting from 5V to 250V
- ❏ Shift clock speed 8MHz @ V_{DD}=5V
- ❏ 8 latch data outputs
- ❏ Output blanking
- ❏ CMOS compatible inputs
- ❏ Programmable POL latch

Applications

- ❏ Piezoelectric transducer driver
- ❏ Weaving applications
- ❏ Braille
- ❏ Printers
- ❏ MEMs
- ❏ Displays

General Description

The HV514 is a low voltage serial to high voltage parallel converter with 8 high voltage push-pull outputs. This device has been designed to drive small capacitve loads such as piezoelectric transducers. It can also be used in any application requiring multiple high voltage outputs, medium current sourcing and sinking capabilities.

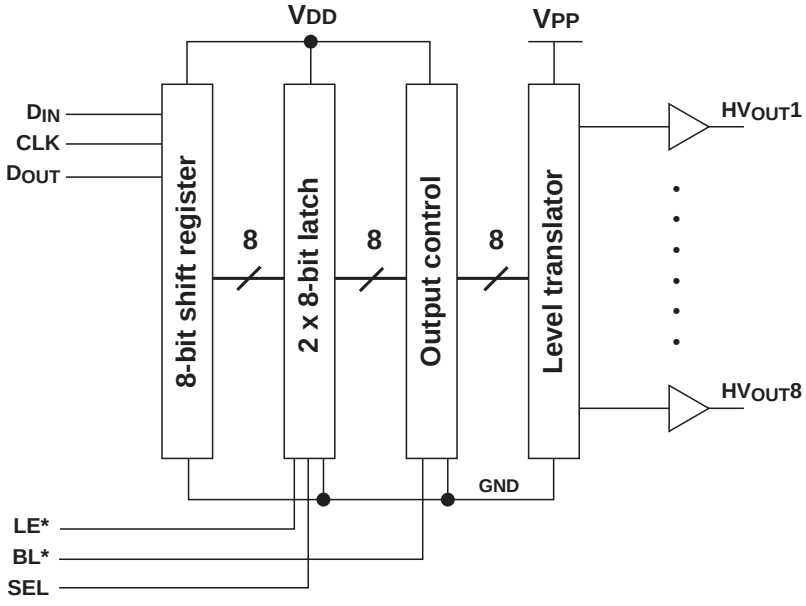
The device consists of an 8-bit shift register, dual 8-bit latches, and control logic to latch data, and control blanking of the outputs. Data is shifted through the shift register on the rising transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the /LE, SEL, or the /BL inputs. Transfer of data from the shift register to the latch occurs when the /LE is high. Shift register data is shifted to the 8-bit Data Latch when SEL is high; and shift register data is shifted to the 8-bit Polarity Latch when SEL is low. The data is held in the output latches whenever /LE is low.

The high voltage output state is primarily dependent on the value in the polarity latch. If the blank, /BL, is low, the output condition is the result of a 1 being exclusively-NOR'ed with the polarity latch value. If /BL is high, the output condition is the result of the data latch being exclusively-NOR'ed with the polarity latch.

All outputs with have a break-before-make circuitry to reduce cross-over current during output state changes.

Note: /LE, SEL, and /BL have internal 20k-ohm pull-up resistors.

Top Block Diagram



DC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current				4	mA	f_{CLK}=8MHz, LE*=LOW
I_{DDQ}	Quiescent V_{DD} supply current				0.1	mA	All $V_{IN}=V_{DD}$
					2.0		All $V_{IN=}$0V
I_{PP}	V_{PP} supply current				100	µA	V_{PP}=250V, f_{OUT}=300Hz, no load
I_{PPQ}	Quiescent V_{PP} supply current				100	µA	V_{PP}=240V, outputs static
I_{IH}	High-level logic input current				10	µA	$V_{IH}=V_{DD}$
I_{IL}	Low-level logic input current				-10	µA	V_{IL}=0V
					-350		V_{IL}=0V, for inputs w/pull-up resistors
I_{DPP}	Dynamic I_{PP}				0.1	mA	f_{OUT}=100kHz, no load
V_{OH}	High-level output	H_{VOUT}	140			V	V_{PP} =200V, I_{HVOUT}=-20mA
		Data out	V_{DD}-1V				I_{DOUT}=-0.1mA
V_{OL}	Low-level output	H_{VOUT}			60	V	V_{DD} =4.5V, I_{HVOUT}=20mA
		Data out			1.0		I_{DOUT}=0.1mA

AC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency	0		8	MHz	
f_{OUT}	Output switching frequency (SOA limited)		300		Hz	C_L=50nF, V_{PP}=200V
t_W	Clock width high and low	62			ns	
t_{SU}	Data setup time before clock rises	15			ns	
t_H	Data hold time after clock rises	30			ns	
t_{WLE}	Width of latch enable pulse	80			ns	
t_{DLE}	/LE delay time after rising edge of clock	35			ns	
t_{SLE}	/LE setup time before rising edge of clock	40			ns	
t_{OR}, t_{OF}	Rise/fall time of HV_{OUT}			1000	µs	C_L=100nF, V_{PP}=200V
$t_{d\ ON/OFF}$	Delay time for output to start rise/fall			500	ns	
t_{DHL}	Delay time clock to D_{OUT} high to low			110	ns	C_L=15pF
t_{DLH}	Delay time clock to D_{OUT} low to high			110	ns	C_L=15pF
T_R, t_F	All logic inputs			5	ns	

Absolute Maximum Ratings*

Supply Voltage, V_{DD}	-0.5V to 6V
Supply Voltage, V_{PP}	275V
Logic input levels	-0.5V to V_{DD}+0.5V
Ground current	0.3A
High voltage supply current	0.25A
Continuous total power dissipation	750mW
Operating temperature range	-40?C to +85?C
Storage temperature range	-65?C +150?C

* All voltages are referenced to device ground.

Ordering Information

Device	Part Number	Package	Die
HV514	HV514WG	20 Lead SOW	HV514X

Operating Supply Voltages

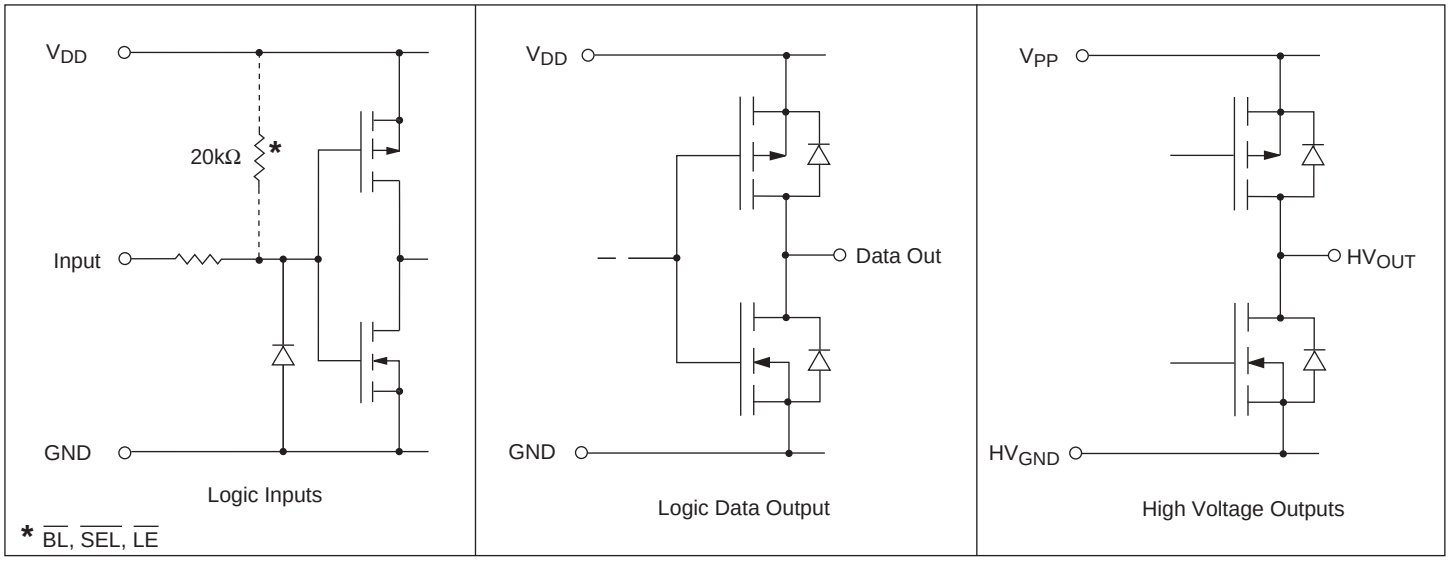
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V	
V_{PP}	High voltage supply	50		250	V	Note 1
V_{IH}	High-level input voltage	V_{DD}-0.9		V_{DD}	V	
V_{IL}	Low-level input voltage	0		0.9	V	
T_A	Operating free-air temperature	-40		+85	° C	

Notes:

1. Below minimum V_{PP} the output may not switch.
2. **Power-up sequence should be the following:**
   1. Connect ground.
   2. Apply V_{DD}.
   3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
   4. Apply V_{PP}.

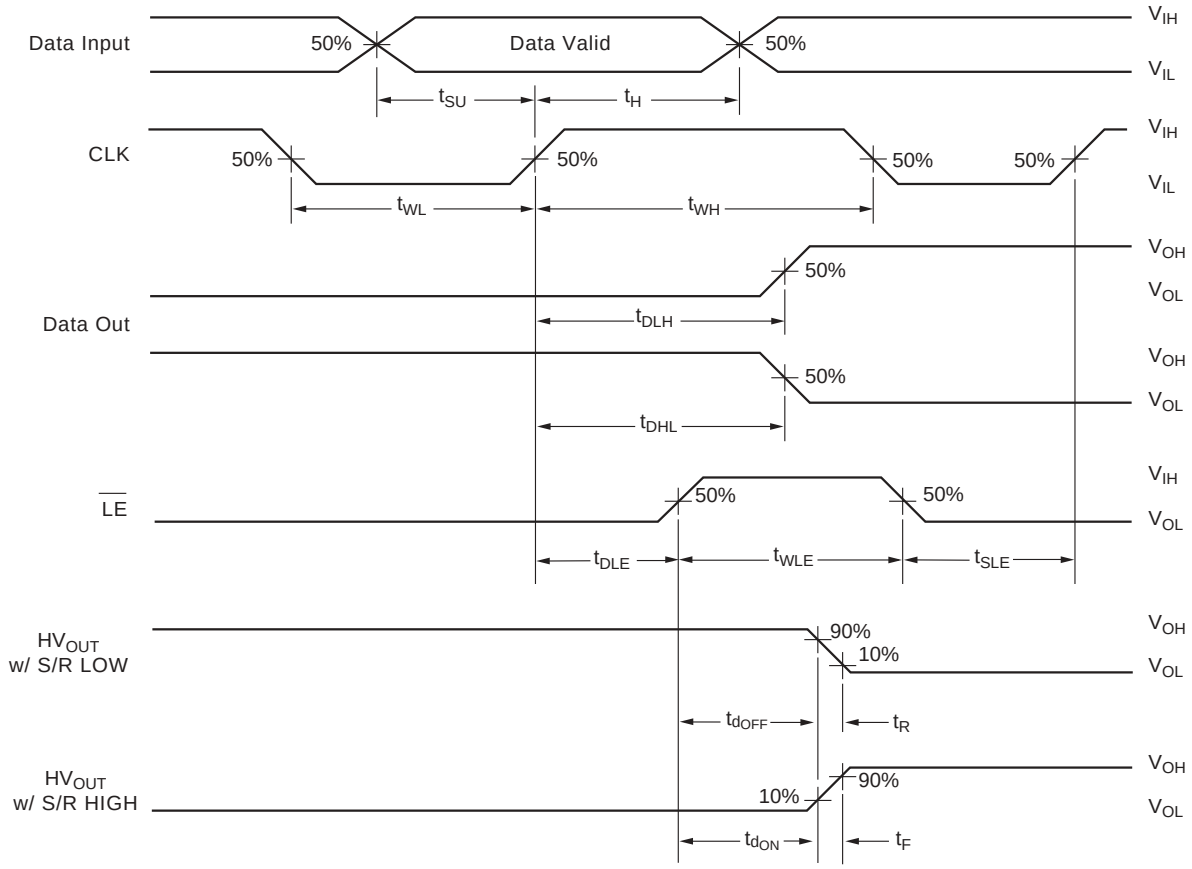
Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



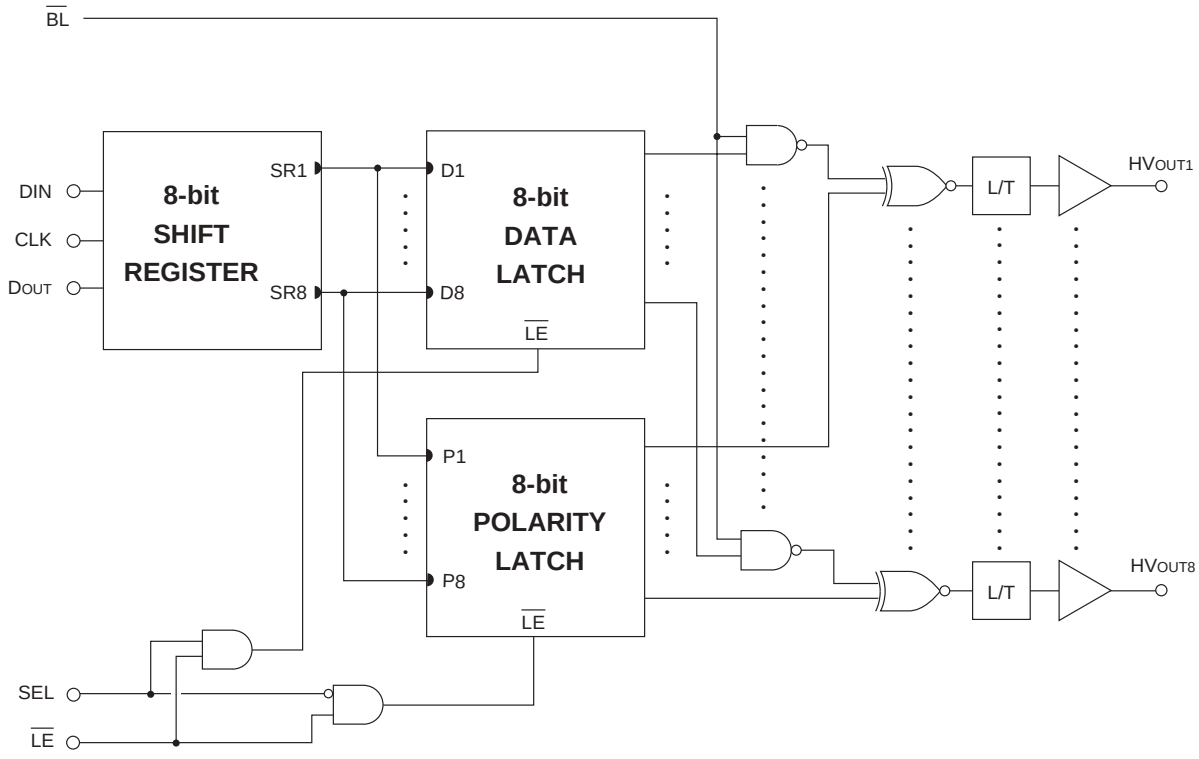
Note: There is an internal output resistor for the high voltage output pin for SOA protection

Switching Waveforms



/BL, /LE, and SEL hav internal 20kΩ pull-up resistors.

Functional Block Diagram



Note: $\overline{BL}$, $\overline{SEL}$, and $\overline{LE}$ have internal 20kΩ pull-up resistors.

Function Table

Function	Inputs					Outputs			
	Data	CLK	/LE	SEL	/BL	Shift Reg 1 2....16	Latch	HV Output Action 1 2....16	Data Out
Load S/R	H or L					H or L *…*	* *…*	* *…*	*
Transfer S/R to Latch	X	X	H	H		H or L *…*	To data	* *…*	*
	X	X	H	L		H or L *…*	To polarity	* *…*	*
Hold latch data	X	X	L			* *…*	* *…*	* *…*	*
Blank Output	X	X	X	X	L	* *…*	* *…*	1 (XNOR) POL	*
Active Output	X	X	X	X	H	* *…*	* *…*	Data (XNOR) POL	*

/BL	Latched Information		HV Output
	Data	Polarity	
L	X	L	L
L	X	H	H
H	L	L	L
H	H	L	H
H	L	H	H
H	H	H	L

Notes:

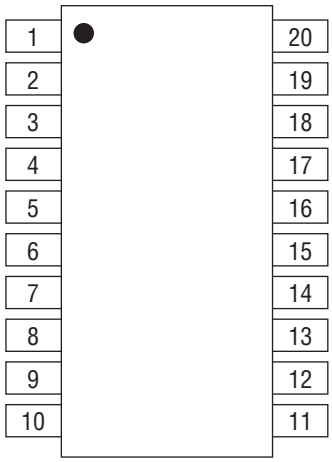
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition

• = dependent on previous stage's satte before the last CLK or last LE* high.

Pin Configuration

Pin	Function
1	CLK
2	$\overline{LE}$
3	D_{IN}
4	LGND
5	HVGND
6	HVGND
7	$HV_{out}1$
8	$HV_{out}2$
9	$HV_{out}3$
10	$HV_{out}4$
11	$HV_{out}5$
12	$HV_{out}6$
13	$HV_{out}7$
14	$HV_{out}8$
15	V_{PP}
16	V_{PP}
17	V_{DD}
18	D_{OUT}
19	$\overline{BL}$
20	SEL

Package Outline



20-Lead SOW Package (WG)
WIde Body

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