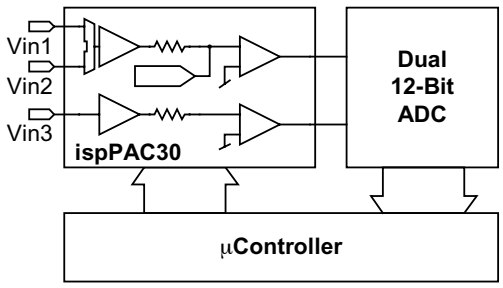
ispPAC30

In-System Programmable Analog Circuit

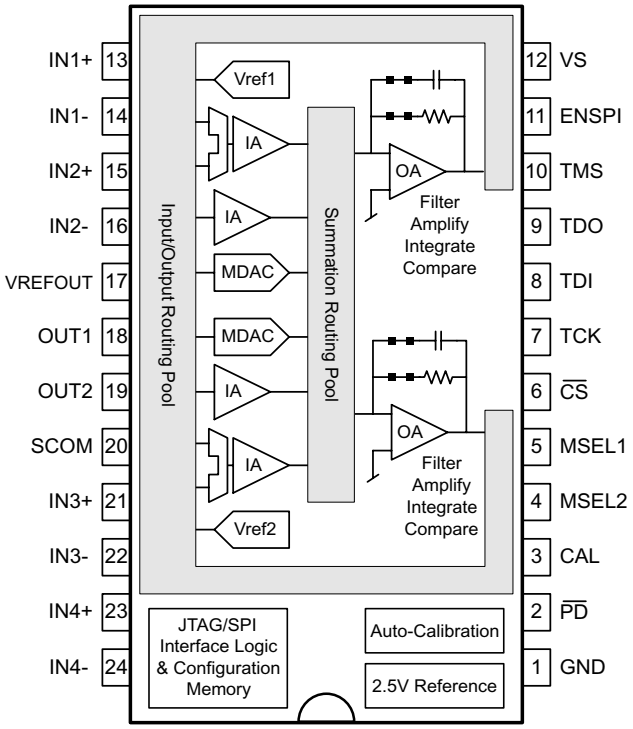
October 2002 **Data Sheet**

Features

- **Flexible Interface and Programming Control**
  - Full configuration capability, SPI or JTAG modes
  - Unlimited device updates using SRAM register
  - E²CMOS® for non-volatile configuration storage
  - Real-time microcontroller configuration/control
- **Four Input Instrumentation Amplifiers (IA's)**
  - High impedance: differential or single-ended
  - 0V to 2.8V with programmable gains (±1 to ±10)
  - Dual multiplexers (pin or serial port controlled)
  - Connects easily to existing system circuits
- **Two Configurable Rail-to-Rail Output Amps**
  - Single-ended, 0V to 5V output swing
  - Gain bandwidth product >15MHz
  - Amplifier, filter, integrator or comparator modes
  - 7 filter frequencies (50kHz to 600kHz)
- **Two 4-Quadrant, 8-Bit Multiplying DACs**
  - Full bandwidth when used as a multiplier
  - Precision gain (<0.01 steps) with signal as input
  - Precision offset (in 7 ranges) using internal Vref
- **Analog Input/Summation Routing Pools**
  - Routing of all I/O to any IA or MDAC
  - Any IA/MDAC summed to either output amplifier
  - Circuits with and without feedback possible
  - Routable to maintain pin location relationships
- **Other Product Features**
  - Single supply (+5V) operation
  - Precision voltage reference output (2.5V)
  - Power-down for μWatt power consumption
  - Auto-calibration of internal offsets
  - Available in 28-pin PDIP or 24-pin SOIC
- **Applications**
  - Reconfigurable or adaptive signal conditioning
  - Analog front end for most A/D converters
  - Programmable analog signal control loops
  - Precision programmable gain amplifiers



Functional Block Diagram



ispPAC30 24-Pin SOIC

Description

The ispPAC®30 is a member of the Lattice family of In-System Programmable (ISP™) analog integrated circuits. It is digitally configured via SRAM and utilizes E²CMOS memory for non-volatile storage of its configuration. The flexibility of ISP enables programming, verification and unlimited reconfiguration, directly on the printed circuit board.

The ispPAC30 is a complete front end solution for data acquisition applications using 10 to 12-bit ADC's. It provides multiple single-ended or differential signal inputs, multiplexing, precision gain, offset adjustment, filtering, and comparison functionality. It also has complete routability of inputs or outputs to any input cell and then from any input cell to either summing node of the two output amplifiers. Designers configure the ispPAC30 and verify its performance using PAC-Designer®, an easy to use, Microsoft Windows® compatible development tool. Device programming is supported using PC parallel port I/O operations.

Electrical Characteristics

TA = 25°C; V_S = 5.0V; 0V < V_{IN} < 2.8V; Gain = 1; Output load = 50pf, 1kΩ. IA1, IA2, MDAC1 connected to OA1 and IA3, IA4, MDAC2 connected to OA2. V_{OUT} biased to swing from 0.5 to 4.5V. Auto-Cal initiated immediately prior. (Unless otherwise specified).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Analog Input						
$V_{IN\pm}$ (1)	Input Voltage Range	Applied to either V_{IN+} or V_{IN-}	0		2.8	V
$V_{IN-DIFF}$ (2)	Differential Voltage Swing	2 $\lvert V_{IN+} - V_{IN-} \rvert$			5.6	V
V_{OS} (3)	Differential Offset Voltage (Input Referred)	G=1		1	2	mV
		G = 10		100		µV
$\Delta V_{OS} / \Delta T$	Differential Offset Drift	-40°C to +85°C; Any gain, input referred		50		µV/°C
R_{IN}	Input Resistance			10^9		Ω
C_{IN}	Input Capacitance			2		pF
I_B	Input Bias Current (at DC)	at 25°C		1		pA
		at 85°C		200		pA
e_N	Input Noise Voltage Density	At 10kHz, referred to input, G=10		70		nV/$\sqrt{Hz}$
Analog Output						
V_{OH}	Output Voltage Swing High	I_L = 250µA	4.95	4.97		V
		I_L = 5mA	4.50	4.65		V
V_{OL}	Output Voltage Swing Low	I_L = -250µA		0.03	0.05	V
		I_L = -5mA		0.11	0.15	V
I_{SC}	Short Circuit Current	Short to ground; V_{OUT} = 4.9V	25	35		mA
I_{OUT}	Maximum Output Current	See graph in typical performance curves		±30		mA
Static Performance						
G	Programmable Gain Range	Individual input amplifier gain	0		20	dB
	Gain Error	V_{OUT} = 0.5V to 4.5V		1	3	%
	Input Gain Matching	Any two inputs; any output		1	3	%
$\Delta G/\Delta T$	Gain Drift	-40°C to +85°C		35		ppm/°C
PSR	Power Supply Rejection	at 10kHz		74		dB
Reference Output ($VREF_{OUT}$)						
$VREF_{OUT}$	Reference Output Range	Nominally 2.500V; I_{LOAD} = 0	-0.2		0.2	%
$IREF_{OUT}$	Reference Output Current	($VREF_{OUT}$ change = -1%) source		40		µA
		($VREF_{OUT}$ change = +1%) sink		-350		µA
	Reference Output Drift	-40 to +85°C		100		ppm/°C
	Reference Output Noise	100kHz bandwidth		40		μV_{RMS}
	Power Supply Rejection	1kHz		80		dB
Comparator Mode Performance						
	Comparator Switching Time	10mV overdrive		4.0		µs
		100mV overdrive		2.5		µs
	Overload Recovery Time	2.8V overload		3.0		µs

Electrical Characteristics, Continued

TA = 25°C; V_S = 5.0V; 0V < V_{IN} < 2.8V; Gain = 1; Output load = 50pf, 1kΩ. IA1, IA2, MDAC1 connected to OA1 and IA3, IA4, MDAC2 connected to OA2. V_{OUT} biased to swing from 0.5 to 4.5V. Auto-Cal initiated immediately prior. (Unless otherwise specified).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
MDAC PACell Performance						
	Resolution		7+sign			bits
INL	Integral Non-Linearity			0.25	0.5	lsb
DNL	Differential Non-Linearity	Guaranteed monotonic			-1	lsb
V_{OS}	Offset Voltage				3	mV
	Gain Error			1	3	%
	Input Bandwidth (F_{3dB})	V_{IN} = 3Vp-p; V_{CM} = 1.4V±0.75V	1.25	1.6		MHz
Internal Voltage Reference Performance						
	V_{REF1}/V_{REF2} Voltage Output	64mV Setting	56	64	72	mV
		128mV Setting	120	128	136	mV
		256mV Setting	246	256	266	mV
		512mV Setting	500	512	524	mV
		1024mV Setting	1000	1024	1048	mV
		2048mV Setting	2000	2048	2096	mV
		2.500V Setting	2.450	2.500	2.550	V
Dynamic Performance						
SNR	Signal to Noise (4)	0.1Hz to 114kHz		83		dB
THD	Total Harmonic Distortion	F_{IN} = 10kHz		-85	-74	dB
	V_{OUT} = 4Vpk (0.5V to 4.5V)	F_{IN} = 100kHz		-75	-60	dB
CMR	Common Mode Rejection	10kHz		75		dB
	(V_{IN} = 0V to 2.8V) (5)	100kHz		65		dB
BW	Small Signal Bandwidth	All gains, minimum feedback capacitor	1	1.57		MHz
BW_{FP}	Full Power Bandwidth	All gains		1.1		MHz
SR	Slew Rate	All gains	10	15		V/µs
t_S	Settling Time, 0.1%	4V output step, low to high		2	4	µs
	V_{OUT} = 4Vpk (0.5V to 4.5V)	4V output step, high to low		4	8	µs
	Crosstalk (6)	R_L = 1kΩ, F_{IN} = 10kHz		-100		dB
Filter Characteristics						
F_C	Corner Frequency Range (7)		49		619	kHz
$\|F_C\|$	Corner Frequency Accuracy	Deviation from calculated -3db point		3	5	%
$\Delta F_C/\Delta T$	Corner Frequency Drift	-40°C + 0 +85°C		0.05		%/°C
Digital I/O						
V_{IL}	Input Low Voltage		0		0.8	V
V_{IH}	Input High Voltage		2		V_S	V

Electrical Characteristics, Continued

TA = 25°C; V_S = 5.0V; 0V < V_{IN} < 2.8V; Gain = 1; Output load = 50pf, 1kΩ. IA1, IA2, MDAC1 connected to OA1 and IA3, IA4, MDAC2 connected to OA2. V_{OUT} biased to swing from 0.5 to 4.5V. Auto-Cal initiated immediately prior. (Unless otherwise specified).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Digital I/O (Continued)						
I_{IL}, I_{IH}	Input Leakage Current	No pull-up/pull-down			10	µA
		With pull-up/pull-down (8)			±50	µA
	Hysteresis	Schmitt Trigger		250		mV
V_{OL}	Output Low Voltage (TDO)	I_{OL} = 4.0mA			0.4	V
V_{OH}	Output High Voltage (TDO)	I_{OH} = -1.0mA	2.4			V
Programming and Calibration						
	Erase/Reprogram Cycles	For E^2CMOS cells	10K	1M		cycles
	Calibration Cycle Time	Initial turn on		140	250	ms
		Subsequent user initiated		50	100	
Power Supplies						
V_S	Operating Supply Voltage		4.75	5	5.25	V
I_S	Supply Current (8)	V_S = 5.0V		10	15	mA
P_D	Power Dissipation (9)	V_S = 5.0V		50	75	mW
	Power Down Supply Current	V_S = 5.0V		10	30	µA
	Wakeup Time	Time to resume normal operation		3.5	5.0	µs
Temperature Range						
	Operation		-40		85	°C
	Storage		-65		150	°C

Notes:

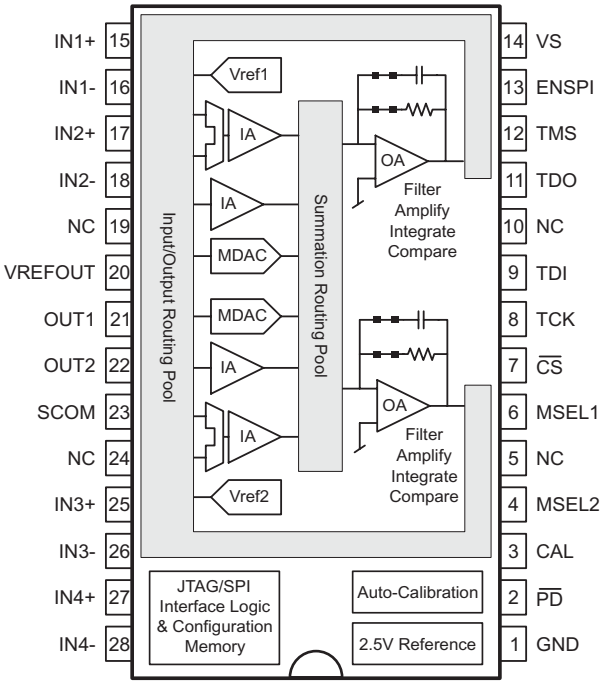
1. Inputs larger than this will be clipped.
2. Inputs can be used fully differential if care is taken to offset signals so as to not force the outputs below 0V or above V_S. The total input swing is measured from one differential extreme, with respect to polarity, to the other, or twice the peak single-ended input range.
3. To insure full spec performance, an auto-calibration should be performed after initial turn-on when the device reaches thermal stability.
4. For all gains except G=1, output is assumed to be driven to 5V by the input signal level (V_{IN} x Gain = 5V). When G=1, the maximum single ended input possible is 2.8V. The consequence is an output of 2.8V instead of 5V. Computed SNR is then 5dB less because of the lower effective signal. With a true differential 2.5V input and G=1, output will again be a full 5V and SNR will be equal to the value shown in the specification table.
5. V_{IN+} and V_{IN-} are connected together for this test.
6. Measured between analog outputs, with an identical signal path configuration used for each. One channel is driven with a 10kHz signal and the other is not (input grounded).
7. Computed 3db corner frequencies are 619kHz, 401kHz, 250kHz, 169kHz, 114kHz, 74kHz and 49kHz. Actual values found in PAC-Designer software.
8. Logic inputs will exhibit positive current configured with a pull-down and negative current with a pull-up.
9. Configured so all internal circuitry is powered on.

Pin Descriptions

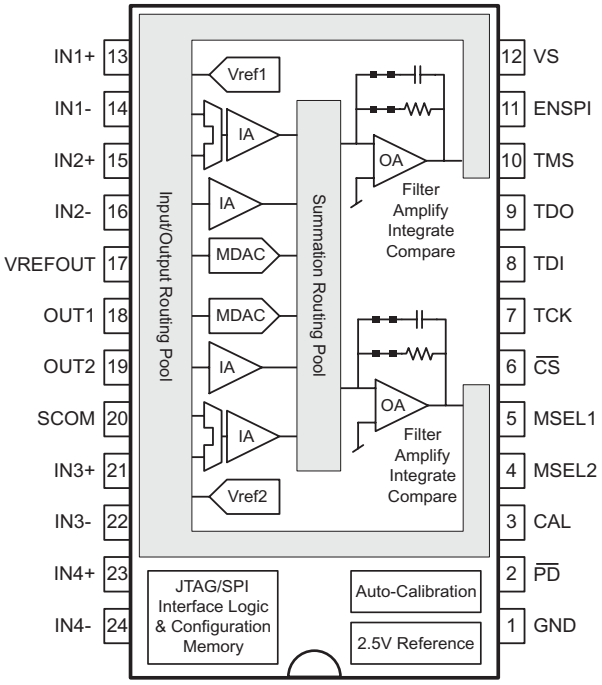
Pins		Symbol	Name	Description
PDIP	SOIC			
15, 16, 17, 18, 25, 26, 27, 28	13, 14, 15, 16, 21, 22, 23, 24	IN	Inputs 1, 2, 3, 4 (+ or -) Plus or Minus	Differential input pins, with two pins per input (e.g., IN2+ and IN2-). Each are components of V_{IN}, where differential $V_{IN} = V_{IN+} - V_{IN-}$.
6	5	MSEL1	Multiplexer 1 Control	Multiplexer logic input pin. Selects either of two analog channels to IA1 (instrument amplifier). Programmable pull-up, pull-down (default), or none.
4	4	MSEL2	Multiplexer 2 Control	Multiplexer logic input pin. Selects either of two analog channels to IA4 (instrument amplifier). Programmable pull-up, pull-down (default), or none.
21, 22	18, 19	OUT	Outputs 1 and 2	Single-ended output pins. Internal feedback to inputs accommodated.
20	17	VREFOUT	Voltage Reference Output	Internal voltage reference output pin (+2.5V nominal). Must be bypassed to GND with a 1µF capacitor.
13	11	ENSPI	Enable SPI Mode	Enable SPI logic input pin. When high, causes serial port to run in SPI mode. Programmable pull-up or pull-down (default).
12	10	TMS	Test Mode Select	Serial interface logic mode select pin (input). JTAG interface mode only. Internal pull-up.
11	9	TDO	Test Data Out	Serial interface logic pin (output) for both JTAG and SPI operation modes. Programmable slew rate, high or low (default).
9	8	TDI	Test Data In	Serial interface logic pin (input) for both JTAG and SPI modes. Internal pull-up.
8	7	TCK	Test Clock	Serial interface logic clock pin (input) for both JTAG and SPI modes. Programmable pull-up, pull-down (default), or none.
7	6	$\overline{CS}$	Chip Select	Chip select logic input pin. SPI data transfer enabled by this input. Internal pull-up.
3	3	CAL	Auto-Calibrate	Digital pin (input). Commands an auto-calibration sequence on a rising edge. Internal pull-down.
2	2	$\overline{PD}$	Power Down	Power down enable logic pin (input). Shuts down all power to device. Programmable pull-up (default), pull-down or none.
14	12	VS	Supply Voltage	Analog supply pin (5V nominal). Should be bypassed to GND with 1µF and .01µF capacitors.
1	1	GND	Ground	Ground pin. Should normally be connected to the analog ground plane.
23	20	SCOM	Signal Common	Analog signal common pin (sense). Always connected to GND. Auto-calibration accuracy is determined with respect to this pin.
5, 10, 19, 24	—	NC	No Connects	No internal connections are made to these pins in the PDIP package.

Connection Notes:

1. All inputs are labeled with plus (+) and minus (-) signs. Polarity is labeled for reference and can be selected externally by reversing pin connections or internally under user programmable control.
2. All analog output pins are “hard-wired” to internal output pins and should be left open if not used.
3. When the signal input is single-ended, the unused half or the differential input (usually the – or minus) must be connected GND or some other reference point. If OA output is routed to an IA or MDAC input, the minus input is automatically connected to 0V internally.



ispPAC30 28-Pin PDIP



ispPAC30 24-Pin SOIC

Absolute Maximum Ratings

Supply Voltage V_S . . . . . -0.5 to +7V

Logic and Analog Input Voltage Applied. . . . . 0 to VS

Logic and Analog Output Short Circuit Duration . . . . . Indefinite

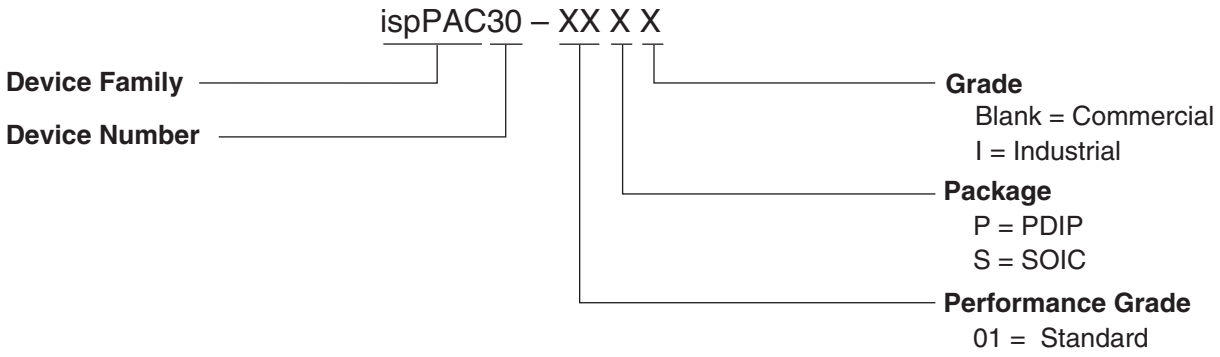
Lead Temperature (Soldering, 10 sec.) . . . . . 260°C

Ambient Temperature with Power Applied . . . . . -55 to 125°C

Storage Temperature . . . . . -65 to 150°C

Note: Stresses above those listed may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

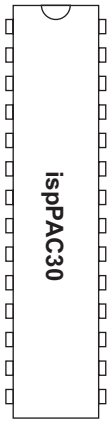
Part Number Description



ispPAC30 Ordering Information

Part Number	Package
ispPAC30-01PI	28-pin PDIP
ispPAC30-01SI	24-pin SOIC

Package Options

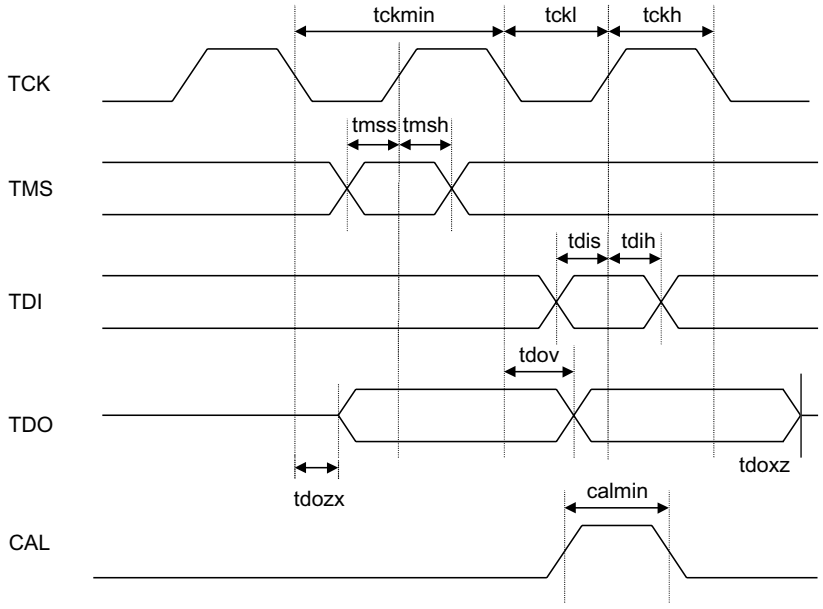


28-Pin PDIP

24-Pin SOIC

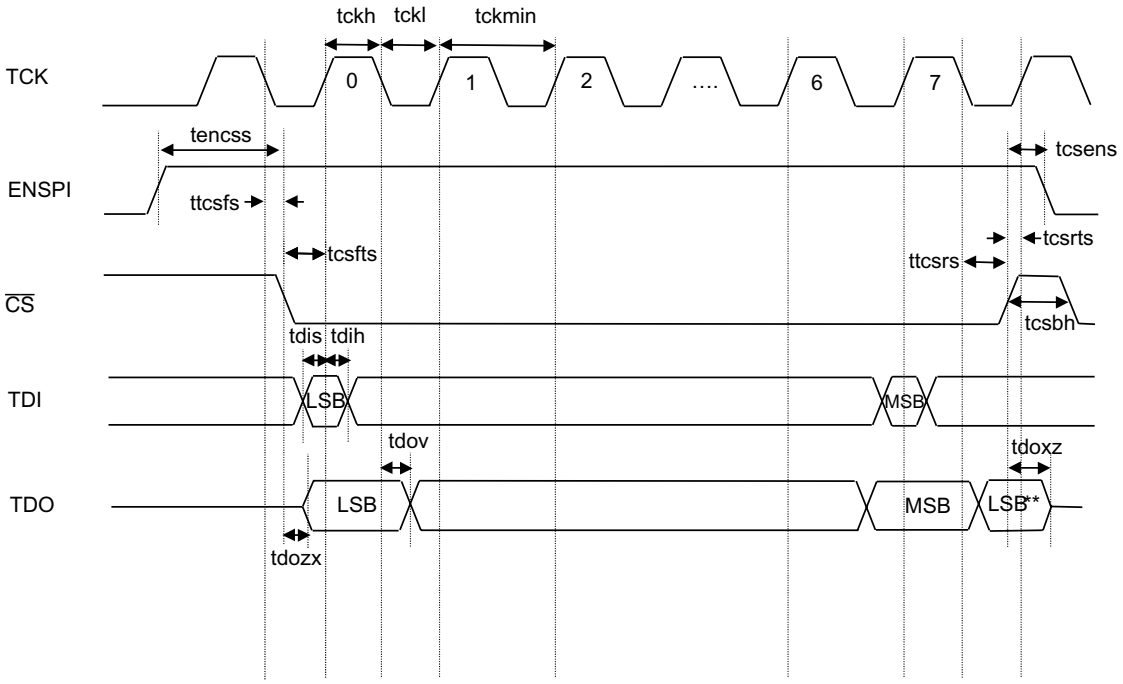
Timing Specifications (JTAG Interface Mode)

Symbol	Parameter	Conditions	Min	Typ	Max
tckmin	Min Clock Period	—	80ns		
tckl	TCK Low Time	—	40ns		
tckh	TCK High Time	—	40ns		
tmss	TMS Setup Time	—	15ns		
tmsh	TMS Hold Time	—	4ns		
tdis	TDI Setup Time	—	15ns		
tdih	TDI Hold Time	—	8ns		
tdozx	TDO Delay Float to Valid	—			60ns
tdov	TDO Delay Clock to Valid	—			60ns
tdoxz	TDO Delay Valid to Float	—		145ns	
calmin	Minimum Calibration Pulse	—	40ns		



Timing Specifications (SPI Interface Mode)

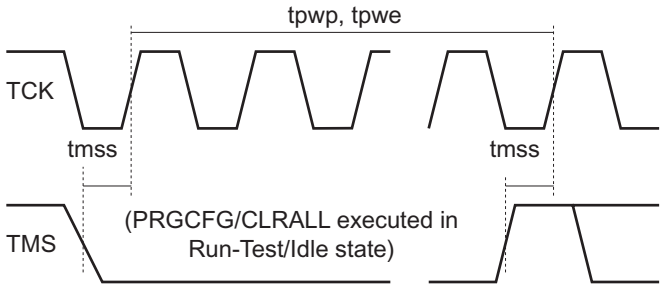
Symbol	Parameter	Min	Typ	Max
tckmin	Min Clock Period	80ns		
tckl	TCK Low Time	40ns		
tckh	TCK High Time	40ns		
tdis	TDI Setup Time	5ns		
tdih	TDI Hold Time	8ns		
tencss	ENSPI Rising Edge to $\overline{CS}$ Falling Edge Setup Time	10ns		
tcsens	$\overline{CS}$ Rising Edge to ENSPI Falling Edge Setup Time	10ns		
ttcsfs	TCK Falling Edge to $\overline{CS}$ Falling Edge Setup Time	10ns		
tcsfts	$\overline{CS}$ Falling Edge to TCK Rising Edge Setup Time	8ns		
ttcsrs	TCK Falling Edge to $\overline{CS}$ Rising Edge Setup Time	25ns		
tcsrts	$\overline{CS}$ Rising Edge to TCK Rising Edge Setup Time	10ns		
tcsbh	$\overline{CS}$ Min High Time			60ns
tdozx	TDO Delay Float to Valid			60ns
tdov	TDO Delay Clock to Valid			60ns
tdoxz	TDO Delay Valid to Float		145ns	
calmin	Minimum Calibration Pulse	30ns		



**LSB of TDI Byte Just Transferred

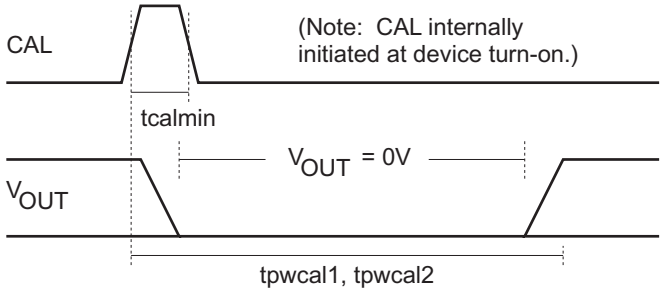
Timing Specifications (E^2 Programming and Auto-cal)

Symbol	Min Clock Period	Conditions	Min	Typ	Max
tpwp	Time for a programming operation	Executed in Run-Test/Idle	80ms		100ms
tpwe	Time for an erase operation	Executed in Run-Test/Idle	80ms		100ms



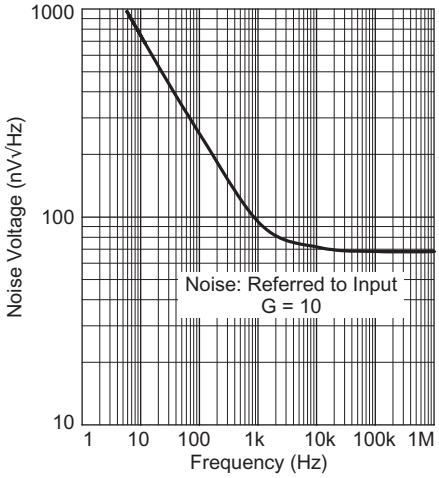
Timing Specifications (Auto-cal)

Symbol	Min Clock Period	Conditions	Min	Typ	Max
tpwcal1	Time for auto-cal operation on power-up	Automatically executed at power-up		140ms	250ms
tcalmin	Minimum auto-cal pulse width	—	30ns		
tpwcal2	Time for user initiated auto-cal operation	Executed on rising edge of CAL		50ms	100ms

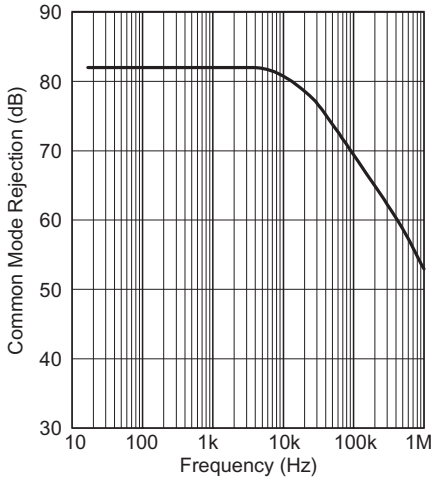


Typical Performance Characteristics

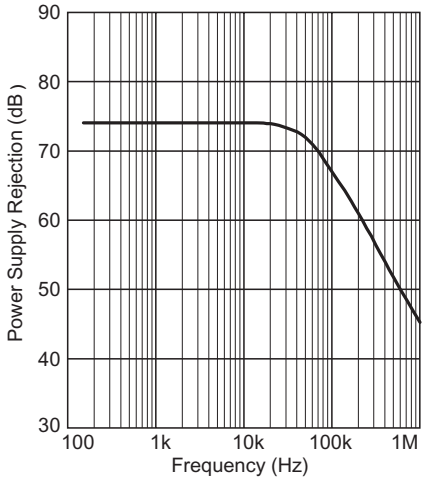
Input Noise Spectrum



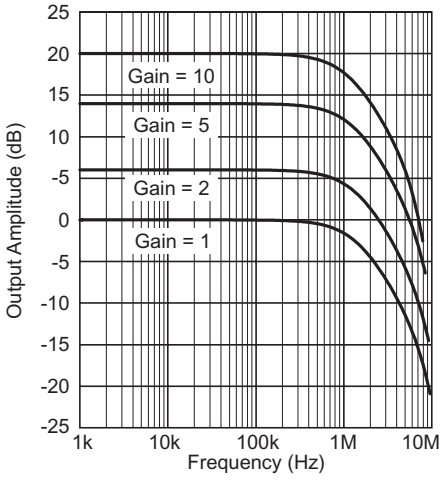
CMR vs. Frequency



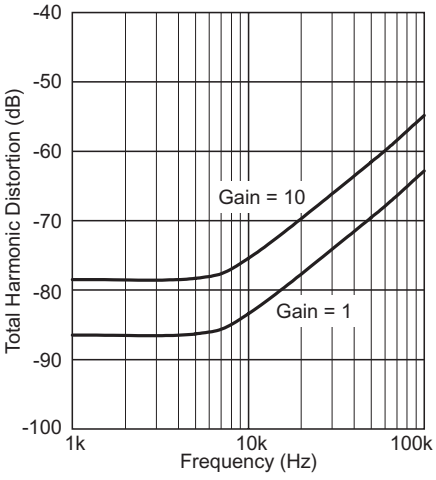
PSR vs. Frequency



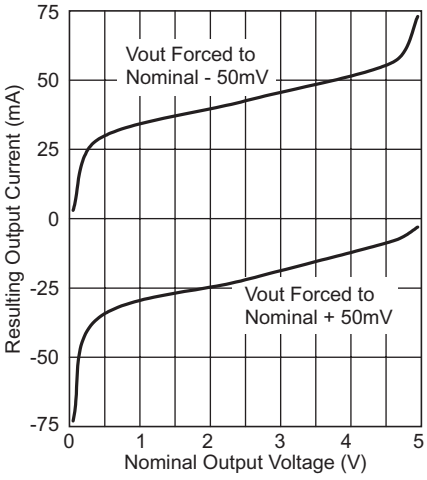
Small Signal BW vs. Gain



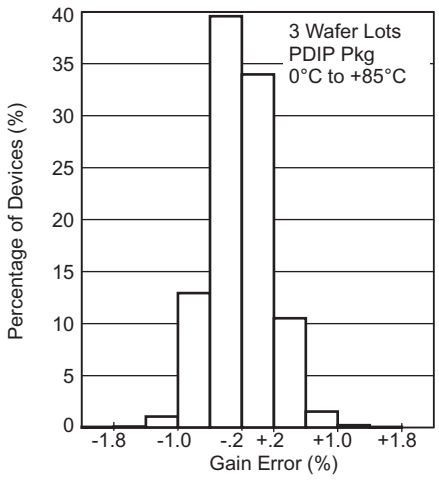
THD vs. Frequency



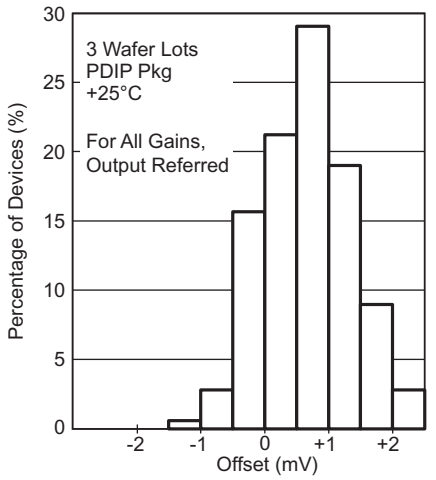
Output Current Drive



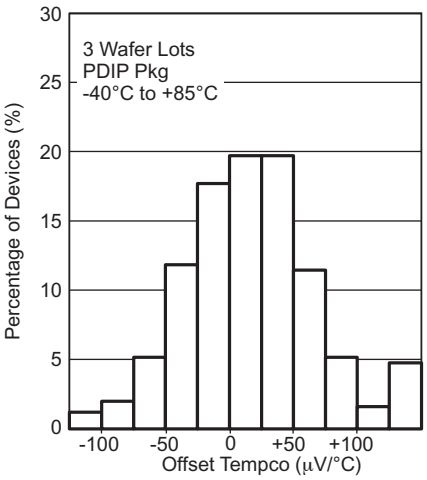
Gain Error (Gain = 1 & 10)



Offset Voltage (V_{OS})

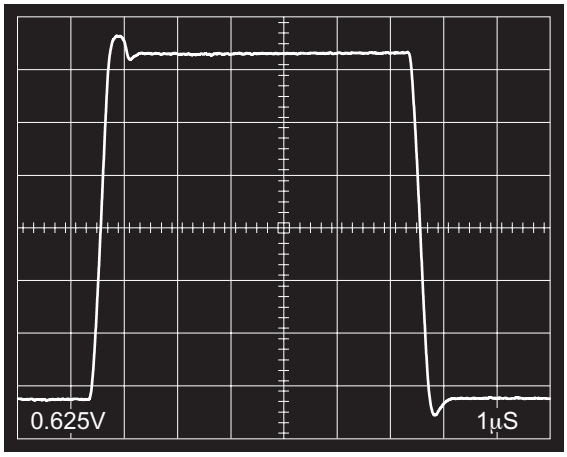


V_{OS} Tempco

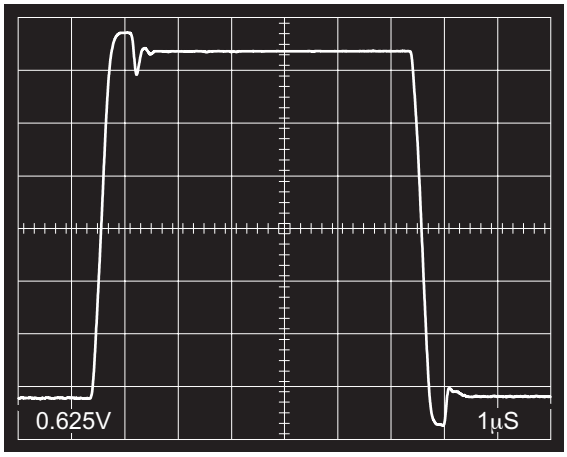


Typical Performance Characteristics, Continued

Large-Signal Response

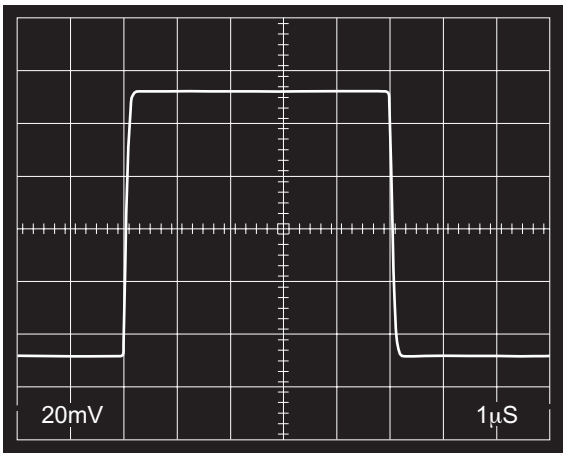


Gain = 1
Load = 1kΩ; 50pF

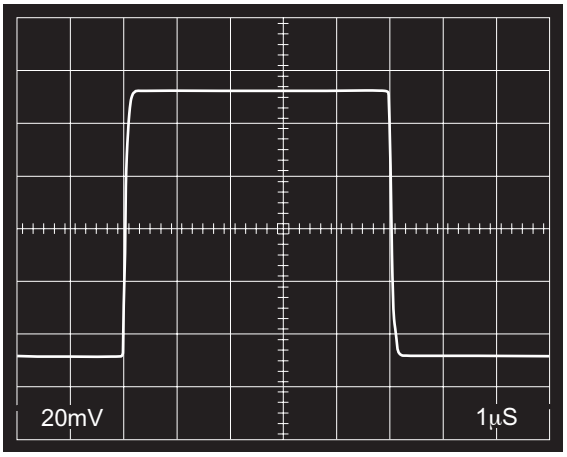


Gain = 1
Load = 1kΩ; 600pF

Small-Signal Response

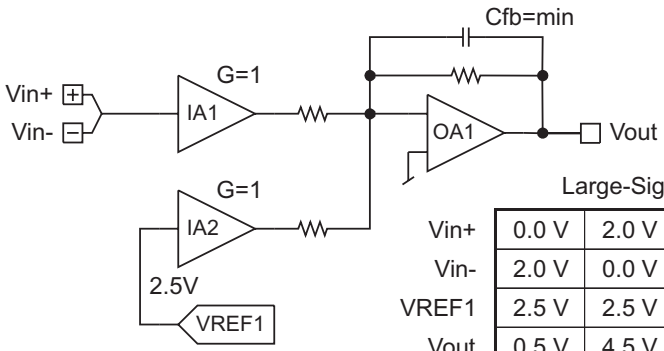


Gain = 1
Load = 1kΩ; 50pF



Gain = 1
Load = 1kΩ; 600pF

Step Response Setup Diagram



	Large-Signal			Small-Signal		
Vin+	0.0 V	2.0 V	0.0 V	0.00 V	0.05 V	0.00 V
Vin-	2.0 V	0.0 V	2.0 V	0.05 V	0.00 V	0.05 V
VREF1	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V
Vout	0.5 V	4.5 V	0.5 V	2.45 V	2.55 V	2.45 V

Theory of Operation

General Description

The ispPAC30 provides programmable, multiple single-ended or differential signal inputs, precision gain, offset adjustment, filtering, and comparison functionality all in a single device. It also has complete routability of inputs or outputs to any input cell and then to either summing node of the internal output amplifiers. A key feature of the ispPAC30 is its capability of being reconfigured in real time, apart from the operation of its non-volatile E^2CMOS or E^2 configuration memory. This enables the user to change or reconfigure the ispPAC30 an unlimited number of times, such as in an automatic gain control circuit or other applications requiring ongoing parametric or routing changes. Because a user chosen configuration is always stored in non-volatile E^2 configuration memory as well, there is a preset configuration ready to go when the device is first turned on, or whenever a return to that stored state is required. Of course, the E^2 configuration can be updated at any time during normal device operation as a completely transparent background operation. All of this functionality and flexibility is combined into the ispPAC30 as a single integrated circuit that greatly simplifies the otherwise burdensome task of designing and customizing circuitry for a wide variety of analog applications.

The following sections of this data sheet give the user a thorough understanding of the general operation and design considerations necessary when using the ispPAC30. Another resource that cannot be overlooked for understanding the ispPAC30 is associated with the PAC-Designer software design tool. Everything that can be configured is accessible in a schematic entry based format. A complete appreciation of the ispPAC30's capabilities is enhanced by exploring and using this design software early to learn more about it. Because a simulator is included, the user can quickly test and prove operational modes and arrive at an understanding sooner while exploring device capabilities. Complete documentation of PAC-Designer is included with the software.

Further technical insight into the ispPAC30 can be gained by referring to the many application notes and circuit solutions that directly relate to this device. All ispPAC technical support literature is available from the Lattice Semiconductor web site at www.latticesemi.com. In addition, Lattice provides expert applications support for all ispPAC devices and their usage.

Device Input Cells

In an ispPAC30 device, any input pin can be routed to any of the four input instrument amplifiers (IA), two of which have dual input multiplexers, or to either of the two multiplying DAC's (MDAC), or any combination of these. In addition, either output amplifier (OA) can be routed to any or all of these same input cells. This enables great flexibility in how an ispPAC30 is configured and allows many functions to be performed, such as signal summation, cascaded gain blocks, complex feedback circuits, etc.

At the ispPAC30 input pins, the input signal range that can be directly applied is 0 to 2.8V. When used differentially, the input pins can be of any polarity with respect to each other as long as the resultant signal is not expected to drive the OA outputs below 0V. Normally, input signals will be single ended, in which case the minus input pin (V_{IN-}) can be tied to ground. Even with single ended measurements, the ispPAC30's differential architecture can be used to an advantage as it will sense ground at the point where it is connected and will also reject any noise common to both ground and the input signal. Input impedances at all input nodes are the same as would be expected for MOSFET devices, and are typically in the Giga-Ohm range. Refer to the specifications section for more detail.

Input Instrument Amplifiers

The input amplifiers (IA's) are referred to as instrument amplifiers because they take the difference of the two input pins and multiply it by the gain setting for which they have been configured. With respect to true differential operation, this means that a negative gain setting is merely a reversal of the plus and minus input (V_{IN}) pins. This is the classical instrument amplifier function and also includes the previously mentioned benefit of remote sensing of signals (not necessarily 0V referenced) and rejection of common mode signals. Both IA's and MDAC's connected to input signals also serve to buffer inputs by virtue of their very high input impedance.

Input Multiplexers

Two of the four input IA's have dual input multiplexers in front of them. They constitute separately selectable input paths to their respective IA's. These paths can be configured either by external pin, or by setting internal E^2 bits. The control pins are named MSEL1 and MSEL2 and control the input path for IA1 and IA4, respectively. The determination of whether either of these select pins asserted high or low for choosing path "A" or "B" internally, and whether an active pull-up or pull-down is programmed is all user-selectable from the software design interface found in PAC-Designer. The initial configuration is called out in the pin description table in the specifications section of this data sheet. With multiplexer control, it is possible to bring in four different input signals and select between them, performing selective signal conditioning on each as required. Or, one or more signals can be routed to one or both multiplexers and thus achieve multiple signal conditioning paths for the same input, selectable by external pins. Finally, all parameters can also be controlled and/or programmed into E^2 configuration memory in real time using either the JTAG or SPI interface.

Internal Voltage References

Two separate voltage references (VREF1 and VREF2) are available to provide fixed voltage references to the ispPAC30's four IA's or two MDAC's. Seven voltage levels are available from each VREF, and each VREF is independently programmable from the other. Table 1 lists the binary weighted values that are available (in addition to 2.5V) and the corresponding least significant bit (LSB) size if this VREF value is applied to the input of either of the MDAC's. Since the IA's/MDAC's have plus and minus polarity control, VREF outputs can be added or subtracted from other signals via the summation bus in addition to being scaled from 1 to 10 by the IA's or attenuated in 128 steps by the MDACs. By selective combination of these various settings, a very large number of user control offset voltages can be summed with any input signal. This is also the basis of how the ispPAC30 can be configured as a comparator. With the output amplifier configured as a comparator, an unknown signal is summed with a precise reference value and an input above or below that reference level will cause a change in state of the output comparator.

Table 1. Available VREF Outputs

VREF (V)	MDAC LSB (mV)
0.064	0.5
0.128	1.0
0.256	2.0
0.512	4.0
1.024	8.0
2.048	16.0
2.500	19.5

Input MDACs

The ispPAC30 has two 8-bit (7+sign) multiplying digital to analog converters (MDAC's) available that accept as their reference input either external signals, internal signals or fixed DC voltages (such as the internal VREFs). The multiplying DAC function means that the input is multiplied (attenuated) by a value corresponding to the code setting of the DAC, resulting in an output that can range from 100% of the input down to a 1 LSB (least significant bit weight) fraction of that value. The exact values output by the MDAC versus input code are detailed in Table 2.

The flexibility of the ispPAC30 allows the MDAC's to act as adjustable attenuators of external input signals, thereby providing fractional or fine gain setting capability. It also means that in combination with the internal VREF's they can also be precision DC sources for providing fixed setpoints, offsets, etc. For example, with the same input signal applied to both an IA and MDAC, and combining both at the summing junction of one of the OA's, an integer gain of 1 to 10 plus the fractional gain as a result of the MDAC attenuation is added together to achieve any gain value from -11 to +11 with a resolution of greater than 0.01 throughout, for a total of more than 2,500 gain settings. See the section on increasing MDAC resolution for more information using the MDAC's as fixed references.

More details about MDAC performance are found in the specifications section of the data sheet. It should be noted that the specifications of the MDAC's in regard to bandwidth, gain and offset errors, and drift over temperature are equivalent to or better than those of the IA's themselves. This means that in addition to having the same high-impedance characteristics of the IA's, the MDAC's will perform in an equivalent fashion when used in combination with the IA's as signal conditioning elements. Predictable performance thereby results when mixing various combinations of input resources together.

Table 2. Outputs vs. Digital Input Code

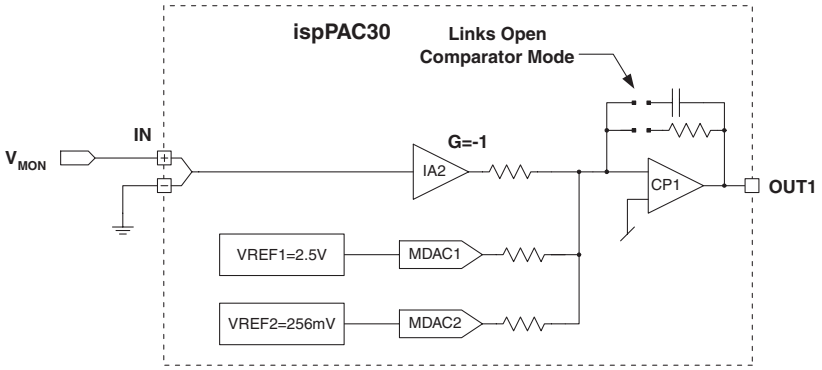
Code		MDAC Equivalent Voltage Output vs. VREF Input (in Volts)								
DEC	**HEX**		**0.0640**	**0.128**	**0.256**	**0.512**	**1.024**	**2.048**	**2.5000**	**Vref Input (V)**
0	00	-100.0%	-0.0640	-0.128	-0.256	-0.512	-1.024	-2.048	-2.5000	Full Scale
1	01	-99.2%	-0.0635	-0.127	-0.254	-0.508	-1.016	-2.032	-2.4805	Full Scale + 1 lsb
32	20	-75.0%	-0.0480	-0.096	-0.192	-0.384	-0.768	-1.536	-1.8750	
64	40	-50.0%	-0.0320	-0.064	-0.128	-0.256	-0.512	-1.024	-1.2500	
96	60	-25.0%	-0.0160	-0.032	-0.064	-0.128	-0.256	-0.512	-0.6250	
127	7F	-0.8%	-0.0005	-0.001	-0.002	-0.004	-0.008	-0.016	-0.0195	Bipolar Zero - 1 lsb
128	80	0.0%	0.0000	0.000	0.000	0.000	0.000	0.000	0.0000	Bipolar Zero
129	81	0.8%	0.0005	0.001	0.002	0.004	0.008	0.016	0.0195	Bipolar Zero + 1 lsb
160	A0	25.0%	0.0160	0.032	0.064	0.128	0.256	0.512	0.6250	
192	C0	50.0%	0.0320	0.064	0.128	0.256	0.512	1.024	1.2500	
224	E0	75.0%	0.0480	0.096	0.192	0.384	0.768	1.536	1.8750	
254	FE	98.4%	0.0630	0.126	0.252	0.504	1.008	2.016	2.4609	+Full Scale - 1 lsb
255	FF	99.2%	0.0635	0.127	0.254	0.508	1.016	2.032	2.4805	+Full Scale
—	—	0.78%	0.00025	0.0005	0.001	0.002	0.004	0.008	0.0098	1 lsb (with sign)
—	—	1.56%	0.00050	0.0010	0.002	0.004	0.008	0.016	0.0195	2 lsb (1 lsb, no sign)

Increasing MDAC Effective Resolution

Because the value of the ispPAC30's voltage references can be set to several output voltages, ranging from 64mV to 2.5V, it is possible to use high-value MDAC settings (>50% full scale) to synthesize most desired thresholds. This means that a given threshold (32mV or greater) can be set with a resolution of +/-0.8%.

If a higher degree of resolution is needed, the two voltage references and MDACs can be combined in a coarse-fine adjustment scheme, as shown in Figure 1. In this circuit, VREF1 and MDAC1 provide an adjustment range of 0-2.5V with 19.5mV of resolution, while VREF2 and MDAC2 provide an adjustment range of +/-64mV with 0.5mV of resolution. By adding these two sources together, a total adjustment range of 0-2.56V with an effective resolution of 0.5mV is achieved.

Figure 1. Coarse-Fine Adjustment using Two References



In this example, the effective resolution provided by combining the two references would normally require a 13-bit DAC to replicate. Keep in mind, however, that resolution is not the same as accuracy. The absolute accuracy provided by an ispPAC30 using this technique is approximately equivalent to that provided by a 10-bit DAC.

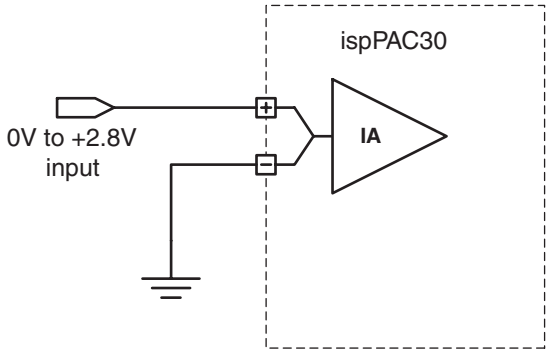
In many situations, such as those in which a parameter is being interactively adjusted for optimal performance, absolute accuracy may not be of paramount importance. In this case, stability and resolution of the adjustment are more important than the absolute accuracy of the adjustment.

Interfacing to ispPAC Inputs

As mentioned in the previous IA section, any input voltage between 0 to 2.8V can be applied directly to an ispPAC30 input. To keep the output from trying to swing below 0V, if Vin- is more positive than Vin+, an offsetting signal must be applied to the appropriate summing node to balance or counteract the negative input. Single-ended connections, however, only require that the minus input be connected to 0V or some other fixed voltage. More information on inputting signals to ispPAC30 can be found in application note AN6026, *Interfacing to ispPAC Differential Inputs*.

Although differential signaling offers many significant benefits in a design, most analog designs today still use single-ended signals where system 'ground' is used as a global zero-volt reference. The differential inputs provided on ispPAC products provide more than enough flexibility to accommodate single-ended signals.

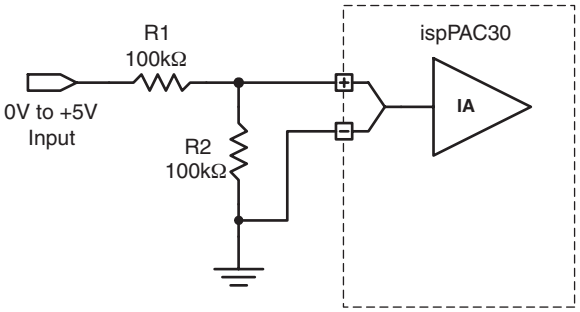
Figure 2. DC Coupling a Single-ended Signal



When using an ispPAC30 with a single-ended input (Figure 2), tie the unused terminal to a reference voltage. Since the common-mode input range for the ispPAC30 includes ground, the minus input is most often connected there. This results in an internal signal value which corresponds directly to the input signal voltage (e.g. a +1.67V input results in +1.67V of signal internally). When using an ispPAC30 in this manner, it will accommodate single-ended input signals ranging from 0V to +2.8V.

In systems operating from single +5V supplies, it is often desirable to be able to accommodate rail-to-rail signals, which range from ground to the positive supply voltage (+5V). Figure 3 shows an interface circuits that allows ispPAC30 inputs to accept 0-5V signals, where R1 and R2 divide down the signal input.

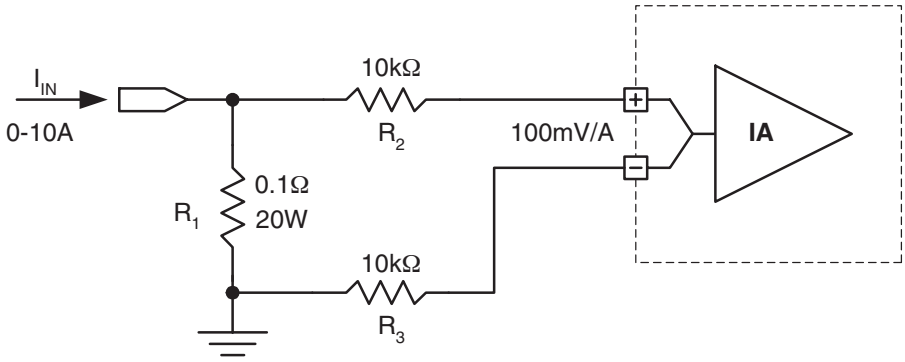
Figure 3. Interfacing to a 0-5V DC Signal



A Ground-Based Current Sense Technique

Because the ispPAC30's common-mode input range extends down to ground, this part is straightforward to use in applications with ground-referenced signals. An example of such an application is the current sensor shown in Figure 4. A 0-10A current input develops a voltage ranging from 0-1V across the 0.1Ω sense resistor. This application also illustrates one of the primary benefits of differential signal processing. Although one can sense the voltage at the resistor's input terminal with a single-ended amplifier, this assumes that the ground terminal of the resistor is really at ground. At ampere-level currents, this is a big, and often unwarranted assumption which can result in significant measurement errors. By sensing the actual voltage at both resistor terminals one can avoid this source of measurement error.

Figure 4. ispPAC30 Sensing Differential Signals Near Ground



In this particular application, where high currents are being measured, there may be the possibility that the voltages at the resistor terminals exceed those that the ispPAC30 can safely handle. If the input voltage becomes lower than -0.6V or higher than +5.6V, input protection diodes inside the device will begin to turn on and shunt input current to either ground or the positive power supply. In this case, since amperes of current are potentially available, significant damage to the ispPAC30 could result if this occurs. Resistors R2 and R3 protect against this possibility, by limiting maximum input current to safe levels (milliamperes) that the device's input protection networks can readily handle.

Voltage Reference Output

The 2.5V voltage reference output of the ispPAC30 ($VREF_{OUT}$) has a high impedance voltage output which should be buffered when using it as an external reference to drive other circuitry. It also should always be decoupled using the recommended capacitor specified in the pin description table of this data sheet. If it is used to reference a high impedance source (e.g., one that does not require more than 40μA), the $VREF_{OUT}$ output can be connected to it directly. An example is shifting the DC level of a signal connected to the input pin of an ispPAC30. Also, by using a current limiting resistor with the $VREF_{OUT}$ pin, it may also be used without buffering and still provide a DC reference. Check the ispPAC applications literature for numerous examples of these and other useful techniques for using $VREF_{OUT}$. Note: If the $VREF_{OUT}$ pin is overloaded or disturbed, it will adversely affect the operation of the rest of the ispPAC30.

Output Amplifiers

The ispPAC30 has two output amplifiers, or OA's. The single-ended outputs of these amplifiers swing from 0V to +5V and are hard-wired internally to the output pins. In addition, the outputs are also routed and available for connection as inputs to any of the input IA's or MDAC's. Each OA can be configured independently to function as either a full-bandwidth amplifier, a low-pass filter, an integrator or a comparator. All these configuration choices are accessed by the user via the PAC-Designer design entry software. They can also be reconfigured along, with any other part of the ispPAC30, using JTAG or SPI serial interface control to directly communicate with the device.

In addition to the multiple functions possible with the OA's, another unique feature is that any or all of the IA's and MDAC's can be selectively routed to either of the OA summing nodes. This provides the maximum amount of flexibility to the user over how the device is ultimately configured. IA's can be connected in parallel to one OA or the

other as necessary to achieve higher gains, for example. Precision gain and offset configurations can be implemented using different combinations of IA's, MDAC's and VREF's to condition signals using a common summing junction to deliver the desired output result. The combination of analog input and summing node route options make the ispPAC30 very powerful in enabling so many different circuit possibilities. Examples of possible circuits are included in the ispPAC30 applications literature.

Output Amplifier Functional Modes

The ispPAC30 output amplifiers (OA's) can be configured to act as wideband amplifiers, lowpass filters, integrators or comparators. Each mode is determined by SRAM (or E^2 configuration memory at turn-on) control bits that open and close feedback elements around the OA's. All available modes of OA operation can be configured during the design phase using PAC-Designer software or during normal operation via JTAG or SPI serial interface control.

Amplifier/Filter Mode

When configured as a wideband amplifier, an ispPAC30's OA feedback resistor connection is closed and the feedback capacitor set to its minimum value. The feedback capacitance set is required to maintain necessary stability. When used in filter mode, the ispPAC30 differs from the wideband amplifier in that it has seven alternative feedback capacitor values available to form the lowpass filter corner frequencies. See Table 3 for these values (listed as the maximum corner frequencies in the precision filter range table). The capacitor values are trimmed for each device to achieve an absolute pole frequency with an accuracy guaranteed to that given in the specifications section. The first order filter formed using the OA in this manner is not the only way a filter can be implemented using the ispPAC30. In the following precision filtering section, an example is given for using an OA in integrator mode and providing proportional feedback by putting one of the MDAC's into the feedback loop. When calculating equivalent time constants for ispPAC30 in filter mode, a nominal resistance of 50kΩ can be assumed. The frequencies called out in PAC-Designer that are associated with individual feedback capacitor values are computed based on the measured –3dB frequency of a single IA/OA combination (gain=1). Again, absolute accuracy is guaranteed as listed in the filter specifications section for all devices shipped.

Integrator Mode

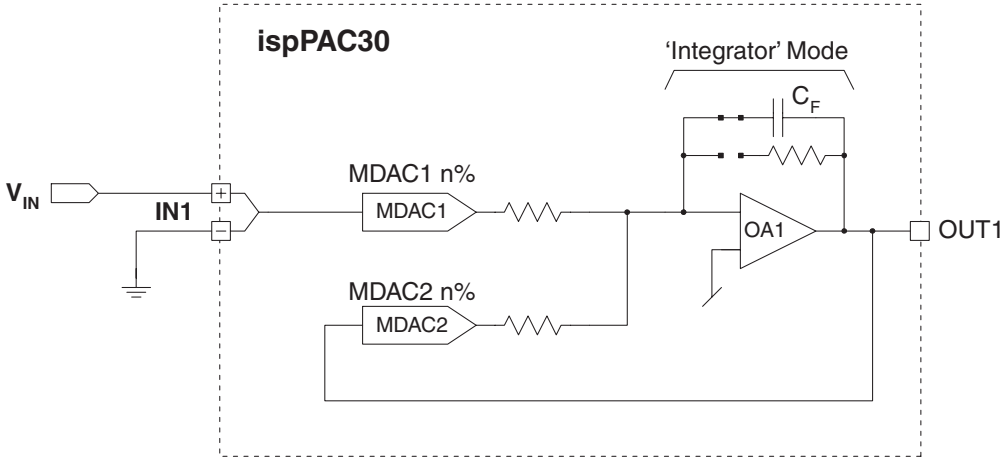
In integrator mode, an OA's feedback capacitor is closed and the feedback resistor is open. Operation then becomes that of an integrator, with the expected non-ideal effects of a real operational amplifier (having finite gain-bandwidth properties). The gain-phase simulator in the PAC-Designer will give the user a very good representation of these first-order effects on ideal operation. The effective time-constant of any given integrator configuration can be computed knowing the feedback capacitor value and that an IA in a gain =1 will yield an effective input resistance, R, equal to 50kΩ (1 time constant = 2 x π x RC). This value of R is divided by the gain setting of the IA, so in a gain of 10 for example, R is equal to 5kΩ. When an MDAC is used as the input to an OA configured as an integrator, the effective R is equal to 50kΩ divided by the fraction of the input signal passed by the MDAC. For example, if the MDAC is set to a code that results in passing 50% of the input signal, then R is equal to 50kΩ/0.5 or 100kΩ. This can, of course, be used to advantage to either extend the effective time constant range or to fine tune it.

Comparator Mode

In comparator mode, both the feedback capacitor and resistor are opened around the OA. Also, the internal compensation of the OA is altered to improve comparator output characteristics. Since only one input is available to the OA in comparator mode, instead of the normally expected two, a slightly different approach is required to realize a true comparison function. This is done by using the reference voltage and summing it with the value it is to be compared with. Whenever the input to be compared is greater than the reference input value the OA output is high and when it is less, the OA output is low. The logic sense of this comparator output can be controlled at will by selecting either plus or minus gains in the IA/MDAC input sections. When examined closely, it may be observed that comparator mode operation appears identical to that of the integrator mode with a minimum feedback capacitance. This is true except in comparator mode the output compensation of the OA is altered to get optimum switching times. That means using the OA in other linear modes without this compensation enabled will likely result in unstable operation. In PAC-Designer, the default configuration modes will not allow this to happen.

Precision Filter Configuration

Figure 5. Using the ispPAC30 as a Variable Lowpass Filter with Extended Frequency Range



Other filter frequencies are possible, in addition to the simple first order filters available by selecting the seven available capacitors of each ispPAC30 output amplifier. The ispPAC30 can be used to implement 1st-order tunable lowpass filters over a range of 5kHz to over 600kHz.

Figure 5 shows the circuit for doing so. This circuit operates by using MDAC2 to emulate a programmable feedback resistor around output amplifier OA1. In this technique, the effective feedback resistance is inversely proportional to MDAC gain. Because negative feedback is essential to maintaining a stable loop, MDAC2's gain must be set to only negative values.

In addition to decreasing the closed-loop bandwidth of OA1, fractional feedback gain also increases the closed loop DC gain. This increase must be compensated for if the filter is to maintain unity gain from input to output. Because there are two MDACs in an ispPAC30, one way to do this is to attenuate the input signal through MDAC1 by the same amount the feedback signal is attenuated by MDAC2. To maintain signal polarity, however, MDAC1 should be set to a positive gain. Deliberately mismatching the values of MDAC1 and MDAC2 also allows one to alter the gain dynamically, providing a variable gain control feature. The following expressions can be used to estimate the resulting corner frequency (F_C) and gain, where F_{CAP} is the frequency associated with the feedback.

$$F_C = |F_{CAP}\,MDAC2(n\%)| \quad (1)$$

$$Gain = |MDAC1(n\%) / MDAC2(n\%)| \quad (2)$$

Note that MDAC2 (n%) must be negative, and that MDAC1 (n%) should normally be positive for the single-ended system shown in Figure 5.

Although this technique can be used to control the corner frequency over a range of 128:1, the attenuation caused by a very low MDAC1 setting can reduce the filter's overall signal-to-noise ratio and increase effective DC offset and gain errors to unacceptable levels. Table 3 shows the ranges of corner frequencies that can be realized with this technique when limiting MDAC2 settings between -10.16% and -100%.

Table 3. Precision Filter Configuration Ranges

Feedback Capacitor #	OA1 Feedback Capacitor Value (pF)	Minimum Corner Frequency (kHz)	Maximum Corner Frequency (kHz)	Frequency Step (kHz)
1	4.320pF	63	619	4.86
2	7.156pF	41	401	3.13
3	11.97pF	25	250	1.95
4	18.16pF	17	169	1.31
5	27.29pF	11	114	0.88
6	42.37pF	7	74	0.58
7	64.01pF	5	49	0.38

Power-Down Mode

The ispPAC30 features a power-down mode whereby the current consumption of the device is reduced to a few microamps. In this mode, the logic sections of the device are still fully active, but draw very little power. This means communication can be maintained with the device while it is in the powered-down state. In the analog sections, the bias currents are reduced or turned off and all sections that can be, are shut down. The analog outputs go to a high impedance state in power-down mode. The maximum current in shutdown mode and the time required to resume normal operation all are specified in the specifications section of this data sheet. Programming or erasing of the E^2 configuration memory is not supported when an ispPAC30 is powered down. Power-down mode is commanded by lowering the $\overline{PD}$ pin to a logic low, or by commanding it through JTAG or SPI serial mode commands.

In addition to full power-down mode, either of the output amplifiers can be shut down independently of all other circuitry. This can be done at any time by setting internal E^2 bits under JTAG or SPI command to reduce power consumption while the rest of the ispPAC30 is in normal operation. This could also be accomplished at the time the device is programmed initially via dialog box commands available in the PAC-Designer software. Note: Any IA or MDAC that has nothing connected to its input is also automatically shut down.

JTAG User Configurable Bits

There are a number of user-configured E^2 bits that control all aspects of ispPAC30. These bits can all be accessed somewhere in either the pull-down menus or directly in the schematic design entry screen of the PAC-Designer software used to interface to the ispPAC30. See the online help associated with the ispPAC30 in PAC-Designer for more details of how to set/program various operation modes. The list of control E^2 bits available are listed in Tables 4 and 5.

Table 4. JTAG Configuration Register (CFG) Bits

Symbol	Name	Description
ARP Bits	Analog Routing Pool Bits	These various bits control the interconnect from input pins to IA's and MDACs, as well as where the VREF's go and which input resources are summed with one OA or the other and whether those OA's are fed back to any of the input cells.
CALSEL	CAL Level Select	Any of the six input devices, IA1, IA2, IA3, IA4, MDAC1 and MDAC2 can be selected independently to have auto calibration performed with 0V (default) or 2.5V applied to their inputs. Because of common-mode errors, choose the level closest to the operating levels for the lowest offset after an auto-cal operation.
ENSPIPU	Enable SPI Mode Pull-up	This bit can set the device for dedicated SPI mode operation without any external strapping of the pin being required. Note that normal JTAG operations cannot occur, such as programming by PAC-Designer when SPI mode is enabled.
FBCAP	Feedback Capacitor	Bits to control the seven capacitors of each of OA's.
IAGAIN	Input Amplifier Gain	These bits determine the gain of IA1, IA2, IA3, and IA4 (from 1 to 10).
IAPOL	Input Amplifier Polarity	These bits determine polarity of IA1, IA2, IA3, and IA4 (positive or inverted).
MDACCode	MDAC Code	Bits to control the code settings of MDAC1 and MDAC2.
MSELPOL	MUX Select 1 & 2 Polarity	Determines via programmed bits whether a logic high activates input a or b of either of the multiplexers in front of IA1 and IA4.
MSELPU1/2	MUX Select 1 & 2 PU/PD	Programs whether MSEL1 and MSEL2 have internal pull-ups or pull-downs.
OACFG	Output Amp Configuration	Determines through various bits whether OA1 and OA2 are acting as filters (both feedback resistor and capacitor in circuit), or as integrators (only the capacitor in feedback), or as comparators (neither feedback resistor or capacitor in circuit).
OAPD1/2	Output Amp Power-Down	Either or both of the output amplifiers can be commanded in power-down mode without the rest of the chip having to be powered down. In this state, their outputs are effectively in high-impedance mode.
PU/PD Bits	Pull-Up/Down	A number of pins on the PAC30 have internal, programmable pull-up and pull-down capability. See the pin description table in the specification section for details on which pins and their default (shipped) states.
TDOSlew Bit	TDO Slew Rate	The serial digital data output pin has two output slew rates. The default is low to reduce digital disruption of the analog circuitry. Sometimes a higher slew rate is needed, so it is provided as a programmable option.
VREF1, VREF2	Voltage References 1 and 2	These bits set any of the seven available voltage outputs of VREF1 and VREF2.

Table 5. JTAG UES Register and ESF Bits

Symbol	Name	Description
UES Bits	User Electronic Signature	These are uncommitted E^2 bits that can be used to store device information for future reference. The ispPAC30 contains 16 UES bits. These bits are accessible from within PAC-Designer by using the Edit Symbol, UES Bits command.
ESF	Electronic Security Fuse	Setting this bit causes all subsequent readouts of the device configuration to be disabled (JTAG Verify commands). Can be reset by performing a JTAG user bulk erase command and reprogramming the device. This feature is used to prevent unauthorized readout of the device's configuration.

Auto-Calibration Mode

Every time the ispPAC30 is powered up, an automatic auto-calibration sequence is initiated. If this adversely affects system operation, provisions must be incorporated that minimize the result as auto-calibration cannot be defeated. The auto-calibration of the ispPAC30 effectively isolates it from external connections and drives the inputs of the device to 0V and checks to see that there is zero offset at the outputs. This check is done maintaining the input-to-

output relationships determined by the current circuit configuration, or in the case of initial turn-on, the stored configuration of the device. During the auto-calibration sequence, the output amplifiers are driven to 0V and any offset error from input to output is calibrated out during a successive-approximation sequence using an internal offset calibration DAC. This calibration setting is not stored in E^2, hence the need to perform calibration every time the device is powered on. The ground reference for auto-calibration is the SCOM pin. The SCOM pin must be connected to the GND pin (0V), preferably in a ground plane. Since SCOM must be at, or very near the same potential as GND, connection to any other point is not recommended.

In addition to the automatic power-on calibration, an auto-calibration sequence can be commanded at any time using the external CAL logic pin, or by issuing an ENCAL command via the JTAG or SPI serial interface. The timing and length of the auto-calibration sequence is called out in the specification tables of this data sheet.

Note: Two options are available for calibrating each of the four input IA's and two MDACs, with respect to what input level is used for auto-calibration. Normally, the inputs are calibrated with a 0V input reference (the default setting). But when the input common mode voltage is recognized to be closer to 2.5V, the user can specify that 2.5V be set as the input calibration level. The IA/MDAC inputs can be set to use any combination of 0V or 2.5V as their auto-cal common-mode reference. This allows the least amount of common-mode error to enter into the offset adjustment, dependent on the user's predetermined operating conditions.

SPI vs. JTAG Operation

The JTAG serial interface is usually sufficient for programming the ispPAC30, but complete support is also provided for the Serial Peripheral Interface (SPI) mode as well. SPI is often chosen when an embedded μController or μProcessor is used to actively control and configure an ispPAC30 in-system. SPI mode can be enabled via the logic level setting of the ENSPI pin. To achieve full control of an ispPAC30, all possible bits used in configuration (112) must be set each time the configuration is updated. This full set of configuration bits is referred to as the CFG or configuration register. There is also a shorter configuration register called the CFGQ or quick configuration register (40 bits). Here, only the bits most often used in reconfiguration are accessed. Less commonly used bits, such as those which determine routing, are left out to simplify and speed up the serial transfer of data. Detailed information about SPI mode operation is found in application note AN6027, which is devoted entirely to the subject of SPI control.

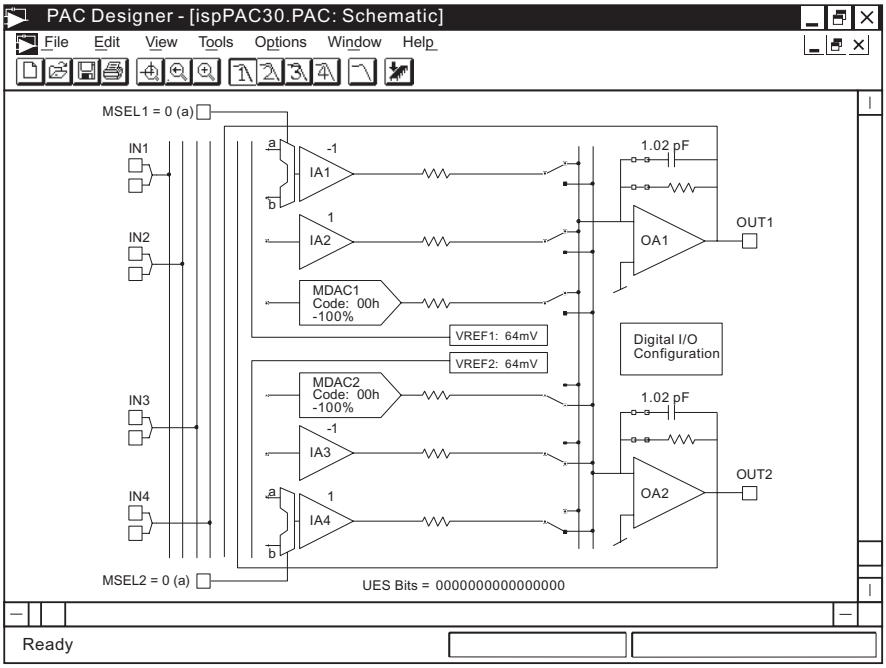
Software-Based Design Environment

Design Entry Software

Designers configure the ispPAC30 and verify its performance using PAC-Designer, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispPAC30. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available on the Lattice web site for downloading. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation.

The PAC-Designer schematic window, shown below in Figure 6, provides access to all configurable ispPAC30 elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground, VREFOUT, and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved, simulated, and downloaded to devices.

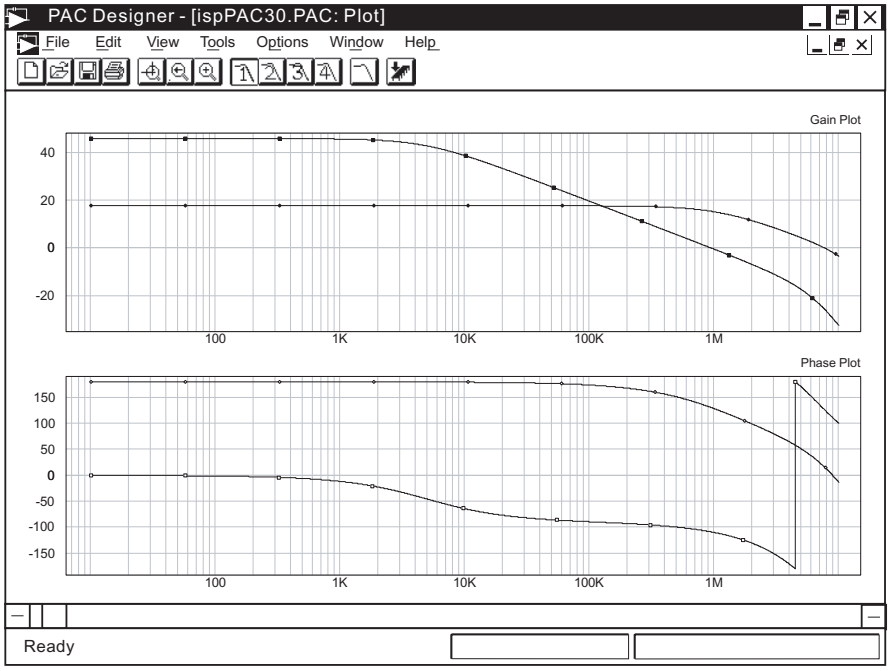
Figure 6. PAC-Designer Design Entry Screen



Design Simulation Capability

A powerful feature of PAC-Designer is its simulation capability, enabling quick and accurate verification of circuit operation and performance. Once a circuit is configured via the interactive design process, gain and phase response between any input and output can then be simulated. This function is part of the simulator capability which derives a transfer equation between the two points and then sweeps it over the user-specified frequency range. Figure 7 shows a typical screen plot of the gain/phase simulator.

Figure 7. PAC-Designer Simulation Plot Screen



In-System Programming

The ispPAC30 is an in-system programmable device. This is accomplished by integrating all E^2 configuration memory and SRAM control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^2CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispPAC30 instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^2CMOS memory of the ispPAC30. This consists of 16 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispPAC30 device to prevent unauthorized readout of the E^2CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

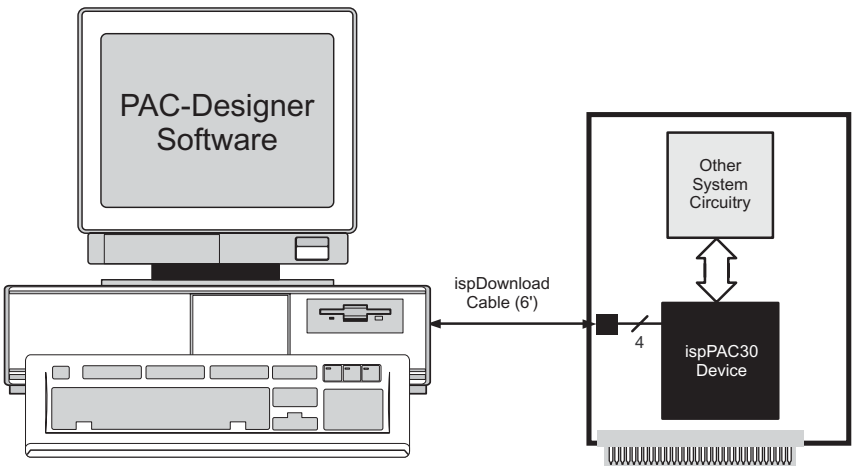
Production Programming Support

Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispPAC30 Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice download cable. It demonstrates proper layout techniques for the ispPAC30 and can be used in real time to check circuit operation as part of the design process. Input and output connections as well as a “breadboard” circuit area are provided to speed debugging of the circuit. This board is also useful as a programming fixture for prototype and short production runs.

Figure 8. Download to a PC



IEEE Standard 1149.1 Interface

Serial Port Programming Interface Communication with the ispPAC30 is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispPAC30 as a serial programming interface, and not for boundary scan test purposes.

There are no boundary scan logic cells in the ispPAC30 architecture. This does not prevent the ispPAC30 from functioning correctly, however, when placed in a valid serial chain with other IEEE 1149.1 compliant devices.

A brief description of the ispPAC30 JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (which now includes IEEE Std 1149.1a-1993). For complete documentation on how to use ispPAC30 in an embedded serial interface control environment using the SPI protocol, please refer to application note AN6027, *Using SPI to Configure and Control the ispPAC30*.

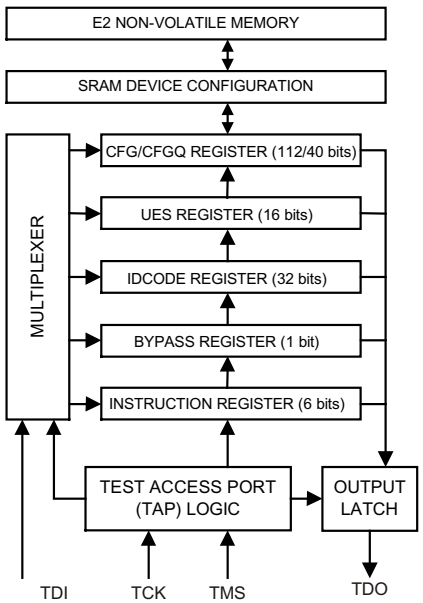
Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispPAC30. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration or the ispPAC30. A separate set of SRAM registers are preloaded at turn-on and determine the configuration of the ispPAC30 while it is under power. By cycling the TAP controller through the necessary states, data can also be shifted out of the configuration register to verify the current ispPAC30 configuration in the control SRAM or of the stored E^2 configuration memory. Instructions exist to access all data registers and perform other internal control operations.

For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. For ispPAC30, the bypass register is a 1-bit shift register that provides a short path through the device when boundary testing or other operations are not being performed. The ispPAC30, as mentioned, has no boundary scan logic and therefore no boundary scan register. All instructions relating to boundary scan operations place the ispPAC30 in the BYPASS mode to maintain compliance with the specification. The optional identification register described in IEEE 1149.1 is also included in the ispPAC30.

Two additional data registers are included in the TAP of the ispPAC30 are the Lattice defined CFG/CFGQ (configuration and quick configuration) and UES (user electronic signature) registers. Figure 9 shows how the instruction and various data registers are placed in an ispPAC30.

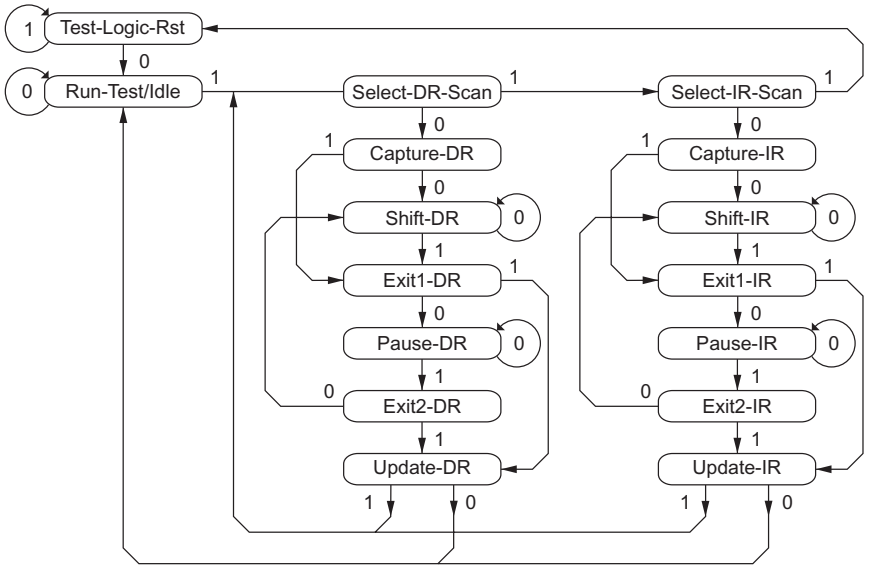
Figure 9. TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 10. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run-Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 10. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain.

From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispPAC30 contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified. For ispPAC30, the instruction word length is six bits. All ispPAC30 instructions available to users are shown in Table 6.

Table 6. ispPAC30 TAP Instructions Table

Instruction	Code	Description
EXTEST	000000	External Test. Defaults to BYPASS.
ADDCFG	000001	Address CFG data register (112 bits).
ADDCFGQ	000010	Address CFG Quick data register (40 bits).
ADDUES	000011	Address UES data register (16 bits).
LATCHCFG	000101	Latch CFG register into control SRAM.
READCFG	000110	Read CFG from E^2 prior to ADDCFG command.
READUES	001010	Read UES from E^2 prior to ADDUES command.
PROGUES	001011	Program shift register contents into UES E^2.
PROGCFG	001100	Program shift register contents into CFG E^2.
IDCODE	001101	Address Identification Code data register.
PROGESF	010001	Program the Electronic Security Fuse bit.
POWERDN	010010	Command a Power Down sequence.
POWERUP	010011	Command a Power Up sequence.
RELOADCFG	010110	Load CFG E^2 into control SRAM.
ERASECFG	010111	Erase the CFG/CFGQ E^2 memory.
ERASEUES	011011	Erase the UES E^2 memory.
ENCAL	011100	Enable a Calibration sequence.
CFGBE	011101	Bulk erase all E^2 memory (CFG, UES and ESF).
SAMPLE	011110	Sample/Preload. Default to BYPASS.
BYPASS	111111	Bypass (connect TDI to TDO).

BYPASS is one of the three required JTAG instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispPAC30. The bit code of this instruction is defined to be all ones by the IEEE 1149.1 standard. With ispPAC30, any instruction beginning with a one will default to BYPASS.

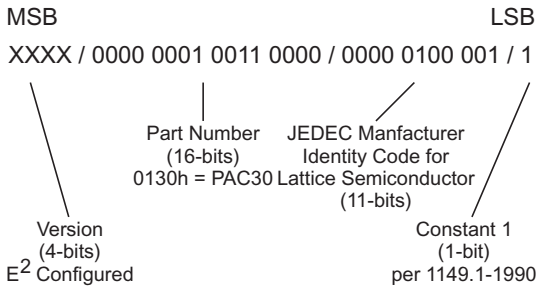
The JTAG required SAMPLE/PRELOAD instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The ispPAC30 has no boundary-scan register, so for compatibility it defaults to the BYPASS mode whenever this instruction is received. The bit code for this instruction is defined by Lattice as shown in Table 6.

The EXTEST (external test) instruction is JTAG required and would normally place the device into an external boundary test mode while also enabling the Boundary-Scan Register to be connected between TDI and TDO. Again, since the ispPAC30 has no boundary-scan logic, the device is put in the BYPASS mode to ensure specification compatibility. The bit code of this instruction is defined by the 1149.1 standard to be all zeros.

The optional IDCODE (identification code) instruction is incorporated in the ispPAC30 and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (see Figure 12). Access to the Identification Register is immediately available, via a TAP data

scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 6.

Figure 12. ID Code



ispPAC30 Specific Instructions

There are three unique address instructions specified by Lattice for the ispPAC30. They are ADDCFG (address CFG), ADDCFGQ (address the CFG quick, or short register), and ADDUES (address the UES or user electronic signature register). They all select their respective registers to be shifted into through TDI during a Shift-DR operation. Normal operation of a device is not interrupted by the execution of these instructions. They usually proceed a program instruction (PROGCFG, or PROGUES) for putting the shifted data into E^2 configuration memory or a load (LATCHCFG) for putting data into the device control SRAM directly. The bit codes for these instructions are found in Table 6.

There are three unique program instructions specified by Lattice for the ispPAC30. They are PROGUES (program UES), PROGCFG (program CFG), and PROGESF (program the electronic security fuse bit). The first two store their respective registers into E^2 configuration memory. The third, PROGESF, has no register associated with it. It simply sets the ESF bit so shifting out CFG information is no longer possible. The only way to recover the ability to shift out meaningful data is to reset ESF by performing a CFGBE instruction. This, of course will reset the device configuration as well, but will keep an unauthorized user from learning the bit pattern of the device. Normal operation of the device is not interrupted during the actual programming time. A programming operation does not begin until entry of the Run-Test/Idle state. The programming time required to insure data retention is given in the timing specifications. The user must ensure that the recommended programming times are observed to ensure specified data retention. Note: When initially programming or reprogramming the ispPAC30 with software other than PAC-Designer, or an authorized third-party programmer (e.g., via microcontroller), refer to the additional Lattice technical literature covering the required algorithms necessary for complete JTAG and SPI device programming control of the ispPAC30 (specific bit assignments, word lengths, etc.).

There are two unique load instructions specified by Lattice for the ispPAC30. They are the LATCHCFG (load CFG register) and RELOADCFG (load CFG from E^2). These instructions load the data in either the CFG register or the stored E^2 configuration into the ispPAC30 device control SRAM. The LATCHCFG updates all or a portion of the control SRAM, depending on whether the preceding address CFG was an ADDCFG or ADDCFGQ instruction. The load operation does not occur until entry of the Run-Test/Idle state. Settling time for the new configuration will depend on the configuration and time-constants of the particular circuit and can be anywhere from microseconds to milliseconds. The actual switching to make the change, however, always occurs in less than a microsecond once the Run-Test/Idle state is entered. The bit codes for these instructions are shown in Table 6.

There are two unique read instructions specified by Lattice for the ispPAC30. They are the READCFG (read CFG) and READUES (read user electronic signature). These instructions read data out of the corresponding E^2 configuration memory into either the CFG or UES register. This is done in preparation for either an ADDCFG or ADDUES and then a subsequent shifting out of the data in these registers. Normal operation of a device is not interrupted by the execution of these instructions. The bit code for these instructions are shown in Table 6.

The ENCAL (enable calibration) is a unique Lattice instruction that enables the start of an auto-calibration sequence. This operation causes both output amplifiers to go to 0V until the calibration sequence is completed

(see timing specifications). As with the programming instructions above, calibration does not begin until entry of the Run-Test/Idle state. The completion of the calibration is not dependent, however, on any further TAP control. This means the state of the TAP can be returned immediately to the Test-Logic-Reset state. The only consideration would be to not clock the TAP during critical analog operations. The first several milliseconds of the calibration routine are consumed waiting for configurations to settle, though, leaving more than enough time to clock the TAP back to the Test-Logic-Reset state. The bit code for this instruction is shown in Table 6.

The POWERDN (power down command) and POWERUP (power up command) are unique instructions specified by Lattice for the ispPAC30 to command the normal and low-power or shut-down states of the device. As with other instructions above, these instructions do not begin until entry of the Run-Test/Idle state. Timing for coming out of power-down mode as well as supply current used in this mode are specified in the spec tables of this data sheet. All analog is shut down and outputs are in a high-impedance mode during power-down state. Device digital circuitry is not shut down and consumes no power unless it is clocked, and even then only a minimal amount. The bit code for these instructions is shown in Table 6.

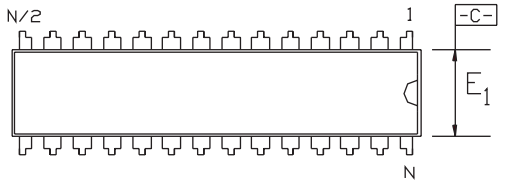
The last unique Lattice instructions are ERASECFG (erase or clear CFG), ERASEUES (erase or clear the UES) and CFGBE (erase or clear all user memory). These instructions set all the bits of their respective E^2 storage cells to all zeros. Operation of the device is not interrupted during any of these instructions. The CFGBE is used to return all user controlled bits to a zero state at the same time (CFG, UES and ESF) and is the only way to erase the ESF bit. The condition after a CFGBE instruction is the default condition of parts shipped from the factory. The same programming timing constraints apply to these instructions as for the PROG programming instructions listed above. The bit code for these instructions are shown in Table 6. Important Note: Programming E^2 configuration memory can only program ones into a device, not zeros. Erase instructions are required to change all bits to zero first. The normal sequence to re-program E^2 configuration memory is first erase either the CFG or UES E^2 cells and then program them with the desired bit sequence and PRG instructions.

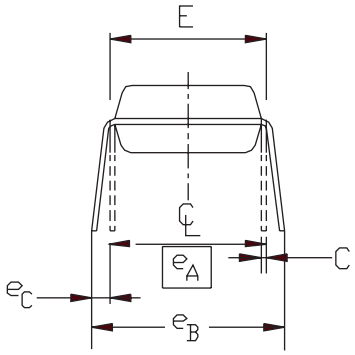
Once again, the JTAG PROG, LATCHCFG, ERASE, POWERUP, POWERDN, RELOADCFG and ENCAL instructions do not execute until entry of the Run-Test/Idle state. All other instructions are executed in the Update-IR state, allowing shifts and other operations to occur without having to leave the inner loop of the JTAG controller.

It is recommended that when all serial interface operations are completed, the TAP controller be reset and left in the Test-Logic-Reset state (the power-up default) and the TCK and TMS inputs idled. This will insure the best analog performance possible by minimizing the effects of digital logic “feed-through.”

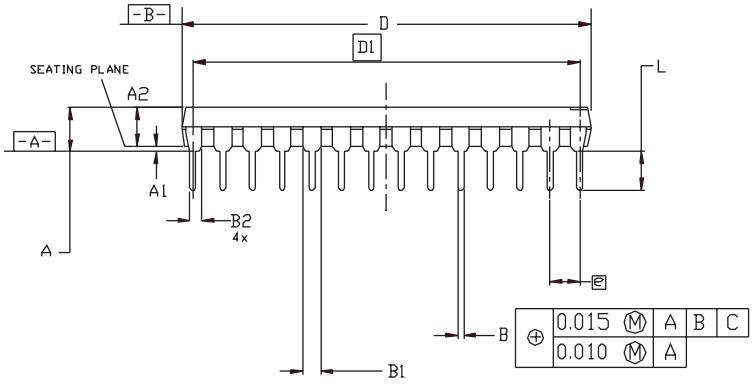
Package Diagrams

28-Pin PDIP (Dimensions in inches)





SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	–	–	.180
A1	.015	–	–
A2	.120	.135	.150
B	.014	.018	.022
B1	.045	.050	.060
B2	.030	.040	.045
C	.008	.010	.015
D	1.345	1.365	1.385
D1	1.300 BSC		
E	.300	.310	.325
E1	.275	.285	.295
e	.100 BSC		
eA	.300 BSC		
eB	–	–	.430
eC	.000	–	.060
L	.110	.130	.150
N	28		



24-Pin SOIC (Dimensions in millimeters)

	MIN.	MAX.
A	2.35	2.65
A1	.10	.30
B	.33	.51
C	.23	.32
D	15.20	15.60
E	7.40	7.60
e	1.27 BSC	
H	10.00	10.65
h	.25	.75
L	.40	1.27
N	24	
α	0°	8°