

Ultra-Low Power Stereo CODEC with Audio Enhancement DSP, 1W Stereo Class D Speaker Drivers and Ground Referenced Headphone Drivers

DESCRIPTION

The WM8962 is a low power, high performance stereo CODEC designed for portable digital audio applications.

An integrated charge pump provides a ground referenced output which removes the need for DC-blocking capacitors on the headphone outputs, and uses the Wolfson 'Class-W' amplifier techniques - incorporating an innovative dual-mode charge pump architecture - to optimise efficiency and power consumption during playback. A DC Servo is used to reduce DC ground offsets. This improves power consumption and minimises pops and clicks.

Stereo class D speaker drivers provide 1W per channel into 8Ω loads, or 2W mono into a 4Ω load, with a 5V supply. Low leakage, excellent PSRR and pop/click suppression mechanisms also allow direct battery connection to the speaker supply. Flexible speaker boost settings allow speaker output power to be maximised while minimising other analogue supply currents.

Control sequences for audio path setup can be pre-loaded and executed by an integrated sequencer to reduce software driver development and eliminate pops and clicks via Wolfson's SilentSwitch™ technology.

Flexible input configuration: four stereo inputs or eight mono inputs on Left or Right ADC, with a complete analogue (four single-ended stereo inputs) and digital microphone interface. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input.

Stereo 24-bit sigma-delta ADCs and DACs are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio interface.

A programmable audio enhancement DSP is included with multiple preset algorithms. Virtual Surround Sound widens the stereo speaker audio image, HD Bass enhances low frequencies, and ReTune™ flattens the frequency response of the speaker or microphone path. A configurable DSP includes additional functions such as 3D widening for recording, a 5-band parametric EQ and Dynamic Range Controller.

Two high performance PLLs and one Exact Fractional Synthesis (EFS) FLL are integrated to enable the user to clock a full audio system.

The WM8962 operates at analogue supply voltages down to 1.7V, although the digital supplies can operate at voltages down to 1.62V to save power. The speaker supply can operate at up to 5.5V. Unused functions can be disabled using software control to save power.

The WM8962 is supplied in a very small W-CSP package, ideal for use in hand-held and portable systems.

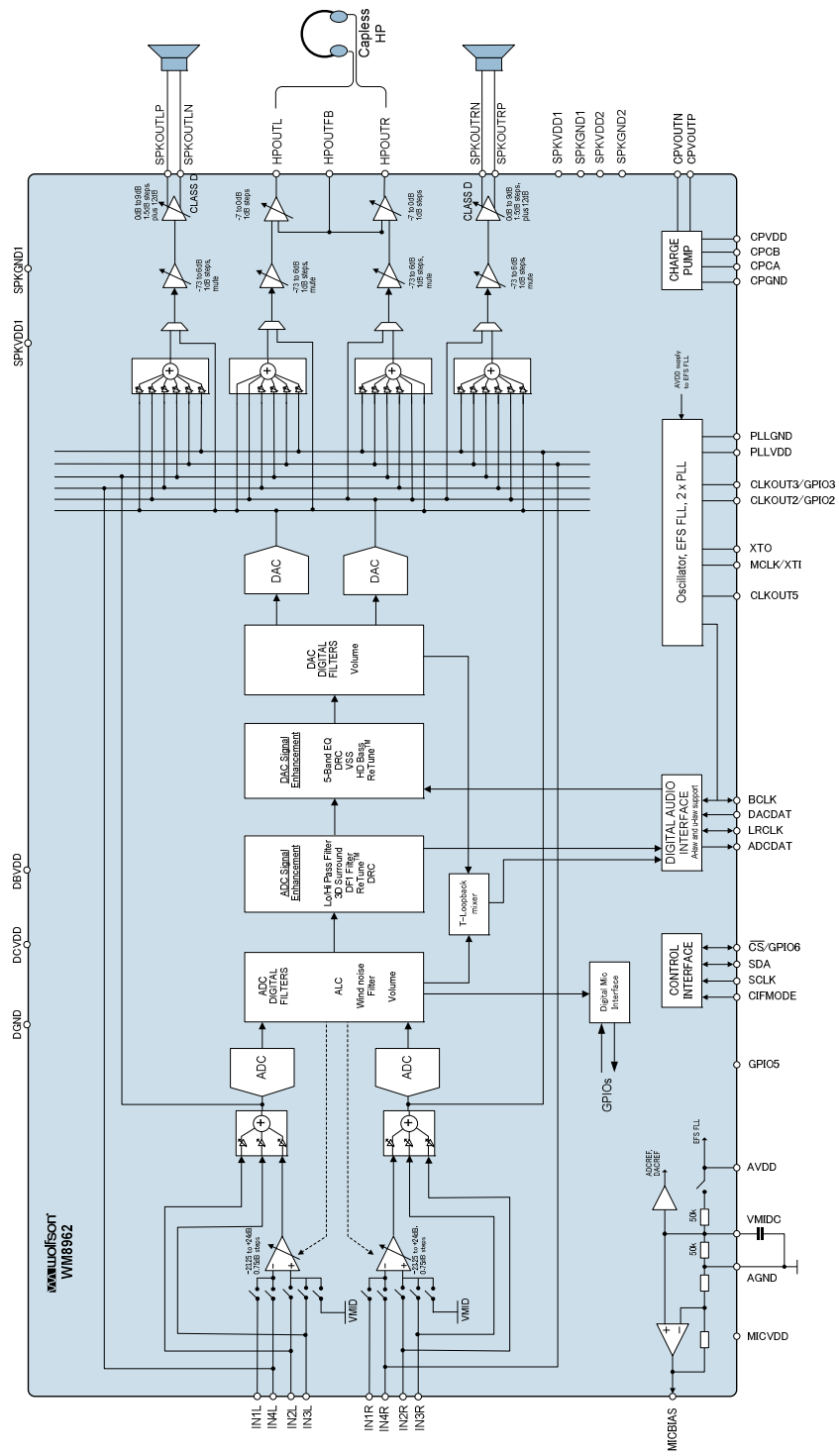
FEATURES

- DAC SNR 98dB ('A' weighted), THD -79dB at 48kHz, 1.8V
- ADC SNR 94dB ('A' weighted), THD -86dB at 48kHz, 1.8V
- Stereo Class D Speaker Driver
 - 1W per channel into 8Ω BTL speakers
 - 2W mono into 4Ω BTL speakers
 - Flexible internal switching clock
- Wolfson 'Class-W' ultra-low power headphone driver
 - Up to 22mW per channel output power at -80dB THD+N into 16Ω at 1.8V
 - Ground Referenced
 - Low offset (+/- 1.5mV)
 - Pop and click suppression
 - Control sequencer for pop-minimised power-up/down
 - Single register write for default start-up sequence
- Microphone Interface
 - Single ended four stereo analogue input
 - Integrated low noise MICBIAS
 - Digital microphone interface
 - Programmable ALC / Limiter and Noise Gate
- Programmable Audio Enhancement DSP with Presets
 - Virtual Surround Sound
 - HD Bass
 - ReTune™
- Fixed Audio Processing DSP
 - 3D stereo widening
 - 5-band Parametric EQ
 - Dynamic range controller
 - Beep generator
- Two integrated PLLs enable clocking of full audio system
- Low Power Consumption
 - 6.99mW headphone playback (1.8V supplies, Low Power mode)
- Low Supply Voltages
 - Analogue 1.7V to 2.0V (Speaker supply up to 5.5V)
 - Charge pump 1.7V to 2.0V
 - MIC bias amp supply 1.7V to 3.6V
 - Digital 1.62V to 2.0V
- 2-wire I2C and 3- or 4-wire SPI serial control interface
- Standard sample rates from 8kHz to 96kHz
- W-CSP, 3.6x3.9mm 49-pin

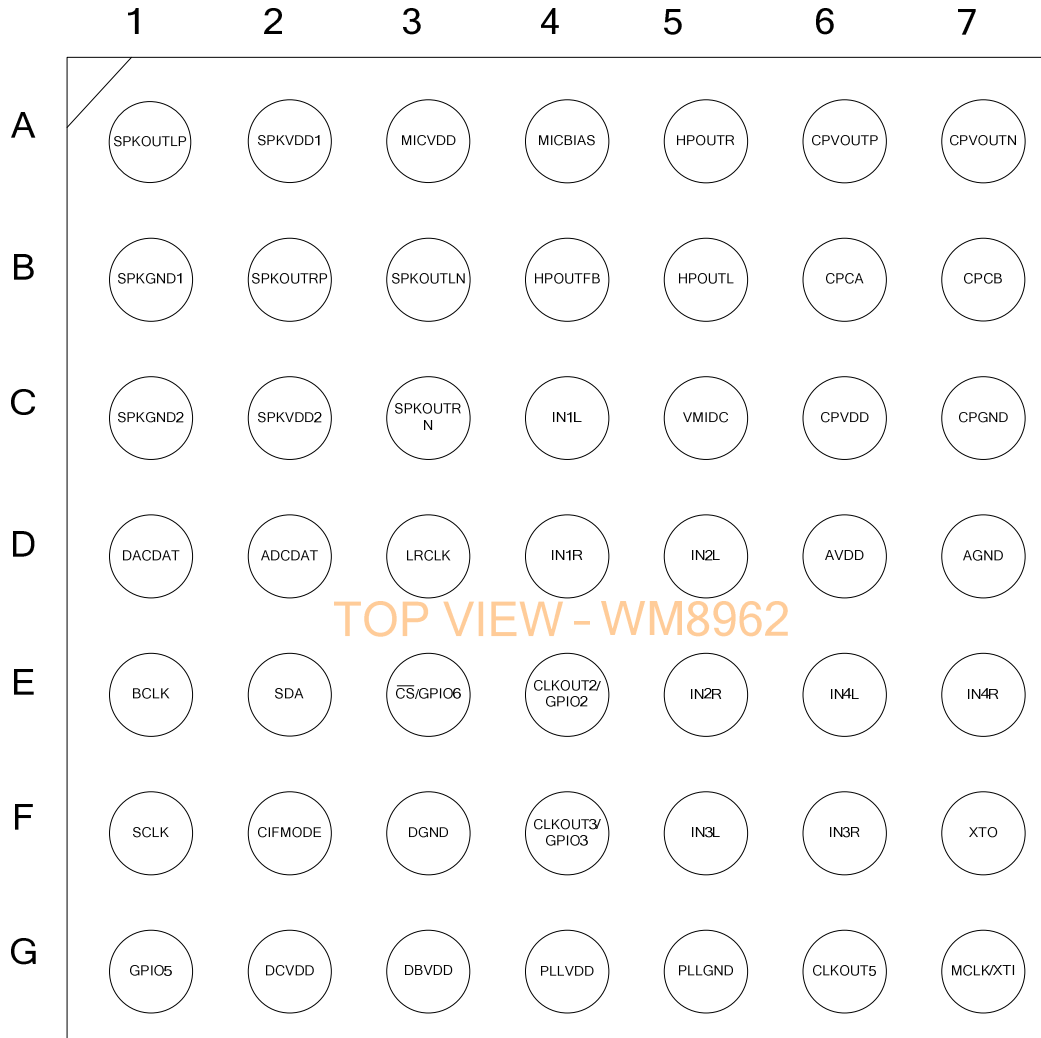
APPLICATIONS

- Portable gaming
- Voice recorders
- Mobile multimedia
- Stereo DSC-Camcorder

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8962ECSN/R	-40°C to +85°C	49-ball CSP (3.6x3.9mm) (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 3,500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKOUTLP	Analogue Output	Left speaker positive output
A2	SPKVDD1	Supply	Supply for left speaker drivers
A3	MICVDD	Supply	Microphone bias amp supply
A4	MICBIAS	Reference	Microphone bias
A5	HPOUTR	Analogue Output	Right output (Line or headphone)
A6	CPVOUTP	Supply	Charge pump positive supply (powers HPOUTL, HPOUTR)
A7	CPVOUTN	Supply	Charge pump negative supply (powers HPOUTL, HPOUTR)
B1	SPKGND1	Supply	Ground for left speaker drivers
B2	SPKOUTRP	Analogue Output	Right speaker positive output
B3	SPKOUTLN	Analogue Output	Left speaker negative output
B4	HPOUTFB	Analogue Input	HPOUTL/R ground loop noise rejection feedback
B5	HPOUTL	Analogue Output	Left output (Line or headphone)
B6	CPCA	Analogue Input	Charge pump fly-back capacitor pin
B7	CPCB	Analogue Input	Charge pump fly-back capacitor pin
C1	SPKGND2	Supply	Ground for right speaker drivers
C2	SPKVDD2	Supply	Supply for right speaker drivers
C3	SPKOUTRN	Analogue Output	Right speaker negative output
C4	IN1L	Analogue Input	Left channel single-ended input 1
C5	VMIDC	Reference	Mid-rail voltage (AVDD/2) - (requires decoupling capacitor)
C6	CPVDD	Supply	Charge pump power supply
C7	CPGND	Supply	Charge pump ground (return path for CPVDD)
D1	DACDAT	Digital Input	DAC digital audio data
D2	ADCDAT	Digital Output	ADC digital audio data
D3	LRCLK	Digital Input / Output	Audio interface left / right clock
D4	IN1R	Analogue Input	Right channel single-ended input 1
D5	IN2L	Analogue Input	Left channel single-ended input 2
D6	AVDD	Supply	Analogue supply
D7	AGND	Supply	Analogue ground (return path for AVDD and MICVDD)
E1	BCLK	Digital Input / Output	Audio interface bit clock
E2	SDA	Digital Input / Output	Control interface data input / 2-wire acknowledge output
E3	CS/GPIO6	Digital Input / Output	CS input / Digital Microphone input / General purpose input / output
E4	CLKOUT2/GPIO2	Digital Output	PLL2 Clock output / General purpose input / output
E5	IN2R	Analogue Input	Right channel single-ended input 2
E6	IN4L	Analogue Input	Left channel single-ended input 4
E7	IN4R	Analogue Input	Right channel single-ended input 4
F1	SCLK	Digital Input	Control interface clock input
F2	CIFMODE	Digital Input	Selects 2-wire or 3 / 4-wire control wire interface
F3	DGND	Supply	Digital ground
F4	CLKOUT3/GPIO3	Digital Output	PLL3 / FLL Clock output / GPIO
F5	IN3L	Analogue Input	Left channel single-ended input 3
F6	IN3R	Analogue Input	Right channel single-ended input 3
F7	XTO	Analogue Output	xtal output
G1	GPIO5	Digital Input / Output	Digital Microphone Input / General purpose input / output
G2	DCVDD	Supply	Digital Core Supply
G3	DBVDD	Supply	Digital Buffer Supply
G4	PLLVDD	Supply	PLL Supply
G5	PLLGND	Supply	PLL Ground
G6	CLKOUT5	Analogue Output	FLL / Oscillator Clock output
G7	MCLK / XT1	Digital Input	Master clock input / xtal input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DCVDD, AVDD, PLLVDD	-0.3V	+2.5V
MICVDD and DBVDD	-0.3V	+4.5V
SPKVDD1, SPKVDD2	-0.3V	+7.0V
CPVDD	-0.3V	+2.2V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Voltage range analogue outputs (HPOUTL, HPOUTR)	-CPVDD-0.3V	+CPVDD+0.3V
Temperature Range, T _A	-40°C	+85°C
Junction Temperature, T _{JMAX}	-40°C	+150°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. AVDD must be less than or equal to MICVDD.
4. AVDD must be less than or equal to SPKVDD1 and SPKVDD2.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital core supply range	DCVDD	1.62	1.8	2.0	V
Digital buffer supply range	DBVDD	1.62	1.8	3.6	V
Microphone bias supply range	MICVDD	1.7	2.5	3.6	V
Analogue supplies range	AVDD	1.7	1.8	2.0	V
PLL supply range	PLLVDD	1.7	1.8	2.0	V
Charge pump supply range (1.8V supply operation)	CPVDD	1.7	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	1.7	5.0	5.5	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, PLLGND		0		V

Notes:

1. SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using CLASSD_VOL function, to avoid output waveform clipping. Peak output voltage is AVDD*CLASSD_VOL.

DEVICE DESCRIPTION

The WM8962 is a low power audio CODEC offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications with stereo speaker and headphone outputs such as games consoles, portable media players and multimedia phones.

A flexible input configuration supports a single-ended stereo microphone interface and a digital microphone interface. A boost amplifier is available for additional gain on the microphone inputs. A programmable gain amplifier (PGA) with an automatic level control (ALC) function can be used to maintain a constant microphone recording volume.

Stereo class D speaker drivers can provide >1W per channel into 8Ω loads, or 2W mono into a 4Ω load. BTL configuration provides high power output and excellent PSRR.

Highly flexible output speaker boost settings provide fully internal level-shifting of analogue output signals, allowing speaker output power to be maximised while minimising other analogue supply currents, and requiring no additional components.

A dual mode (Level Shifting or Inverting Mode) charge pump generates split supplies for the headphone output amplifiers allowing these to be ground referenced.

A DC servo to remove offsets from the headphone outputs, low leakage and a user controlled power-up/power-down Control Sequencer provides powerful pop and click suppression mechanisms which enable direct battery connection. These anti-pop/click mechanisms, and no requirement for any external DC blocking capacitors to the headphone, result in a reduced external component count and reduced power consumption in portable battery-powered applications.

The hi-fi quality stereo ADC and DAC uses a 24-bit, low-order over-sampling architecture to deliver optimum performance. ADC and DAC operate at the same sample rate.

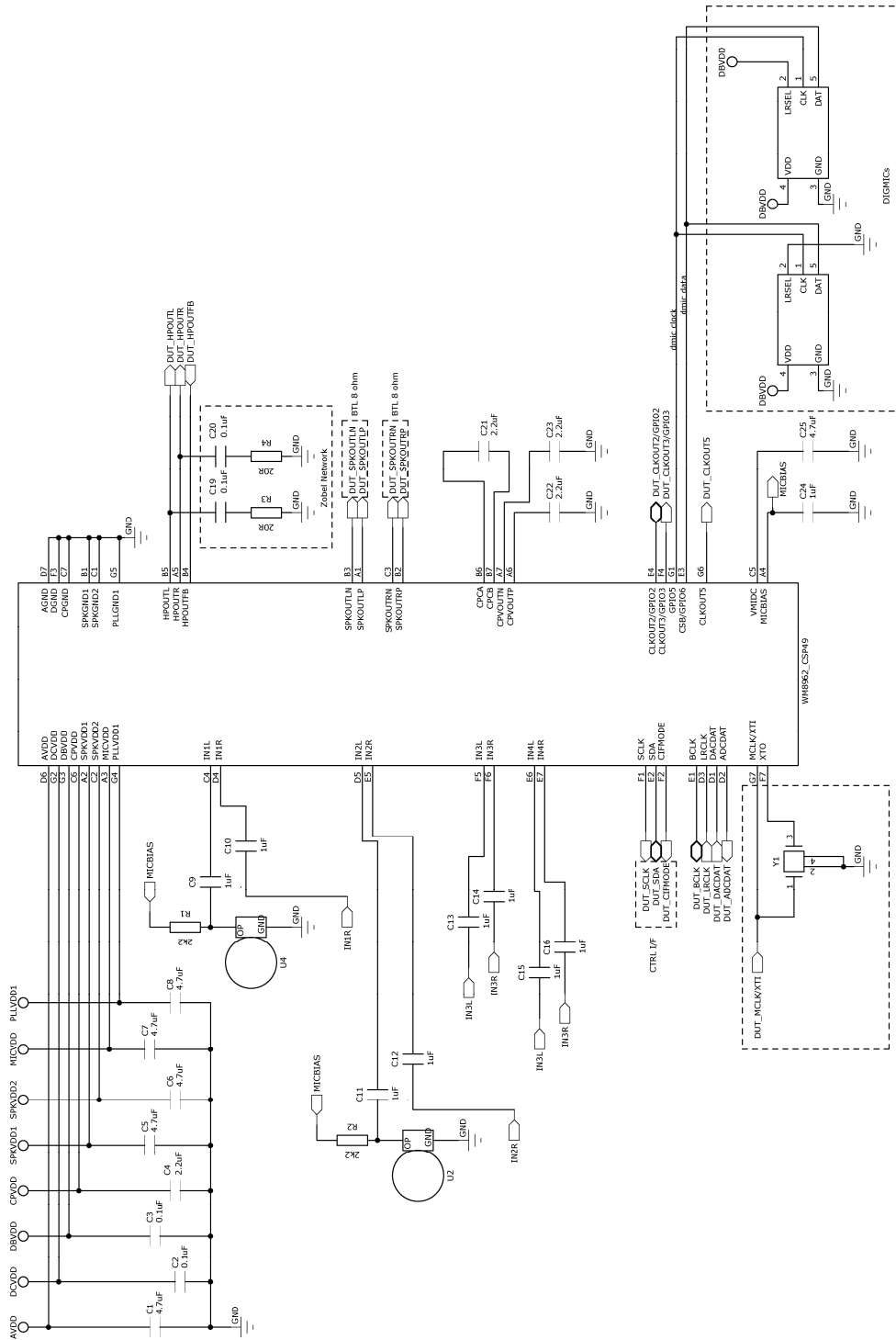
An audio enhancement DSP provides powerful benefits in audio processing. Three algorithms are pre-programmed in the DSP. ReTune™ flattens the frequency response of the full record and/or playback path, including microphone, speaker and housing. Virtual Surround Sound widens the stereo speaker audio image. High Definition Bass enhances low frequencies, improving the performance of small speakers. Further audio enhancements are provided in a fix function DSP – 3D enhancement, a 5-band parametric equaliser, and a Dynamic Range Controller.

The WM8962 has a highly flexible digital audio interface, supporting a number of protocols, including I2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

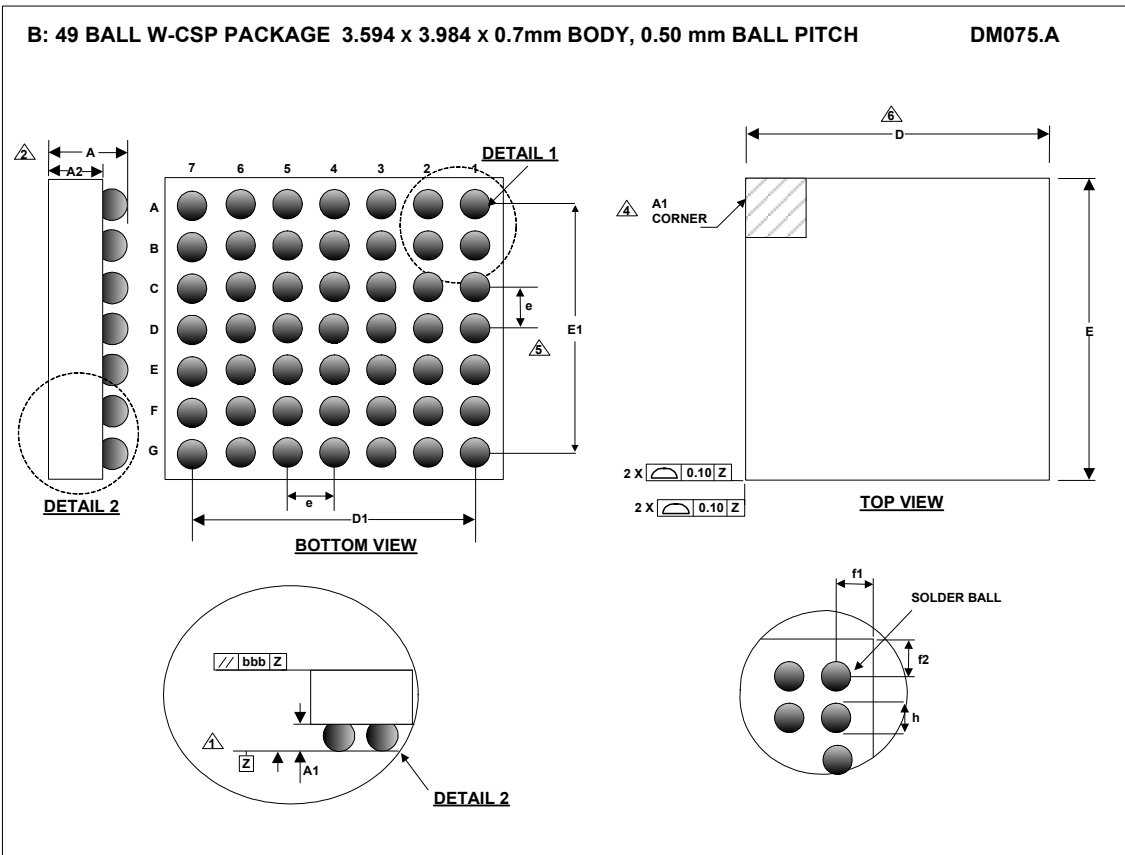
The WM8962 provides two integrated PLLs and one Exact Fractional Synthesis (EFS) FLL to generate internal and external clock signals. The SYSCLK (internal system clock) provides clocking for all internal functions. SYSCLK can be derived directly from the MCLK pin, or else using one of the PLLs or the FLL. All MCLK frequencies typically used in portable systems are supported for sample rates between 8 kHz and 96 kHz. The ADC and DAC must be configured to operate at the same sample rate. A flexible switching clock for the class D speaker drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8962 supports 2-wire (I2C) and 3- or 4-wire (SPI) serial control interface modes, with full read-back capability on all registers. The WM8962 is fully compatible with, and an ideal partner to, a wide range of industry standard microprocessors, controllers and DSPs. Unused functions can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

RECOMMENDED EXTERNAL COMPONENTS



PACKAGE DIMENSIONS



Symbols	Dimensions (mm)			NOTE
	MIN	NOM	MAX	
A	0.650	0.7	0.750	
A1	0.219	0.244	0.269	
A2	0.431	0.456	0.481	
D	3.564	3.594	3.624	
D1		3.00 BSC		
E	3.954	3.984	4.014	
E1		3.00 BSC		
e		0.50 BSC		5
f1	0.282			
f2	0.477			
h		0.314 BSC		

- NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
 3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
 4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
 5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
 6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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