WM8982

Mono CODEC With Speaker Driver and Video Buffer

DESCRIPTION

The WM8982 is a low power, high quality CODEC with integrated video buffer designed for portable applications such as digital still camera or digital camcorder.

The device integrates a preamp for a differential mic, and includes drivers for speaker and line outputs. External component requirements are reduced as no separate microphone or headphone/speaker amplifiers are required.

An integrated video buffer is provided which has programmable gain from 0-6dB, sync-tip clamp and a 3rd order input low pass filter for signal re-construction.

Advanced on-chip digital signal processing includes a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. Additional digital filtering options are available in the ADC path, to cater for application filtering such as 'wind noise reduction'.

The WM8982 CODEC can operate as a master or a slave. An internal PLL can generate all required audio clocks for the CODEC from common reference clock frequencies, such as 12MHz and 13MHz.

The WM8982 operates at analogue supply voltages from 2.5V to 3.3V, although the digital core can operate at voltages down to 1.71V to save power. The speaker outputs and mono line output can run from a 5V supply if increased output power is required. Individual sections of the chip can also be powered down under software control.

FEATURES

CODEC:

- DAC SNR 98dB, THD -84dB ('A' weighted @ 48kHz)
- ADC SNR 90dB, THD -80dB ('A' weighted @ 48kHz)
- 1W output power into 8Ω BTL speaker / 5V SPKVDD
  - Capable of driving piezo speakers

Mic Preamp:

- Differential microphone Interface
  - Programmable preamp gain
  - Psuedo differential inputs with common mode rejection
  - Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphones

Other features:

- Integrated 0-6dB video buffer with LPF filter and clamp.
- Digital playback limiter
- 5-band Equaliser (record or playback)
- Programmable ADC High Pass Filter (wind noise reduction)
- Programmable ADC Notch Filter
- Aux inputs for analog input signals or 'beep'
- On-chip PLL supporting 12, 13, 19.2MHz and other clocks
- Low power, low voltage
  - 2.5V to 3.6V (digital: 1.71V to 3.6V)
- 5x5mm 32-lead QFN package

APPLICATIONS

- Camcorder or DSC

BLOCK DIAGRAM

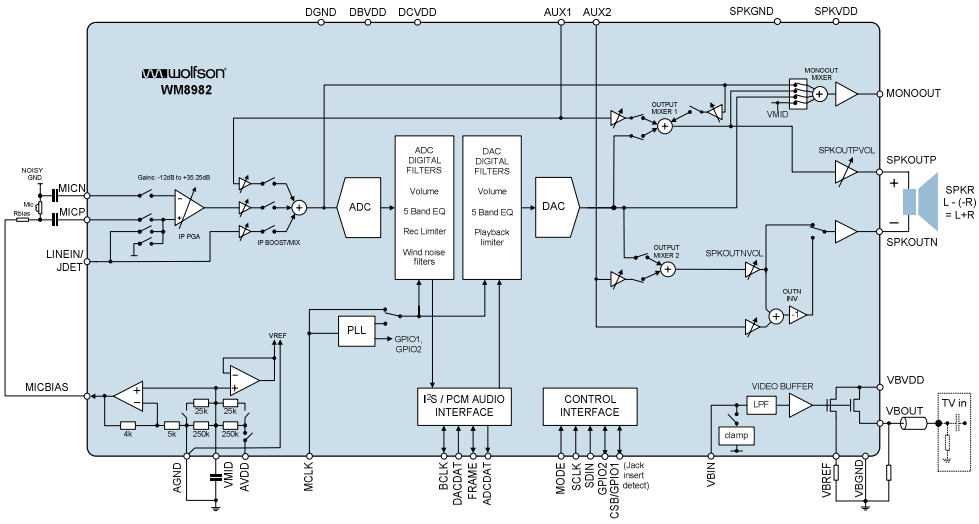
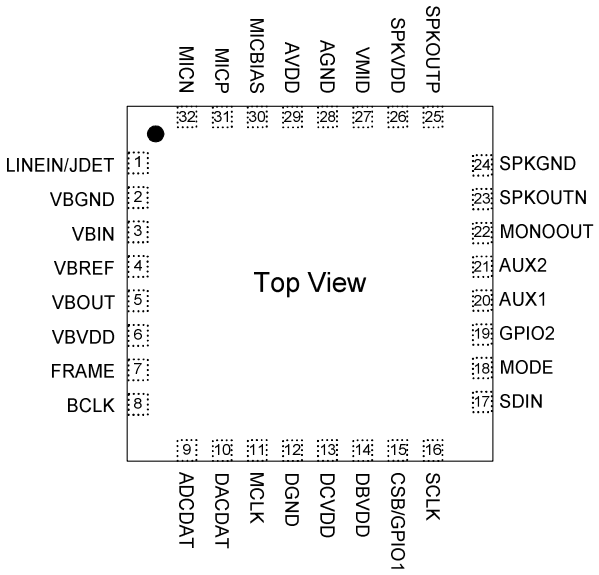


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8982GEFL/V	-25°C to +85°C	32-lead QFN (5 x 5 mm) (Pb-free)	MSL3	260°C
WM8982GEFL/RV	-25°C to +85°C	32-lead QFN (5 x 5 mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LINEIN/JDET	Analogue input	Line level input/secondary mic pre-amp input/jack detect pin
2	VBGND	Supply	Video buffer ground pin
3	VBIN	Analogue input	Video buffer signal input
4	VBREF	Analogue output	Video buffer reference resistor pin
5	VBOUT	Analogue output	Video buffer output
6	VBVDD	Supply	Video buffer analogue supply
7	FRAME	Digital Input / Output	DAC and ADC Sample Rate Clock
8	BCLK	Digital Input / Output	Digital Audio Port Clock
9	ADCDAT	Digital Output	ADC Digital Audio Data Output
10	DACDAT	Digital Input	DAC Digital Audio Data Input
11	MCLK	Digital Input	Master Clock Input
12	DGND	Supply	Digital ground
13	DCVDD	Supply	Digital core logic supply
14	DBVDD	Supply	Digital buffer (I/O) supply
15	CSB/GPIO1	Digital Input / Output	3-Wire control interface chip select / GPIO1
16	SCLK	Digital Input	3-Wire control interface clock input / 2-Wire control interface clock input
17	SDIN	Digital Input / Output	3-Wire control interface data input / 2-Wire control interface data input
18	MODE	Digital Input	Control Interface Selection
19	GPIO2	Digital Input / Output	GPIO2
20	AUX1	Analogue input	Auxiliary input 1
21	AUX2	Analogue input	Auxiliary input 2
22	MONOOUT	Analogue Output	Buffered midrail pseudo-ground, or mono line output
23	SPKOUTN	Analogue Output	BTL speaker driver negative output
24	SPKGND	Supply	Speaker ground (feeds speaker amp and MONOOUT)
25	SPKOUTP	Analogue Output	BTL speaker driver positive output
26	SPKVDD	Supply	Speaker supply (feeds speaker amp only)
27	VMID	Reference	Decoupling for ADC and DAC reference voltage
28	AGND	Supply	Analogue ground (feeds ADC and DAC)
29	AVDD	Supply	Analogue supply (feeds ADC and DAC)
30	MICBIAS	Analogue Output	Microphone Bias
31	MICP	Analogue input	Mic Pre-amp positive input
32	MICN	Analogue input	Mic Pre-amp negative input

Note:
It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB. Refer to the application note WAN_0118 on "Guidelines on How to Use QFN Packages and Create Associated PCB Footprints"

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD, VBVDD supply voltages	-0.3V	+4.5V
SPKVDD supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. Analogue supply voltage has to be ≥ to digital.
4. In non-boosted mode, SPKVDD should = AVDD, if boosted SPKVDD should be ≥ 1.5x AVDD.
5. When using PLL, DCVDD should be ≥ 1.9V.
6. DBVDD must be greater than or equal to DCVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71[1]		3.6	V
Digital supply range (Buffer)	DBVDD		1.71		3.6	V
Analogue core supply range	AVDD		2.5		3.6	V
Video buffer supply range	VBVDD		2.5		3.6	V
Analogue output supply range	SPKVDD		2.5		5.5	V
Ground	DGND,AGND, SPKGND,VBGND			0		V

Notes:

1. When using the PLL, DCVDD must be >= 1.9V.
2. DBVDD must be greater than or equal to DCVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, AVDD=DBVDD=SPKVDD=VBVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs (MICN, MICP, LINEIN/JDET)						
Full-scale Input Signal Level – note this changes with AVDD	V_{INFS}	PGABOOST = 0dB INPPGAVOL = 0dB		1.0 0		Vrms dBV
Full-scale Input Signal Level – Pseudo-differential input	V_{INFS}	PGABOOST = 0dB INPPGAVOL = 0dB		AVDD1*0.7/ 3.3		Vrms
Mic PGA equivalent input noise	At 35.25dB gain	0 to 20kHz		150		uV
Input resistance	R_{MICIN}	Gain set to 35.25dB		1.6		kΩ
	R_{MICIN}	Gain set to 0dB		47		kΩ
	R_{MICIN}	Gain set to -12dB		75		kΩ
	R_{MICIP}	MICP2INPPGA = 1		94		kΩ
	C_{MICIN}			10		pF
MIC Programmable Gain Amplifier (PGA)						
Maximum Programmable Gain				35.25		dB
Minimum Programmable Gain				-12		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation				120		dB
Selectable Input Gain Boost (0/+20dB)						
Gain Boost on PGA input		Boost disabled		0		dB
		Boost enabled		20		dB
Maximum Gain from AUX1/2 or LINEIN input to boost/mixer				+6		dB
Minimum Gain from AUX1/2 or LINEIN input to boost/mixer				-12		dB
Gain step size to boost/mixer		Guaranteed monotonic		3		dB
Auxiliary Analogue Inputs (AUX1, AUX2)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			AVDD/3.3 0		Vrms dBV
Input Resistance (Note 2)	$R_{AUXIN1MIN}$	Input boost and mixer enabled, at max gain		4.3		kΩ
	$R_{AUXIN1TYP}$	Input boost and mixer enabled, at 0dB gain		8.6		kΩ
	$R_{AUXIN1MAX}$	Input boost and mixer enabled, at min gain		39.1		kΩ
Input Capacitance	C_{MICIN}			10		pF
Automatic Level Control (ALC)						
Target Record Level			-22.5		-1.5	dB
Programmable gain			-12		35.25	
Gain Hold Time (Note 2,4)	t_{HOLD}	MCLK = 12.288MHz (Note 3)	0, 2.67, 5.33, 10.67, … , 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time (Note 3,4)	t_{DCY}	ALCMODE=0 (ALC), MCLK=12.288MHz (Note 3)	3.3, 6.6, 13.1, … , 3360 (time doubles with each step)			ms
		ALCMODE=1 (limiter), MCLK=12.288MHz (Note 3)	0.73, 1.45, 2.91, … , 744 (time doubles with each step)			
Gain Ramp-Down (Attack) Time (Note 3,4)	t_{ATK}	ALCMODE=0 (ALC), MCLK=12.288MHz (Note 3)	0.83, 1.66, 3.33, … , 852 (time doubles with each step)			ms

Test Conditions

DCVDD=1.8V, AVDD=DBVDD=SPKVDD=VBVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		ALCMODE=1 (limiter), MCLK=12.288MHz (Note 3)		0.18, 0.36, 0.73, … , 186 (time doubles with each step)		
Mute Attenuation				120		dB
Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 5)	SNR	A-weighted, 0dB gain	85	95		dB
Total Harmonic Distortion (Note 6)	THD	-3dBFS input		-84	-74	dB
Digital to Analogue Converter (DAC) to Line-Out (MONOOUT with 10kΩ / 50pF load)						
Full-scale output		PGA gains set to 0dB, SPK/MONOBOOST=0		AVDD/3.3		Vrms
		PGA gains set to 0dB, SPK/MONOBOOST=1		1.5x (AVDD/3.3)		
Signal to Noise Ratio (Note 5)	SNR	A-weighted	90	98		dB
Total Harmonic Distortion (Note 6)	THD	R_L = 10kΩ full-scale signal		-84	-76	dB
Output Mixers (MX1, MX2)						
Maximum PGA gain into mixer				+6		dB
Minimum PGA gain into mixer				-15		dB
PGA gain step into mixer		Guaranteed monotonic		3		dB
Analogue Outputs (SPKOUTP, SPKOUTN)						
Maximum Programmable Gain				+6		dB
Minimum Programmable Gain				-57		dB
Programmable Gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz, full scale signal		85		dB
Speaker Output (SPKOUTP, SPKOUTN with 8Ω bridge tied load, INVOUTN=1)						
Full scale output voltage, 0dB gain. (Note 7)		SPKRBOOST=0		SPKVDD/3.3		Vrms
		SPKRBOOST=1		(SPKVDD/3.3)*1.5		
Output Power	P_O	Output power is very closely correlated with THD; see below				
Total Harmonic Distortion	THD	P_O =200mW, R_L = 8Ω, SPKVDD=3.3V		0.04 -68		% dB
		P_O =320mW, R_L = 8Ω, SPKVDD=3.3V		1.0 -40		% dB
		P_O =500mW, R_L = 8Ω, SPKVDD=5V		0.02 -74		% dB
		P_O =860mW, R_L = 8Ω, SPKVDD=5V		1.0 -40		% dB
Signal to Noise Ratio	SNR	SPKVDD=3.3V, R_L = 8Ω		90		dB
		SPKVDD=5V, R_L = 8Ω		90		dB
Power Supply Rejection Ratio (50Hz-22kHz)	PSRR	R_L = 8Ω BTL		80		dB
		R_L = 8Ω BTL SPKVDD=5V (boost)		69		dB
MONOOUT Output (with 10kΩ / 50pF load)						
Full-scale output voltage, 0dB gain (Note 7)		MONOBOOST=0		SPKVDD/3.3		Vrms
		MONOBOOST=1		(SPKVDD/3.3)*1.5		Vrms
Signal to Noise Ratio (Note 5)	SNR	A-weighted		98		dB
Total Harmonic Distortion (Note 6)	THD	R_L = 10 kΩ full-scale signal		-84		dB
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	MBVSEL=0		0.9*AVDD		V

Test Conditions

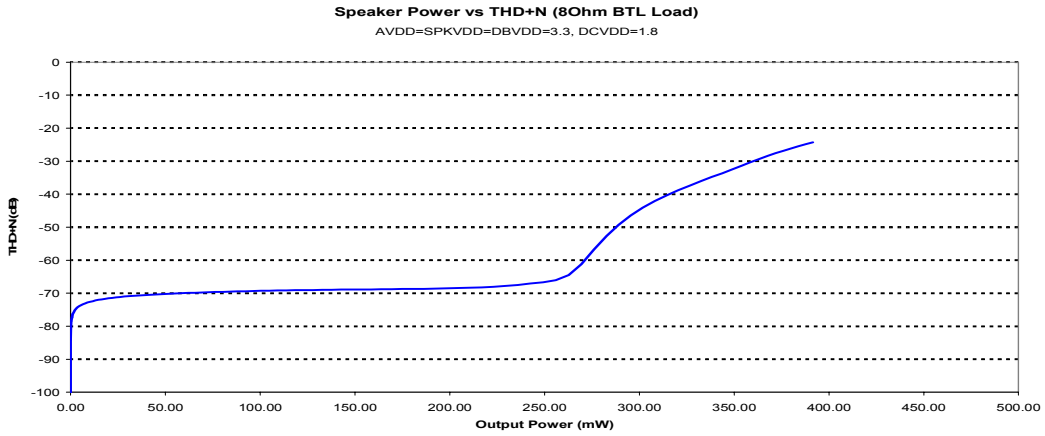
DCVDD=1.8V, AVDD=DBVDD=SPKVDD=VBVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

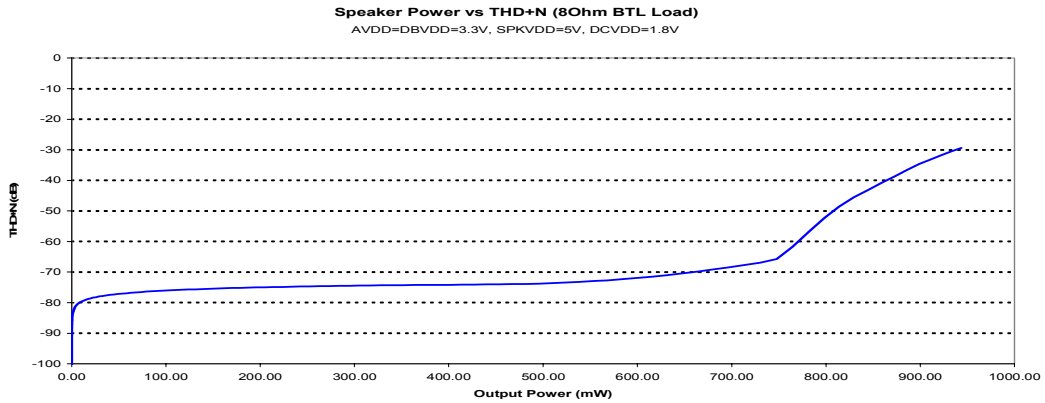
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		MBVSEL=1		0.65*AVDD		V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Video Buffer						
Low pass filter order				3rd order		
LPF -3dB cutoff				10		MHz
LPF gain flat to within 0.1dB				5.3		MHz
Maximum output voltage swing	Vom	f=100kHz, THD=1%		1.25		Vp-p
Programmable Voltage Gain	Av		0		6	dB
Differential gain	DG	Vin=1Vp-p		0.3		%
Differential phase	DP	Vin=1Vp-p		0.7		Deg
Signal to Noise Ratio	VSNR			+60		dB
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1xDBVDD	V
Input capacitance				TBD		pF
Input leakage				TBD		pA

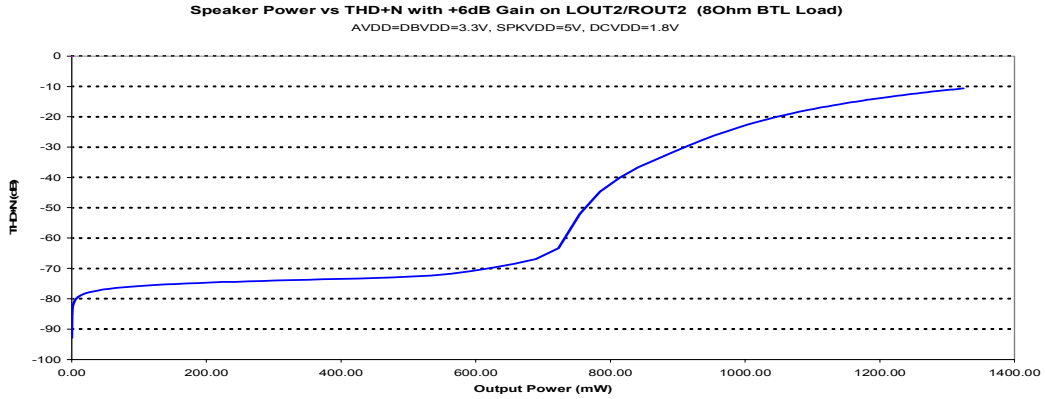
TERMINOLOGY

1. Note when BEEP path is not enabled then AUX1 and AUX2 have the same input impedances.
2. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
3. Ramp-up and Ramp-Down times are defined as the time it takes for the PGA to sweep across 90% of its gain range.
4. All hold, ramp-up and ramp-down times scale proportionally with MCLK
5. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
6. THD+N (dB) – THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
7. The maximum output voltage can be limited by the speaker power supply. If MONOBOOST or SPKRBOOST is set then SPKVDD should be 1.5xAVDD to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

SPEAKER OUTPUT THD VERSUS POWER







POWER CONSUMPTION

Estimated current consumption for typical scenarios are shown below.

For more information on current consumption of individual blocks, see "Estimated Supply Currents" section.

MODE	AVDD	DBVDD	DCVDD	VBVDD	UNITS
Off	0	0	0	0	mA
Sleep (VREF maintained)	0.1	0	0	0	mA
Record (8kHz, PLL enabled)	6.1	0.001	1.2	0	mA
Playback to BTL speaker (8kHz, PLL enabled)	6.3	0.001	1.2	0	mA
Playback to BTL speaker (8kHz, PLL enabled, Video Buffer enabled)	6.3	0.001	1.2	4.0	mA

Table 1 Power Consumption

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

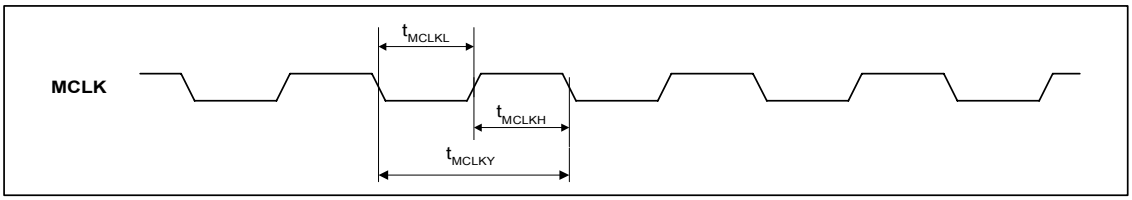


Figure 1 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK=SYSCLK (=256fs)	81.38			ns
		MCLK input to PLL Note 1	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note 1:

PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

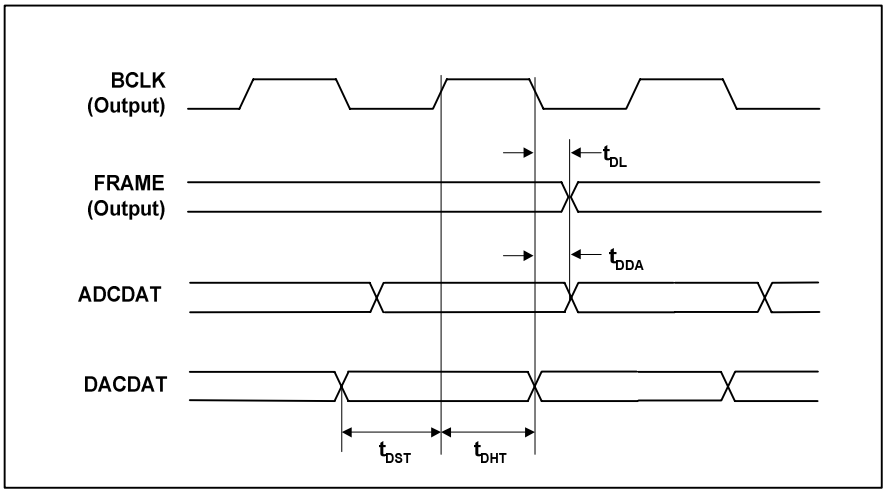


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
FRAME propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

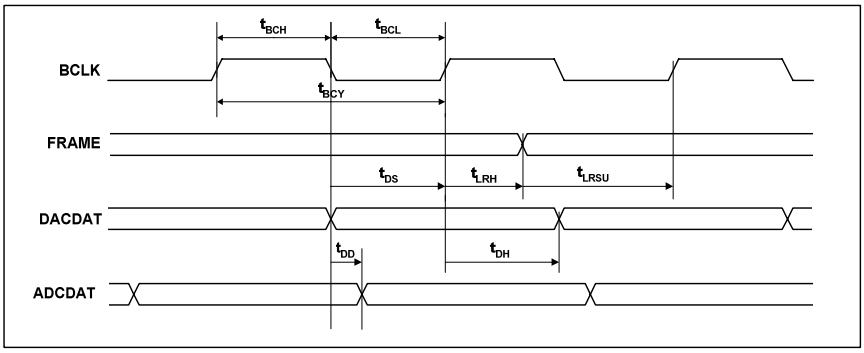


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
FRAME set-up time to BCLK rising edge	t_{LRSU}	10			ns
FRAME hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT setup time to BCLK rising edge	t_{Ds}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

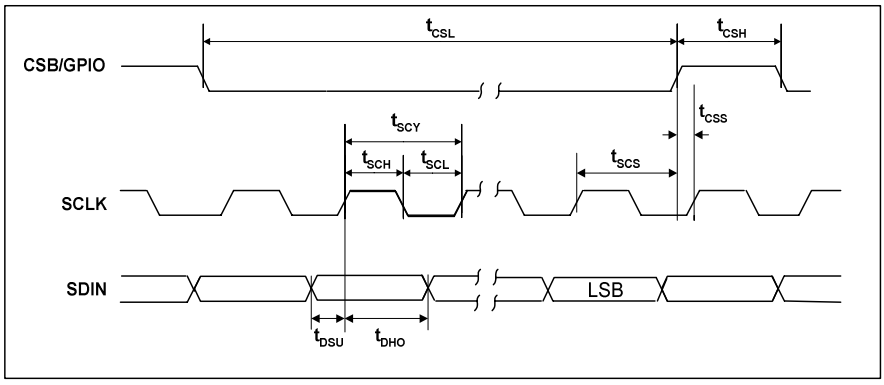


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = AVDD = SPKVDD = 3.3V, DGND = AGND = SPKGND = 0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

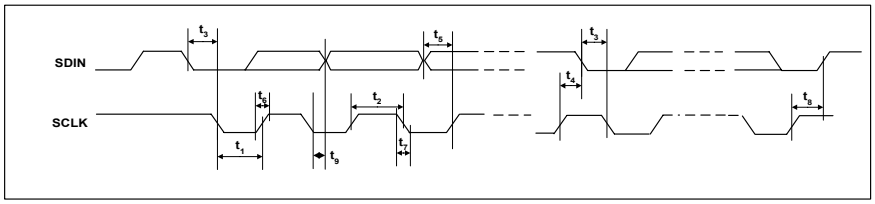


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

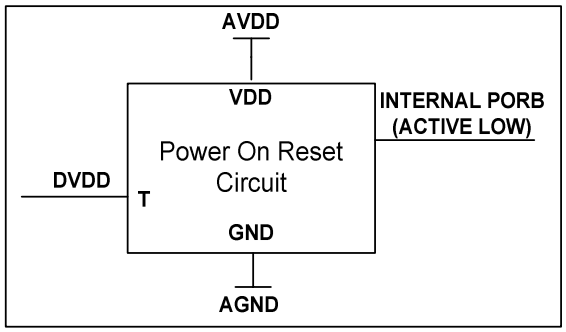


Figure 6 Internal Power on Reset Circuit Schematic

The WM8982 includes an internal Power-On-Reset Circuit (POR), as shown in Figure 6, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD. It asserts PORB low if AVDD or DVDD is below a minimum threshold.

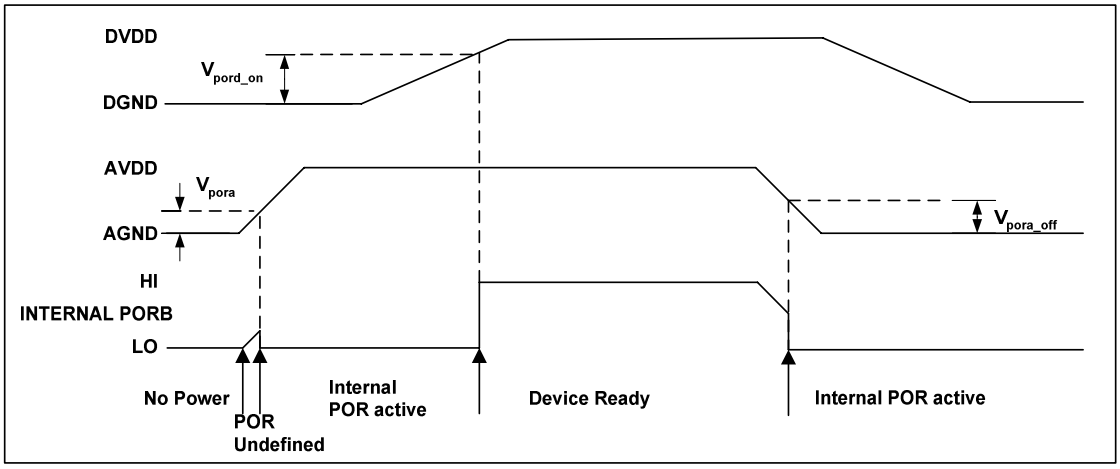


Figure 7 Typical Power up Sequence where AVDD is Powered before DVDD

Figure 7 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. AVDD will then ramp up to full supply level. Next DVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

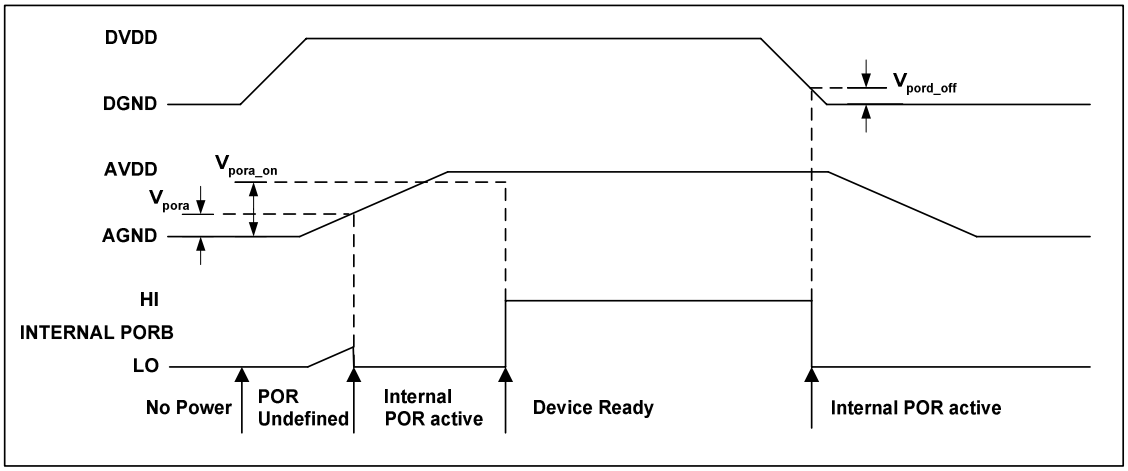


Figure 8 Typical Power up Sequence where DVDD is Powered before AVDD

Figure 8 shows a typical power-up sequence where DVDD comes up first. First it is assumed that DVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD falls first, PORB is asserted low whenever DVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 2 Typical POR operation (simulated values)

Notes:

If AVDD and DVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.

The chip will enter reset at power down when AVDD or DVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.

The minimum t_{por} period is maintained even if DVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8982 is a low power audio CODEC combining a high quality audio DAC and ADC. Applications for this device include digital camcorders and digital still cameras with audio and video, record and playback capability. The integrated video buffer makes the device suitable for driving both audio and video signals directly to a television or VCR.

FEATURES

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

MICROPHONE INPUTS

A microphone input is provided, allowing for a microphone to be pseudo-differentially connected, with user defined gain using internal resistors. The provision of the common mode input pin allows for rejection of common mode noise on the microphone input (level depends on gain setting chosen). A microphone bias is output from the chip which can be used to bias the microphone. The signal routing can be configured to allow manual adjustment of mic levels, or indeed to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone path of up to +55.25dB can be selected.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

LINE INPUTS (AUX1, AUX2)

The inputs, AUX1 and AUX2, can be used as a stereo line input or as an input for warning tones (or 'beeps') etc. These inputs can be summed into the record paths, along with the microphone preamp outputs, so allowing for mixing of audio with 'backing music' etc as required.

ADC

The ADC uses a multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption.

DAC

The DAC provides high quality audio playback suitable for all portable mono applications, including DSCs and camcorders.

OUTPUT MIXERS

Flexible mixing is provided on the outputs of the device. Gain adjustment PGAs are provided for the SPKOUTN/P outputs, and signal switching is provided to allow for all possible signal combinations. The SPKOUTN/P output buffers can be configured as BTL speaker drivers. Thermal implications should be considered before simultaneous full power operation of all outputs is attempted.

Alternatively, if a speaker output is not required, the SPKOUTP and SPKOUTN pins might be used as a stereo headphone driver, (disable output invert buffer on SPKOUTN).

AUDIO INTERFACES

The WM8982 has a standard audio interface, to support the transmission of data to and from the chip. This interface is a 3 wire standard audio interface which supports a number of audio data formats including I2S, DSP/PCM Mode (a burst mode in which FRAME sync plus data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

CONTROL INTERFACES

To allow full software control over all its features, the WM8982 offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

Selection between the modes is via the MODE pin. In 2 wire mode the address of the device is fixed as 0011010.

CLOCKING SCHEMES

WM8982 offers the normal audio DAC clocking scheme operation, where 256fs MCLK is provided to the DAC and ADC.
A PLL is included which may be used to generate these clocks in the event that they are not available from the system controller. This PLL uses an input clock, typically the 12MHz USB or ilink clock, to generate high quality audio clocks. If this PLL is not required for generation of these clocks, it can be reconfigured to generate alternative clocks which may then be output on the GPIO pins and used elsewhere in the system.

VIDEO BUFFER

The WM8982 incorporates a current mode output video buffer with an input 3rd order Low Pass Filter (LPF) and clamp. The gain through this buffer can be programmed as 0dB or 6dB via the control interface. The current mode output means that the signal swing seen at the output of the buffer will be the same as that at the connection to the receiving equipment (e.g. a TV). Note that the input to the receiver should be AC coupled and terminated to 75Ω, as is standard, for best performance.

POWER CONTROL

The WM8982 provides the ability to disable any unused parts of the circuitry under software control, to save power and includes standby and power off modes.

INPUT SIGNAL PATH

The WM8982 has a number of flexible analogue inputs, consisting of an input PGA stage followed by a boost/mix stage which is input to the ADC. The input path has three input pins which can be configured in a variety of ways to accommodate single-ended or differential microphones. There is an auxiliary input pin which can be fed into to the input boost/mix stage as well as driving into the output path. A bypass path exists from the output of the boost/mix stage into the output mixer.

MICROPHONE INPUT

The WM8982 can accommodate a variety of microphone configurations including single ended and differential inputs. The inputs to the input PGA are MICN, MICP and LINEIN.

In single-ended microphone input configuration the microphone signal should be input to MICN and the internal NOR gate configured to clamp the non-inverting input of the input PGA to VMID.

In differential mode the larger signal should be input to LIP and the smaller (eg noisy ground connections) should be input to LIN.

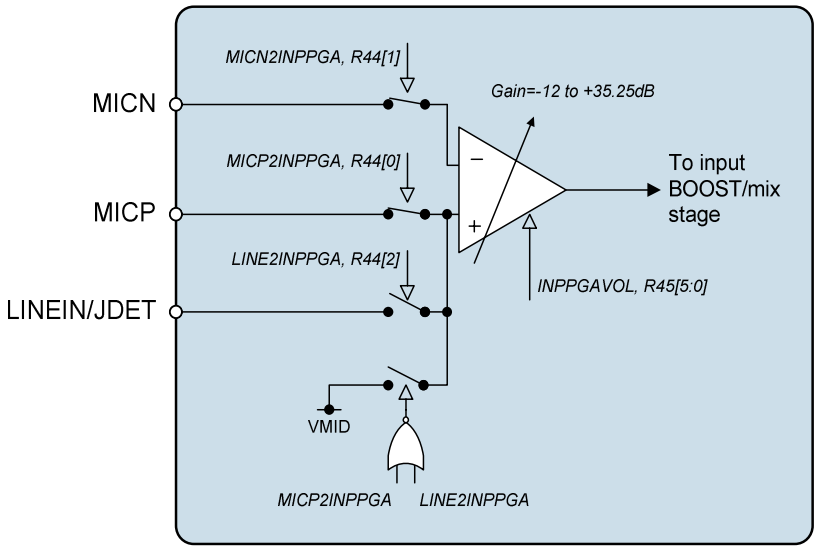


Figure 9 Microphone Input PGA Circuit

The input PGA is enabled by the IPPGAEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power Management 2	2	INPPGAEN	0	Input PGA enable: 0 = disabled 1 = enabled

Table 3 Input PGA Enable Register Settings

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	0	MICP2INPPGA	1	Connect MICP pin to input PGA amplifier positive terminal. 0 = MICP not connected to input PGA 1 = input PGA amplifier positive terminal connected to MICP (constant input impedance)
	1	MICN2INPPGA	1	Connect MICN pin to input PGA negative terminal. 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	2	LINE2INPPGA	0	Connect LINEIN pin to input PGA positive terminal. 0=LINEIN not connected to input PGA 1=LINEIN connected to input PGA amplifier positive terminal (constant input impedance).

Table 4 Input PGA Control

INPUT PGA VOLUME CONTROL

The input microphone PGA has a gain range from -12dB to +35.25dB in 0.75dB steps. The gain from the MICN input to the PGA output and from the LINEIN amplifier to the PGA output are always common and controlled by the register bits INPPGAVOL[5:0]. These register bits also affect the MICP pin when MICP2INPPGA=1 and the LINEIN pin when LINE2INPPGA=1.

When the Automatic Level Control (ALC) is enabled the input PGA gains are controlled automatically and the INPPGAVOL bits should not be used.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA volume control	5:0	INPPGAVOL	010000	Input PGA volume: 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB
	6	INPPGAMUTE	0	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
	7	INPPGAZC	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1st zero cross after gain register write.
	8	INPPGAUPDATE	Not latched	INPPGAVOL volume does not update until a 1 is written to INPGAUPDATE
R32 ALC control 1	8	ALCSEL	0	ALC function select: 0=ALC off 1=ALC on

Table 5 Input PGA Volume Control

VOLUME UPDATES

Volume settings will not be applied to the PGAs until a '1' is written to one of the INPPGAUPDATE bits. This is to allow left and right channels to be updated at the same time, as shown in Figure 10.

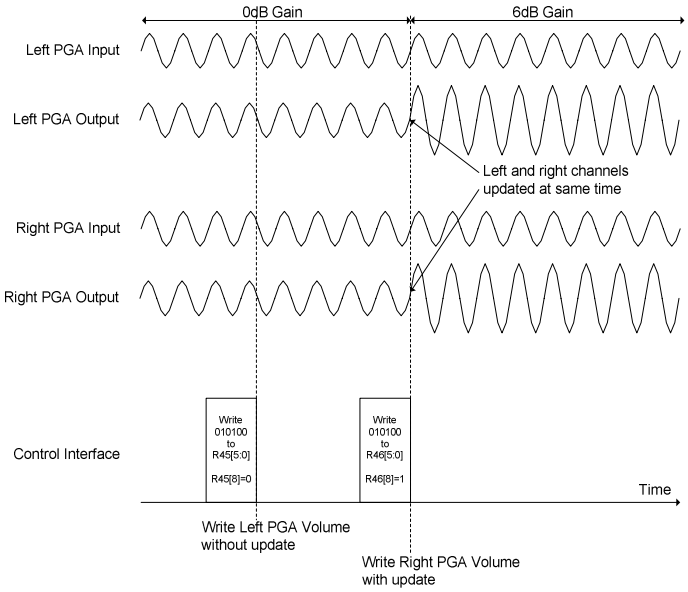


Figure 10 Simultaneous Left and Right Volume Updates

If the volume is adjusted while the signal is a non-zero value, an audible click can occur as shown in Figure 11.

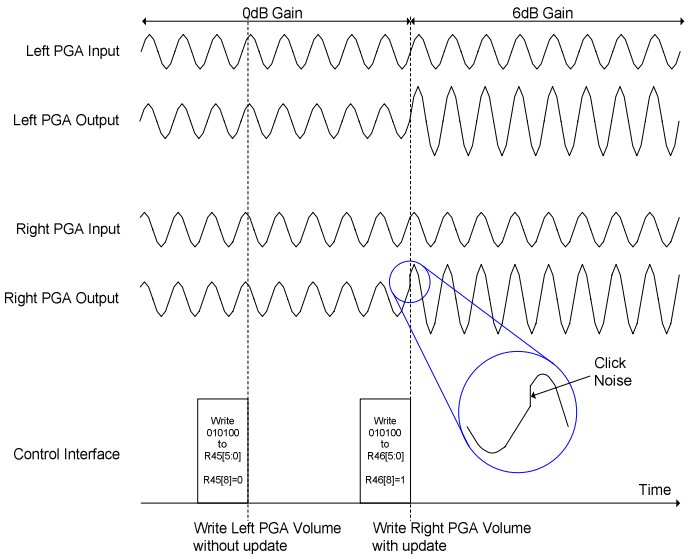


Figure 11 Click Noise During Volume Update

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 12.

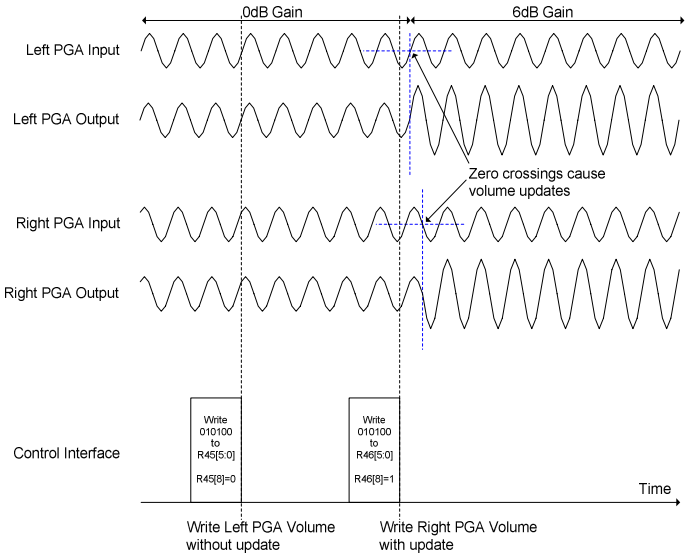


Figure 12 Volume Update Using Zero Cross Detection

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8980 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the INPPGAUPDATE bit is set as shown in Figure 13.

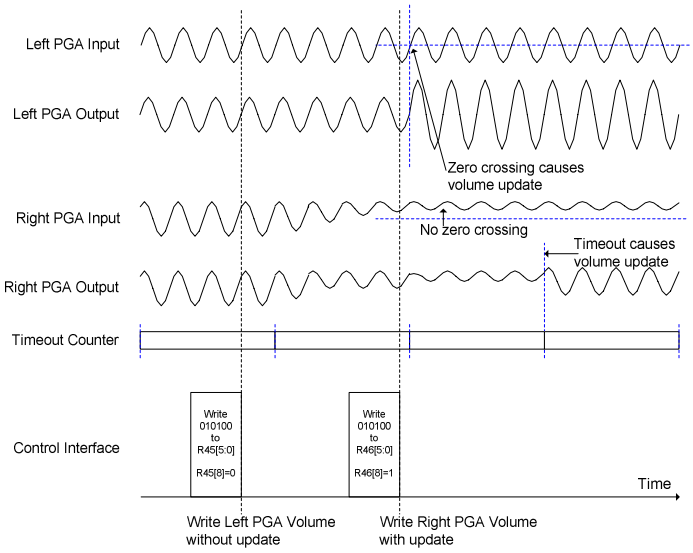


Figure 13 Volume Update after Timeout

AUXILLIARY INPUTS

There are two auxiliary inputs, AUX1 and AUX2 which can be used for a variety of purposes such as line inputs or as a 'beep' input signal to be mixed with the outputs.

The AUX1 input can be used as a line input to the input BOOST stage which has gain adjust of -12dB to +6dB in 3dB steps (plus off). See the INPUT BOOST section for further details.

The AUX1/2 inputs can also be mixed into the output channel mixers, with a gain of -15dB to +6dB plus off.

In addition the AUX2 input can be summed into the speaker output path (SPKOUTN) with a gain adjust of -15 to +6dB. This allows a 'beep' input to be output on the speaker outputs only without affecting the lineout signal.

INPUT BOOST

The input PGA stage is followed by an input BOOST circuit. The input BOOST circuit has 3 selectable inputs: the input microphone PGA output, the AUX amplifier output and the LINEIN input pin (can be used as a line input, bypassing the input PGA). These three inputs can be mixed together and have individual gain boost/adjust as shown in Figure 14.

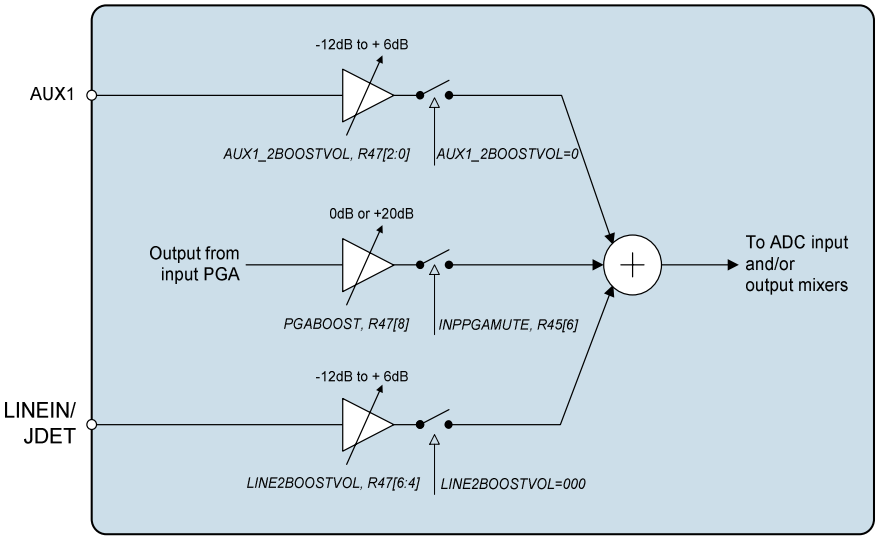


Figure 14 Input Boost Stage

The input PGA paths can have a +20dB boost (PGABOOST=1) , a 0dB pass through (PGABOOST=0) or be completely isolated from the input boost circuit (INPPGAMUTE=1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 Input BOOST control	8	PGABOOST	1	Boost enable for input PGA: 0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.

Table 6 Input BOOST Stage Control

The Auxiliary amplifier path to the BOOST stages is controlled by the AUX1_2BOOSTVOL[2:0] register bits. When AUX1_2BOOSTVOL=000 this path is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

The LINEIN path to the BOOST stage is controlled by the LINE2BOOSTVOL[2:0] register bits. When LINE2BOOSTVOL=000 the LINEIN input pin is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 Input BOOST control	2:0	AUX1_2BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage
	6:4	LINE2BOOSTVOL	000	Controls the LINEIN pin to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage

Table 7 Input BOOST Stage Control

The BOOST stage is enabled under control of the BOOSTEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	4	BOOSTEN	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON

Table 8 Input BOOST Enable Control

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBVSEL register bit. When MBVSEL=0, MICBIAS=0.9*AVDD and when MBVSEL=1, MICBIAS=0.65*AVDD. The output can be enabled or disabled using the MICBEN control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 9 Microphone Bias Enable Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input control	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 10 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 15. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

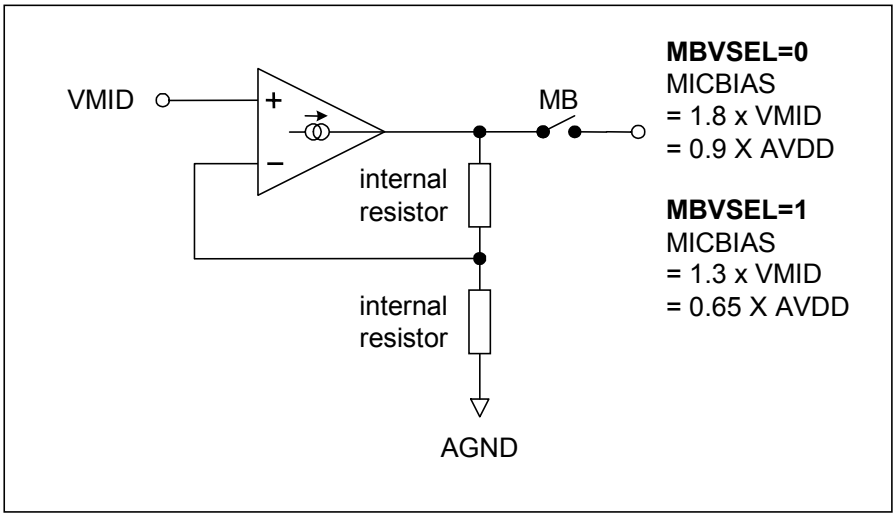


Figure 15 Microphone Bias Schematic

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8982 uses a multi-bit, oversampled sigma-delta ADC. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is $1.0V_{rms}$. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path for the ADC channel is illustrated in Figure 16.

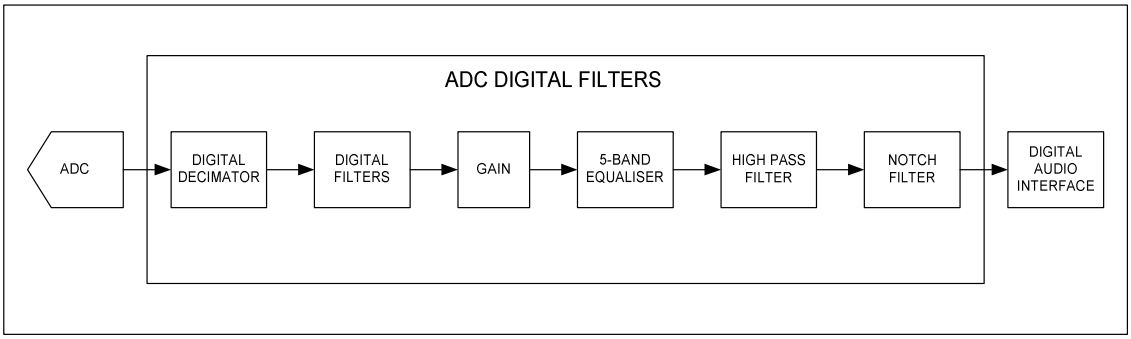


Figure 16 ADC Digital Filter Path

The ADCs are enabled by the ADCEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	0	ADCEN	0	Enable ADC: 0 = ADC disabled 1 = ADC enabled

Table 11 ADC Enable Control

The polarity of the output signal can also be changed under software control using the ADCPOL register bit. The oversampling rate of the ADC can be adjusted using the ADCOSR register bit. With ADCOSR=0 the oversample rate is 64x which gives lowest power operation and when ADCOSR=1 the oversample rate is 128x which gives best performance.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	0	ADCPOL	0	ADC polarity adjust: 0=normal 1=inverted
	3	ADCOSR	0	ADC oversample rate select: 0=64x (lower power) 1=128x (best performance)

Table 12 ADC Control

SELECTABLE HIGH PASS FILTER

A selectable high pass filter is provided. To disable this filter set HPFEN=0. The filter has two modes controlled by HPFAPP. In Audio Mode (HPFAPP=0) the filter is first order, with a cut-off frequency of 3.7Hz. In Application Mode (HPFAPP=1) the filter is second order, with a cut-off frequency selectable via the HPFCUT register. The cut-off frequencies when HPFAPP=1 are shown in Table 14.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1st order, fc = ~3.7Hz) 1=Application mode (2nd order, fc = HPFCUT)
	6:4	HPFCUT	000	Application mode cut-off frequency **See** Table 14 for details.

Table 13 ADC Enable Control

HPFCUT [2:0]	SR=101/100			SR=011/010			SR=001/000		
	fs (kHz)								
	8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	196	131	180	196	131	180	196
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 14 High Pass Filter Cut-off Frequencies (HPFAPP=1). Values in Hz.

Note that the High Pass filter values (when HPFAPP=1) acre calculated on the assumption that the SR register bits are set correctly for the actual sample rate as shown in Table 14.

PROGRAMMABLE NOTCH FILTER

A programmable notch filter is provided. This filter has a variable centre frequency and bandwidth, programmable via two coefficients, a0 and a1. The coefficients must be entered in 2's complement notation. a0 and a1 are represented by the register bits NFA0[13:0] and NFA1[13:0]. Because these coefficient values require four register writes to setup there is an NFU (Notch Filter Update) flag which should be set only when all four registers are setup.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 Notch Filter 1	6:0	NFA0[13:7]	0	Notch Filter a0 coefficient, bits [13:7]
	7	NFEN	0	Notch filter enable: 0=Disabled 1=Enabled
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R28 Notch Filter 2	6:0	NFA0[6:0]	0	Notch Filter a0 coefficient, bits [6:0]
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R29 Notch Filter 3	6:0	NFA1[13:7]	0	Notch Filter a1 coefficient, bits [13:7]
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R30 Notch Filter 4	6:0	NFA1[6:0]	0	Notch Filter a1 coefficient, bits [6:0]
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.

Table 15 Notch Filter Function

The coefficients are calculated as follows:

$$a_0 = \frac{1 - \tan(w_b / 2)}{1 + \tan(w_b / 2)}$$

$$a_1 = -(1 + a_0)\cos(w_0)$$

Where:

$$w_0 = 2\pi f_c / f_s$$

$$w_b = 2\pi f_b / f_s$$

f_c = centre frequency in Hz, f_b = -3dB bandwidth in Hz, f_s = sample frequency in Hz

The actual register values can be determined from the coefficients as follows:

NFA0 = -a0 x 2^{13}

NFA1 = -a1 x 2^{12}

NOTCH FILTER WORKED EXAMPLE

The following example illustrates how to calculate the a0 and a1 coefficients for a desired centre frequency and -3dB bandwidth.

fc = 1000 Hz

fb = 100 Hz

fs = 48000 Hz

$w_0 = 2\pi f_c / f_s$ = 2π x (1000 / 48000) = 0.1308996939 rads

$w_b = 2\pi f_b / f_s$ = 2π x (100 / 48000) = 0.01308996939 rads

$$a_0 = \frac{1-\tan(w_b/2)}{1+\tan(w_b/2)} = \frac{1-\tan(0.01308996939/2)}{1+\tan(0.01308996939/2)} = 0.9869949627$$

$$a_1 = -(1+a_0)\cos(w_0) = -(1+0.9869949627)\cos(0.1308996939) = -1.969995945$$

NFA0 = -a0 x 213 = -8085 (rounded to nearest whole number)

NFA1 = -a1 x 212 = 8069 (rounded to nearest whole number)

These values are then converted to a 2's complement notation:

NfnA0[12:0] = 13'h1F95; Converting to 2's complement NFA0 = 14'h4000 – 14'h1F95 = 14'h206B

NfnA1[12:0] = 13'h1F85; Converting to 2's complement NFA0 = 14'h1F85

DIGITAL ADC VOLUME CONTROL

The output of the ADC can be digitally attenuated over a range from –127dB to 0dB in 0.5dB steps. The gain for a given eight-bit code X is given by:

0.5 × (G-255) dB for 1 ≤ G ≤ 255; MUTE for G = 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 ADC Digital Volume	7:0	ADCVOL [7:0]	11111111 (0dB)	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
	8	ADCVU	Not latched	ADC volume does not update until a 1 is written to ADCVU

Table 16 ADC Digital Volume Control

INPUT LIMITER / AUTOMATIC LEVEL CONTROL (ALC)

The WM8982 has an automatic PGA gain control circuit, which can function as an input peak limiter or as an automatic level control (ALC).

The Automatic Level Control (ALC) provides continuous adjustment of the input PGA in response to the amplitude of the input signal. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level (ALCLVL).

If the signal is below the threshold, the ALC will increase the gain of the PGA at a rate set by ALCDCY. If the signal is above the threshold, the ALC will reduce the gain of the PGA at a rate set by ALCATK.

The ALC has two modes selected by the ALCMODE register: normal mode and peak limiter mode. The ALC/limiter function is enabled by setting the register bit R32[8] ALCSEL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ALC Control 1	2:0	ALCMIN [2:0]	000 (-12dB)	Set minimum gain of PGA 000 = -12dB 001 = -6dB 010 = 0dB 011 = +6dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +30dB
	5:3	ALCMAX [2:0]	111 (+35.25dB)	Set Maximum Gain of PGA 111 = +35.25dB 110 = +29.25dB 101 = +23.25dB 100 = +17.25dB 011 = +11.25dB 010 = +5.25dB 001 = -0.75dB 000 = -6.75dB
	8:7	ALCSEL	00	ALC function select 00 = ALC disabled 01 = Right channel ALC enabled 10 = Left channel ALC enabled 11 = Both channels ALC enabled
R33 (21h) ALC Control 2	3:0	ALCLVL [3:0]	1011 (-6dB)	ALC target – sets signal level at ADC input 1111 = -1.5dBFS 1110 = -1.5dBFS 1101 = -3dBFS 1100 = -4.5dBFS 1011 = -6dBFS 1010 = -7.5dBFS 1001 = -9dBFS 1000 = -10.5dBFS 0111 = -12dBFS 0110 = -13.5dBFS 0101 = -15dBFS 0100 = -16.5dBFS 0011 = -18dBFS 0010 = -19.5dBFS 0001 = -21dBFS 0000 = -22.5dBFS
	8		0	Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:4	ALCHLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms 0011 = 10.66ms 0100 = 21.32ms 0101 = 42.64ms 0110 = 85.28ms 0111 = 0.17s 1000 = 0.34s 1001 = 0.68s 1010 or higher = 1.36s
R34 (22h) ALC Control 3	8	ALCMODE	0	Determines the ALC mode of operation: 0 = ALC mode (Normal Operation) 1 = Limiter mode.
	7:4	ALCDCY [3:0]	0011 (26ms/6dB)	Decay (gain ramp-up) time (ALCMODE == 0)
				Per step: Per 6dB: 90% of range
				0000: 410us: 3.28ms: 23.6ms
				0001: 820us: 6.56ms: 47.2ms
				0010: 1.64ms: 13.1ms: 94.5ms
				… (time doubles with every step)
				1010 or higher: 420ms: 3.36s: 24.2s
			0011 (5.8ms/6dB)	Decay (gain ramp-up) time (ALCMODE == 1)
				Per step: Per 6dB: 90% of range
				0000: 90.8us: 726us: 5.23ms
				0001: 182us: 1.45ms: 10.5ms
				0010: 363us: 2.91ms: 20.9ms
				… (time doubles with every step)
				1010: 93ms: 744ms: 5.36s
	3:0	ALCATK [3:0]	0010 (3.3ms/6dB)	ALC attack (gain ramp-down) time (ALCMODE == 0)
				Per step: Per 6dB: 90% of range
				0000: 104us: 832us: 6ms
				0001: 208us: 1.66ms: 12ms
				0010: 416us: 3.33ms: 24ms
				… (time doubles with every step)
				1010 or higher: 106ms: 852ms: 6.13s
			0010 (726us/6dB)	ALC attack (gain ramp-down) time (ALCMODE == 1)
				Per step: Per 6dB: 90% of range
				0000: 22.7us: 182us: 1.31ms
				0001: 45.4us: 363us: 2.62ms
				0010: 90.8us: 726us: 5.23ms
				… (time doubles with every step)
				1010 or higher: 23.2ms: 186ms: 1.34s

Table 17 ALC Control Registers

When the ALC is disabled, the input PGA remains at the last controlled value of the ALC. An input gain update must be made by writing to the INPPGAVOLL/R register bits.

NORMAL MODE

In normal mode, the ALC will attempt to maintain a constant signal level by increasing or decreasing the gain of the PGA. The following diagram shows an example of this.

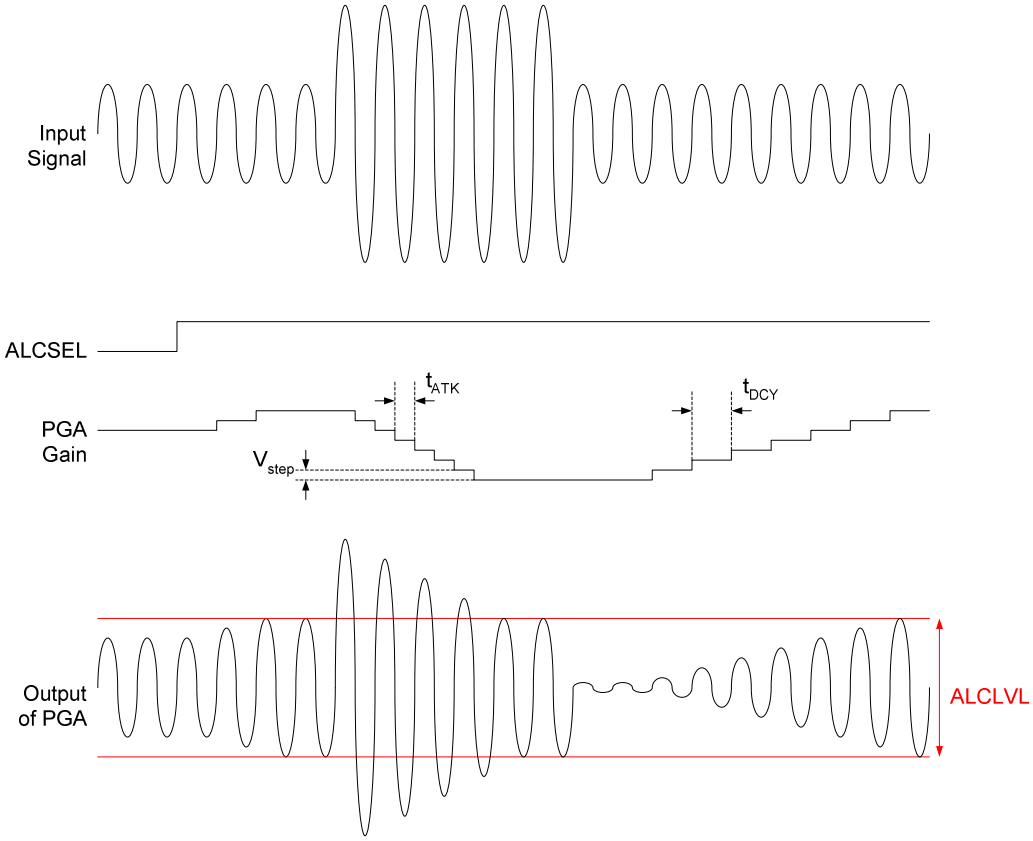


Figure 17 ALC Normal Mode Operation

LIMITER MODE

In limiter mode, the ALC will reduce peaks that go above the threshold level, but will not increase the PGA gain beyond the starting level. The starting level is the PGA gain setting when the ALC is enabled in limiter mode. If the ALC is started in limiter mode, this is the gain setting of the PGA at start-up. If the ALC is switched into limiter mode after running in ALC mode, the starting gain will be the gain at switchover. The diagram below shows an example of limiter mode.

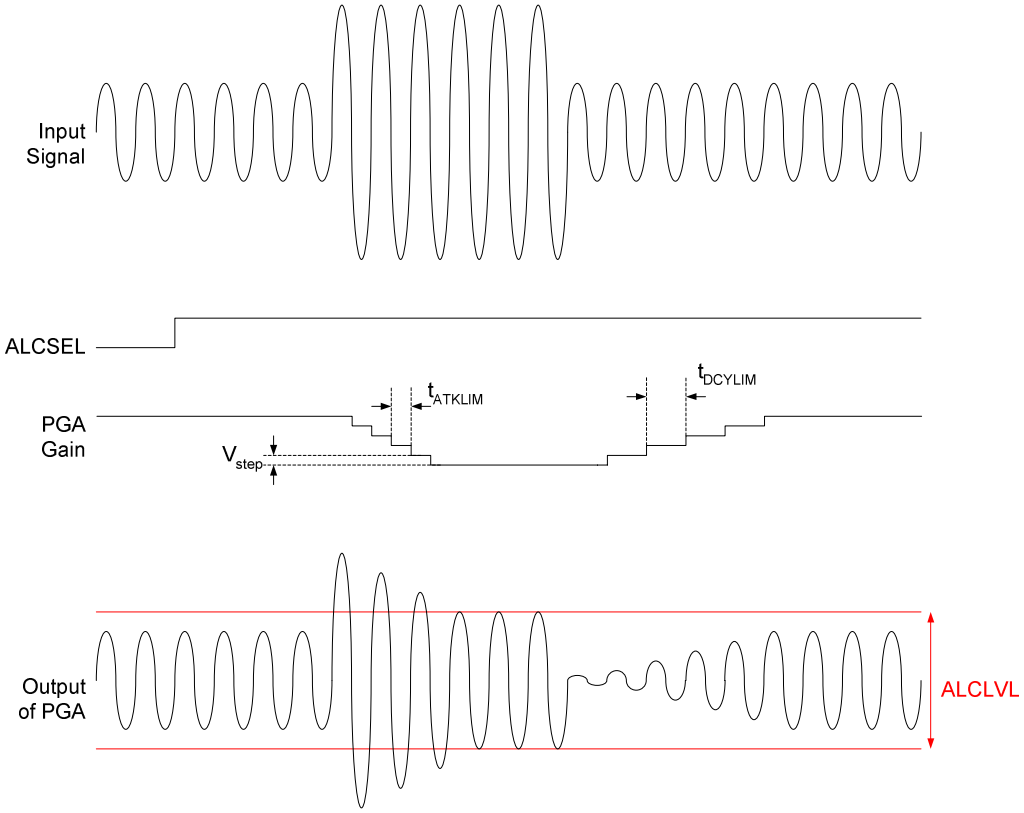


Figure 18 ALC Limiter Mode Operation

ALC LIMITER MODE INITIALISATION SEQUENCE

In order to properly initialise the ALC function, the following sequence of register writes is required:

1. Set INPPGAVOLL to the required input PGA gain (R45[5:0]).
2. Enable analogue inputs (R44[2:0]) as required.
3. Disable INPPGAENL (R2[2] =0).
4. Set ALCMAXGAIN (R32[5:3]) and ALCMINGAIN (R32[2:0]) to the required level for operation.
5. Set ALCLVL (R33[3:0]) to the required level for operation.
6. Set R34 to 0x000.
7. Wait for 1ms to allow the input PGA gain to update by the limiter circuit.
8. Enable Limiter mode (R34[8]=1).
9. Wait for 1ms to allow the input PGA gain to update by the limiter circuit.
10. Enable INPPGAENL (R2[2] =1).

ATTACK AND DECAY TIMES

The attack and decay times set the update times for the PGA gain. The attack time is the time constant used when the gain is reducing. The decay time is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode. The time constants are shown below in terms of a single gain step, a change of 6dB and a change of 90% of the PGAs gain range.

Note that, these times will vary slightly depending on the sample rate used (specified by the SR register).

NORMAL MODE

ALCMODE = 0 (Normal Mode)			
	Attack Time (s)		
ALCATK	t_{ATK}	t_{ATK6dB}	$t_{ATK90\%}$
0000	104µs	832µs	6ms
0001	208µs	1.66ms	12ms
0010	416µs	3.33ms	24ms
0011	832µs	6.66ms	48ms
0100	1.66ms	13.3ms	96ms
0101	3.33ms	26.6ms	192ms
0110	6.66ms	53.2ms	384ms
0111	13.3ms	106ms	767ms
1000	26.6ms	213.2ms	1.53s
1001	53.2ms	426ms	3.07s
1010	106ms	852ms	6.13s

ALCMODE = 0 (Normal Mode)			
	Decay Time (s)		
ALCDCY	t_{DCY}	t_{DCY6dB}	$t_{DCY90\%}$
0000	410µs	3.28ms	23.6ms
0001	820µs	6.56ms	47.2ms
0010	1.64ms	13.1ms	94.5ms
0011	3.28ms	26.2ms	189ms
0100	6.56ms	52.5ms	378ms
0101	13.1ms	105ms	756ms
0110	26.2ms	210ms	1.51s
0111	52.5ms	420ms	3.02s
1000	105ms	840ms	6.05s
1001	210ms	1.68s	12.1s
1010	420ms	3.36s	24.2s

Table 18 ALC Normal Mode (Attack and Decay times)

LIMITER MODE

ALCMODE = 1 (Limiter Mode)			
	Attack Time (s)		
ALCATK	t_{ATKLIM}	$t_{ATKLIM6dB}$	$t_{ATKLIM90\%}$
0000	22.7µs	182µs	1.31ms
0001	45.4µS	363µs	2.62ms
0010	90.8µS	726µs	5.23ms
0011	182µS	1.45ms	10.5ms
0100	363µS	2.91ms	20.9ms
0101	726µS	5.81ms	41.8ms
0110	1.45ms	11.6ms	83.7ms
0111	2.9ms	23.2ms	167ms
1000	5.81ms	46.5ms	335ms
1001	11.6ms	93ms	669ms
1010	23.2ms	186ms	1.34s

ALCMODE = 1 (Limiter Mode)			
	Attack Time (s)		
ALCDCY	t_{DCYLIM}	$t_{DCYLIM6dB}$	$t_{DCYLIM90\%}$
0000	90.8µs	726µs	5.23ms
0001	182µS	1.45ms	10.5ms
0010	363µS	2.91ms	20.9ms
0011	726µS	5.81ms	41.8ms
0100	1.45ms	11.6ms	83.7ms
0101	2.91ms	23.2ms	167ms
0110	5.81ms	46.5ms	335ms
0111	11.6ms	93ms	669ms
1000	23.2ms	186ms	1.34s
1001	46.5ms	372ms	2.68s
1010	93ms	744ms	5.36s

Table 19 ALC Limiter Mode (Attack and Decay times)

MINIMUM AND MAXIMUM GAIN

The ALCMIN and ALCMAX register bits set the minimum/maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32	5:3	ALCMAX	111	Set Maximum Gain of PGA
ALC Control 1	2:0	ALCMIN	000	Set minimum gain of PGA

Table 20 ALC Max/Min Gain

In normal mode, ALCMAX sets the maximum boost which can be applied to the signal. In limiter mode, ALCMAX will normally have no effect (assuming the starting gain value is less than the maximum gain specified by ALCMAX) because the maximum gain is set at the starting gain level.

ALCMIN sets the minimum gain value which can be applied to the signal.

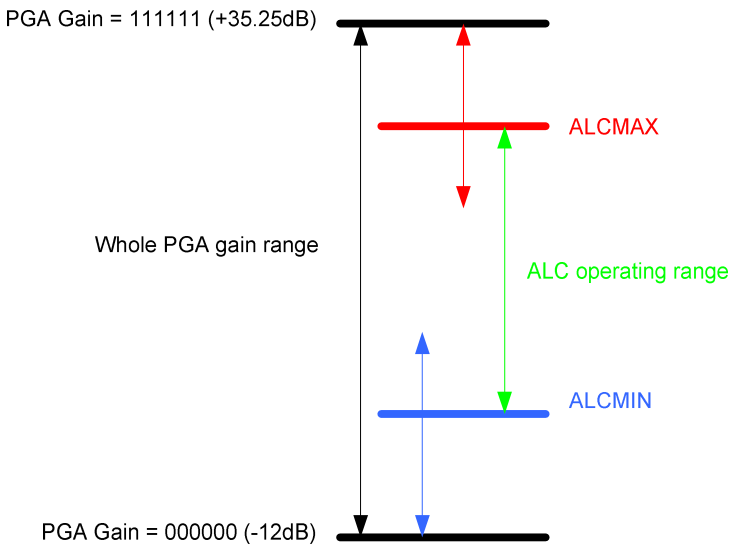


Figure 19 ALC Min/Max Gain

ALCMAX	Maximum Gain (dB)
111	35.25
110	29.25
101	23.25
100	17.25
011	11.25
010	5.25
001	-0.75
000	-6.75

Table 21 ALC Max Gain Values

ALCMIN	Minimum Gain (dB)
000	-12
001	-6
010	0
011	6
100	12
101	18
110	24
111	30

Table 22 ALC Min Gain Values

Note that if the ALC gain setting strays outside the ALC operating range, either by starting the ALC outside of the range or changing the ALCMAX or ALCMIN settings during operation, the ALC will immediately adjust the gain to return to the ALC operating range. It is recommended that the ALC starting gain is set between the ALCMAX and ALCMIN limits.

ALC HOLD TIME (NORMAL MODE ONLY)

In Normal mode, the ALC has an adjustable hold time which sets a time delay before the ALC begins its decay phase (gain increasing). The hold time is set by the ALCHLD register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 ALC Control 2	7:4	ALCHLD	0000	ALC hold time before gain is increased.

Table 23 ALC Hold Time

If the hold time is exceeded this indicates that the signal has reached a new average level and the ALC will increase the gain to adjust for that new average level. If the signal goes above the threshold during the hold period, the hold phase is abandoned and the ALC returns to normal operation.

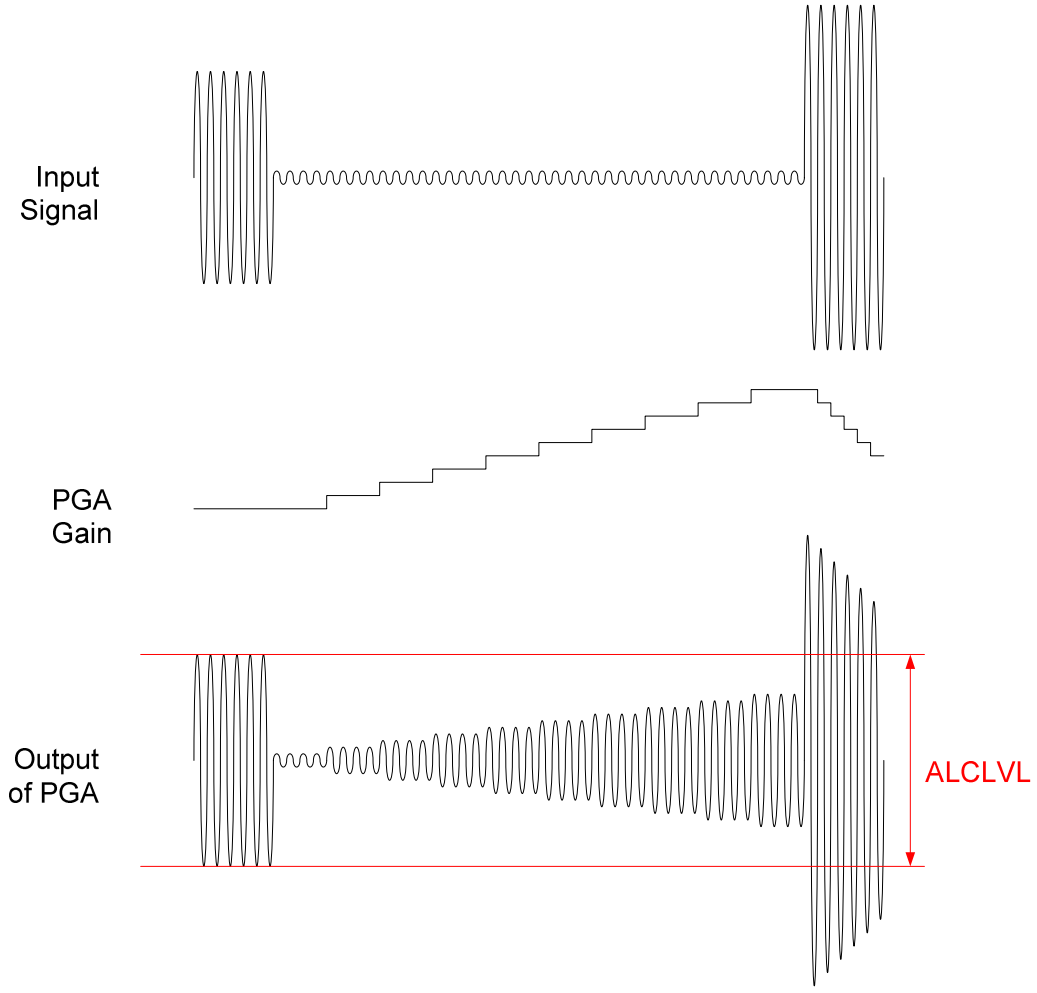


Figure 20 ALCLVL

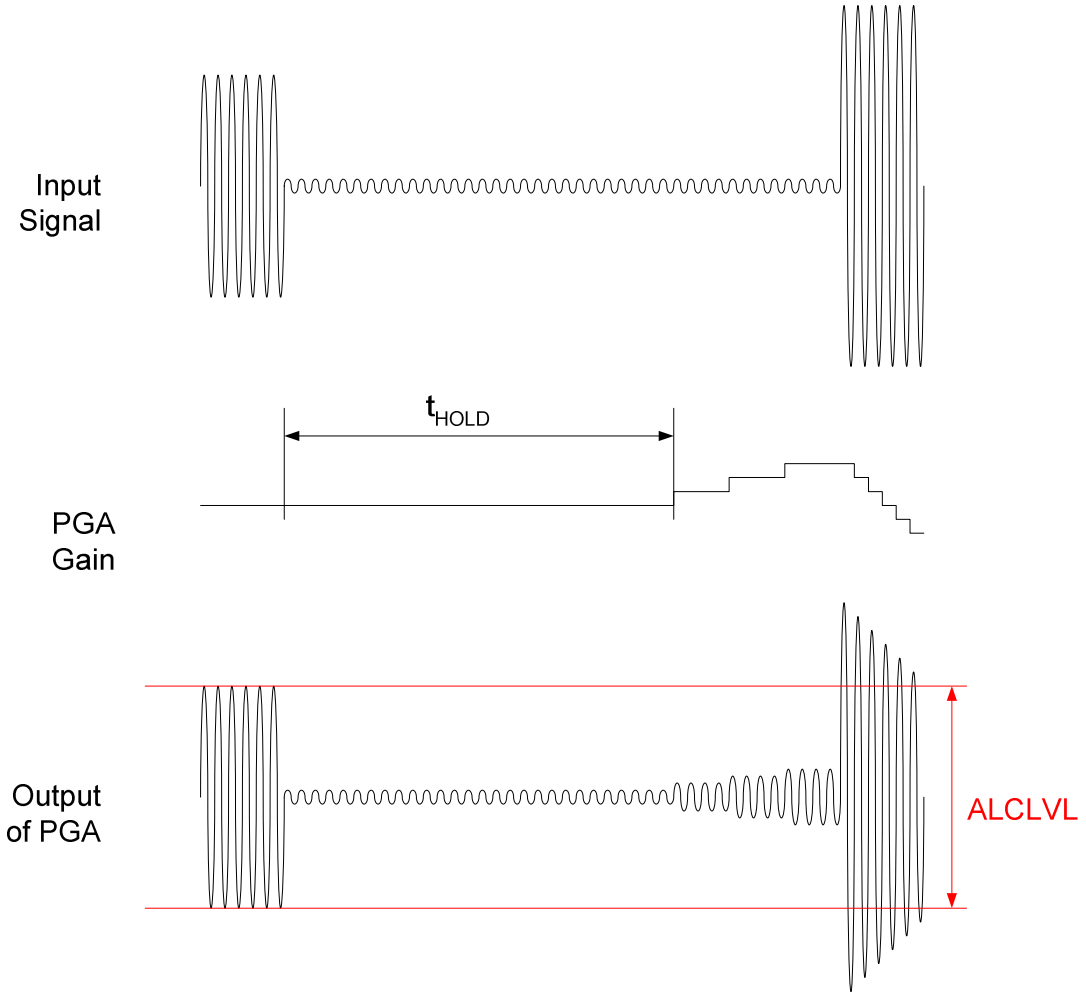


Figure 21 ALC Hold Time

ALCHLD	t_{HOLD} (s)
0000	0
0001	2.67ms
0010	5.34ms
0011	10.7ms
0100	21.4ms
0101	42.7ms
0110	85.4ms
0111	171ms
1000	342ms
1001	684ms
1010	1.37s

Table 24 ALC Hold Time Values

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ALCATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note: If ALCATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE (NORMAL MODE ONLY)

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM8982 has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

Signal level at ADC [dBFS] < NGTH [dBFS] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

Signal level at input pin [dBFS] < NGTH [dBFS]

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 6dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. The noise gate only operates in conjunction with the ALC and cannot be used in limiter mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h) ALC Noise Gate Control	2:0	NGTH	000	Noise gate threshold: 000 = -39dB 001 = -45dB 010 = -51db 011 = -57dB 100 = -63dB 101 = -69dB 110 = -75dB 111 = -81dB
	3	NGATEN	0	Noise gate function enable 1 = enable 0 = disable

Table 25 ALC Noise Gate Control

The diagrams below show the response of the system to the same signal with and without noise gate.

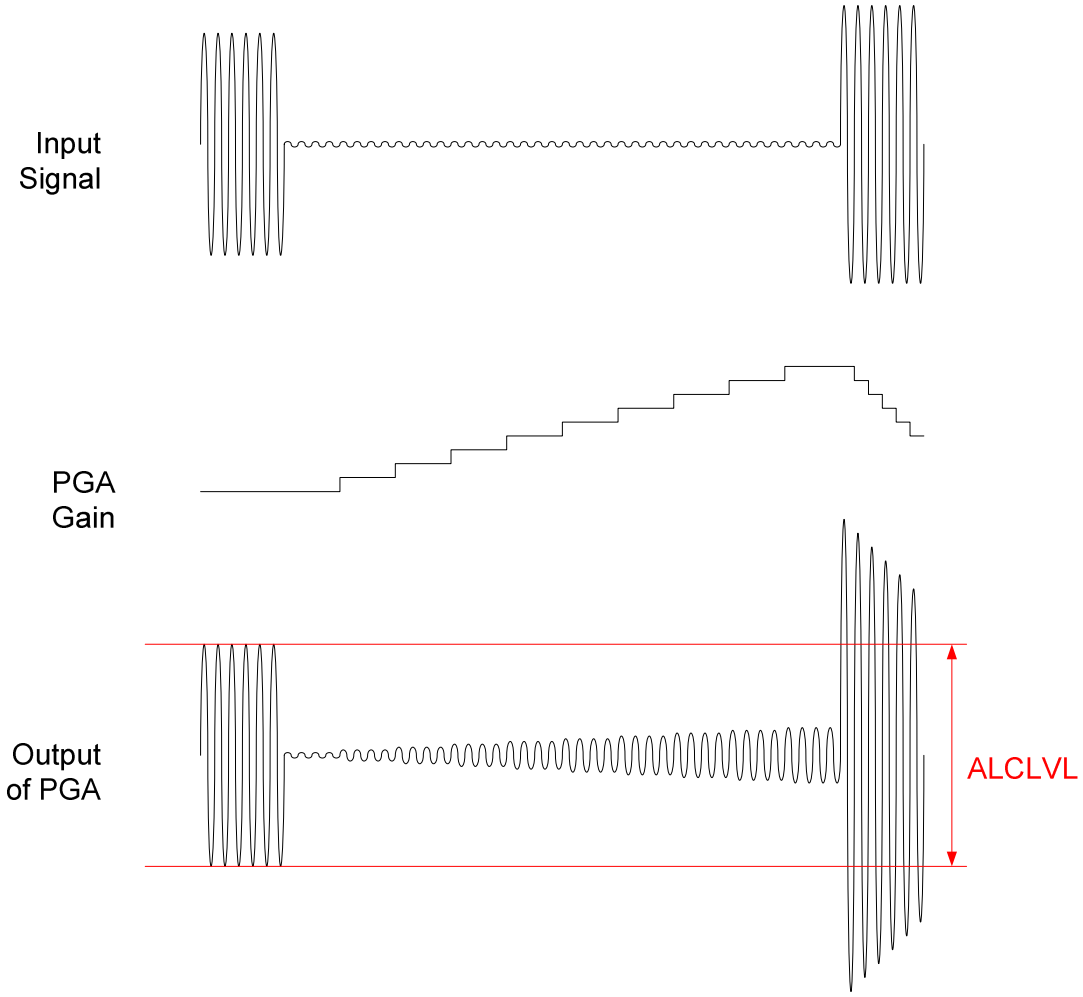


Figure 22 ALC Operation Above Noise Gate Threshold

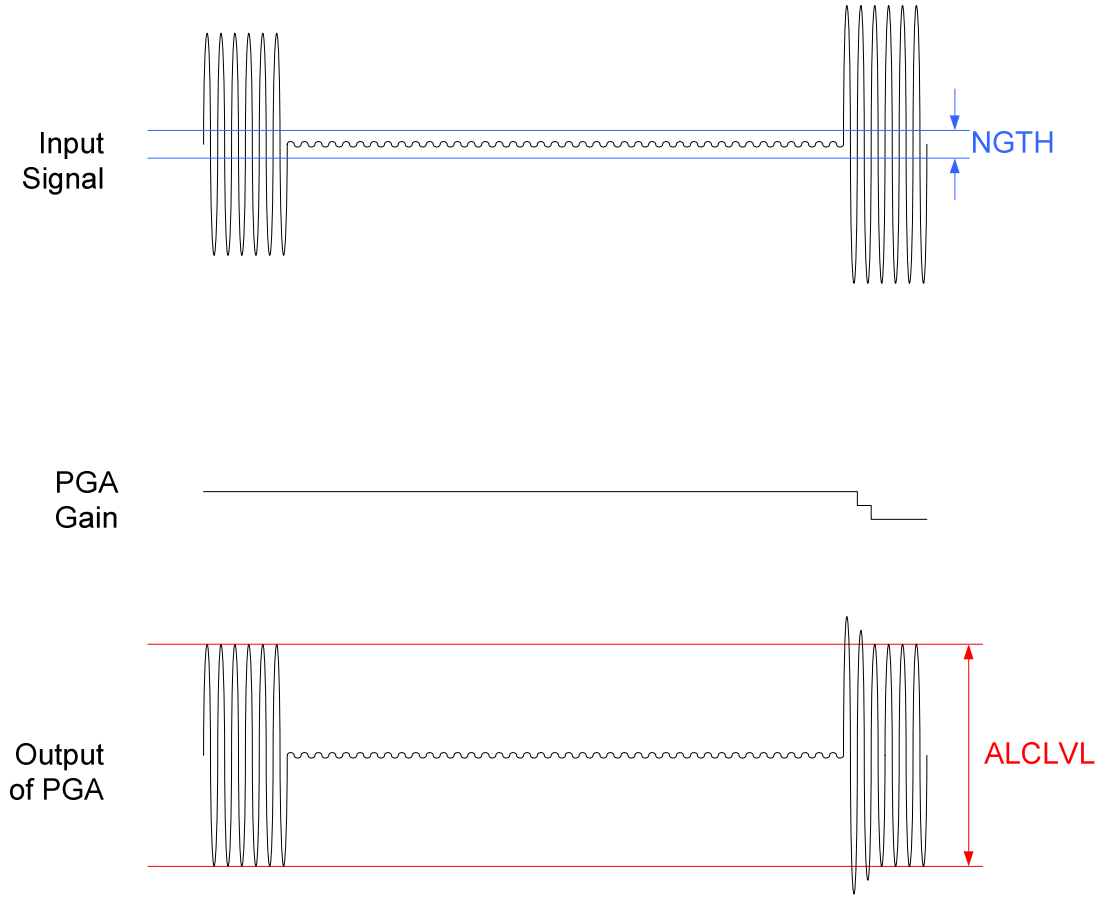


Figure 23 Noise Gate Operation

OUTPUT SIGNAL PATH

The WM8982 output signal paths consist of digital application filters, up-sampling filters, Hi-Fi DAC, analogue mixers, speaker/headphone, and line/mono/midrail output drivers. The digital filters and DAC are enabled by register bit DACEN. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8982, irrespective of whether the DAC is running or not.

The WM8982 DAC receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Graphic equaliser
- A digital peak limiter.
- Sigma-Delta Modulation

A high performance sigma-delta audio DAC converts the digital data into an analogue signal.

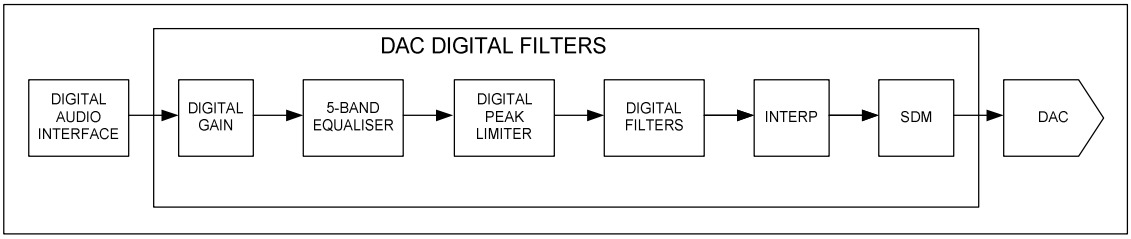


Figure 24 DAC Digital Filter Path

The analogue output from the DAC can then be mixed with the aux analogue inputs and the ADC analogue inputs. The mix is fed to the output drivers for headphone or speaker (SPKOUTP/N) or line (MONOOUT). MONOOUT has an additional mixer which allows it to output a different signals to the speaker outputs.

DIGITAL PLAYBACK (DAC) PATH

Digital data is passed to the WM8982 via the flexible audio interface and is then passed through a variety of advanced digital filters as shown in Figure 24 to the hi-fi DAC. The DAC is enabled by the DACEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 Power Management 3	0	DACEN	0	DAC enable 0 = DAC disabled 1 = DAC enabled

Table 26 DAC Enable Control

The WM8982 also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will ramp back up to the digital gain setting.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 DAC Control	0	DACPOL	0	DAC output polarity: 0 = non-inverted 1 = inverted (180 degrees phase shift)
	2	AMUTE	0	Automute enable 0 = Amute disabled 1 = Amute enabled
	3	DACOSR	0	DAC oversampling rate: 0=64x (lowest power) 1=128x (best performance)
	6	SOFTMUTE	0	Softmute enable: 0=Enabled 1=Disabled

Table 27 DAC Control Register

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters the multi-bit, sigma-delta DAC, which converts it to a high quality analogue audio signal. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The DAC output defaults to non-inverted. Setting DACPOL will invert the DAC output phase.

AUTOMUTE

The DAC has an automute function which applies an analogue mute when 1024 consecutive zeros are detected. The mute is released as soon as a non-zero sample is detected. Automute can be disabled using the AMUTE control bit.

DIGITAL HI-FI DAC VOLUME (GAIN) CONTROL

The signal volume from the Hi-Fi DAC can be controlled digitally. The gain and attenuation range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$0.5 \times (X-255)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 DAC Digital Volume	7:0	DACVOL [7:0]	11111111 (0dB)	DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
	8	DACVU	Not latched	DAC volume does not update until a 1 is written to DACVU

Table 28 DAC Digital Volume Control

Note: An additional gain of up to +12dB can be added using the gain block embedded in the digital peak limiter circuit (see DAC OUTPUT LIMITER section).

DAC 5-BAND EQUALISER

A 5-band graphic equaliser function which can be used to change the output frequency levels to suit the environment. This can be applied to the ADC or DAC path and is described in the 5-BAND EQUALISER section for further details on this feature.

DAC DIGITAL OUTPUT LIMITER

The WM8982 has a digital output limiter function. The operation of this is shown in Figure 25. In this diagram the upper graph shows the envelope of the input/output signals and the lower graph shows the gain characteristic.

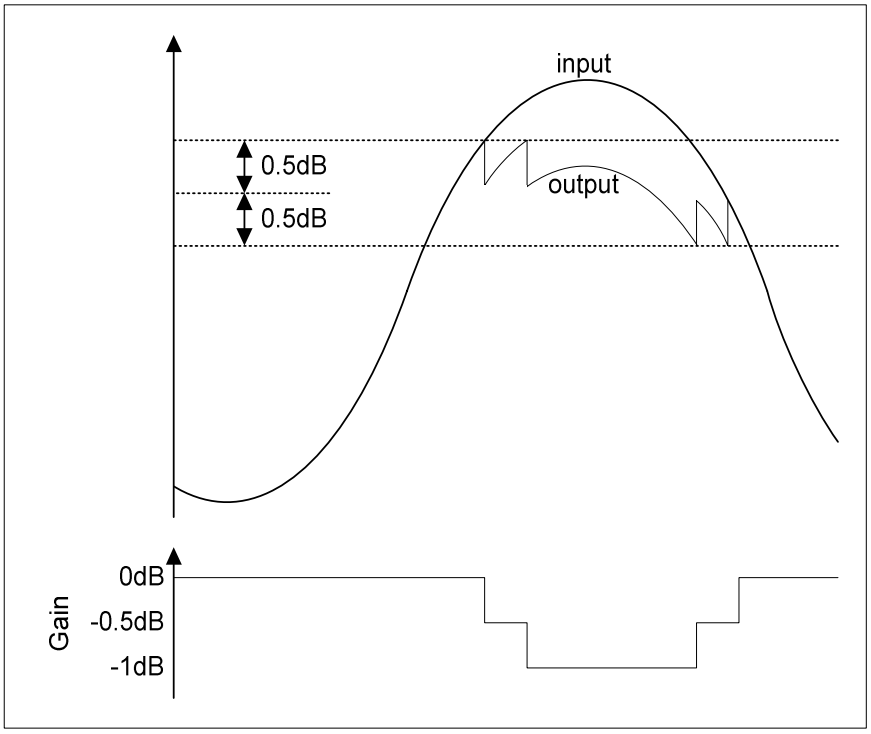


Figure 25 DAC Digital Limiter Operation

The limiter has a programmable upper threshold which is close to 0dB. Referring to Figure 25, in normal operation (LIMBOOST=000 => limit only) signals below this threshold are unaffected by the limiter. Signals above the upper threshold are attenuated at a specific attack rate (set by the LIMATK register bits) until the signal falls below the threshold. The limiter also has a lower threshold 1dB below the upper threshold. When the signal falls below the lower threshold the signal is amplified at a specific decay rate (controlled by LIMDCY register bits) until a gain of 0dB is reached. Both threshold levels are controlled by the LIMLVL register bits. The upper threshold is 0.5dB above the value programmed by LIMLVL and the lower threshold is 0.5dB below the LIMLVL value.

VOLUME BOOST

The limiter has programmable upper gain which boosts signals below the threshold to compress the dynamic range of the signal and increase its perceived loudness. This operates as an ALC function with limited boost capability. The volume boost is from 0dB to +12dB in 1dB steps, controlled by the LIMBOOST register bits.

The output limiter volume boost can also be used as a stand alone digital gain boost when the limiter is disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 DAC digital limiter control 1	3:0	LIMATK	0010	Limiter Attack time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate. 0000=94us 0001=188s 0010=375us 0011=750us 0100=1.5ms 0101=3ms 0110=6ms 0111=12ms 1000=24ms 1001=48ms 1010=96ms 1011 to 1111=192ms
	7:4	LIMDCY	0011	Limiter Decay time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate: 0000=750us 0001=1.5ms 0010=3ms 0011=6ms 0100=12ms 0101=24ms 0110=48ms 0111=96ms 1000=192ms 1001=384ms 1010=768ms 1011 to 1111=1.536s
	8	LIMEN	0	Enable the DAC digital limiter: 0=disabled 1=enabled
R25 DAC digital limiter control 2	3:0	LIMBOOST	0000	Limiter volume boost (can be used as a stand alone volume boost when LIMEN=0): 0000=0dB 0001=+1dB 0010=+2dB … (1dB steps) 1011=+11dB 1100=+12dB 1101 to 1111=reserved
	6:4	LIMLVL	000	Programmable signal threshold level (determines level at which the limiter starts to operate) 000=-1dB 001=-2dB 010=-3dB 011=-4dB 100=-5dB 101 to 111=-6dB

Table 29 DAC Digital Limiter Control

5-BAND GRAPHIC EQUALISER

A 5-band graphic EQ is provided, which can be applied to the ADC or DAC path, under control of the EQMODE register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 EQ Control 1	8	EQMODE	1	0 = Equaliser applied to ADC path 1 = Equaliser applied to DAC path

Table 30 EQ DAC or ADC Path Select

The equaliser consists of low and high frequency shelving filters (Band 1 and 5) and three peak filters for the centre bands. Each has adjustable cut-off or centre frequency, and selectable boost (+/-12dB in 1dB steps). The peak filters have selectable bandwidth.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 EQ Band 1 Control	4:0	EQ1G	01100 (0dB)	Band 1 Gain Control. See Table 36 for details.
	6:5	EQ1C	01	Band 1 Cut-off Frequency: 00=80Hz 01=105Hz 10=135Hz 11=175Hz

Table 31 EQ Band 1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 EQ Band 2 Control	4:0	EQ2G	01100 (0dB)	Band 2 Gain Control. See Table 36 for details.
	6:5	EQ2C	01	Band 2 Centre Frequency: 00=230Hz 01=300Hz 10=385Hz 11=500Hz
	8	EQ2BW	0	Band 2 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth

Table 32 EQ Band 2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 EQ Band 3 Control	4:0	EQ3G	01100 (0dB)	Band 3 Gain Control. See Table 36 for details.
	6:5	EQ3C	01	Band 3 Centre Frequency: 00=650Hz 01=850Hz 10=1.1kHz 11=1.4kHz
	8	EQ3BW	0	Band 3 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth

Table 33 EQ Band 3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 EQ Band 4 Control	4:0	EQ4G	01100 (0dB)	Band 4 Gain Control. See Table 36 for details
	6:5	EQ4C	01	Band 4 Centre Frequency: 00=1.8kHz 01=2.4kHz 10=3.2kHz 11=4.1kHz
	8	EQ4BW	0	Band 4 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth

Table 34 EQ Band 4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 EQ Band 5 Gain Control	4:0	EQ5G	01100 (0dB)	Band 5 Gain Control. See Table 36 for details.
	6:5	EQ5C	01	Band 5 Cut-off Frequency: 00=5.3kHz 01=6.9kHz 10=9kHz 11=11.7kHz

Table 35 EQ Band 5 Control

GAIN REGISTER	GAIN
00000	+12dB
00001	+11dB
00010	+10dB
…. (1dB steps)	
01100	0dB
01101	-1dB
11000	-12dB
11001 to 11111	Reserved

Table 36 Gain Register Table

ANALOGUE OUTPUTS

The WM8982 has three analogue outputs. These are:

- SPKOUTP and SPKOUTN – normally used to drive an 8Ω BTL speaker.
- MONOOUT – line output.

SPKOUTP/N and MONOOUT are supplied from SPKVDD and are capable of driving up to 1.5Vrms signals as shown in Figure 26.

SPKOUTP and SPKOUTN have individual analogue volume PGAs with -57dB to +6dB ranges.

There are three output mixers in the output signal path, the two SPKOUTN/P mixers which control the signals to speaker, and also a dedicated MONOOUT mixer.

SPEAKER OUTPUT CHANNEL MIXERS

The speaker output channel mixers are shown in Figure 26. These mixers allow the AUX inputs, the ADC bypass and the DAC channels to be combined as desired. This allows a mix of the DAC channel with external line-in from the AUX or speech from the input bypass path.

The AUX and bypass inputs have individual volume control from -15dB to +6dB and the DAC volume can be adjusted in the digital domain if required. The output of these mixers goes to the speaker (SPKOUTP/N) and can optionally go to the MONOOUT mixer.

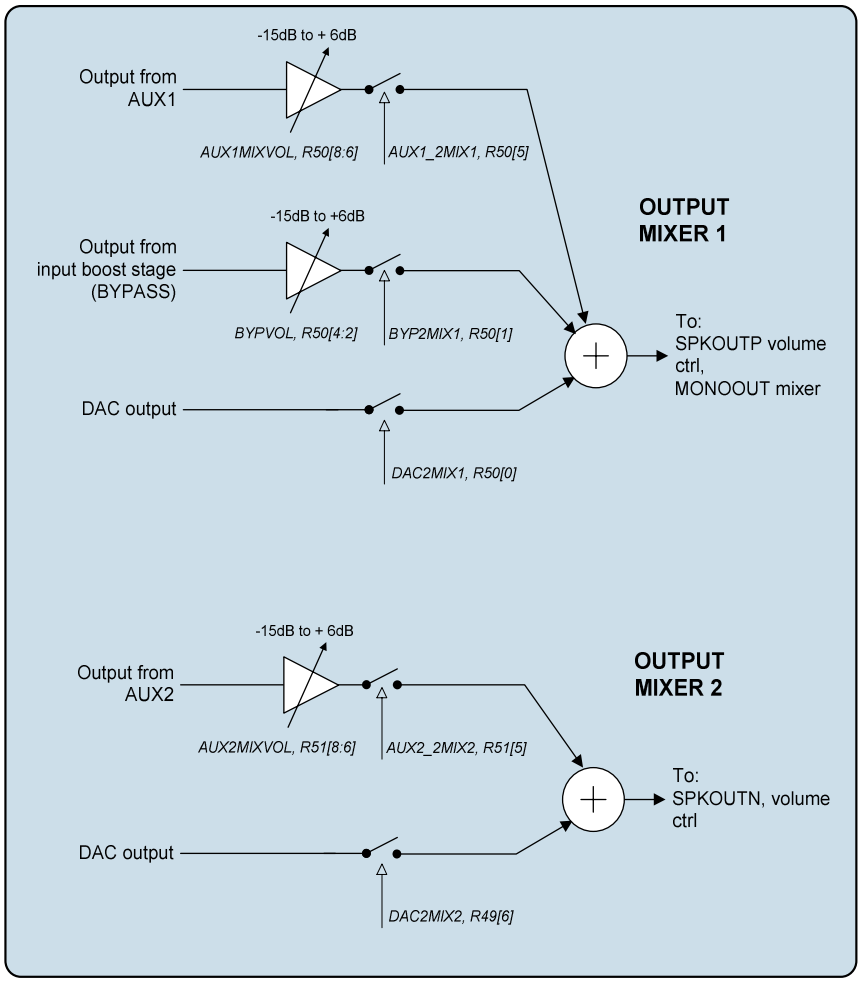


Figure 26 Output Mixers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 Output mixer control	6	DAC2MIX2	0	DAC output to output mixer 2 0 = not selected 1 = selected
R50 Output mixer 1 control	0	DAC2MIX1	1	DAC output to output mixer 1 0 = not selected 1 = selected
	1	BYP2MIX1	0	Bypass path (from the input boost output) to output mixer 1 0 = not selected 1 = selected
	4:2	BYPVOL	000	Bypass volume contol to output mixer 1: 000 = -15dB 001 = -12dB … 101 = 0dB 110 = +3dB 111 = +6dB
	5	AUX1_2MIX1	0	Aux 1 input to output mixer 1: 0 = not selected 1 = selected
	8:6	AUX1MIXVOL	000	Aux 1 input to output mixer 1 volume control: 000 = -15dB 001 = -12dB … 101 = 0dB 110 = +3dB 111 = +6dB
R51 Output mixer 2 control	5	AUX2_2MIX2	0	Aux 2 input to output mixer 2: 0 = not selected 1 = selected
	8:6	AUX2MIXVOL	000	Aux 2 input to output mixer 2 volume control: 000 = -15dB 001 = -12dB … 101 = 0dB 110 = +3dB 111 = +6dB
R3 Power management 3	2	MIX1EN	0	Output mixer 1 enable: 0 = disabled 1= enabled
	3	MIX2EN	0	Output mixer 2 enable: 0 = disabled 1 = enabled

Table 37 Output Mixer Control

SPEAKER OUTPUTS (SPKOUTP AND SPKOUTN)

The outputs SPKOUTP and SPKOUTN are designed to drive an 8Ω BTL speaker but can optionally drive two headphone loads of 16Ω/32Ω or a line output. Each output has an individual volume control PGA, an output boost/level shift bit, a mute and an enable as shown in Figure 27. SPKOUTP and SPKOUTN output the Output Mixer 1 and Output Mixer 2 mixer outputs respectively.

The SPKOUTN signal path also has an optional invert. The amplifier used for this invert can be used to mix in the AUX2 signal with an adjustable gain range of -15dB -> +6dB. This allows a 'beep' signal to be applied only to the speaker output without affecting the line output.

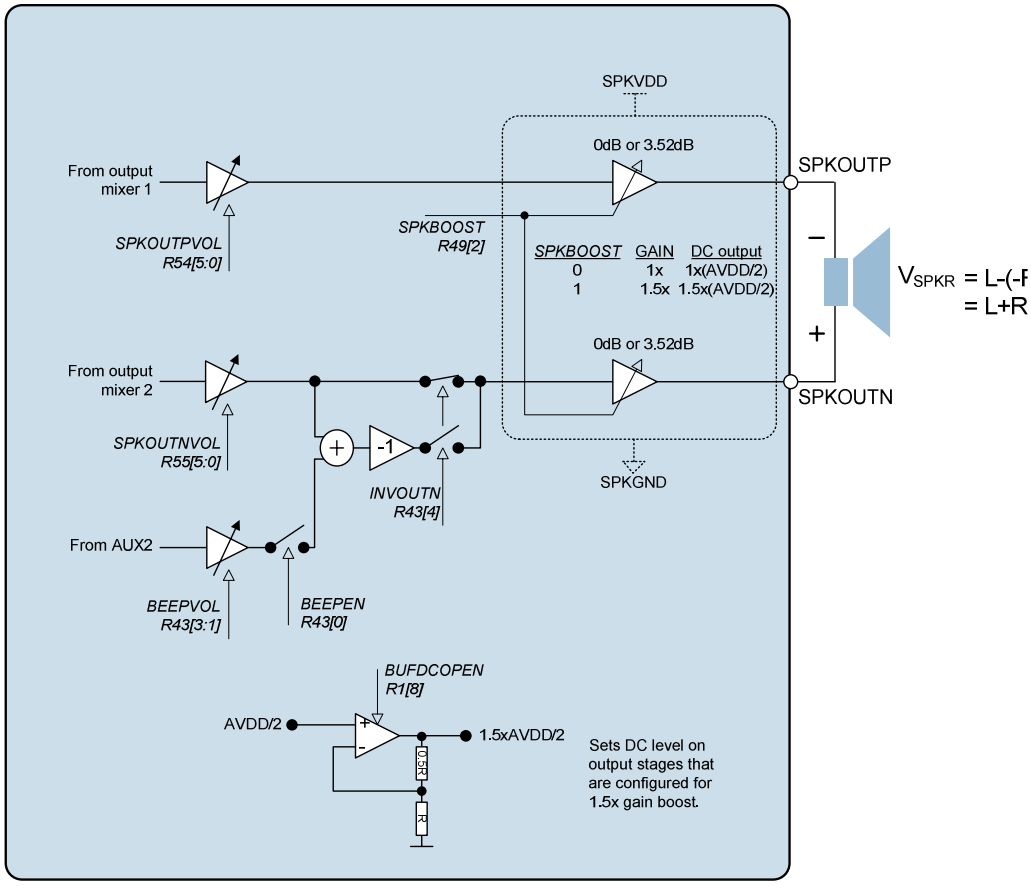


Figure 27 Speaker Outputs SPKOUTP and SPKOUTN

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 SPKOUTP Volume control	7	SPKOUTPZC	0	Speaker volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately
	6	SPKOUTPMUTE	0	Speaker +ve output mute: 0 = Normal operation 1 = Mute
	5:0	SPKOUTPVOL	111001	Speaker +ve output volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB
	8	SPKVU	Not latched	SPKOUTP and SPKOUTN volumes do not update until a 1 is written to SPKVU (in reg 54 or 55)
R55 SPKOUTN Volume control	7	SPKOUTNZC	0	Speaker volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately
	6	SPKOUTNMUTE	0	Speaker -ve output mute: 0 = Normal operation 1 = Mute
	5:0	SPKOUTNVOL	111001	Speaker -ve output volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB
	8	SPKVU	Not latched	SPKOUTP and SPKOUTN volumes do not update until a 1 is written to SPKVU (in reg 54 or 55)

Table 38 Speaker Volume Control

The signal to be output on SPKOUTP/SPKOUTN comes from Output Mixer 1 / Output Mixer 2 circuits and can be any combination of the DAC output, the Bypass path (output of the input boost stage) and the AUX inputs. The SPKOUTP/SPKOUTN volume is controlled by the SPKOUTPVOL/ SPKOUTNVOL register bits. Note that gains over 0dB may cause clipping if the signal is large. The SPKOUTPMUTE/ SPKOUTNMUTE register bits cause the speaker outputs to be muted (the output DC level is driven out). The output pins remain at the same DC level (DCOP), so that no click noise is produced when muting or un-muting

The speaker output stages also have a selectable gain boost of 1.5x (3.52dB). When this boost is enabled the output DC level is also level shifted (from AVDD/2 to 1.5xAVDD/2) to prevent the signal from clipping. A dedicated amplifier BUFDCOP, as shown in Figure 28, is used to perform the DC level shift operation. This buffer must be enabled using the BUFDCOPEN register bit for this operating mode. It should also be noted that if SPKVDD is not equal to or greater than 1.5xAVDD this boost mode may result in signals clipping. Table 40 summarises the effect of the SPKRBOOST control bits.

Note: When boost mode is selected, it is necessary to set LOUT2MUTE (R54[6]) and ROUT2MUTE (R55[6]) bits for either output to be muted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 Output control	2	SPKRBOOST	0	0 = speaker gain = -1; DC = AVDD / 2 1 = speaker gain = +1.5; DC = 1.5 x AVDD / 2
R1 Power management 1	8	BUFDCOPEN	0	Dedicated buffer for DC level shifting output stages when in 1.5x gain boost configuration. 0=Buffer disabled 1=Buffer enabled (required for 1.5x gain boost)

Table 39 Speaker Boost Stage Control

SPKRBOOST	OUTPUT STAGE GAIN	OUTPUT DC LEVEL	OUTPUT STAGE CONFIGURATION
0	1x (0dB)	AVDD/2	Inverting
1	1.5x (3.52dB)	1.5xAVDD/2	Non-inverting

Table 40 Output Boost Stage Details

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 Beep control	5	MUTEPGA2INV	0	Mute input to INVOUTN mixer
	4	INVOUTN	0	Invert SPKOUTN output
	3:1	BEEPVOL	000	AUX2 input to SPKOUTN inverter gain 000 = -15dB ... 111 = +6dB
	0	BEEPEN	0	0 = mute AUX2 beep input 1 = enable AUX2 beep input

Table 41 AUX2 – SPKOUTN BEEP Mixer Function

ZERO CROSS TIMEOUT

A zero-cross timeout function is also provided so that if zero cross is enabled on the input or output PGAs the gain will automatically update after a timeout period if a zero cross has not occurred. This is enabled by setting SLOWCLKEN. The timeout period is dependent on the clock input to the digital and is equal to 2^{21} * input clock period.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional Control	0	SLOWCLKEN	0	Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout. 0 = slow clock disabled 1 = slow clock enabled

Table 42 Timeout Clock Enable Control

MONOOUT MIXER AND OUTPUT STAGE

The MONOOUT pin can provide an additional line output, or a pseudo ground connection for headphones. There is a dedicated analogue mixer for MONOOUT as shown in Figure 29.

The MONOOUT output stage is powered from SPKVDD and SPKGND. The output also incorporates an optional 1.5x boost and level shifting stage.

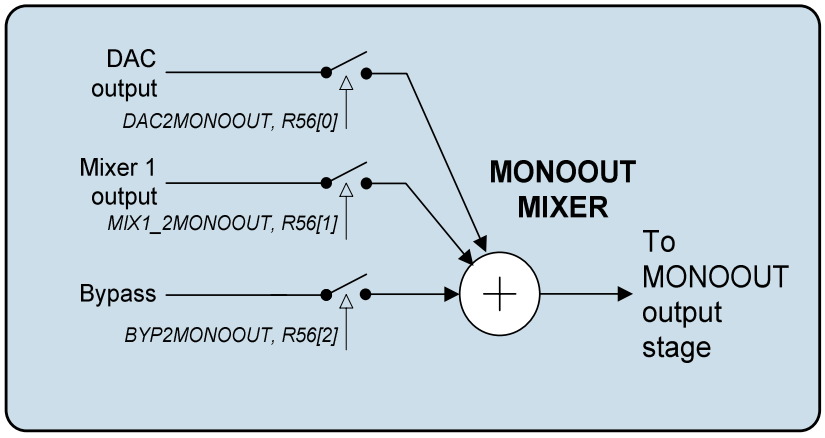


Figure 29 Mono Output Mixer

MONOOUT can provide a buffered midrail headphone pseudo-ground, or a mono line output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 MONOOUT mixer control	6	MONOOUT MUTE	0	0 = Output stage outputs MONOOUT mixer 1 = Output stage muted – drives out VMID. Can be used as VMID buffer in this mode.
	2	BYPL2MONO OUT	0	ADC input to MONOOUT 0 = disabled 1= enabled
	1	MIX1_2MONO OUT	0	Mixer 1 to MONOOUT 0 = disabled 1= enabled
	0	DAC2MONO OUT	1	DAC output to MONOOUT 0 = disabled 1= enabled

Table 43 MONOOUT Mixer Registers

The MONOOUT output stage has a selectable gain boost of 1.5x (3.52dB). When this boost is enabled the output DC level is also level shifted (from AVDD/2 to 1.5xAVDD/2) to prevent the signal from clipping. A dedicated amplifier BUFDCOP, as shown in Figure 30, is used to perform the DC level shift operation. This buffer must be enabled using the BUFDCOPEN register bit for this operating mode. It should also be noted that if SPKVDD is not equal to or greater than 1.5xAVDD this boost mode may result in signals clipping. Table 40 summarises the effect of the MONOBOOST control bit.

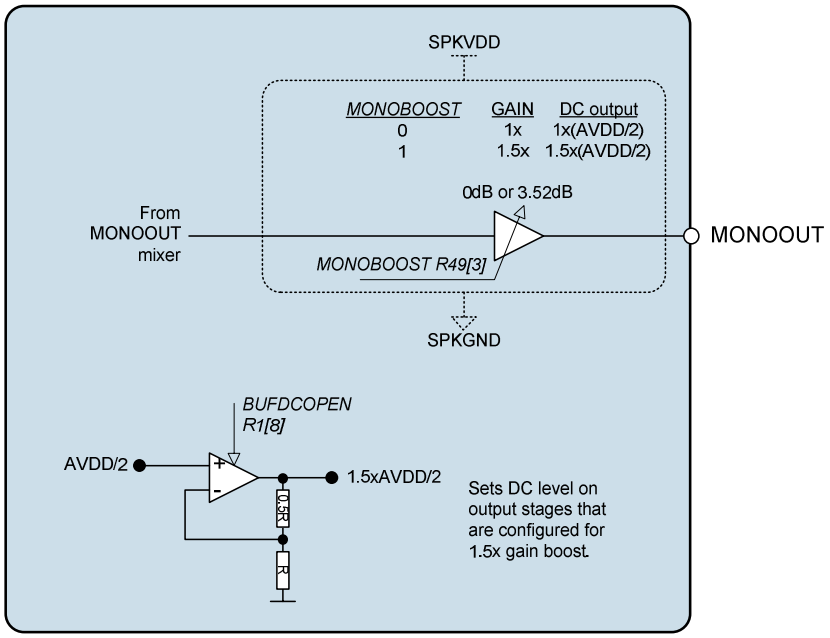


Figure 31 MONOOUT

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 Output control	3	MONOBOOST	0	0 = MONOOUT output gain = -1; DC = AVDD / 2 1 = MONOOUT output gain = +1.5 DC = 1.5 x AVDD / 2
R1 Power management 1	8	BUFDCOPEN	0	Dedicated buffer for DC level shifting output stages when in 1.5x gain boost configuration. 0=Buffer disabled 1=Buffer enabled (required for 1.5x gain boost)

Table 44 MONOOUT Boost Stage Control

MONOBOOST	OUTPUT STAGE GAIN	OUTPUT DC LEVEL	OUTPUT STAGE CONFIGURATION
0	1x	AVDD/2	Inverting
1	1.5x	1.5xAVDD/2	Non-inverting

Table 45 MONOOUT Boost Stage Details

ENABLING THE OUTPUTS

Each analogue output of the WM8982 can be separately enabled or disabled. The analogue mixer associated with each output has a separate enable. All outputs are disabled by default. To save power, unused parts of the WM8982 should remain disabled. The SLEEP bit should only be set on to reduce residual device currents once all the other power management bits have been set to off.

Outputs can be enabled at any time, but it is not recommended to do so when BUFIO is disabled (BUFIOEN=0) or when BUFDCOP is disabled (BUFDCOPEN=0) when configured in output boost mode, as this may cause pop noise (see "Power Management" and "Applications Information" sections).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power Management 1	2	BUFIOEN	0	Unused input/output tie off buffer enable
	6	MONOMIXEN	0	MONOOUT mixer enable
	8	BUFDCOPEN	0	Output stage 1.5xAVDD/2 driver enable
R2 Power Management 2	6	SLEEP	0	0 = normal device operation 1 = residual current reduced in device standby mode if clocks still running
R3 Power Management 3	2	MIX1EN	0	Mixer 1 enable
	3	MIX2EN	0	Mixer 2 enable
	4	VBUFEN	0	Video buffer enable
	5	SPKOUTNEN	0	SPKOUTN output enable
	6	SPKOUTPEN	0	SPKOUTP output enable
	7	MONOOUTEN	0	MONOOUT enable
Note: All "Enable" bits are 1 = ON, 0 = OFF				

Table 46 Output Stages Power Management Control

THERMAL SHUTDOWN

The speaker outputs can drive very large currents. To protect the WM8982 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 125^0C and the thermal shutdown circuit is enabled (TSDEN=1) then the speaker amplifiers will be disabled if TSDEN is set. The thermal shutdown may also be configured to generate an interrupt. See the GPIO and Interrupt Controller section for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 Output control	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled

Table 47 Thermal Shutdown

UNUSED ANALOGUE INPUTS/OUTPUTS

Whenever an analogue input/output is disabled, it remains connected to a voltage source (either AVDD/2 or 1.5xAVDD/2 as appropriate) through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between the voltage buffer and the output pins can be controlled using the VROI control bit. The default impedance is low, so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 30kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49	0	VROI	0	VREF (AVDD/2 or 1.5xAVDD/2) to analogue output resistance 0: approx 1kΩ 1: approx 30 kΩ

Table 48 Disabled Outputs to VREF Resistance

A dedicated buffer is available for tying off unused analogue I/O pins as shown in Figure 32. This buffer can be enabled using the BUFIOEN register bit.

If the SPKRBOOST or MONOBOOST bits are set then the relevant outputs will be tied to the output of the DC level shift buffer at 1.5xAVDD/2 when disabled.

Figure 32 summarises the tie-off options for the speaker and mono output pins.

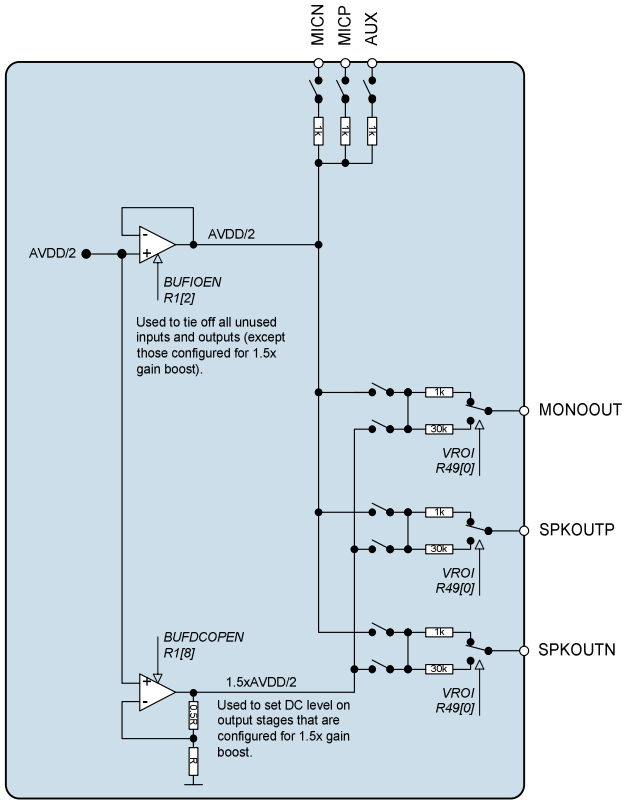


Figure 32 Unused Input/Output Pin Tie-off Buffers

SPKOUTEN/ MONOOUTEN	MONOBOOST/ SPKRBOOST	VROI	OUTPUT CONFIGURATION
0	0	0	1kΩ tie-off to AVDD/2
0	0	1	30kΩ tie-off to AVDD/2
0	1	0	1kΩ tie-off to 1.5xAVDD/2
0	1	1	30kΩ tie-off to 1.5xAVDD/2
1	0	X	Output enabled (DC level=AVDD/2)
1	1	X	Output enabled (DC level=1.5xAVDD/2)

Table 49 Unused Output Pin Tie-off Options

VIDEO BUFFER

DESCRIPTION

The WM8982 incorporates a current mode output video buffer capable of operating from a 2.5V supply, with an input 3rd order Low Pass Filter (LPF) and clamp. The gain through this buffer can be programmed as 0dB or 6dB via the control interface. The current mode output means that the signal swing seen at the output of the buffer will be the same as that at the connection to the receiving equipment (e.g. a TV). Note that the input to the receiver should be AC coupled and terminated to 75Ω, as is standard, for best performance.

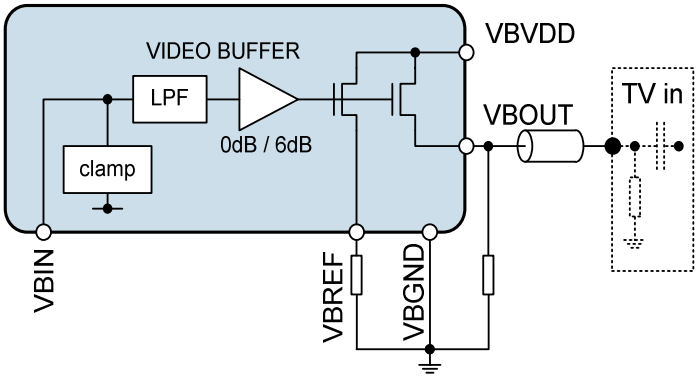


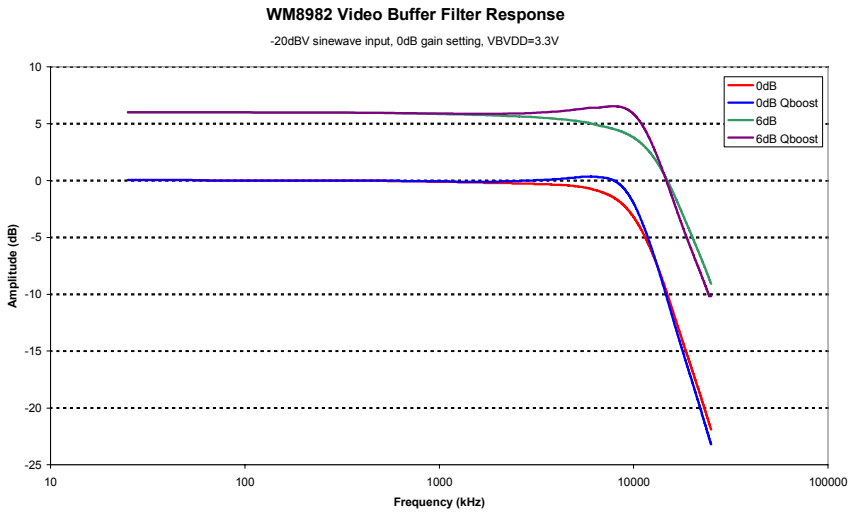
Figure 33 Video Buffer

The input clamp should be enabled when using AC coupling at the input to the video buffer, using the VBCLAMPEN register bit.

Care should be taken with PCB layout, designing for at least 1GHz frequencies to avoid degrading performance. Vias and sharp corners should be avoided and parasitic capacitance minimised on signal paths, which should be kept as short and straight as possible. The VBVDD supply should be decoupled as close to the pin as possible. See the "External Components" section for more information.

LOW PASS FILTER

A low pass filter is integrated at the video buffer input, which is intended to remove images in the video DAC output waveform at multiples of the DAC clock frequency. A 3rd order filter is used, with the following characteristics:



VIDEO BUFFER REGISTERS

Video buffer enable / disable and gain are controlled via the following registers:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 Power management 3	4	VBUFEN	0	Video buffer enable 0 = disabled 1 = enabled
R40 Video Buffer	0	VBGAIN	0	Video buffer gain 0 = 0dB (=6dB unloaded) 1 = +6dB (=12dB unloaded)
	1	VBCLAMPEN	0	Video buffer clamp enable 0 = disabled 1 = enabled
	4	QBOOST	0	Increases the filter's Q.

Table 50 Video Buffer Registers

TEST WAVEFORMS

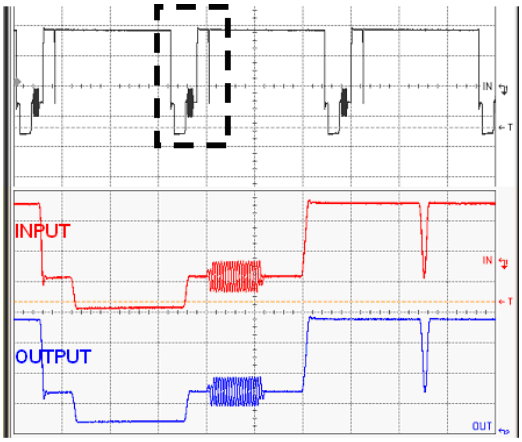


Figure 34 Black Needle Pulse
(Full frame of white with a vertical black line)

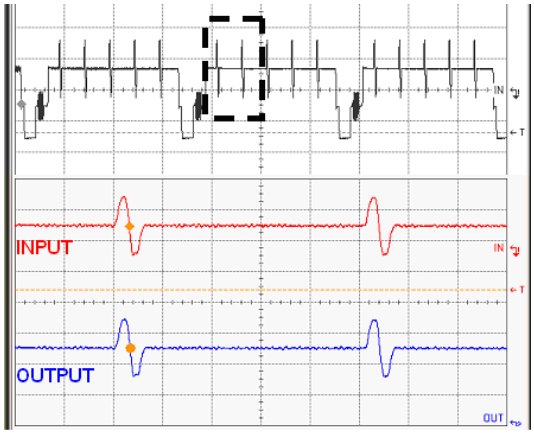


Figure 35 Dual Needle Pulse
(50% grey field with closely-spaced white and black vertical lines spaced across the line scan)

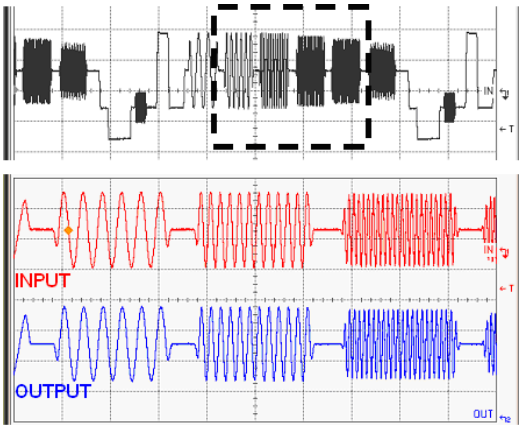


Figure 36 Multiburst
(A horizontal multiburst of signals with frequencies ranging from 0.5MHz to 5.75MHz)

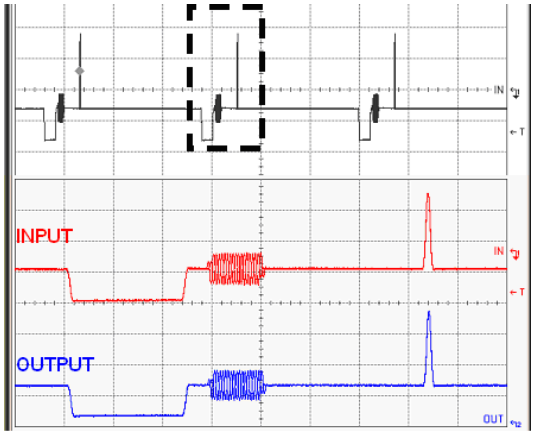


Figure 37 White Needle Pulse
(A full frame of black with a vertical white line)

CURRENT MODE OUTPUT

The current mode output employed by the WM8982 video buffer allows VBVDD to operate at lower voltages than voltage mode video buffers, reducing power consumption, while the use of a current reference resistor close to the WM8982 ensures that the signal swing seen at the output of the buffer will be the same as that at the connection to the receiving equipment (e.g. a TV), providing excellent signal reproduction. Current mode output also provides inherent short circuit protection at the output.

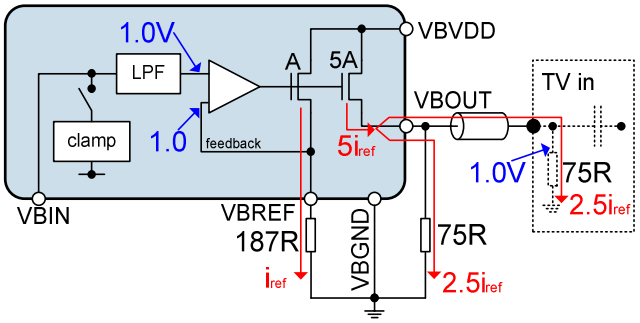


Figure 38 Video Buffer with 0dB Gain

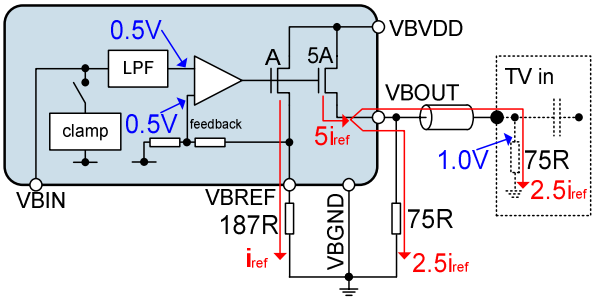


Figure 39 Video Buffer with 6dB Gain

The outputs VBREF and VBOUT are current mirrored transistors with a 5:1 ratio, so that:

$i_{VBOUT} = 5 \times i_{VBREF}$.

A reference resistor (187R in above examples) is used for feedback on the video buffer amplifier via the VBREF pin. The output current from VBOUT will be split between the source termination and load termination (75R each in above examples).

Overall voltage gain (i.e. VBIN to TV input) is calculated as follows:

VBGAIN (R40[1])	LOADED GAIN FORMULA (SOURCE AND LOAD BOTH TERMINATED WITH 75R)	LOADED GAIN (VREF=187R; RSOURCE=75R; RLOAD=75R)	UNLOADED GAIN (VREF=187R; RSOURCE=75R; RLOAD=0)
0	$5 \times (R_{LOAD} \parallel R_{SOURCE}) / R_{VBREF}$	0dB	+6dB
1	$10 \times (R_{LOAD} \parallel R_{SOURCE}) / R_{VBREF}$	+6dB	+12dB

See applications note WAN-0166 for further information.

DIGITAL AUDIO INTERFACES

The audio interface has four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- FRAME: Data Left/Right alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK, and FRAME can be outputs when the WM8982 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Five different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode A
- DSP mode B

All of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8982 audio interface may be configured as either master or slave. As a master interface device the WM8982 generates BCLK and FRAME and thus controls sequencing of the data transfer on ADCDAT and DACDAT. To set the device to master mode register bit MS should be set high. In slave mode (MS=0), the WM8982 responds with data to clocks it receives over the digital audio interfaces.

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an FRAME transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each FRAME transition.

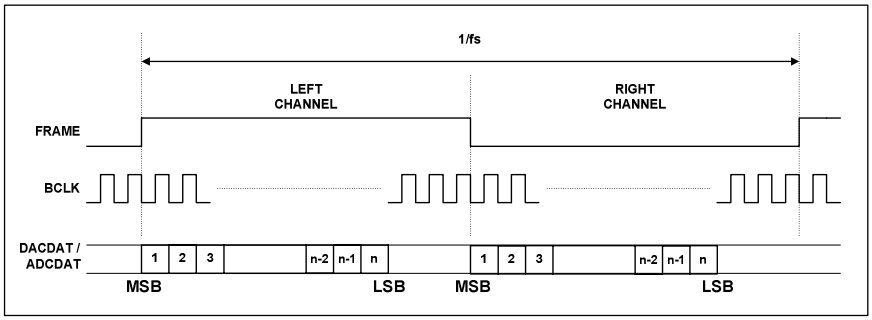


Figure 40 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a FRAME transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each FRAME transition.

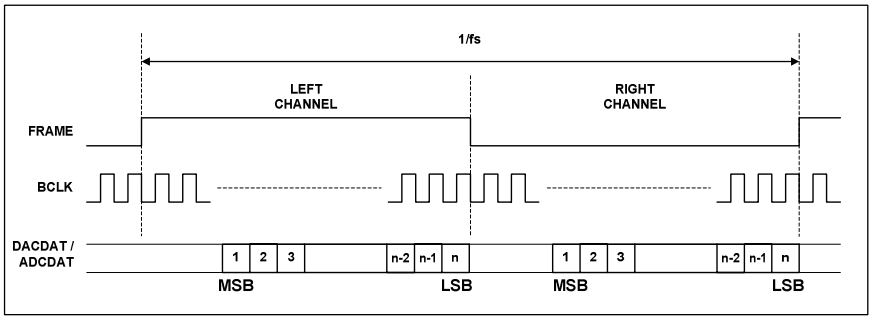


Figure 41 Right Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a FRAME transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

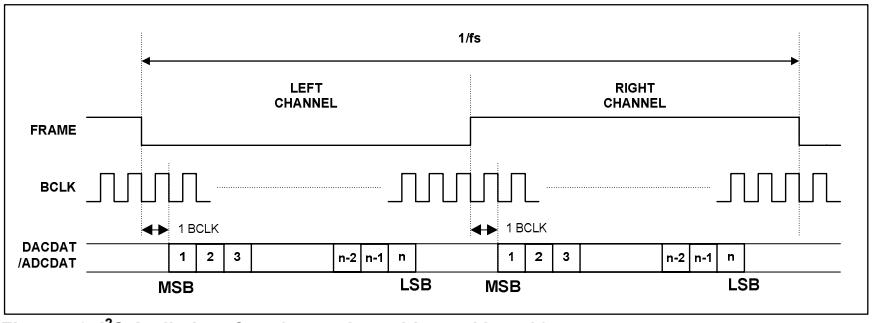


Figure 42 I^2S Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by FRAMEP) following a rising edge of FRAME. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

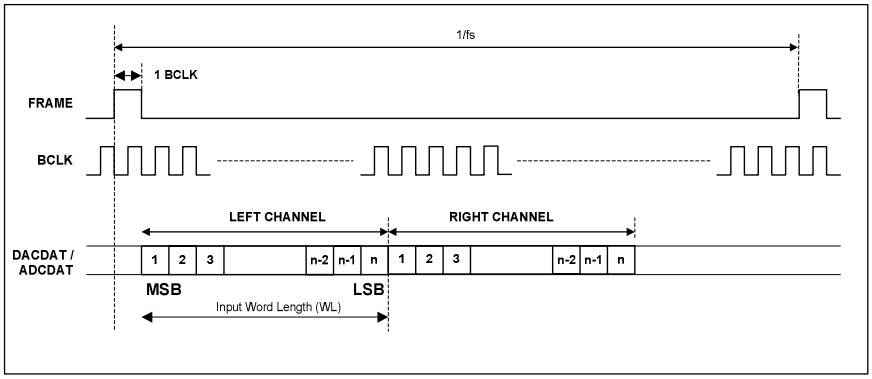


Figure 43 DSP/PCM Mode Audio Interface (mode A, FRAMEP=0)

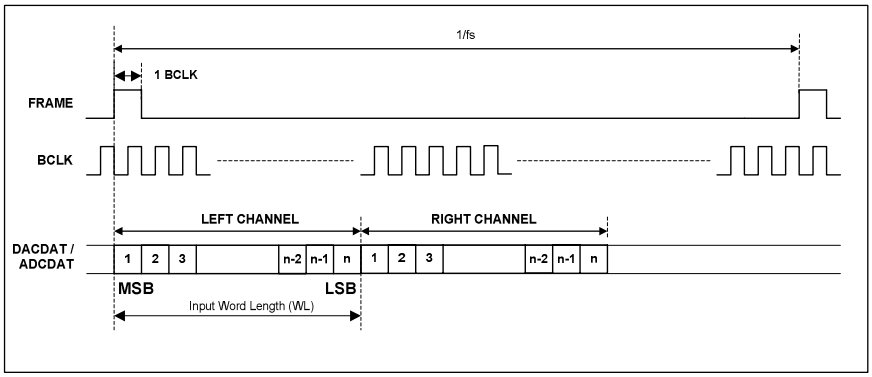


Figure 44 DSP/PCM Mode Audio Interface (mode B, FRAMEP=1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Audio Interface Control	0	MONO	0	Selects between stereo and mono device operation: 0=Stereo device operation 1=Mono device operation. Data appears in 'left' phase of FRAME
	1	ADCLRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of FRAME clock: 0=ADC data appear in 'left' phase of FRAME 1=ADC data appears in 'right' phase of FRAME
	2	DACLRSWAP	0	Controls whether DAC data appears in 'right' or 'left' phases of FRAME clock: 0=DAC data appear in 'left' phase of FRAME 1=DAC data appears in 'right' phase of FRAME
	4:3	FMT	10	Audio interface Data Format Select: 00=Right Justified 01=Left Justified 10=I^2S format 11= DSP/PCM mode
	6:5	WL	10	Word length 00=16 bits 01=20 bits 10=24 bits 11=32 bits (see note)
	7	FRAMEP		right, left and i2s modes – FCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity
				DSP Mode – mode A/B select 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)
	8	BCP		BCLK polarity 0=normal 1=inverted

Table 51 Audio Interface Control

ADCLRSWAP bit controls whether the ADC data appears in the right or left phase of the LRC clock as defined for each audio format. Similarly, DACLRSWAP can be used to swap the left DAC data from the left phase to the right phase of the LRC clock and the right DAC data from the right phase to the left phase of the LRC clock.

Note: Right Justified Mode will only operate with a maximum of 24 bits.

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised below. Each audio interface can be controlled individually.

Register bit MS selects audio interface operation in master or slave mode. In Master mode BCLK, and FRAME are outputs. The frequency of BCLK in master mode are controlled with BCLKDIV. These are divided down versions of master clock.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Clock Generation Control	0	MS	0	Sets the chip to be master over FRAME and BCLK 0=BCLK and FRAME clock are inputs 1=BCLK and FRAME clock are outputs generated by the WM8982 (MASTER)
	4:2	BCLKDIV	000	Configures the BCLK output frequency, for use when the chip is master over BCLK. 000=divide by 1 (BCLK=SYSCLK) 001=divide by 2 (BCLK=SYSCLK) 010=divide by 4 011=divide by 8 100=divide by 16 101=divide by 32 110=reserved 111=reserved
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL) 000=divide by 1 001=divide by 1.5 010=divide by 2 011=divide by 3 100=divide by 4 101=divide by 6 110=divide by 8 111=divide by 12
	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output

Table 52 Clock Control

The CLKSEL bit selects the internal source of the Master clock from the PLL (CLKSEL=1) or from MCLK (CLKSEL=0). When the internal clock is switched from one source to another using the CLKSEL bit, the clock originally selected must generate at least one falling edge after CLKSEL has changed for the switching of clocks to be successful.

EXAMPLE:

If the PLL is the current source of the internal clock (CLKSEL=1) and it is required to switch to the MCLK, change CLKSEL to select MCLK (CLKSEL=0) and then disable PLL (PLLEN=0).

AUDIO SAMPLE RATES

The WM8982 sample rates for the ADC and the DAC are set using the SR register bits. The cutoffs for the digital filters and the ALC attack/decay times stated are determined using these values and assume a 256fs master clock rate.

If a sample rate that is not explicitly supported by the SR register settings is required then the closest SR value to that sample rate should be chosen, the filter characteristics and the ALC attack, decay and hold times will scale appropriately.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional Control	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters): 000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved

Table 53 Sample Rate Control

MASTER CLOCK AND PHASE LOCKED LOOP (PLL)

The WM8982 has an on-chip phase-locked loop (PLL) circuit that can be used to:

Generate master clocks for the WM8982 audio functions from another external clock, e.g. in telecoms applications.

Generate and output (on pin CSB/GPIO1 and/or GPI04) a clock for another part of the system that is derived from an existing audio master clock.

Figure 45 shows the PLL and internal clocking arrangment on the WM8982.

The PLL can be enabled or disabled by the PLLEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	5	PLLEN	0	PLL enable 0=PLL off 1=PLL on

Table 54 PLLEN Control Bit

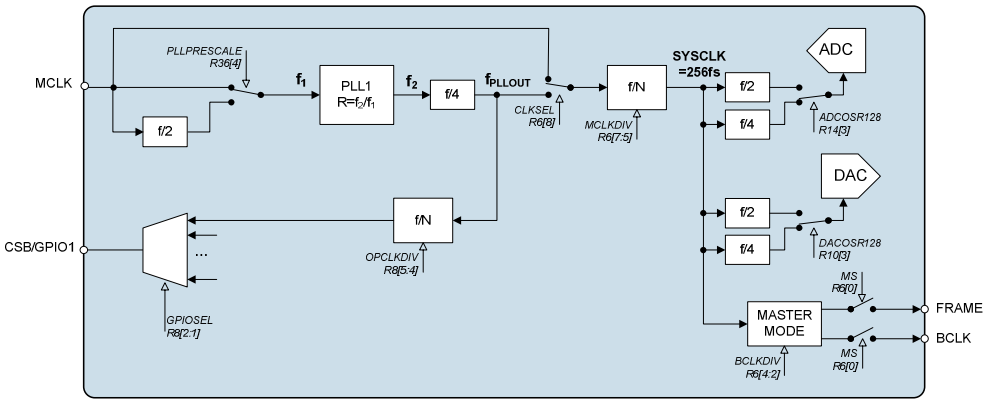


Figure 45 PLL and Clock Select Circuit

The PLL frequency ratio R = f_2/f_1 (see Figure 45) can be set using the register bits PLLK and PLLN:

PLLN = int R

PLLK = int (2^{24} (R-PLLN))

EXAMPLE:

MCLK=12MHz, required clock = 12.288MHz.

R should be chosen to ensure 5 < PLLN < 13. There is a fixed divide by 4 in the PLL and a selectable divide by N after the PLL which should be set to divide by 2 to meet this requirement.

Enabling the divide by 2 sets the required f_2 = 4 x 2 x 12.288MHz = 98.304MHz.

R = 98.304 / 12 = 8.192

PLLN = int R = 8

k = int (2^{24} x (8.192 – 8)) = 3221225 = 3126E9h

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 PLL N value	4	PLLPRESCALE	0	0 = MCLK input not divided (default) 1 = Divide MCLK by 2 before input to PLL
	3:0	PLLN	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.
R37 PLL K value 1	5:0	PLLK [23:18]	0Ch	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).
R38 PLL K Value 2	8:0	PLLK [17:9]	093h	
R39 PLL K Value 3	8:0	PLLK [8:0]	0E9h	

Table 55 PLL Frequency Ratio Control

The PLL performs best when f_2 is around 90MHz. Its stability peaks at N=8. Some example settings are shown in Table 56.

MCLK (MHz) (f1)	DESIRED OUTPUT (SYSCLK) (MHz)	f2 (MHz)	PLLPRESCALE	MCLKDIV	R	N	K	N REGISTER R36[3:0]	K REGISTERS		
									R37	R38	R39
12	11.29	90.3168	1	2	7.5264	7h	86C226h	XX7h	021h	161h	026h
12	12.288	98.304	1	2	8.192	8h	3126E8h	XX8h	00Ch	093h	0E8h
13	11.29	90.3168	1	2	6.947446	6h	F28BD4h	XX6h	03Ch	145h	1D4h
13	12.288	98.304	1	2	7.561846	7h	8FD525h	XX7h	023h	1EAh	125h
14.4	11.29	90.3168	1	2	6.272	6h	45A1CAh	XX6h	011h	0D0h	1CAh
14.4	12.288	98.304	1	2	6.826667	6h	D3A06Eh	XX6h	034h	1D0h	06Eh
19.2	11.29	90.3168	2	2	9.408	9h	6872AFh	XX9h	01Ah	039h	0AFh
19.2	12.288	98.304	2	2	10.24	Ah	3D70A3h	XXAh	00Fh	0B8h	0A3h
19.68	11.29	90.3168	2	2	9.178537	9h	2DB492h	XX9h	00Bh	0DAh	092h
19.68	12.288	98.304	2	2	9.990243	9h	FD809Fh	XX9h	03Fh	0C0h	09Fh
19.8	11.29	90.3168	2	2	9.122909	9h	1F76F7h	XX9h	007h	1BBh	0F7h
19.8	12.288	98.304	2	2	9.929697	9h	EE009Eh	XX9h	03Bh	100h	09Eh
24	11.29	90.3168	2	2	7.5264	7h	86C226h	XX7h	021h	161h	026h
24	12.288	98.304	2	2	8.192	8h	3126E8h	XX8h	00Ch	093h	0E8h
26	11.29	90.3168	2	2	6.947446	6h	F28BD4h	XX6h	03Ch	145h	1D4h
26	12.288	98.304	2	2	7.561846	7h	8FD525h	XX7h	023h	1EAh	125h
27	11.29	90.3168	2	2	6.690133	6h	B0AC93h	XX6h	02Ch	056h	093h
27	12.288	98.304	2	2	7.281778	7h	482296h	XX7h	012h	011h	096h

Table 56 PLL Frequency Examples

LOOPBACK

Setting the LOOPBACK register bit enables digital loopback. When this bit is set the output data from the ADC audio interface is fed directly into the DAC data input.

COMPANDING

The WM8982 supports A-law and μ-law companding and linear mode on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DAC_COMP or ADC_COMP register bits respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Companding Control	0	LOOPBACK	0	Digital loopback function 0=No loopback 1=Loopback enabled, ADC data output is fed directly into DAC data input.
	2:1	ADC_COMP	0	ADC companding 00=off (linear mode) 01=reserved 10=μ-law 11=A-law
	4:3	DAC_COMP	0	DAC companding 00=off (linear mode) 01=reserved 10=μ-law 11=A-law
	5	WL8	0	0=off 1=device operates in 8-bit mode

Table 57 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $-1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ } for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ } for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

Setting the WL8 register bit allows the device to operate with 8-bit data. In this mode it is possible to use 8 BCLK's per FRAME. When using DSP mode B, this allows 8-bit data words to be output consecutively every 8 BCLK's and can be used with 8-bit data words using the A-law and u-law companding functions.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 58 8-bit Companded Word Composition

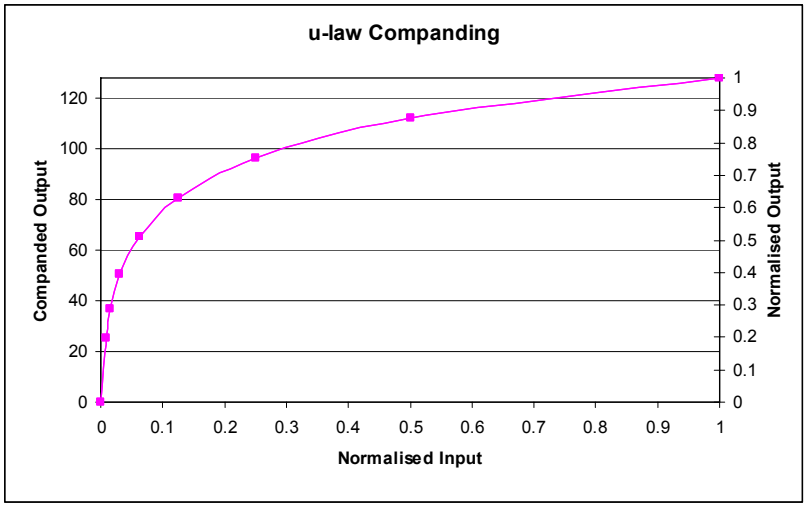


Figure 46 u-Law Companding

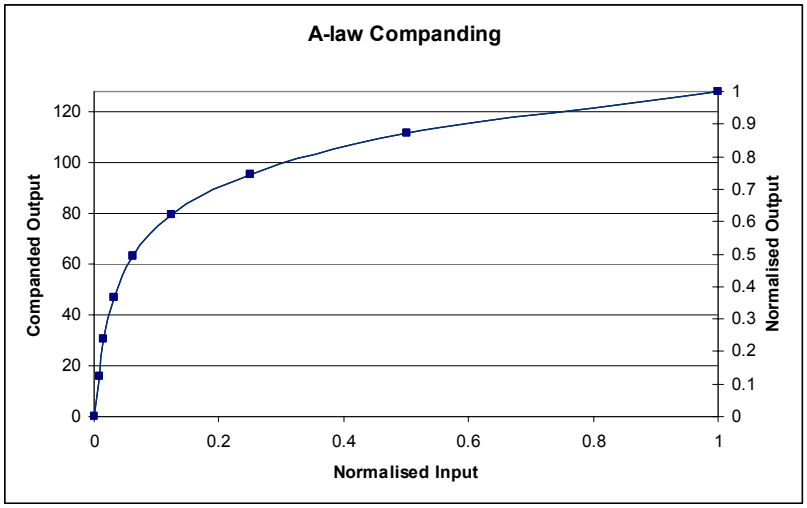


Figure 47 A-Law Companding

GENERAL PURPOSE INPUT/OUTPUT

The WM8982 has two dual purpose input/output pins and one dedicated GPIO.

- CSB/GPIO1: CSB / GPIO pin
- LINEIN/JDET: Line input / headphone detection input
- GPIO2: Dedicated GPIO

The JDET function is provided for use as a jack detection input.

The GPIO1 and GPIO2 functions are provided for use as jack detection inputs or general purpose outputs.

The default configuration for the CSB/GPIO1 and GPIO2 pins are to be inputs.

When setup as an input, the CSB/GPIO1 pin can either be used as CSB or for jack detection, depending on how the MODE pin is set.

If setup as an input the GPIO2 pin can also be used for jack detection.

Table 49 illustrates the functionality of the GPIO1 and GPIO2 pins when used as general purpose outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 GPIO Control	2:0	GPIO1SEL	000	CSB/GPIO1 pin function select: 000= input (CSB/jack detection: depending on MODE setting) 001= reserved 010=Temp ok 011=Amute active 100=PLL clk o/p 101=PLL lock 110=logic 0 111=logic 1
	3	GPIO1POL	0	GPIO1 Polarity invert 0=Non inverted 1=Inverted
	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4
R9 GPIO Control	2:0	GPIO2SEL	000	GPIO2 pin function select: 000= input jack detection 001= reserved 010=Temp ok 011=Amute active 100=PLL clk o/p 101=PLL lock 110=logic 0 111=logic 1
	3	GPIO2POL	0	GPIO2 Polarity invert 0=Non inverted 1=Inverted

Table 59 CSB/GPIO Control

Note: If MODE is set to 3 wire mode, CSB/GPIO1 shall be used as CSB input irrespective of the GPIO1SEL[2:] bits.

Note that SLOWCLKEN must be enabled when using the Jack Detect function.

For further details of the Jack detect operation see the OUTPUT SWITCHING section.

OUTPUT SWITCHING (JACK DETECT)

When the device is operated using a 2-wire interface the CSB/GPIO1 pin can be used as a switch control input to automatically disable one set of outputs and enable another the most common use for this functionality is as jack detect circuitry. The GPIO2 pin can also be used for this purpose.

The GPIO pins have an internal de-bounce circuit when in this mode in order to prevent the output enables from toggling multiple times due to input glitches. This de-bounce circuit is clocked from a slow clock with period 2^{21} x MCLK and is enabled by the SLOWCLKEN bit.

Notes:

The SLOWCLKEN bit must be enabled for the jack detect circuitry to operate.

The GPIOPOL bit is not relevant for jack detection, it is the signal detected at the pin which is used

Switching on/off of the outputs is fully configurable by the user. Each output, OUT1, OUT2, OUT3 and OUT4 has 2 associated enables. OUT1_EN_0, OUT2_EN_0, OUT3_EN_0 and OUT4_EN_0 are the output enable signals which are used if the selected jack detection pin is at logic 0 (after de-bounce). OUT1_EN_1, OUT2_EN_1, OUT3_EN_1 and OUT4_EN_1 are the output enable signals which are used if the selected jack detection pin is at logic 1 (after de-bounce).

The jack detection enables operate as follows:

All OUT_EN signals have an AND function performed with their normal enable signals (in Table 46). When an output is normally enabled at per Table 46 the selected jack detection enable (controlled by selected jack detection pin polarity) is set 0; it will turn the output off. If the normal enable signal is already OFF (0), the jack detection signal will have no effect due to the AND function.

During jack detection if the user desires an output to be un-changed whether the jack is in or not, both the JD_EN settings i.e. JD_EN0 and JD_EN1, should be set to 0000.

The VMID_EN signal has an OR function performed with the normal VMID driver enable. If the VMID_EN signal is to have no effect to normal functionality when jack detection is enabled, it should set to 0 for all JD_EN0 or JD_EN1 settings.

If jack detection is not enabled (JD_EN=0), the output enables default to all 1's, allowing the outputs to be controlled as normal via the normal output enables found in Table 47.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 GPIO control	5:4	JD_SEL	00	Pin selected as jack detection input 00 = GPIO1 01 = GPIO2 10 = Reserved 11 = Reserved
	6	JD_EN	0	Jack Detection Enable 0 = disabled 1 = enabled
	8:7	JD_VMID	00	[7] VMID_EN_0 [8] VMID_EN_1
R13	3:0	JD_EN0	0000	Output enables when selected jack detection input is logic 0. [0]= OUT1_EN_0 [1]= OUT2_EN_0 [2]= OUT3_EN_0 [3]= OUT4_EN_0
	7:4	JD_EN1	0000	Output enables when selected jack detection input is logic 1 0000-0011 = Reserved [4]= OUT1_EN_1 [5]= OUT2_EN_1 [6]= OUT3_EN_1 [7]= OUT4_EN_1

Table 60 Jack Detect Register Control Bits

CONTROL INTERFACE

SELECTION OF CONTROL MODE AND 2-WIRE MODE ADDRESS

The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE pin determines the 2 or 3 wire mode as shown in Table 61.

The WM8982 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are register bits, corresponding to the 9 bits in each control register.

MODE	INTERFACE FORMAT
Low	2 wire
High	3 wire

Table 61 Control Interface Mode Selection

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/GPIO1 pin latches in a complete control word consisting of the last 16 bits.

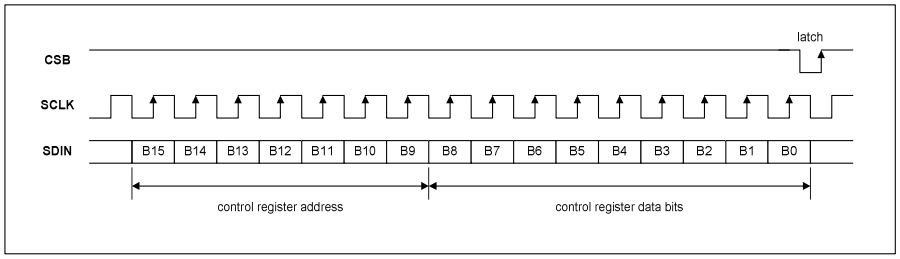


Figure 48 3-Wire Serial Control Interface

2-WIRE SERIAL CONTROL MODE

The WM8982 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit device address (this is not the same as the 7-bit address of each register in the WM8982).

The WM8982 operates as a slave 2-wire device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8982, then the WM8982 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8982 returns to the idle condition and wait for a new start condition and valid address.

During a write, once the WM8982 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8982 register address plus the first bit of register data). The WM8982 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8982 acknowledges again by pulling SDIN low.

Transfers are complete when there is a low to high transition on SDIN while SCLK is high. After a complete sequence the WM8982 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

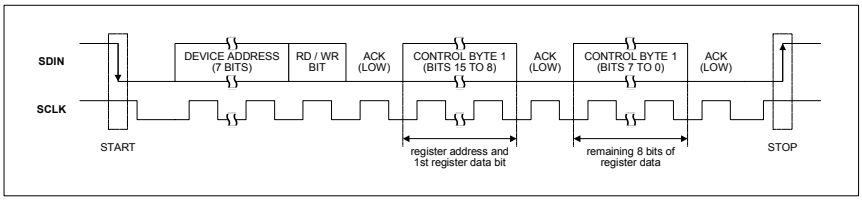


Figure 49 2-Wire Serial Control Interface

In 2-wire mode the WM8982 has a fixed device address, 0011010.

RESETTING THE CHIP

The WM8982 can be reset by performing a write of any value to the software reset register (address 0h). This will cause all register values to be reset to their default values. In addition to this there is a Power-On Reset (POR) circuit which ensures that the registers are set to default when the device is powered up.

POWER SUPPLIES

The WM8982 can use up to five separate power supplies:

AVDD and AGND: Analogue supply, powers all analogue functions except the speaker output and mono output drivers. AVDD can range from 2.5V to 3.6V and has the most significant impact on overall power consumption. A large AVDD slightly improves audio quality.

SPKVDD and SPKGND: Speaker supplies, power the speaker and mono output drivers. SPKVDD can range from 2.5V to 5V. SPKVDD can be tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. With a larger SPKVDD, louder speaker outputs can be achieved with lower distortion. If SPKVDD is lower than AVDD, the output signal may be clipped.

DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD can range from 1.71V to 3.6V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD. When using the PLL, DCVDD should be 1.9V or higher.

DBVDD can range from 1.71V to 3.6V. DBVDD return path is through DGND.

VBVDD and VBGND: Supplies for video buffer circuit. VBVDD can range from 2.5V to 3.6V.

It is possible to use the same supply voltage for all four supplies. However, digital and analogue supplies should be routed and decoupled separately on the PCB to keep digital switching noise out of the analogue signal paths.

DCVDD should be greater than or equal to 1.9V when using the PLL.

RECOMMENDED POWER UP/DOWN SEQUENCE

In order to minimise output pop and click noise, it is recommended that the WM8982 device is powered up and down using one of the following sequences:

Power-up when NOT using the output 1.5x boost stage:

1. Turn on external power supplies. Wait for supply voltage to settle.
2. Mute all analogue outputs.
3. Set MIX1EN = 1, MIX2EN = 1 and DACENL/R = 1 in register R3.
4. Set BUFIOEN = 1 and VMIDSEL[1:0] to required value in register R1. Wait for the VMID supply to settle. *Refer notes 1 and 2.
5. Set BIASEN = 1 in register R1.
6. Set MONOOUTEN = 1 and SPKOUTP/NEN = 1 in register R3.
7. Enable other mixers as required.
8. Enable other outputs as required.
9. Set remaining registers.

Power-up when using the output 1.5x boost stage:

1. Turn on external power supplies. Wait for supply voltage to settle.
2. Mute all analogue outputs.
3. Set BUFDCOPEN = 1 and BUFIOEN = 1 in register R1.
4. Set SPKBOOST = 1 in register R49.
5. Set VMIDSEL[1:0] to required value in register R1. Wait for the VMID supply to settle. *Refer notes 1 and 2.
6. Set MIX1EN = 1, MIX2EN = 1 and DACENL/R = 1 in register R3.
7. Set BIASEN = 1 in register R1.
8. Set SPKOUTEN = 1 and SPKOUTNEN = 1 in register R3. *Note 3.
9. Enable other mixers as required.
10. Enable other outputs as required.
11. Set remaining registers.

Power Down (all cases):

1. Mute all analogue outputs.
2. Disable Power Management Register 1. R1 = 0x00.
3. Disable Power Management Register 2. R2 = 0x00.
4. Disable Power Management Register 3. R3 = 0x00.
5. Remove external power supplies.

Notes:

This step enables the internal device bias buffer and the VMID buffer for unassigned inputs/outputs. This will provide a startup reference voltage for all inputs and outputs. This will cause the inputs and outputs to ramp towards VMID (NOT using output 1.5x boost) or 1.5 x (AVDD/2) (using output 1.5x boost) in a way that is controlled and predictable (see note 2).

Choose the value of the VMIDSEL bits based on the startup time (VMIDSEL=10 for slowest startup, VMIDSEL=11 for fastest startup). Startup time is defined by the value of the VMIDSEL bits (the reference impedance) and the external decoupling capacitor on VMID.

Setting DACEN to off while operating in x1.5 boost mode will cause the VMID voltage to drop to AVDD/2 midrail level and cause an output pop.

In addition to the power on sequence, it is recommended that the zero cross functions are used when changing the volume in the PGAs to avoid any audible pops or clicks.

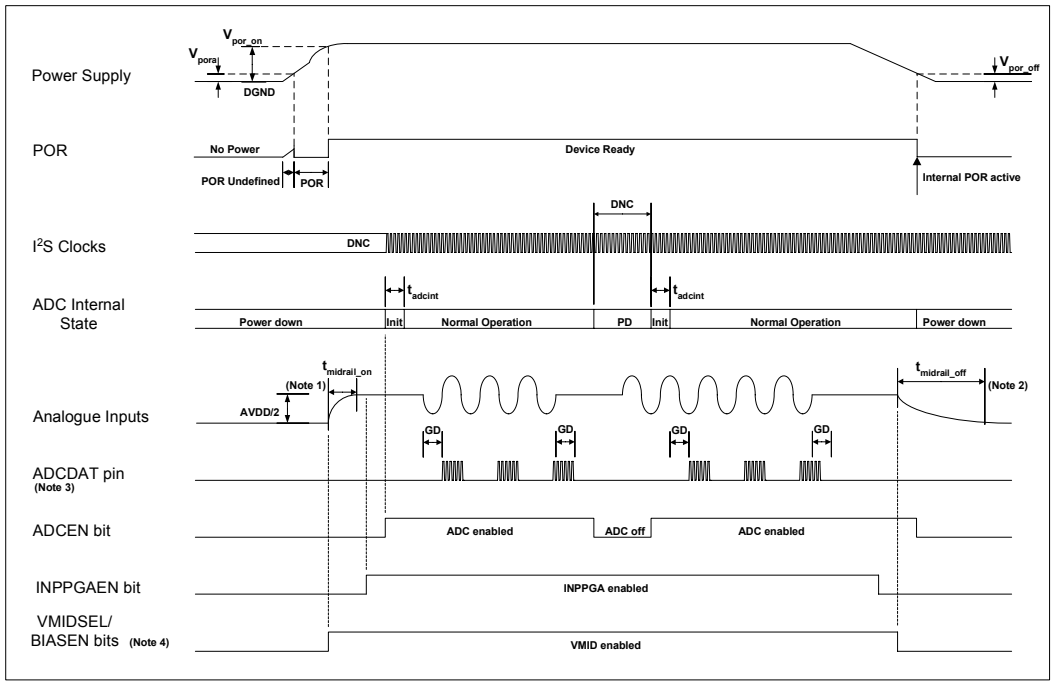


Figure 50 ADC Power Up and Down Sequence (not to scale)

SYMBOL	MIN	TYPICAL	MAX	UNIT
$t_{midrail\_on}$		500		ms
$t_{midrail\_off}$		>10		s
t_{adcint}		2/fs		*n*/fs
ADC Group Delay		29/fs		*n*/fs

Table 62 Typical POR Operation (simulated values)

Notes:

The analogue input pin charge time, $t_{midrail\_on,}$ is determined by the VMID pin charge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time.

The analogue input pin discharge time, $t_{midrail\_off,}$ is determined by the analogue input coupling capacitor discharge time. The time, $t_{midrail\_off}$, is measured using a 1µF capacitor on the analogue input but will vary dependent upon the value of input coupling capacitor.

While the ADC is enabled there will be LSB data bit activity on the ADCDAT pin due to system noise but no significant digital output will be present.

The VMIDSEL and BIASEN bits must be set to enable analogue input midrail voltage and for normal ADC operation.

ADCDAT data output delay from power up - with power supplies starting from 0V - is determined primarily by the VMID charge time. ADC initialisation and power management bits may be set immediately after POR is released; VMID charge time will be significantly longer and will dictate when the device is stabilised for analogue input.

ADCDAT data output delay at power up from device standby (power supplies already applied) is determined by ADC initialisation time, 2/fs.

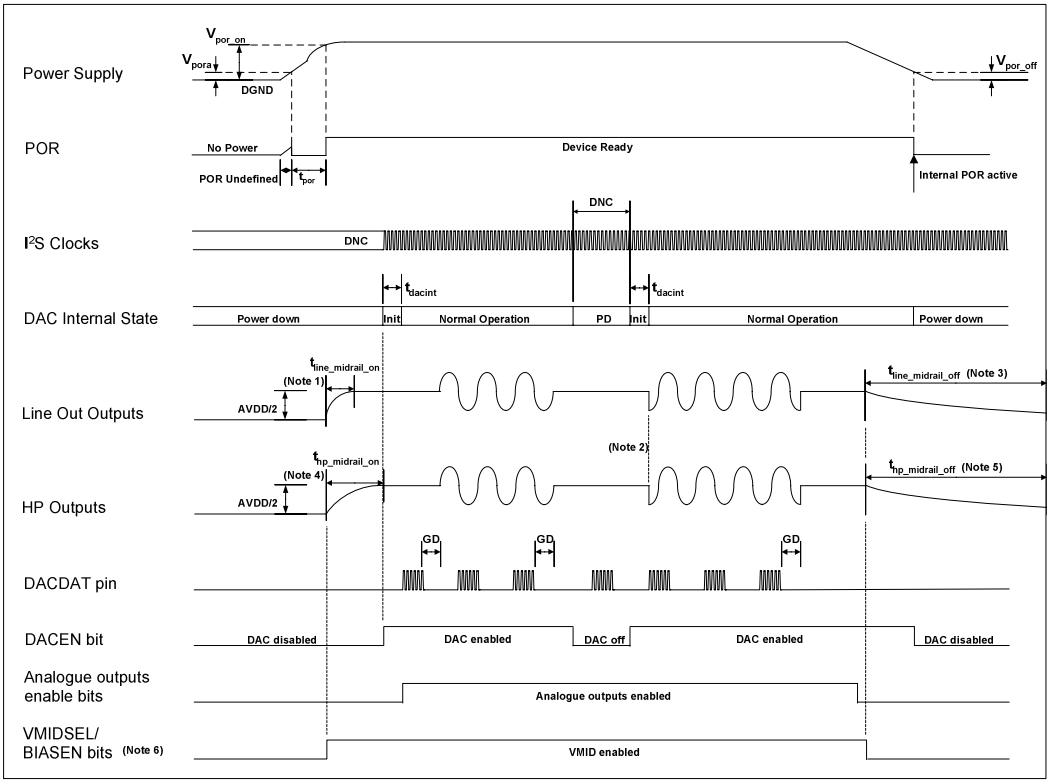


Figure 51 DAC Power Up and Down Sequence (not to scale)

SYMBOL	MIN	TYPICAL	MAX	UNIT
$t_{line\_midrail\_on}$		500		ms
$t_{line\_midrail\_off}$		>1		s
$t_{hp\_midrail\_on}$		500		ms
$t_{hp\_\_midrail\_off}$		>6		s
t_{dacint}		2/fs		*n*/fs
DAC Group Delay		29/fs		*n*/fs

Table 63 Typical POR Operation (simulated values)

Notes:

The lineout charge time, $t_{line\_midrail\_on,}$ is mainly determined by the VMID pin charge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time. The values above were measured using a 4.7µF capacitor.

It is not advisable to allow DACDAT data input during initialisation of the DAC. If the DAC data value is not zero at point of initialisation, then this is likely to cause a pop noise on the analogue outputs. The same is also true if the DACDAT is removed at a non-zero value, and no mute function has been applied to the signal beforehand.

The lineout discharge time, $t_{line\_midrail\_off,}$ is dependent upon the value of the lineout coupling capacitor and the leakage resistance path to ground. The values above were measured using a 10µF output capacitor.

The headphone charge time, $t_{hp\_midrail\_on,}$ is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time. The values above were measured using a 4.7µF VMID decoupling capacitor.

The headphone discharge time, $t_{hp\_midrail\_off,}$ is dependent upon the value of the headphone coupling capacitor and the leakage resistance path to ground. The values above were measured using a 100µF capacitor.

The VMIDSEL and BIASEN bits must be set to enable analogue output midrail voltage and for normal DAC operation.

POWER MANAGEMENT

SAVING POWER BY REDUCING OVERSAMPLING RATE

The default mode of operation of the ADC and DAC digital filters is in 64x oversampling mode. Under the control of ADCOSR and DACOSR the oversampling rate may be doubled. 64x oversampling results in a slight decrease in noise performance compared to 128x but lowers the power consumption of the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 DAC control	3	DACOSR128	0	DAC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)
R14 ADC control	3	ADCOSR128	0	ADC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)

Table 64 ADC and DAC Oversampling Rate Selection

VMID

The analogue will not work unless VMID is enabled (VMIDSEL≠00). The impedance of the VMID resistor string, together with the decoupling capacitor on the VMID pin will determine the startup time of the VMID circuit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	1:0	VMIDSEL	00	Reference string impedance to VMID pin (detemines startup time): 00=off (open circuit) 01=75kΩ 10=300kΩ 11=5kΩ (for fastest startup)

Table 65 VMID Impedance Control

BIASEN

The analogue amplifiers will not operate unless BIASEN is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	3	BIASEN	0	Analogue amplifier bias control 0=disabled 1=enabled

Table 66 Analogue Bias Control

ESTIMATED SUPPLY CURRENTS

When either the DAC or ADC are enabled approximately 7mA will be drawn from DCVDD when DCVDD=1.8V and fs=48kHz (This will be lower at lower sample rates). When the PLL is enabled approximately 1.5mA additional current will be drawn from DCVDD. The video buffer will draw about 4mA with no load attached, in normal operating up to 30 mA will be drawn.

Table 67 shows the estimated 3.3V AVDD current drawn by various circuits, by register bit.

REGISTER BIT	AVDD CURRENT (MILLIAMPS)
BUFDCOPEN	0.1
MONOMIXEN	0.2
PLLEN	1.4 (with clocks applied)
MICBEN	0.5
BIASEN	0.3
BUFIOEN	0.1
VMIDSEL	5KΩ=>0.3, less than 0.1 for 75kΩ/300Ωk settings
BOOSTEN	0.2
INPPGAEN	0.2
ADCEN	x64 (ADCOSR=0)=>2.6, x128 (ADCOSR=1)=>4.9
MONOOUTEN	0.2
SPKOUTPEN	1mA from SPKVDD + 0.2mA from AVDD in 5V mode
SPKOUTNEN	1mA from SPKVDD + 0.2mA from AVDD in 5V mode
MIX2EN	0.2
MIX1EN	0.2
DACEN	x64 (DACOSR=0)=>1.8, x128(DACOSR=1)=>1.9

Table 67 AVDD Supply Current

REGISTER MAP

ADDR B[15:9] DEC	ADDR B[15:9] HEX	REGISTER NAME	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEF'T VAL (HEX)
0	00	Software Reset	Software reset									
1	01	Power manage't 1	BUFDCOPEN	0	MONOMIXEN	PLLEN	MICBEN	BIASEN	BUFIOEN	VMIDSEL		000
2	02	Power manage't 2	0	0	SLEEP	0	BOOSTEN	0	INPPGAEN	0	ADCEN	000
3	03	Power manage't 3	0	MONOOUTEN	SPKOUTPEN	SPKOUTNEN	VBUFEN	MIX2EN	MIX1EN	0	DACEN	000
4	04	Audio Interface	BCP	FRAMEP	WL		FMT		DAC LRSWAP	ADC LRSWAP	MONO	050
5	05	Companding ctrl	0	0	0	WL8	DAC_COMP		ADC_COMP		LOOPBACK	000
6	06	Clock Gen ctrl	CLKSEL	MCLKDIV			BCLKDIV			0	MS	140
7	07	Additional ctrl	0	0	0	0	0	SR			SLOWCLKEN	000
8	08	GPIO	0	0	0	OPCLKDIV		GPIO1POL	GPIO1SEL[2:0]			000
9	09	Jack detect control	JD_VMID		JD_EN	JD_SEL		GPIO2POL	GPIO2SEL[2:0]			000
10	0A	DAC Control	0	0	SOFTMUTE	0	0	DACOSR128	AMUTE	0	DACPOL	000
11	0B	DAC digital Vol	DACVU	DACVOL								0FF
13	0D	Jack Detect Control		JD_EN1				JD_EN0				000
14	0E	ADC Control	HPFEN	HPFAPP	HPFCUT			ADCOSR128	0	0	ADCPOL	100
15	0F	ADC Digital Vol	ADCVU	ADCVOL								0FF
18	12	EQ1 – low shelf	EQMODE	0	EQ1C		EQ1G					12C
19	13	EQ2 – peak 1	EQ2BW	0	EQ2C		EQ2G					02C
20	14	EQ3 – peak 2	EQ3BW	0	EQ3C		EQ3G					02C
21	15	EQ4 – peak 3	EQ4BW	0	EQ4C		EQ4G					02C
22	16	EQ5 – high shelf	0	0	EQ5C		EQ5G					02C
24	18	DAC Limiter 1	LIMEN	LIMDCY				LIMATK				032
25	19	DAC Limiter 2	0	0	LIMLVL			LIMBOOST				000
27	1B	Notch Filter 1	NFU	NFEN	NFA0[13:7]							000
28	1C	Notch Filter 2	NFU	0	NFA0[6:0]							000
29	1D	Notch Filter 3	NFU	0	NFA1[13:7]							000
30	1E	Notch Filter 4	NFU	0	NFA1[6:0]							000
32	20	ALC control 1	ALCSEL	0	0	ALCMAXGAIN		ALCMINGAIN				038
33	21	ALC control 2	0	ALCHLD				ALCLVL				00B
34	22	ALC control 3	ALCMODE	ALCDCY				ALCATK				032
35	23	Noise Gate	0	0	0	0	0	NGEN	NGTH			000
36	24	PLL N	0	0	0	0	PLL_PRESCALE	PLLN[3:0]				008
37	25	PLL K 1	0	0	0	PLLK[23:18]						00C
38	26	PLL K 2	PLLK[17:9]									093
39	27	PLL K 3	PLLK[8:0]									0E9
40	28	Video Buffer	0	0	0	0	0	0	0	VBGAIN	VBCLAMPEN	000
43	2B	Beep control	0	0	0	MUTE PGA2INV	INVOUTN	BEEPVOL			BEEPEN	000

ADDR B[15:9]		REGISTER NAME	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEF'T VAL
DEC	HEX											(HEX)
44	2C	Input ctrl	MBVSEL	0	0	0	0	0	LINE2 INPPGA	MICN2 INPPGA	MICP2 INPPGA	033
45	2D	INP PGA gain ctrl	INPGA UPDATE	INPPGAZC	INPPGA MUTE	INPPGAVOL						010
47	2F	ADC Boost ctrl	PGABOOST	0	LINE2BOOSTVOL			0	AUX1_2BOOSTVOL			100
49	31	Output ctrl	0	0	DAC2 MIX2	0	0	MONO BOOST	SPKR BOOST	TSDEN	VROI	002
50	32	Output mixer 1 ctrl	AUX1MIXVOL			AUX1_2 MIX1	BYPVOL			BYP2MIX1	DAC2MIX1	001
51	33	Output mixer 2 ctrl	AUX2MIXVOL			AUX2_2 MIX2	0	0	0	0	1	001
54	36	SPKOUTP volume ctrl	UPDATE	SPKOUTP ZC	SPKOUTP MUTE	SPKOUTPVOL						039
55	37	SPKOUTN volume ctrl	UPDATE	SPKOUTN ZC	SPKOUTN MUTE	SPKOUTNVOL						039
56	38	MONOOUT mixer ctrl	0	0	MONOOUT MUTE	0	0	0	BYPL2 MONOOUT	MIX1_2 MONOOUT	DAC2 MONOOUT	001

Table 68 WM8982 Register Map

REGISTER BITS BY ADDRESS

Notes:

1. Default values of N/A indicate non-latched data bits (e.g. software reset or volume update bits).

2. Register bits marked as "Reserved" should not be changed from the default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
0 (00h)	[8:0]	RESET	N/A	Software reset	Resetting the Chip
1 (01h)	8	BUFDCOPEN	0	Dedicated buffer for DC level shifting output stages when in 1.5x gain boost configuration. 0=Buffer disabled 1=Buffer enabled (required for 1.5x gain boost)	Analogue Outputs
	7	OUT4MIXEN	0	OUT4 mixer enable 0=disabled 1=enabled	Power Management
	6	OUT3MIXEN	0	OUT3 mixer enable 0=disabled 1=enabled	Power Management
	5	PLLEN	0	PLL enable 0=PLL off 1=PLL on	Master Clock and Phase Locked Loop (PLL)
	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON	Input Signal Path
	3	BIASEN	0	Analogue amplifier bias control 0=disabled 1=enabled	Power Management
	2	BUFIOEN	0	Unused input/output tie off buffer enable 0=disabled 1=enabled	Power Management
	1:0	VMIDSEL	00	Reference string impedance to VMID pin 00=off (open circuit) 01=75kΩ 10=300kΩ 11=5kΩ	Power Management
2 (02h)	8	ROUT1EN	0	ROUT1 output enable 0=disabled 1=enabled	Power Management
	7	LOUT1EN	0	LOUT1 output enable 0=disabled 1=enabled	Power Management
	6	SLEEP	0	0 = normal device operation 1 = residual current reduced in device standby mode	Power Management
	5		0	Reserved	
	4	BOOSTENL	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON	Power Management
	3		0	Reserved	
	2	INPPGAENL	0	Input PGA enable 0 = disabled 1 = enabled	Power Management
	1		0	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	ADCENL	0	Enable ADC: 0 = ADC disabled 1 = ADC enabled	Analogue to Digital Converter (ADC)
3 (03h)	8	OUT4EN	0	OUT4 enable 0 = disabled 1 = enabled	Power Management
	7	OUT3EN	0	OUT3 enable 0 = disabled 1 = enabled	Power Management
	6	LOUT2EN	0	LOUT2 enable 0 = disabled 1 = enabled	Power Management
	5	ROUT2EN	0	ROUT2 enable 0 = disabled 1 = enabled	Power Management
	3	RMIXEN	0	Right output channel mixer enable: 0 = disabled 1 = enabled	Analogue Outputs
	2	LMIXEN	0	Left output channel mixer enable: 0 = disabled 1 = enabled	Analogue Outputs
	1	DACENR	0	Right channel DAC enable 0 = DAC disabled 1 = DAC enabled	Analogue Outputs
	0	DACENL	0	Left channel DAC enable 0 = DAC disabled 1 = DAC enabled	Analogue Outputs
4 (04h)	8	BCP	0	BCLK polarity 0=normal 1=inverted	Digital Audio Interfaces
	7	FRAMEP	0	right, left and i2s modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity DSP Mode – mode A/B select 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)	Digital Audio Interfaces
	6:5	WL	10	Word length 00=16 bits 01=20 bits 10=24 bits 11=32 bits	Digital Audio Interfaces
	4:3	FMT	10	Audio interface Data Format Select: 00=Right Justified 01=Left Justified 10=I^2S format 11= DSP/PCM mode	Digital Audio Interfaces
	2	DACLRSWAP	0	Controls whether DAC data appears in 'right' or 'left' phases of LRC clock: 0=DAC data appear in 'left' phase of LRC 1=DAC data appears in 'right' phase of LRC	Digital Audio Interfaces

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	ADCLRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of LRC clock: 0=ADC data appear in 'left' phase of LRC 1=ADC data appears in 'right' phase of LRC	Digital Audio Interfaces
	0	DACMONO	0	Selects between stereo and mono DAC operation: 0=Stereo device operation 1=Mono device operation. DAC data appears in 'left' phase of LRC	Digital Audio Interfaces
5 (05h)	8:6		000	Reserved	
	5	WL8	0	Companding Control 8-bit mode 0=off 1=device operates in 8-bit mode	Digital Audio Interfaces
	4:3	DAC_COMP	00	DAC companding 00=off (linear mode) 01=reserved 10=μ-law 11=A-law	Digital Audio Interfaces
	2:1	ADC_COMP	00	ADC companding 00=off (linear mode) 01=reserved 10=μ-law 11=A-law	Digital Audio Interfaces
	0	LOOPBACK	0	Digital loopback function 0=No loopback 1=Loopback enabled, ADC data output is fed directly into DAC data input.	Digital Audio Interfaces
6 (06h)	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output	Digital Audio Interfaces
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL) 000=divide by 1 001=divide by 1.5 010=divide by 2 011=divide by 3 100=divide by 4 101=divide by 6 110=divide by 8 111=divide by 12	Digital Audio Interfaces
	4:2	BCLKDIV	000	Configures the BCLK output frequency, for use when the chip is master over BCLK. 000=divide by 1 (BCLK=MCLK) 001=divide by 2 (BCLK=MCLK/2) 010=divide by 4 011=divide by 8 100=divide by 16 101=divide by 32 110=reserved 111=reserved	Digital Audio Interfaces
	1		0	Reserved	
	0	MS	0	Sets the chip to be master over LRC and BCLK 0=BCLK and LRC clock are inputs 1=BCLK and LRC clock are outputs generated by the WM8976 (MASTER)	Digital Audio Interfaces

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
7 (07h)	8:4		00000	Reserved	
	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters): 000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved	Audio Sample Rates
	0	SLOWCLKEN	0	Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout. 0 = slow clock disabled 1 = slow clock enabled	Analogue Outputs
8 (08h)	8:6		000	Reserved	
	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4	General Purpose Input/Output (GPIO)
	3	GPIO1POL	0	GPIO1 Polarity invert 0=Non inverted 1=Inverted	General Purpose Input/Output (GPIO)
	2:0	GPIO1SEL [2:0]	000	CSB/GPIO1 pin function select: 000= input (CSB/jack detection: depending on MODE setting) 001= reserved 010=Temp ok 011=Amute active 100=PLL clk o/p 101=PLL lock 110=logic 1 111=logic 0	General Purpose Input/Output (GPIO)
9 (09h)	8:7	JD_VMID	00	[7] VMID_EN_0 [8] VMID_EN_1	Output Switching (Jack Detect)
	6	JD_EN	0	Jack Detection Enable 0=disabled 1=enabled	Output Switching (Jack Detect)
	5		0	Reserved	
	4	JD_SEL	0	Pin selected as jack detection input 0 = GPIO1 1 = GPIO2	Output Switching (Jack Detect)
	3:0		0	Reserved	
10 (0Ah)	8:7		00	Reserved	
	6	SOFTMUTE	0	Softmute enable: 0=Disabled 1=Enabled	Output Signal Path
	5:4		00	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	DACOSR128	0	DAC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)	Power Management
	2	AMUTE	0	Automute enable 0 = Amute disabled 1 = Amute enabled	Output Signal Path
	1	DACPOLR	0	Right DAC output polarity: 0 = non-inverted 1 = inverted (180 degrees phase shift)	Output Signal Path
	0	DACPOLL	0	Left DAC output polarity: 0 = non-inverted 1 = inverted (180 degrees phase shift)	Output Signal Path
11 (0Bh)	8	DACVU	N/A	DAC left and DAC right volume do not update until a 1 is written to DACVU (in reg 11 or 12)	Digital to Analogue Converter (DAC)
	7:0	DACVOLL	11111111	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Digital to Analogue Converter (DAC)
12 (0Ch)	8	DACVU	N/A	DAC left and DAC right volume do not update until a 1 is written to DACVU (in reg 11 or 12)	Output Signal Path
	7:0	DACVOLR	11111111	Right DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path
13 (0Dh)	8		0	Reserved	
	7:4	JD_EN1	0000	Output enabled when selected jack detection input is logic 1 [4]= OUT1_EN_1 [5]= OUT2_EN_1 [6]= OUT3_EN_1 [7]= OUT4_EN_1	Output Switching (Jack Detect)
	3:0	JD_EN0	0000	Output enabled when selected jack detection input is logic 0. [0]= OUT1_EN_0 [1]= OUT2_EN_0 [2]= OUT3_EN_0 [3]= OUT4_EN_0	Output Switching (Jack Detect)
14 (0Eh)	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled	Analogue to Digital Converter (ADC)
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1st order, fc = ~3.7Hz) 1=Application mode (2nd order, fc = HPFCUT)	Analogue to Digital Converter (ADC)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 14 for details.	Analogue to Digital Converter (ADC)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	ADCOSR 128	0	ADC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)	Power Management
	2:1		00	Reserved	
	0	ADCLPOL	0	ADC polarity adjust: 0=normal 1=inverted	Analogue to Digital Converter (ADC)
15 (0Fh)	8	ADCVU	N/A	ADC volume does not update until a 1 is written to ADCVU	Analogue to Digital Converter (ADC)
	7:0	ADCVOLL	11111111	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Analogue to Digital Converter (ADC)
16 (10h)	8:0		11111111	Reserved	
18 (12h)	8	EQ3DMODE	1	0 = Equaliser and 3D Enhancement applied to ADC path 1 = Equaliser and 3D Enhancement applied to DAC path	Output Signal Path
	7		0	Reserved	
	6:5	EQ1C		EQ Band 1 Cut-off Frequency: 00=80Hz 01=105Hz 10=135Hz 11=175Hz	Output Signal Path
	4:0	EQ1G	01100	EQ Band 1 Gain Control. See Table 36 for details.	Output Signal Path
19 (13h)	8	EQ2BW	0	EQ Band 2 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth	Output Signal Path
	7		0	Reserved	
	6:5	EQ2C	01	EQ Band 2 Centre Frequency: 00=230Hz 01=300Hz 10=385Hz 11=500Hz	Output Signal Path
	4:0	EQ2G	01100	EQ Band 2 Gain Control. See Table 36 for details.	Output Signal Path
20 (14h)	8	EQ3BW	0	EQ Band 3 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth	Output Signal Path
	7		0	Reserved	
	6:5	EQ3C	01	EQ Band 3 Centre Frequency: 00=650Hz 01=850Hz 10=1.1kHz 11=1.4kHz	Output Signal Path
	4:0	EQ3G	01100	EQ Band 3 Gain Control. See Table 36 for details.	Output Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
21 (15h)	8	EQ4BW	0	EQ Band 4 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth	Output Signal Path
	7		0	Reserved	
	6:5	EQ4C	01	EQ Band 4 Centre Frequency: 00=1.8kHz 01=2.4kHz 10=3.2kHz 11=4.1kHz	Output Signal Path
	4:0	EQ4G	01100	EQ Band 4 Gain Control. See Table 36 for details.	Output Signal Path
22 (16h)	8:7		00	Reserved	
	6:5	EQ5C	01	EQ Band 5 Cut-off Frequency: 00=5.3kHz 01=6.9kHz 10=9kHz 11=11.7kHz	Output Signal Path
	4:0	EQ5G	01100	EQ Band 5 Gain Control. See Table 36 for details.	Output Signal Path
24 (18h)	8	LIMEN	0	Enable the DAC digital limiter: 0=disabled 1=enabled	Output Signal Path
	7:4	LIMDCY	0011	DAC Limiter Decay time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate: 0000=750us 0001=1.5ms 0010=3ms 0011=6ms 0100=12ms 0101=24ms 0110=48ms 0111=96ms 1000=192ms 1001=384ms 1010=768ms	Output Signal Path
	3:0	LIMATK	0010	DAC Limiter Attack time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate. 0000=94us 0001=188s 0010=375us 0011=750us 0100=1.5ms 0101=3ms 0110=6ms 0111=12ms 1000=24ms 1001=48ms 1010=96ms 1011 to 1111=192ms	Output Signal Path
25 (19h)	8:7		00	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	LIMLVL	000	Programmable signal threshold level (determines level at which the DAC limiter starts to operate) 000=-1dB 001=-2dB 010=-3dB 011=-4dB 100=-5dB 101 to 111=-6dB	Output Signal Path
	3:0	LIMBOOST	0000	DAC Limiter volume boost (can be used as a stand alone volume boost when LIMEN=0): 0000=0dB 0001=+1dB 0010=+2dB … (1dB steps) 1011=+11dB 1100=+12dB 1101 to 1111=reserved	Output Signal Path
27 (1Bh)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7	NFEN	0	Notch filter enable: 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	6:0	NFA0[13:7]	0000000	Notch Filter a0 coefficient, bits [13:7]	Analogue to Digital Converter (ADC)
28 (1Ch)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7		0	Reserved	
	6:0	NFA0[6:0]	0000000	Notch Filter a0 coefficient, bits [6:0]	Analogue to Digital Converter (ADC)
29 (1Dh)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7		0	Reserved	
	6:0	NFA1[13:7]	0000000	Notch Filter a1 coefficient, bits [13:7]	Analogue to Digital Converter (ADC)
30 (1Eh)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7		0	Reserved	
	6:0	NFA1[6:0]	0000000	Notch Filter a1 coefficient, bits [6:0]	Analogue to Digital Converter (ADC)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
32 (20h)	8	ALCSEL	0	ALC function select: 0=ALC off 1=ALC on	Input Limiter/ Automatic Level Control (ALC)
	7:6		00	Reserved	
	5:3	ALCMAXGAIN	111	Set Maximum Gain of PGA 111=+35.25dB 110=+29.25dB 101=+23.25dB 100=+17.25dB 011=+11.25dB 010=+5.25dB 001=-0.75dB 000=-6.75dB	Input Limiter/ Automatic Level Control (ALC)
	2:0	ALCMINGAIN	000	Set minimum gain of PGA 000=-12dB 001=-6dB 010=0dB 011=+6dB 100=+12dB 101=+18dB 110=+24dB 111=+30dB	Input Limiter/ Automatic Level Control (ALC)
33 (21h)f	8		0	Reserved	
	7:4	ALCHLD	0000	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1010 or higher = 1.36s	Input Limiter/ Automatic Level Control (ALC)
	3:0	ALCLVL	1011	ALC target – sets signal level at ADC input 1111 : -1.5dBFS 1110 : -1.5dBFS 1101 : -3dBFS 1100 : -4.5dBFS ..... (-1.5dB steps) 0001 : -21dBFS 0000 : -22.5dBFS	Input Limiter/ Automatic Level Control (ALC)
34 (22h)	8	ALCMODE	0	Determines the ALC mode of operation: 0=ALC mode 1=Limiter mode	Input Limiter/ Automatic Level Control (ALC)
	7:4	ALCDCY [3:0]	0011	Decay (gain ramp-up) time (ALCMODE ==0)	Input Limiter/ Automatic Level Control (ALC)

	Per step	Per 6dB	90% of range
0000	410us	3.28ms	23.6ms
0001	820us	6.56ms	47.2ms
0010	1.64ms	13.1ms	94.5ms
… (time doubles with every step)			
1010 or higher	420ms	3.36s	24.2s

			0011	Decay (gain ramp-up) time (ALCMODE ==1)	

	Per step	Per 6dB	90% of range

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION				REFER TO
				0000	90.8us	726us	5.23ms	
				0001	182us	1.45ms	10.5ms	
				0010	363us	2.91ms	20.9ms	
				… (time doubles with every step)				
				1010	93ms	744ms	5.36s	
	3:0	ALCATK	0010	ALC attack (gain ramp-down) time (ALCMODE == 0)				Input Limiter/ Automatic Level Control (ALC)
					Per step	Per 6dB	90% of range	
				0000	104us	832us	6ms	
				0001	208us	1.66ms	12ms	
				0010	416us	3.33ms	24ms	
				… (time doubles with every step)				
				1010 or higher	106ms	852ms	6.13s	
			0010	ALC attack (gain ramp-down) time (ALCMODE == 1)				
					Per step	Per 6dB	90% of range	
				0000	22.7us	182us	1.31ms	
				0001	45.4us	363us	2.62ms	
				0010	90.8us	726us	5.26ms	
				… (time doubles with every step)				
				1010	23.2ms	186ms	1.34s	
35 (23h)	8:4		00000	Reserved				
	3	NGEN	0	ALC Noise gate function enable 1 = enable 0 = disable				Input Limiter/ Automatic Level Control (ALC)
	2:0	NGTH	000	ALC Noise gate threshold: 000=-39dB 001=-45dB 010=-51db … (6dB steps) 111=-81dB				Input Limiter/ Automatic Level Control (ALC)
36 (24h)	8:5		0000	Reserved				
	4	PLL PRESCALE	0	0 = MCLK input not divided (default) 1 = Divide MCLK by 2 before input to PLL				Master Clock and Phase Locked Loop (PLL)
	3:0	PLLN[3:0]	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.				Master Clock and Phase Locked Loop (PLL)
37 (25h)	8:6		000	Reserved				
	5:0	PLLK[23:18]	01100	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).				Master Clock and Phase Locked Loop (PLL)
38 (26h)	8:0	PLLK[17:9]	010010011	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).				Master Clock and Phase Locked Loop (PLL)
39 (27h)	8:0	PLLK[8:0]	011101001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).				Master Clock and Phase Locked Loop (PLL)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
40 (28h)	8:0		000000000	Reserved	
41 (29h)	8:4		00000	Reserved	
	3:0	DEPTH3D	0000	Stereo depth 0000: 0% (minimum 3D effect) 0001: 6.67% .... 1110: 93.3% 1111: 100% (maximum 3D effect)	3D Stereo Enhancement
43 (2Bh)	8:6		000	Reserved	
	5	MUTERPGA2INV	0	Mute input to INVROUT2 mixer	Analogue Outputs
	4	INVROUT2	0	Mute input to INVROUT2 mixer	Analogue Outputs
	3:1	BEEPVOL	000	AUXR input to ROUT2 inverter gain 000 = -15dB ... 111 = +6dB	Analogue Outputs
	0	BEEPEN	0	0 = mute AUXR beep input 1 = enable AUXR beep input	Analogue Outputs
44 (2Ch)	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.6 * AVDD	Input Signal Path
	7:3		00000	Reserved	
	2	L2_2INPPGA	0	Connect L2 pin to input PGA positive terminal. 0=L2 not connected to input PGA 1=L2 connected to input PGA amplifier positive terminal (constant input impedance).	Input Signal Path
	1	LIN2INPPGA	1	Connect LIN pin to input PGA negative terminal. 0=LIN not connected to input PGA 1=LIN connected to input PGA amplifier negative terminal.	Input Signal Path
	0	LIP2INPPGA	1	Connect LIP pin to input PGA amplifier positive terminal. 0 = LIP not connected to input PGA 1 = input PGA amplifier positive terminal connected to LIP (constant input impedance)	Input Signal Path
45 (2Dh)	8	INPPGAUPDATE	N/A	INPPGAVOLL and INPPGAVOLR volume do not update until a 1 is written to INPPGAUPDATE (in reg 45 or 46)	Input Signal Path
	7	INPPGAZCL	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1st zero cross after gain register write.	Input Signal Path
	6	INPPGAMUTEL	0	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).	Input Signal Path
	5:0	INPPGAVOLL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB	Input Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
46 (2Eh)	8:0		000010000	Reserved	
47 (2Fh)	8	PGA BOOSTL	1	Boost enable for input PGA: 0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.	Input Signal Path
	7		0	Reserved	
	6:4	L2_2 BOOSTVOL	000	Controls the L2 pin to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage	Input Signal Path
	3		0	Reserved	
	2:0	AUXL2 BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage	Input Signal Path
48 (30h)	8:0		100000000	Reserved	
49 (31h)	8:7		00	Reserved	
	6	DACL2RMIX	0	Left DAC output to right output mixer 0 = not selected 1 = selected	Analogue Outputs
	5	DACR2LMIX	0	Right DAC output to left output mixer 0 = not selected 1 = selected	Analogue Outputs
	4	OUT4 BOOST	0	0 = OUT4 output gain = -1; DC = AVDD / 2 1 = OUT4 output gain = +1.5 DC = 1.5 x AVDD / 2	Analogue Outputs
	3	OUT3 BOOST	0	0 = OUT3 output gain = -1; DC = AVDD / 2 1 = OUT3 output gain = +1.5 DC = 1.5 x AVDD / 2	Analogue Outputs
	2	SPKBOOST	0	0 = speaker gain = -1; DC = AVDD / 2 1 = speaker gain = +1.5; DC = 1.5 x AVDD / 2	Analogue Outputs
	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled	Analogue Outputs
	0	VROI	0	VREF (AVDD/2 or 1.5xAVDD/2) to analogue output resistance 0: approx 1kΩ 1: approx 30 kΩ	Analogue Outputs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
50 (32h)	8:6	AUXLMIX VOL	000	Aux left channel input to left mixer volume control: 000 = -15dB 001 = -12dB … 101 = 0dB 110 = +3dB 111 = +6dB	Analogue Outputs
	5	AUXL2L MIX	0	Left Auxiliary input to left channel output mixer: 0 = not selected 1 = selected	Analogue Outputs
	4:2	BYPLMIX VOL	000	Bypass volume contol to left output channel mixer: 000 = -15dB 001 = -12dB … 101 = 0dB 110 = +3dB 111 = +6dB	Analogue Outputs
	1	BYPL2L MIX	0	Bypass path (from the input boost output) to left output mixer 0 = not selected 1 = selected	Analogue Outputs
	0	DACL2L MIX	1	Left DAC output to left output mixer 0 = not selected 1 = selected	Analogue Outputs
51 (33h)	8:6	AUXRMIX VOL	000	Aux right channel input to right mixer volume control: 000 = -15dB 001 = -12dB … 101 = 0dB 110 = +3dB 111 = +6dB	Analogue Outputs
	5	AUXR2R MIX	0	Right Auxiliary input to right channel output mixer: 0 = not selected 1 = selected	Analogue Outputs
	4:1		0000	Reserved	
	0	DACR2R MIX	1	Right DAC output to right output mixer 0 = not selected 1 = selected	Analogue Outputs
52 (34h)	8	HPVU	N/A	LOUT1 and ROUT1 volumes do not update until a 1 is written to HPVU (in reg 52 or 53)	Analogue Outputs
	7	LOUT1ZC	0	Headphone volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6	LOUT1 MUTE	0	Left headphone output mute: 0 = Normal operation 1 = Mute	Analogue Outputs
	5:0	LOUT1VOL	111001	Left headphone output volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	Analogue Outputs
53 (35h)	8	HPVU	N/A	LOUT1 and ROUT1 volumes do not update until a 1 is written to HPVU (in reg 52 or 53)	Analogue Outputs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7	ROUT1ZC	0	Headphone volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6	ROUT1 MUTE	0	Right headphone output mute: 0 = Normal operation 1 = Mute	Analogue Outputs
	5:0	ROUT1VOL	111001	Right headphone output volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	Analogue Outputs
54 (36h)	8	SPKVU	N/A	LOUT2 and ROUT2 volumes do not update until a 1 is written to SPKVU (in reg 54 or 55)	Analogue Outputs
	7	LOUT2ZC	0	Speaker volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6	LOUT2 MUTE	0	Left speaker output mute: 0 = Normal operation 1 = Mute	Analogue Outputs
	5:0	LOUT2VOL	111001	Left speaker output volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	Analogue Outputs
55 (37h)	8	SPKVU	N/A	LOUT2 and ROUT2 volumes do not update until a 1 is written to SPKVU (in reg 54 or 55)	Analogue Outputs
	7	ROUT2ZC	0	Speaker volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6	ROUT2 MUTE	0	Right speaker output mute: 0 = Normal operation 1 = Mute	Analogue Outputs
	5:0	ROUT2VOL	111001	Right speaker output volume: 000000 = -57dB ... 111001 = 0dB ... 111111 = +6dB	Analogue Outputs
56 (38h)	8:7		00	Reserved	
	6	OUT3MUTE	0	0 = Output stage outputs OUT3 mixer 1 = Output stage muted – drives out VMID. Can be used as VMID buffer in this mode.	Analogue Outputs
	5:4		00	Reserved	
	3	OUT4_2OUT3	0	OUT4 mixer output to OUT3 0 = disabled 1= enabled	Analogue Outputs
	2	BYPL2OUT3	0	ADC input to OUT3 0 = disabled 1= enabled	Analogue Outputs
	1	LMIX2OUT3	0	Left DAC mixer to OUT3 0 = disabled 1= enabled	Analogue Outputs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	LDAC2OUT3	1	Left DAC output to OUT3 0 = disabled 1= enabled	Analogue Outputs
57 (39h)	8:7		00	Reserved	
	6	OUT4MUTE	0	0 = Output stage outputs OUT4 mixer 1 = Output stage muted – drives out VMID. Can be used as VMID buffer in this mode.	Analogue Outputs
	5	HALFSIG	0	0=OUT4 normal output 1=OUT4 attenuated by 6dB	Analogue Outputs
	4	LMIX2OUT4	0	Left DAC mixer to OUT4 0 = disabled 1= enabled	Analogue Outputs
	3	LDAC2OUT4	0	Left DAC to OUT4 0 = disabled 1= enabled	Analogue Outputs
	2		0	Reserved	
	1	RMIX2OUT4	0	Right DAC mixer to OUT4 0 = disabled 1= enabled	Analogue Outputs
	0	RDAC2OUT4	1	Right DAC output to OUT4 0 = disabled 1= enabled	Analogue Outputs

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.025	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-60			dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter					
Passband	+/- 0.035dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.035	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-55			dB
Group Delay			29/fs		

Table 69 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES

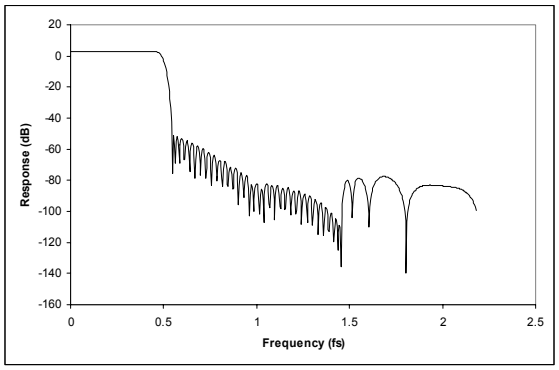


Figure 52 DAC Digital Filter Frequency Response (128xOSR)

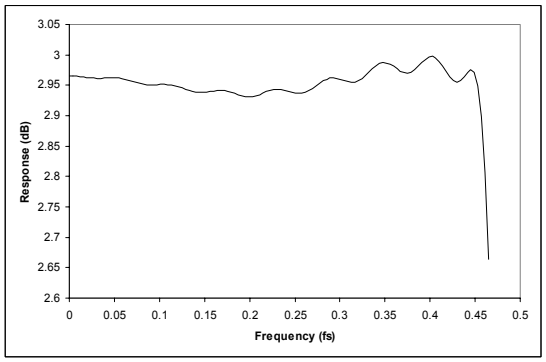


Figure 53 DAC Digital Filter Ripple (128xOSR)

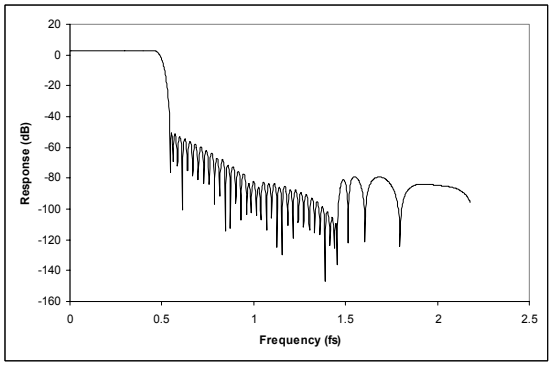


Figure 54 DAC Digital Filter Frequency Response (64xOSR)

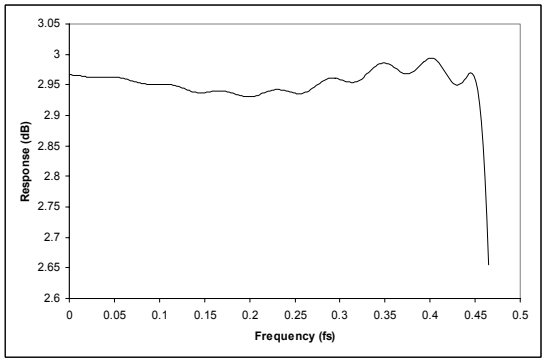


Figure 55 DAC Digital Filter Ripple (64xOSR)

ADC FILTER RESPONSES

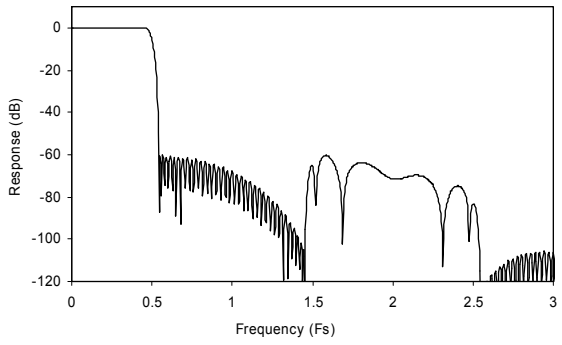


Figure 56 ADC Digital Filter Frequency Response

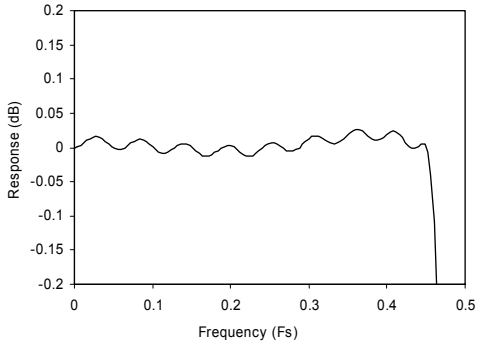


Figure 57 ADC Digital Filter Ripple

HIGHPASS FILTER

The WM8982 has a selectable digital highpass filter in the ADC filter path. This filter has two modes, audio and applications. In audio mode the filter is a 1st order IIR with a cut-off of around 3.7Hz. In applications mode the filter is a 2nd order high pass filter with a selectable cut-off frequency.

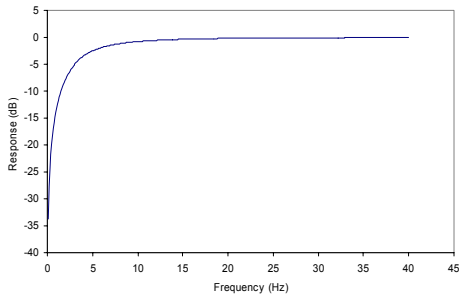


Figure 58 ADC Highpass Filter Response, HPFAPP=0

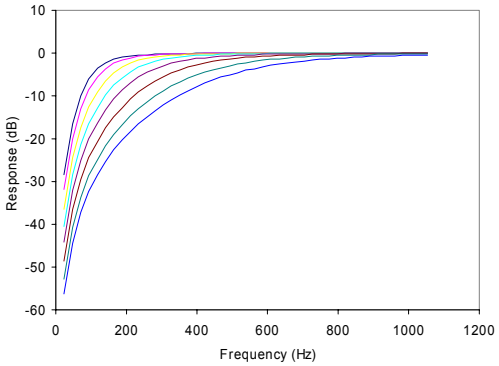


Figure 59 ADC Highpass Filter Responses (48kHz), HPFAPP=1, all cut-off settings shown.

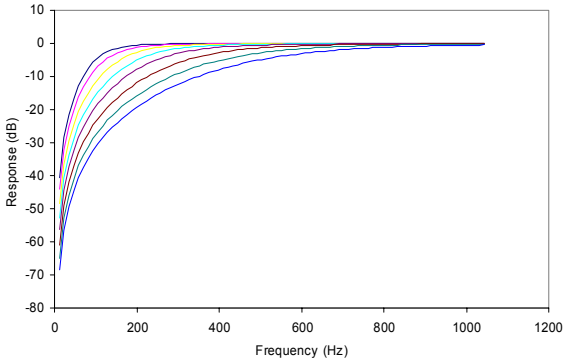


Figure 60 ADC Highpass Filter Responses (24kHz), HPFAPP=1, all cut-off settings shown.

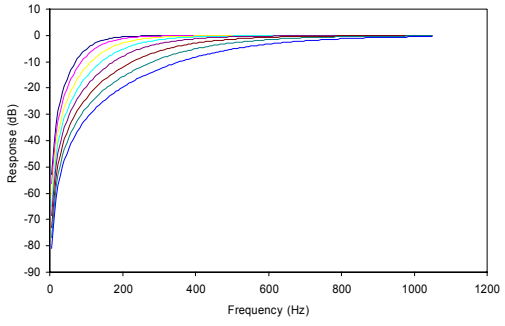


Figure 61 ADC Highpass Filter Responses (12kHz), HPFAPP=1, all cut-off settings shown.

5-BAND EQUALISER

The WM8982 has a 5-band equaliser which can be applied to either the ADC path or the DAC path. The plots from Figure 62 to Figure 75 show the frequency responses of each filter with a sampling frequency of 48kHz, firstly showing the different cut-off/centre frequencies with a gain of ±12dB, and secondly a sweep of the gain from -12dB to +12dB for the lowest cut-off/centre frequency of each filter.

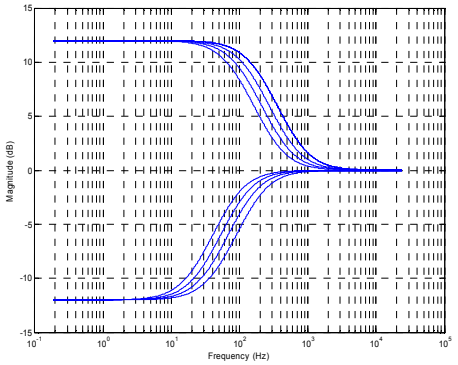


Figure 62 EQ Band 1 Low Frequency Shelf Filter Cut-offs

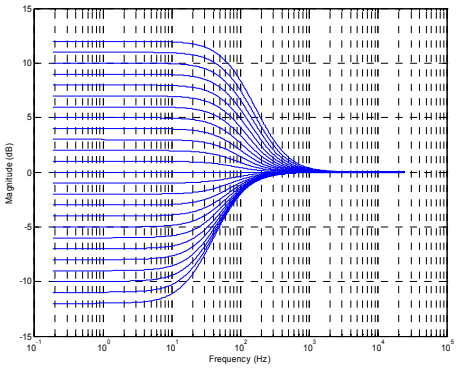


Figure 63 EQ Band 1 Gains for Lowest Cut-off Frequency

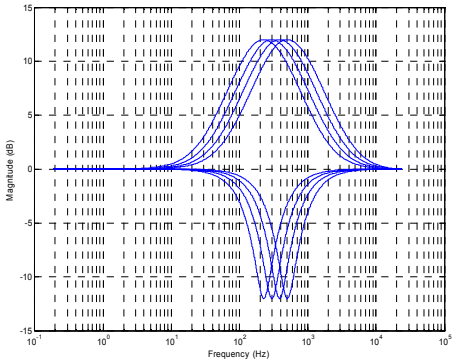


Figure 64 EQ Band 2 – Peak Filter Centre Frequencies, EQ2BW=0

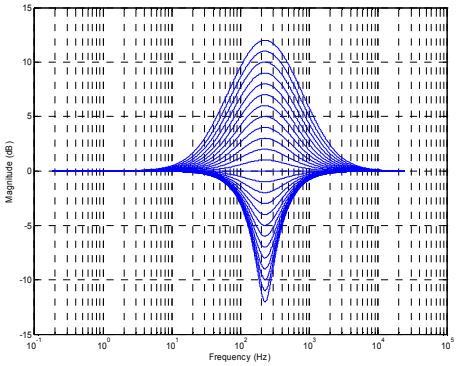


Figure 65 EQ Band 2 – Peak Filter Gains for Lowest Cut- off Frequency, EQ2BW=0

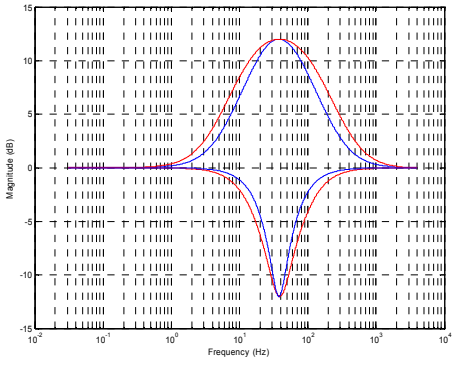


Figure 66 EQ Band 2 – EQ2BW=0, EQ2BW=1

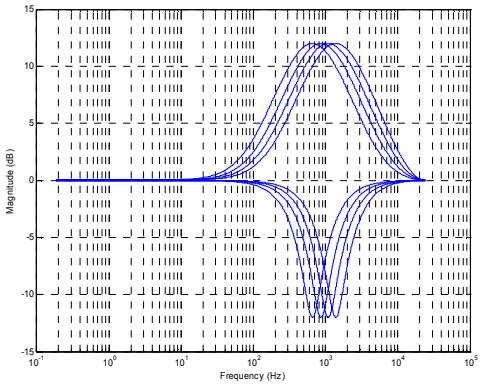


Figure 67 EQ Band 3 – Peak Filter Centre Frequencies, EQ3BW=0

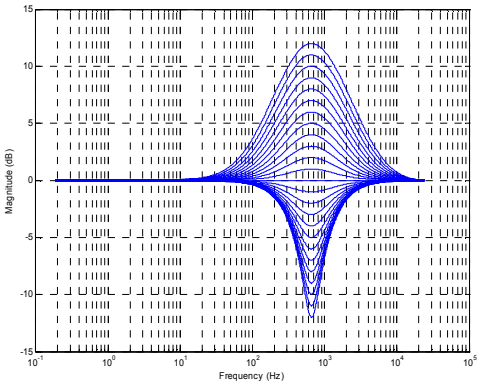


Figure 68 EQ Band 3 – Peak Filter Gains for Lowest Cut-off Frequency, EQ3BW=0

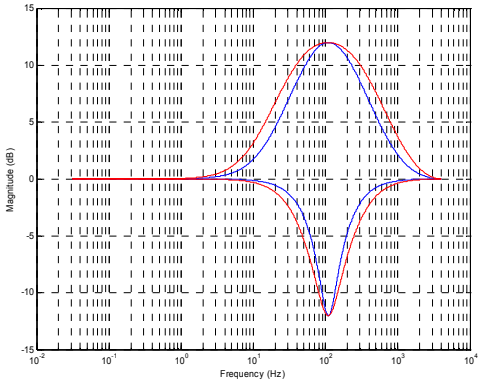


Figure 69 EQ Band 3 – EQ3BW=0, EQ3BW=1

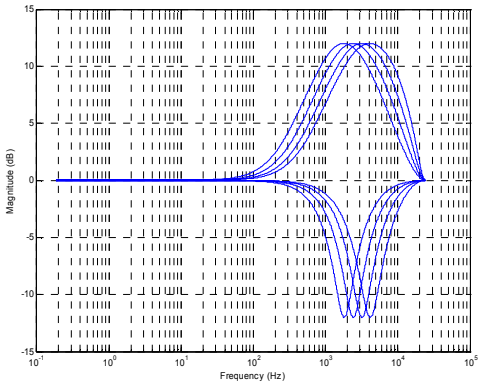


Figure 70 EQ Band 4 – Peak Filter Centre Frequencies, EQ3BW=0

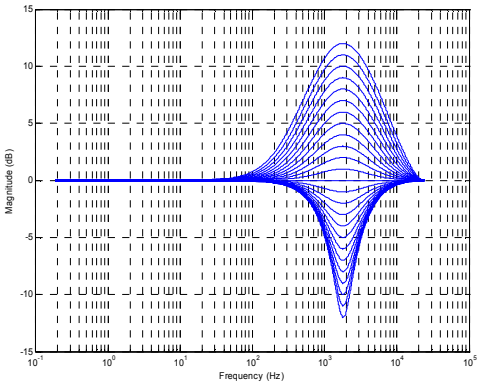


Figure 71 EQ Band 4 – Peak Filter Gains for Lowest Cut-off Frequency, EQ4BW=0

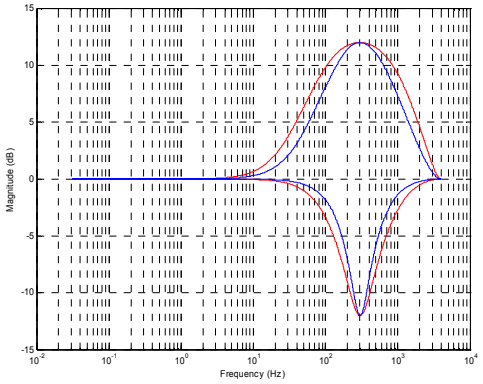


Figure 72 EQ Band 4 – EQ3BW=0, EQ3BW=1

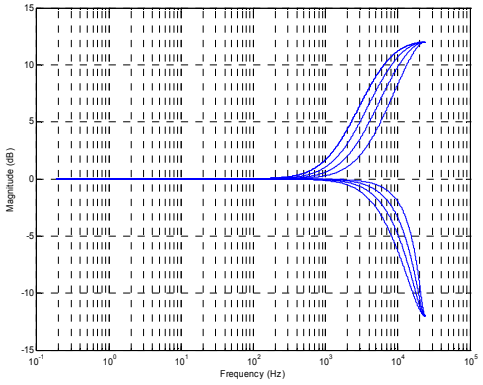


Figure 73 EQ Band 5 High Frequency Shelf Filter Cut-offs

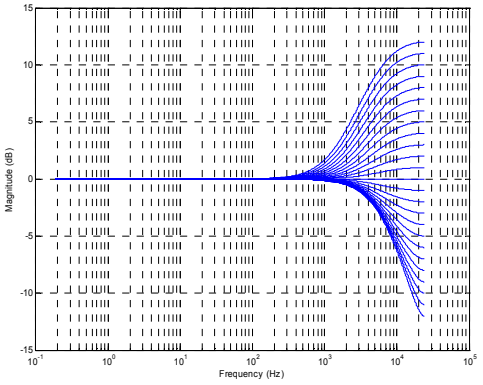


Figure 74 EQ Band 5 Gains for Lowest Cut-off Frequency

Figure 75 shows the result of having the gain set on more than one channel simultaneously. The blue traces show each band (lowest cut-off/centre frequency) with ±12dB gain. The red traces show the cumulative effect of all bands with +12dB gain and all bands -12dB gain, with EqxBW=0 for the peak filters.

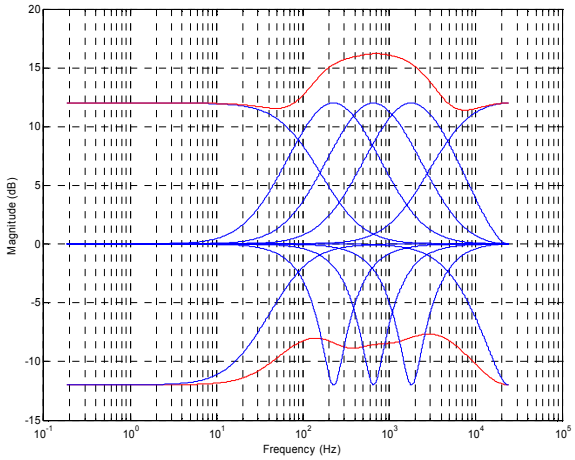


Figure 75 Cumulative Frequency Boost/Cut

APPLICATION INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

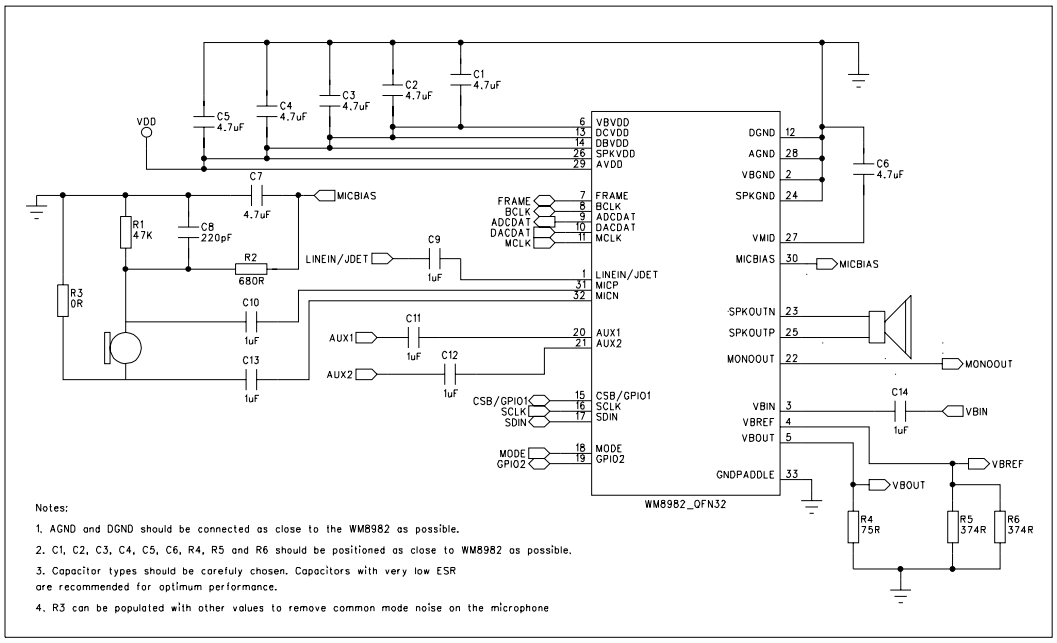
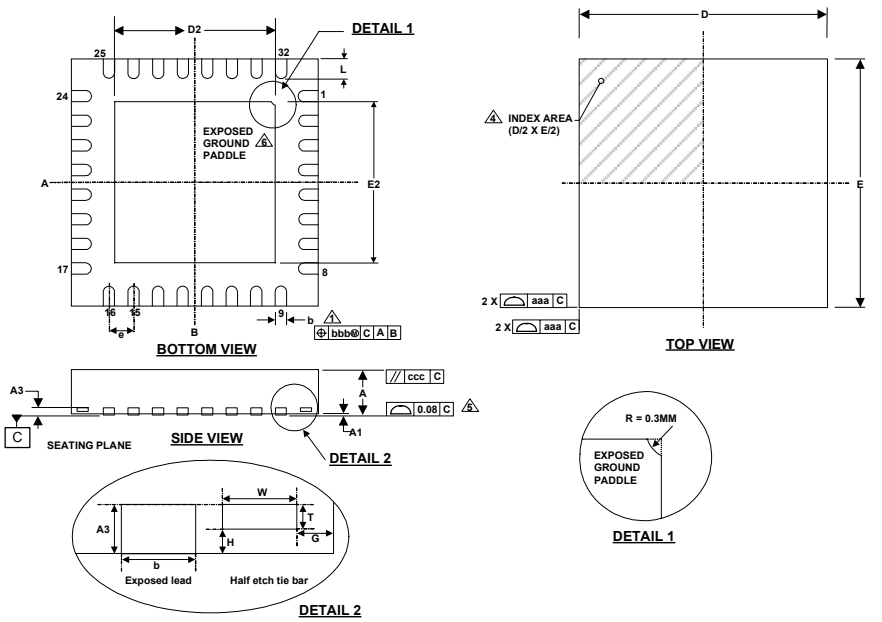


Figure 76 Recommended External Component Diagram

PACKAGE DIAGRAM

FL: 32 PIN QFN PLASTIC PACKAGE 5 x 5 x 0.9 mm BODY, 0.50 mm LEAD PITCH **DM033.E**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	1
D		5.00 BSC		
D2	3.30	3.45	3.55	2
E		5.00 BSC		
E2	3.30	3.45	3.55	2
e		0.50 BSC		
G		0.213		
H		0.1		
L	0.30	0.40	0.50	
T		0.1		
W		0.2		
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-5.			

NOTES:
1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VHHD-5.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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