# WM8955BL

## Stereo DAC For Portable Audio Applications

## DESCRIPTION

The WM8955BL is a low power, high quality stereo DAC with integrated headphone and earpiece amplifiers, designed to reduce external component requirements in portable digital audio applications.

The on-chip headphone amplifiers can deliver 40mW into a 16Ω load. Advanced on-chip digital signal processing performs bass and treble tone control.

The WM8955BL can operate as a master or a slave, and includes an on-chip PLL. It can use most master clock frequencies commonly found in portable systems, including USB, GSM, CDMA or PDC clocks, or standard 256$f_s$ clock rates. Different audio sample rates such as 48kHz, 44.1kHz, 8kHz and many others are supported.

The WM8955BL operates on supply voltages from 1.8V up to 3.6V, although the digital core can operate on a separate supply down to 1.42V, saving power. Different sections of the chip can also be powered down under software control.

The WM8955BL is supplied in a very small and thin 4x4mm QFN package, ideal for use in hand-held and portable systems.

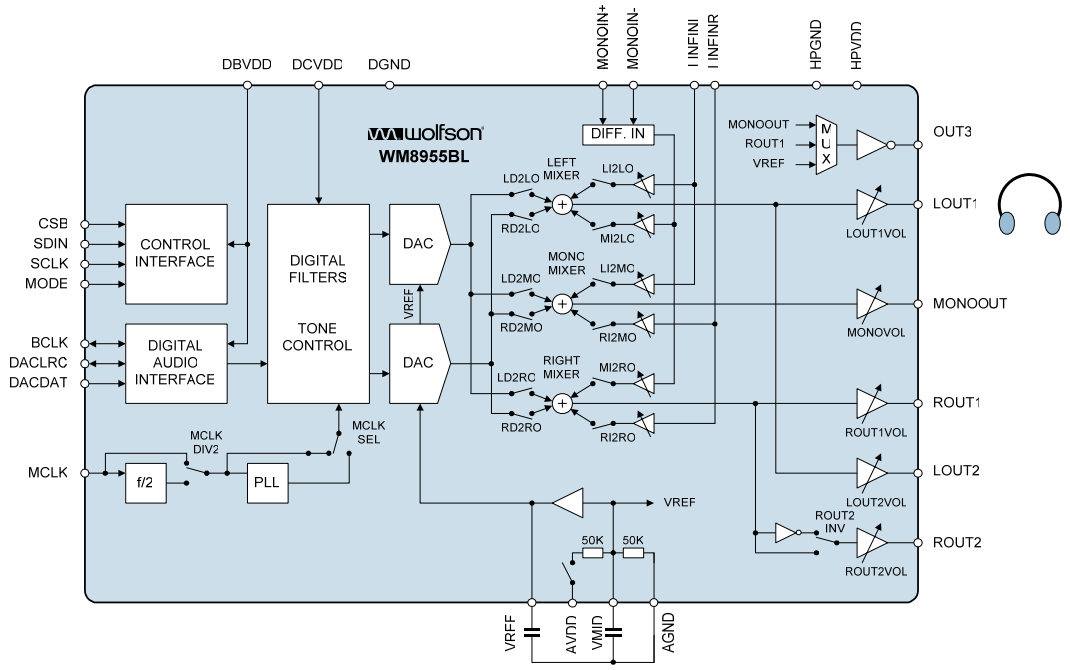
## FEATURES

- DAC SNR 98dB, THD -86dB ('A' weighted @ 48kHz, 3.3V)
- On-chip Headphone Driver
  - 40mW output power on 16Ω / 3.3V
  - SNR 96dB, THD –79dB at 20mW with 16Ω load
- On-chip BTL Earpiece Driver (mono)
- Stereo and Mono Line-in mix into DAC output
- Separately Mixed Stereo and Mono Outputs
- Digital Tone Control and Bass Boost
- Low Power
  - Down to 7mW for stereo playback (1.8V / 1.5V supplies)
  - 10µW Shutdown Mode
- Low Supply Voltages
  - Analogue and Digital I/O: 1.8V to 3.6V
  - Digital core: 1.42V to 3.6V
- Master clocks supported: GSM, CDMA, PDC, USB or standard audio clocks
- Audio sample rates supported: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96kHz
- 28-lead QFN package, 4x4x0.75mm size
- Software compatible with WM8750L, WM8751L, WM8955L

## APPLICATIONS

- Smartphone / Multimedia Phone
- Digital Audio Player

## BLOCK DIAGRAM



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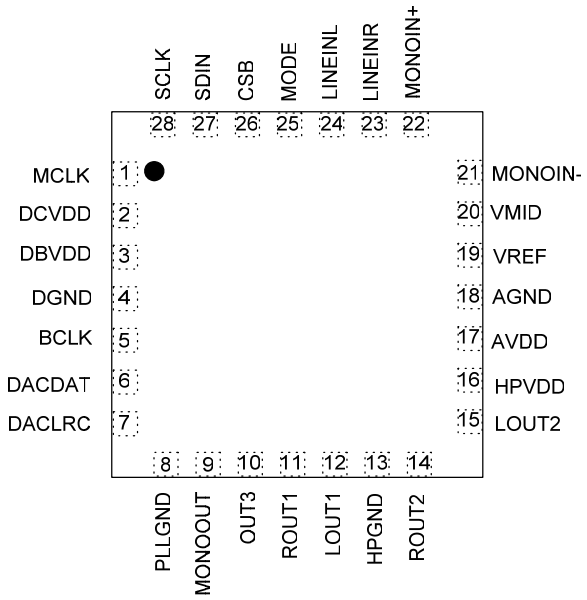
## PIN CONFIGURATION




**TOP VIEW**

## ORDERING INFORMATION

| ORDER CODE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---|---|---|---|---|
| WM8955BLGECO/V | -25°C to +85°C | 28-lead COL QFN (4x4x0.75mm) (Pb-free) | MSL3 | 260°C |
| WM8955BLGECO/RV | -25°C to +85°C | 28-lead COL QFN (4x4x0.75mm) (Pb-free, tape and reel) | MSL3 | 260°C |

**Note:**

Reel quantity = 3,500

## PIN DESCRIPTION

| PIN NO | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | MCLK | Digital Input | Master Clock |
| 2 | DCVDD | Supply | Digital Core Supply |
| 3 | DBVDD | Supply | Digital Buffer (I/O) Supply |
| 4 | DGND | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 5 | BCLK | Digital Input / Output | Audio Interface Bit Clock |
| 6 | DACDAT | Digital Input | DAC Digital Audio Data |
| 7 | DACLRC | Digital Input / Output | Audio Interface Left / Right Clock |
| 8 | PLLGND | Supply | Internally connected to AGND. Connect this pin to AGND externally for best PLL performance, or leave floating. |
| 9 | MONOOUT | Analogue Output | Mono Output |
| 10 | OUT3 | Analogue Output | Output 3 (can be used as Headphone Pseudo Ground) |
| 11 | ROUT1 | Analogue Output | Right Output 1 (Line or Headphone) |
| 12 | LOUT1 | Analogue Output | Left Output 1 (Line or Headphone) |
| 13 | HPGND | Supply | Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2) |
| 14 | ROUT2 | Analogue Output | Right Output 2 (Line or Headphone or Earpiece) |
| 15 | LOUT2 | Analogue Output | Left Output 2 (Line or Headphone or Earpiece) |
| 16 | HPVDD | Supply | Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2, MONOUT) |
| 17 | AVDD | Supply | Analogue Supply |
| 18 | AGND | Supply | Analogue Ground (return path for AVDD) |
| 19 | VREF | Analogue Output | Reference Voltage Decoupling Capacitor |
| 20 | VMID | Analogue Output | Midrail Voltage Decoupling Capacitor |
| 21 | MONOIN- | Analogue Input | Negative end of MONOIN+, for differential mono signals |
| 22 | MONOIN+ | Analogue Input | Analogue Line-in to mixers (mono channel) |
| 23 | LINEINR | Analogue Input | Analogue Line-in to mixers (right channel) |
| 24 | LINEINL | Analogue Input | Analogue Line-in to mixers (left channel) |
| 25 | MODE | Digital Input | Control Interface Selection |
| 26 | CSB | Digital Input | Chip Select / Device Address Selection |
| 27 | SDIN | Digital Input/Output | Control Interface Data Input / 2-wire Acknowledge output |
| 28 | SCLK | Digital Input | Control Interface Clock Input |

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|---|---|
| Supply voltages | -0.3V | +4.5V |
| Voltage range digital inputs | DGND -0.3V | DBVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Operating temperature range, $T_A$ | -25°C | +85°C |
| Storage temperature after soldering | -65°C | +150°C |

**Notes**

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Digital supply range (Core) | DCVDD | | 1.42 | | 3.6 | V |
| Digital supply range (Buffer) | DBVDD | | 1.71 | | 3.6 | V |
| Analogue supplies range | AVDD, HPVDD | | 1.8 | | 3.6 | V |
| Ground | DGND, AGND, HPGND | | | 0 | | V |

**Notes**

1. The DCVDD voltage must be lower than or equal to the DBVDD voltage.

# ELECTRICAL CHARACTERISTICS

**Test Conditions**

DCVDD = 1.5V, AVDD = HPVDD = 3.3V, $T_A$ = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DAC to Line-Out (10kΩ / 50pF load)** | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | AVDD = 3.3V (L/ROUT1 and L/ROUT2) | 90 | 98 | | dB |
| | | AVDD = 1.8V (L/ROUT2 only) | 89 | 95 | | |
| Total Harmonic Distortion | THD | AVDD = 3.3V (L/ROUT1 and L/ROUT2) | | -86 | -75 | dB |
| | | AVDD = 1.8V (L/ROUT2 only) | | -82 | -60 | |
| Channel Separation | | 1kHz signal | | 100 | | dB |
| **Analogue Mixer Inputs (LINEINL/R to L/ROUT1 with 10kΩ / 50pF load)** | | | | | | |
| Full-scale Input Signal Level | $V_{INFS}$ | AVDD = 3.3V | | 1.0 | | V rms |
| | | AVDD = other | | AVDD/3.3 | | |
| Signal to Noise Ratio Line-in to Line-Out (A-weighted) | SNR | AVDD = 3.3V | | 98 | | dB |
| | | AVDD = 1.8V | | 95 | | |
| Total Harmonic Distortion | THD | AVDD = 3.3V | | -94 | | dB |
| | | AVDD = 1.8V | | -90 | | |
| Input Resistance (signal enters one mixer only) | $R_{LINEIN}$ | PGA gain = 0dB | 18 | 20.5 | | kΩ |
| | | PGA gain = +6dB | 6 | 10.5 | | |
| Input Resistance (signal enters two mixers) | | PGA gain = 0dB | | 10.25 | | |
| | | PGA gain = +6dB | | 5.25 | | |
| MONOIN+/- input resistance | $R_{MONOIN}$ | PGA gain = 0dB | 18 | 20 | | kΩ |
| | | PGA gain = +6dB | 18 | 20 | | |
| Mute Attenuation | | | | 91 | | dB |
| **Analogue Outputs (LOUT1/2, ROUT1/2, MONOOUT)** | | | | | | |
| 0dB Full scale output voltage | | AVDD = 3.3V | 0.95 | 1 | 1.05 | Vrms |
| | | AVDD = other | | AVDD/3.3 | | |
| Mute attenuation | | 1kHz, full scale signal | | 94 | | dB |
| **Headphone Output (LOUT1/2, ROUT1/2 with 16 or 32Ω load)** | | | | | | |
| Output Power per channel | $P_O$ | Output power is very closely correlated with THD; see below. | | | | |
| Total Harmonic Distortion | THD | HPVDD=1.8V, $R_L$=32Ω $P_O$=5mW | | 0.018 -75 | | % dB |
| | | HPVDD=1.8V, $R_L$=16Ω $P_O$=5mW | | 0.025 -72 | | |
| | | HPVDD=3.3V, $R_L$=32Ω, $P_O$=20mW | | 0.013 -78 | | |
| | | HPVDD=3.3V, $R_L$=16Ω, $P_O$=20mW | | 0.011 -79 | 0.03 -70 | |
| Signal to Noise Ratio (A-weighted) | SNR | HPVDD = 3.3V | 92 | 96 | | dB |
| | | HPVDD = 1.8V (L/ROUT2 only) | 89 | 95 | | |

**Test Conditions**

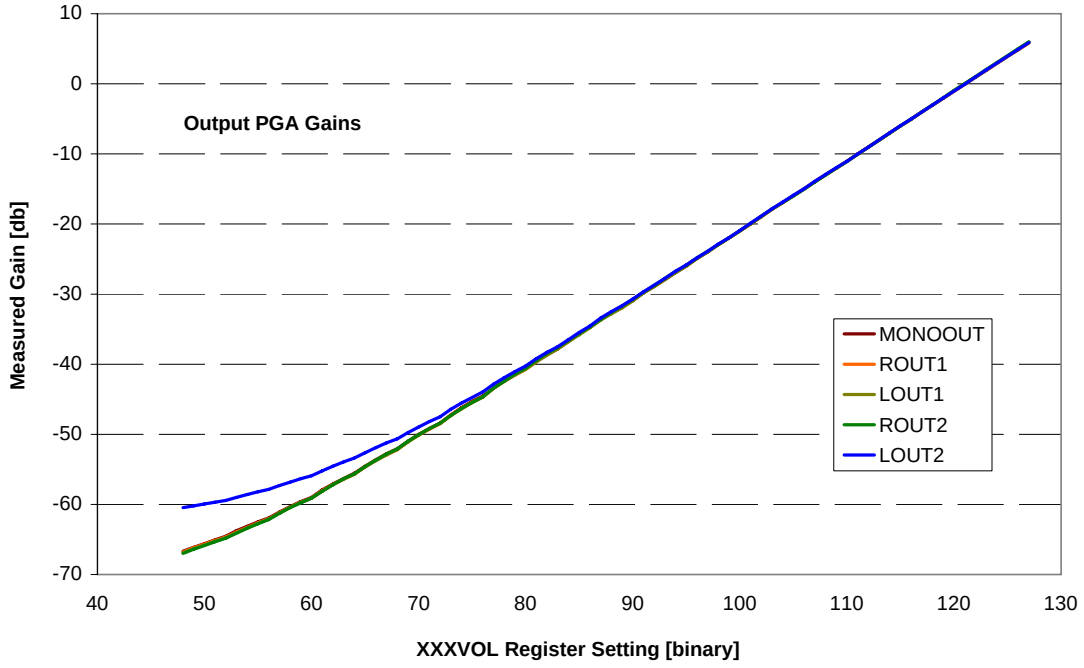
DCVDD = 1.5V, AVDD = HPVDD = 3.3V, $T_A$ = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

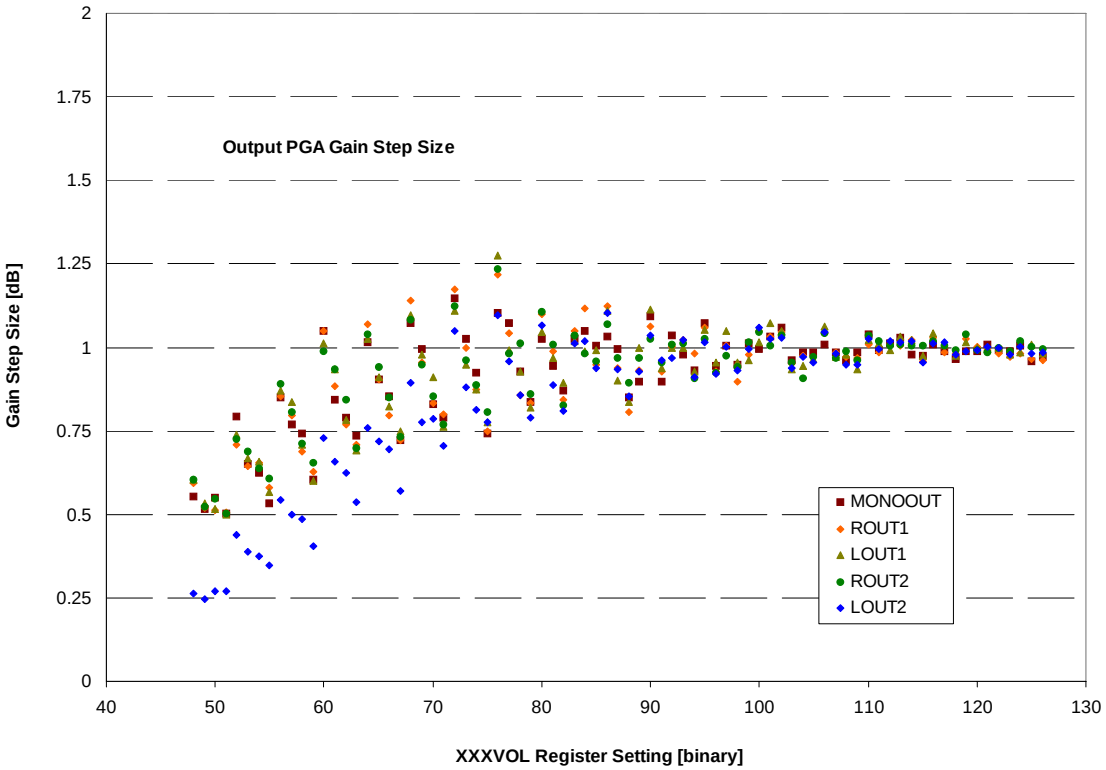
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analogue Reference Levels** | | | | | | |
| Midrail Reference Voltage | VMID | | –3% | AVDD/2 | +3% | V |
| Buffered Reference Voltage | VREF | | –3% | AVDD/2 | +3% | V |
| **Digital Input / Output** | | | | | | |
| Input HIGH Level | $V_{IH}$ | | 0.7×DBVDD | | | V |
| Input LOW Level | $V_{IL}$ | | | | 0.3×DBVDD | V |
| Output HIGH Level | $V_{OH}$ | $I_{OH}$ = -1mA | 0.9×DBVDD | | | V |
| Output LOW Level | $V_{OL}$ | $I_{OL}$ = 1mA | | | 0.1×DBVDD | V |

## TERMINOLOGY

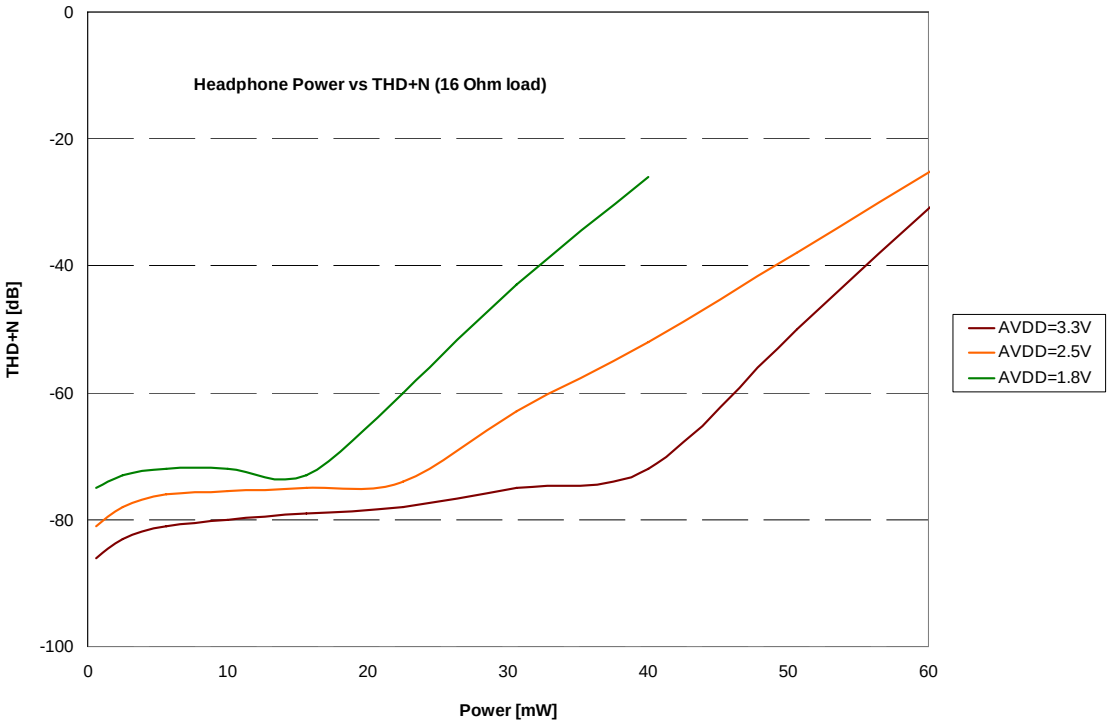
1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

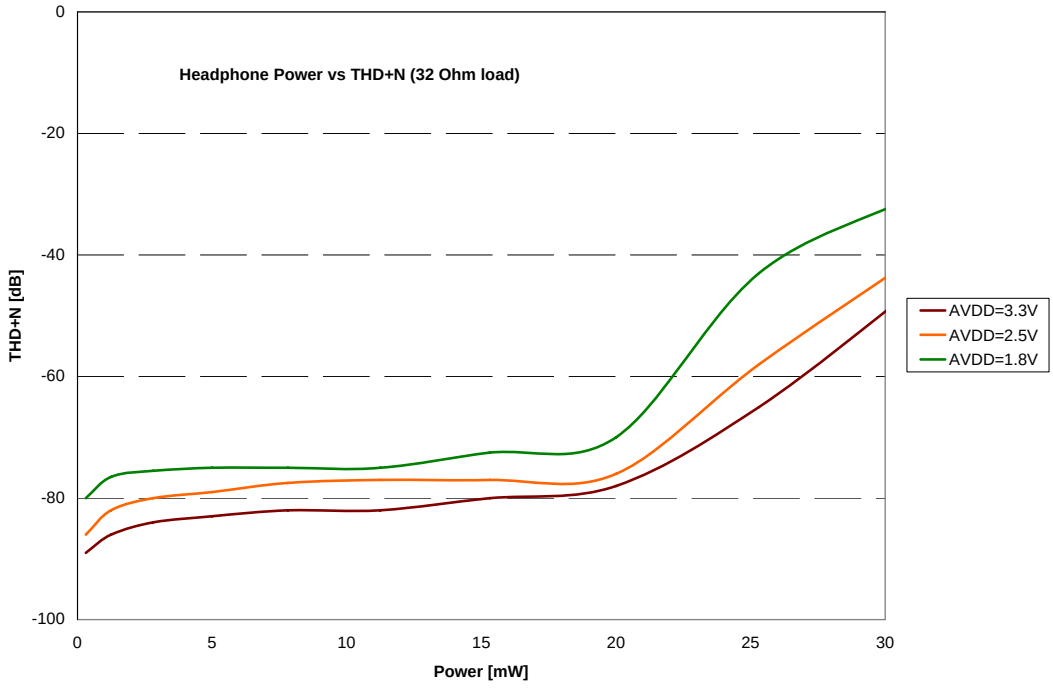
## OUTPUT PGA'S LINEARITY



## HEADPHONE OUTPUT THD VERSUS POWER



## POWER CONSUMPTION

The power consumption of the WM8955BL depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings.
- Operating mode: Power consumption is lower in mono modes than in stereo, as one DAC is switched OFF. Unused analogue outputs should be switched off.

| Control Register | R25 | | R26 (1Ah) | | | | | | | | R24 | R23 | R38 | R43 | Other settings | AVDD | | DCVDD | | DBVDD | | HPVDD | | Tot. Power |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | VMIDSEL | VREF | DACL | DACR | LOUT1 | ROUT1 | LOUT2 | ROUT2 | MONO | OUT3 | DACOSR | VSEL | DMEN | PLLEN | | V | I (mA) | V | I (mA) | V | I (mA) | V | I (mA) | (mW) |
| OFF | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 0 | 0 | Clocks stopped | 3.3 | 0.0001 | 3.3 | 0.0103 | 3.3 | 0 | 3.3 | 0 | 0.03432 |
| | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 0.0001 | 2.5 | 0.0084 | 2.5 | 0 | 2.5 | 0 | 0.02125 |
| | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 0.0001 | 1.5 | 0.0067 | 1.8 | 0 | 1.8 | 0 | 0.01023 |
| Low-power standby (LPS) | 10 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 0 | 0 | | 3.3 | 0.2339 | 3.3 | 0.409 | 3.3 | 0.0856 | 3.3 | 0 | 2.40405 |
| using 500 KOhm VMID string | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 0.1737 | 2.5 | 0.2556 | 2.5 | 0.0616 | 2.5 | 0 | 1.22725 |
| | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 0.1208 | 1.5 | 0.1416 | 1.8 | 0.042 | 1.8 | 0 | 0.50544 |
| Playback to Line-out | 01 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 11 | 0 | 0 | | 3.3 | 3.9903 | 3.3 | 5.1104 | 3.3 | 0.0878 | 3.3 | 0.6621 | 32.50698 |
| | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 2.9459 | 2.5 | 3.5193 | 2.5 | 0.0632 | 2.5 | 0.6553 | 17.95925 |
| | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 2.0701 | 1.5 | 1.9742 | 1.8 | 0.0432 | 1.8 | 0.3845 | 7.45734 |
| Playback to Line-out | 01 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 11 | 0 | 0 | | 3.3 | 3.7821 | 3.3 | 4.2678 | 3.3 | 0.0879 | 3.3 | 0.6619 | 29.03901 |
| (64x oversampling mode) | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 2.7924 | 2.5 | 2.9224 | 2.5 | 0.0632 | 2.5 | 0.6557 | 16.08425 |
| | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 1.9604 | 1.5 | 1.6299 | 1.8 | 0.0432 | 1.8 | 0.3847 | 6.74379 |
| Playback | 01 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 11 | 0 | 0 | | 3.3 | 3.9623 | 3.3 | 5.0846 | 3.3 | 0.0878 | 3.3 | 0.6913 | 32.4258 |
| to 16 Ohm headphone | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 2.946 | 2.5 | 3.5187 | 2.5 | 0.0632 | 2.5 | 0.6691 | 17.9925 |
| using caps on HPOUTL/R | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 2.0702 | 1.5 | 1.9742 | 1.8 | 0.04332 | 1.8 | 0.3852 | 7.458996 |
| Playback | 01 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 11 | 0 | 0 | R24, OUT3SW=00 | 3.3 | 4.0662 | 3.3 | 5.1007 | 3.3 | 0.0881 | 3.3 | 1.172 | 34.4091 |
| to 16 Ohm headphone | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 2.999 | 2.5 | 3.557 | 2.5 | 0.064 | 2.5 | 1.167 | 19.4675 |
| capless mode using OUT3 | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 2.0705 | 1.5 | 1.9164 | 1.8 | 0.04272 | 1.8 | 0.914 | 8.8857 |
| Headphone Amp | 01 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 11 | 0 | 0 | Clocks stopped | 3.3 | 1.7135 | 3.3 | 0.0901 | 3.3 | 0 | 3.3 | 0.6624 | 8.1378 |
| line-in to 16 Ohm h/phone | | | | | | | | | | | | 01 | 0 | 0 | | 2.5 | 1.211 | 2.5 | 0.009 | 2.5 | 0 | 2.5 | 0.6291 | 4.62275 |
| | | | | | | | | | | | | 00 | 0 | 0 | | 1.8 | 0.8017 | 1.5 | 0.0071 | 1.8 | 0 | 1.8 | 0.3869 | 2.15013 |
| Phone Call | 01 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 11 | 1 | 0 | Clocks stopped | 3.3 | 1.9574 | 3.3 | 0.0905 | 3.3 | 0 | 3.3 | 1.1675 | 10.61082 |
| diff. mono line-in to h/phone, | | | | | | | | | | | | 01 | 1 | 0 | | 2.5 | 1.4258 | 2.5 | 0.009 | 2.5 | 0 | 2.5 | 1.1017 | 6.34125 |
| diff. mono line-out to TX | | | | | | | | | | | | 00 | 1 | 0 | | 1.8 | 0.9076 | 1.5 | 0.0071 | 1.8 | 0 | 1.8 | 0.6576 | 2.82801 |
| PLL only | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 0 | 1 | | 3.3 | 0.5389 | 3.3 | 0.4966 | 3.3 | 0.0855 | 3.3 | 0 | 3.6993 |
| | | | | | | | | | | | | 01 | 0 | 1 | | 2.5 | 0.4554 | 2.5 | 0.2774 | 2.5 | 0.0616 | 2.5 | 0 | 1.986 |
| | | | | | | | | | | | | 00 | 0 | 1 | | 1.8 | 0.4034 | 1.5 | 0.145 | 1.8 | 0.04188 | 1.8 | 0 | 1.019004 |

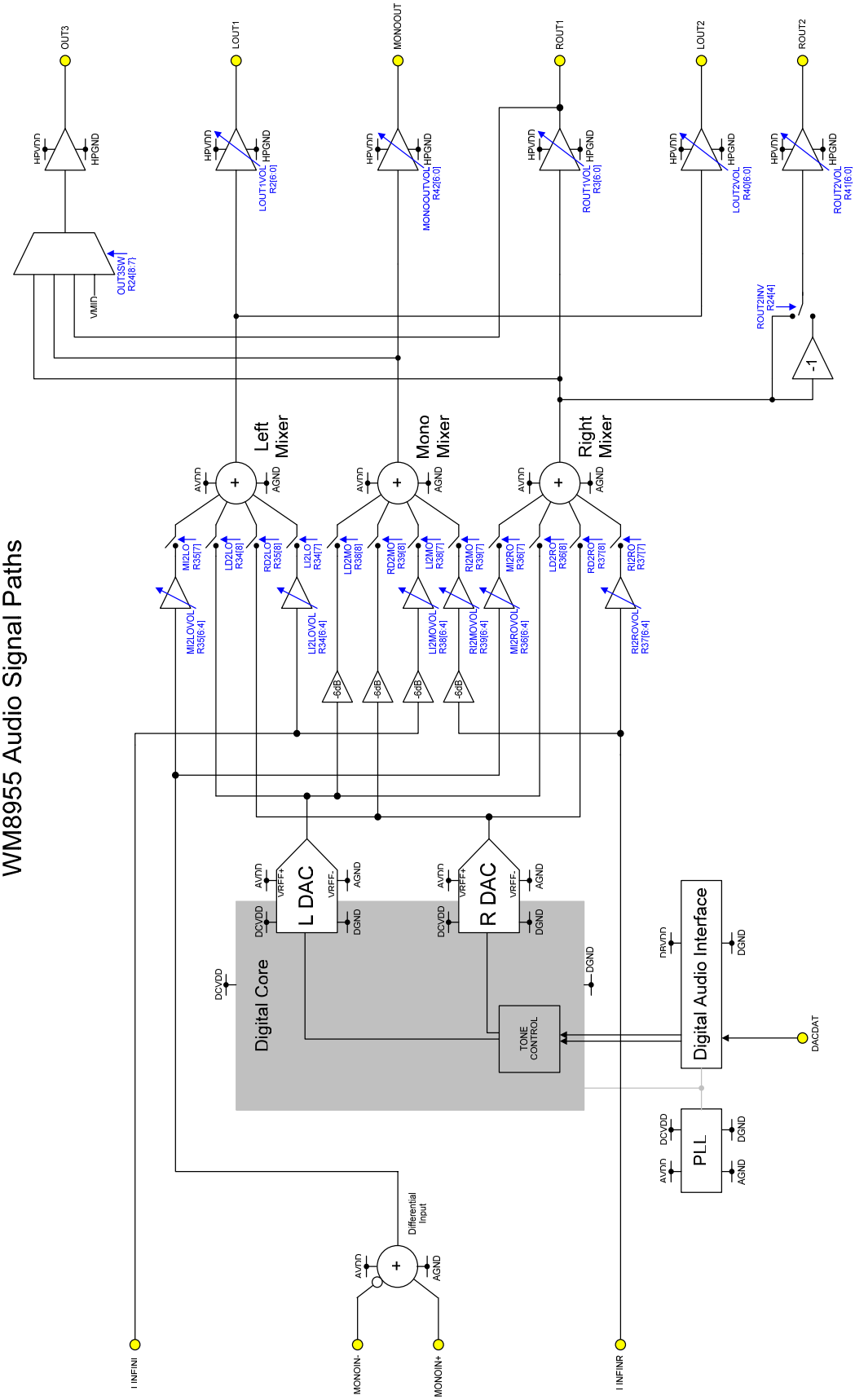
**Table 1 Supply Current Consumption**

**Notes:**

1. $T_A$ = +25°C, Slave Mode, fs = 48kHz, MCLK = 12.288 MHz (256fs), 24-bit data
2. All figures are quiescent, with no signal.
3. The power dissipated in the headphone itself is not included in the above table.

## AUDIO PATHS OVERVIEW

WM8955 Audio Signal Paths



# SIGNAL TIMING REQUIREMENTS

## SYSTEM CLOCK TIMING

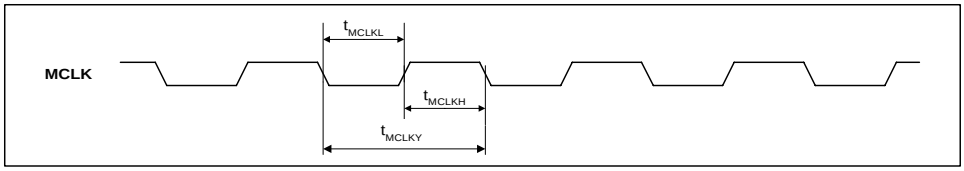



**Figure 1 System Clock Timing Requirements**

**Test Conditions**

**CLKDIV2 = 0**, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **System Clock Timing Information** | | | | | |
| MCLK System clock pulse width high | $T_{MCLKL}$ | 21 | | | ns |
| MCLK System clock pulse width low | $T_{MCLKH}$ | 21 | | | ns |
| MCLK System clock cycle time | $T_{MCLKY}$ | 54 | | | ns |
| MCLK duty cycle | $T_{MCLKDS}$ | 60:40 | | 40:60 | |

**Test Conditions**

**CLKDIV2 = 1**, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **System Clock Timing Information** | | | | | |
| MCLK System clock pulse width high | $T_{MCLKL}$ | 10 | | | ns |
| MCLK System clock pulse width low | $T_{MCLKH}$ | 10 | | | ns |
| MCLK System clock cycle time | $T_{MCLKY}$ | 27 | | | ns |

## AUDIO INTERFACE TIMING – MASTER MODE

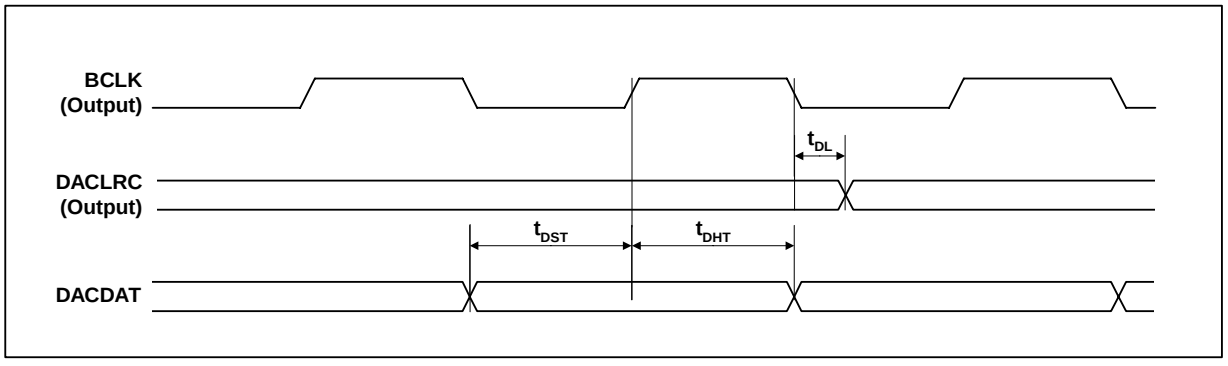



**Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)**

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Bit Clock Timing Information** | | | | | |
| BCLK rise time (10pF load) | $t_{BCLKR}$ | | | 3 | ns |
| BCLK fall time (10pF load) | $t_{BCLKF}$ | | | 3 | ns |
| BCLK duty cycle (normal mode, BCLK = MCLK/n) | $t_{BCLKDS}$ | | 50:50 | | |
| BCLK duty cycle (USB mode, BCLK = MCLK) | $t_{BCLKDS}$ | | $T_{MCLKDS}$ | | |

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **System Clock Timing Information** | | | | | |
| DACLRC propagation delay from BCLK falling edge | $t_{DL}$ | | | 10 | ns |
| DACDAT setup time to BCLK rising edge | $t_{DST}$ | 10 | | | ns |
| DACDAT hold time from BCLK rising edge | $t_{DHT}$ | 10 | | | ns |

## AUDIO INTERFACE TIMING – SLAVE MODE

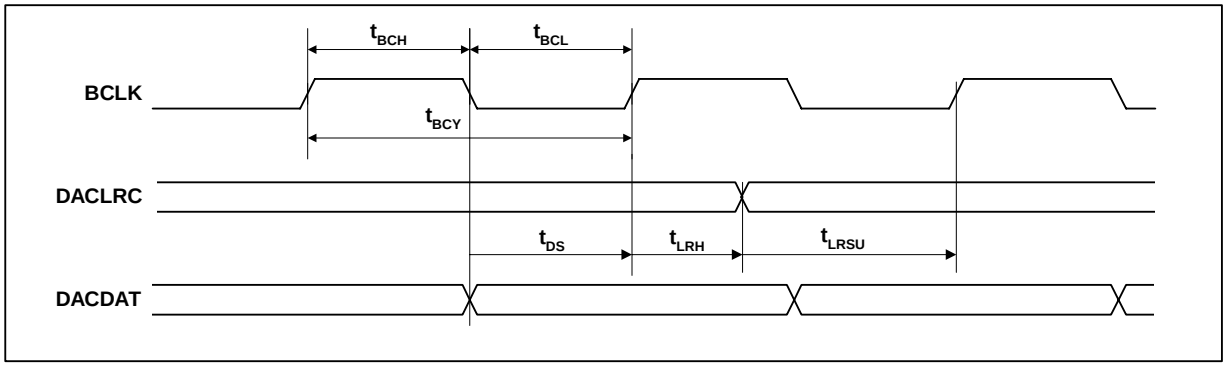



**Figure 3 Digital Audio Data Timing – Slave Mode (see Control Interface)**

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **System Clock Timing Information** | | | | | |
| BCLK cycle time | $t_{BCY}$ | 50 | | | ns |
| BCLK pulse width high | $t_{BCH}$ | 20 | | | ns |
| BCLK pulse width low | $t_{BCL}$ | 20 | | | ns |
| DACLRC setup time to BCLK rising edge | $t_{LRSU}$ | 10 | | | ns |
| DACLRC hold time from BCLK rising edge | $t_{LRH}$ | 10 | | | ns |
| DACDAT hold time from BCLK rising edge | $t_{DH}$ | 10 | | | ns |

## CONTROL INTERFACE TIMING – 3-WIRE MODE

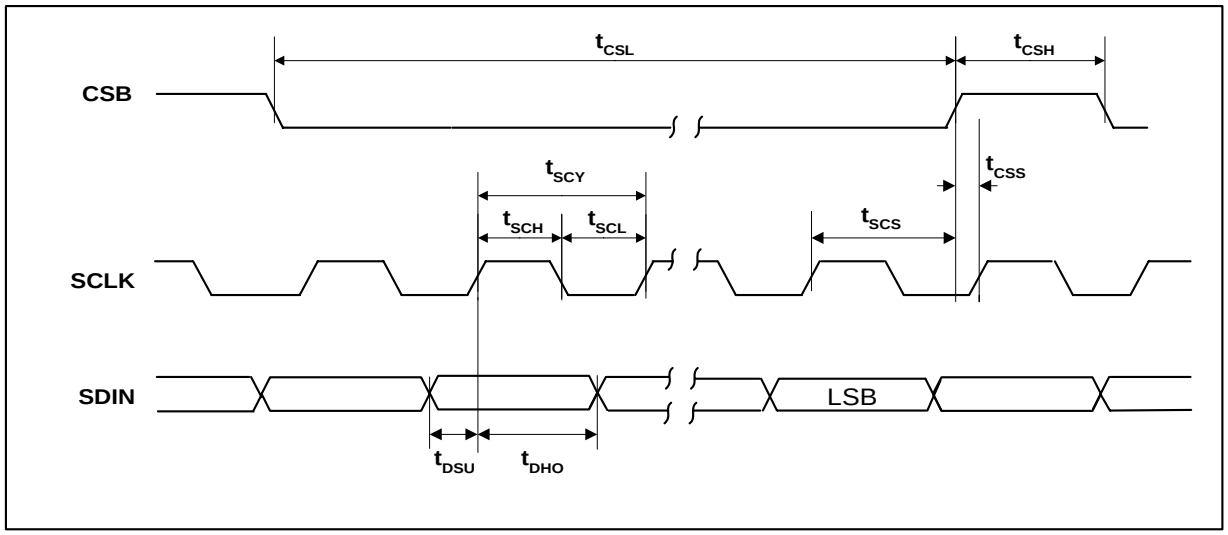



**Figure 4 Control Interface Timing – 3-Wire Serial Control Mode**

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Program Register Input Information** | | | | | |
| SCLK rising edge to CSB rising edge | $t_{SCS}$ | 500 | | | ns |
| SCLK pulse cycle time | $t_{SCY}$ | 200 | | | ns |
| SCLK pulse width low | $t_{SCL}$ | 80 | | | ns |
| SCLK pulse width high | $t_{SCH}$ | 80 | | | ns |
| SDIN to SCLK set-up time | $t_{DSU}$ | 40 | | | ns |
| SCLK to SDIN hold time | $t_{DHO}$ | 40 | | | ns |
| CSB pulse width low | $t_{CSL}$ | 40 | | | ns |
| CSB pulse width high | $t_{CSH}$ | 40 | | | ns |
| CSB rising to SCLK rising | $t_{CSS}$ | 40 | | | ns |
| Pulse width of spikes that will be suppressed | $t_{ps}$ | 0 | | 5 | ns |

## CONTROL INTERFACE TIMING – 2-WIRE MODE

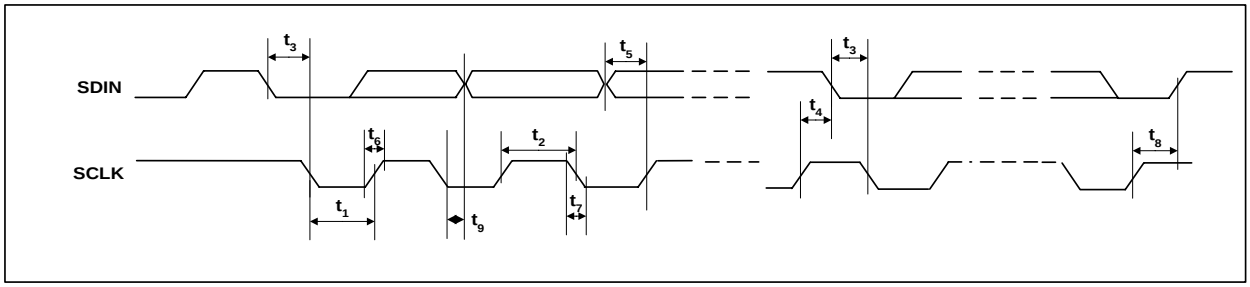



**Figure 5 Control Interface Timing – 2-Wire Serial Control Mode**

**Test Conditions**

DBVDD = 3.3V, DGND = 0V, $T_A$ = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Program Register Input Information** | | | | | |
| SCLK Frequency | | 0 | | 526 | kHz |
| SCLK Low Pulse-Width | $t_1$ | 1.3 | | | us |
| SCLK High Pulse-Width | $t_2$ | 600 | | | ns |
| Hold Time (Start Condition) | $t_3$ | 600 | | | ns |
| Setup Time (Start Condition) | $t_4$ | 600 | | | ns |
| Data Setup Time | $t_5$ | 100 | | | ns |
| SDIN, SCLK Rise Time | $t_6$ | | | 300 | ns |
| SDIN, SCLK Fall Time | $t_7$ | | | 300 | ns |
| Setup Time (Stop Condition) | $t_8$ | 600 | | | ns |
| Data Hold Time | $t_9$ | | | 900 | ns |
| Pulse width of spikes that will be suppressed | $t_{ps}$ | 0 | | 5 | ns |

## INTERNAL POWER ON RESET CIRCUIT

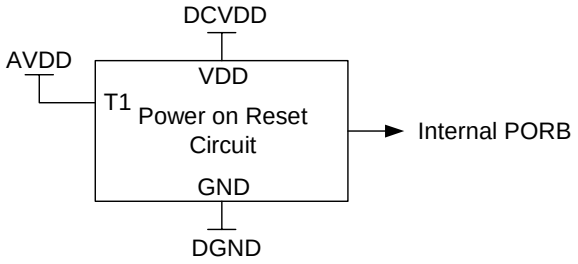



**Figure 6 Internal Power on Reset Circuit Schematic**

The WM8955BL includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

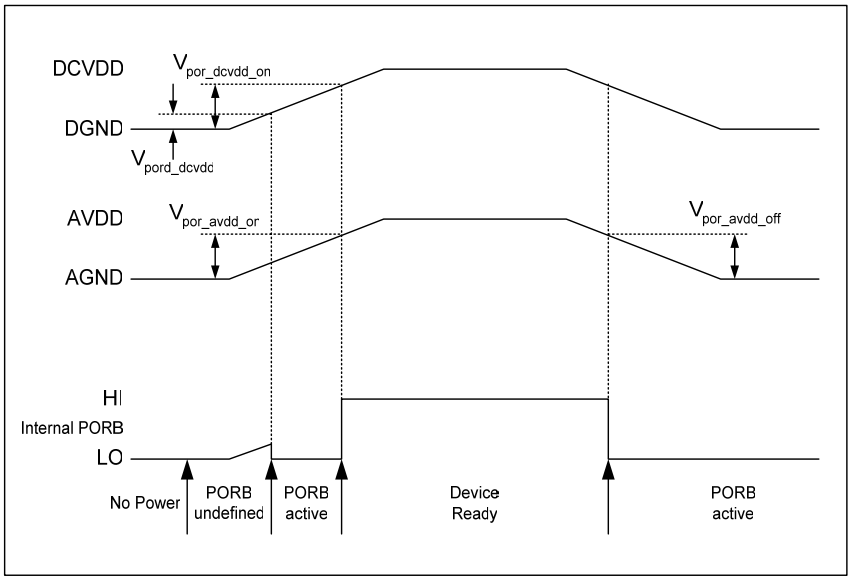



**Figure 7 Typical Power-Up Sequence**

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

| SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $V_{pord\_dcvdd}$ | 0.4 | 0.6 | 0.8 | V |
| $V_{por\_dcvdd\_on}$ | 0.9 | 1.26 | 1.6 | V |
| $V_{por\_avdd\_on}$ | 0.5 | 0.7 | 0.9 | V |
| $V_{por\_avdd\_off}$ | 0.4 | 0.6 | 0.8 | V |

**Table 2 Typical POR Operation (typical values, not tested)**

# DEVICE DESCRIPTION

## INTRODUCTION

The WM8955BL is a low power audio DAC offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications such as portable music players and smartphones.

The device has a configurable digital audio interface where digital audio data is fed to the internal digital filters and then the DAC. The interface supports a number of audio data formats including $I^2S$, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), Left Justified and Right Justified formats, and can operate in master or slave modes.

The on-chip digital filters perform tone control and digital volume control according to the user setting, and convert the audio data into oversampled bitstreams, which are passed to the left and right channel DACs. A multi-bit, low-order $\Sigma\Delta$ DAC architecture with dynamic element matching is used, delivering optimum performance with low power consumption.

The DAC output signal enters an analogue mixer where analogue input signals can be added to it. The WM8955BL has a total of six analogue output pins, which can be configured as stereo line-outs, mono line-outs, differential mono line-outs, stereo headphone outputs or differential mono (BTL) earpiece outputs.

The WM8955BL includes an on-chip PLL to generate commonly used audio rates, such as 48kHz and 44.1kHz, from system clocks found in GSM, CDMA and PDC phones and other portable systems.

To allow full software control over all its features, the WM8955BL offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

The design of the WM8955BL has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off parts of the circuitry under software control, including standby and power off modes.

## SIGNAL PATH

The WM8955BL signal paths consists of digital filters, DACs, analogue mixers and output drivers. Each circuit block can be enabled or disabled separately using the control bits in register 26 (see “Power Management”). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8955BL, irrespective of whether the DACs are running or not.

The WM8955BL receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Tone control and Bass Boost
- Digital Mono Mix
- Sigma-Delta Modulation

Two high performance, sigma-delta audio DACs convert the digital data into two analogue signals (left and right). These can then be mixed with analogue signals from the LINEINL, LINEINR and MONOIN pins, and the mix is fed to the output drivers, LOUT1/ROUT1, LOUT2/ROUT2, MONOOUT and OUT3.

- LOUT1/ROUT1: can drive 16Ω or 32Ω stereo headphones or stereo line output.
- LOUT2/ROUT2: can drive a 32Ω earpiece, stereo headphones or a stereo line-out.
- MONOOUT: line output designed to drive a 10kΩ load.
- OUT3: multi-function output, may be used for capacitor-less headphone drive, differential mono-out, line-out or 32Ω earpiece driver.

## DIGITAL VOLUME CONTROL

The WM8955BL has on-chip digital attenuation from –127dB to 0dB in 0.5dB steps, allowing the user to adjust the volume of each channel separately. The level of attenuation for an eight-bit code X is given by:

$-0.5 \times (255 - X)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The LDVU and RDVU control bits control the loading of digital volume control data. When LDVU or RDVU are set to 0, the LDACVOL or RDACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both left and right gain settings are updated simultaneously when either LDVU or RDVU are set to 1.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R10 (0Ah)<br>Left Channel Digital Volume | 7:0 | LDACVOL[7:0] | 11111111<br>( 0dB ) | Left DAC Digital Volume Control<br>0000 0000 = Digital Mute<br>0000 0001 = -127dB<br>0000 0010 = -126.5dB<br>... 0.5dB steps up to<br>1111 1111 = 0dB |
| | 8 | LDVU | 0 | Left DAC Volume Update<br>0 = Store LDACVOL in intermediate latch (no gain change)<br>1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch) |
| R11 (0Bh)<br>Right Channel Digital Volume | 7:0 | RDACVOL[7:0] | 11111111<br>( 0dB ) | Right DAC Digital Volume Control<br>similar to LDACVOL |
| | 8 | RDVU | 0 | Right DAC Volume Update<br>0 = Store RDACVOL in intermediate latch (no gain change)<br>1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL) |

**Table 3 Digital Volume Control**

## TONE CONTROL

The WM8955BL provides separate controls for bass and treble with programmable gains and filter characteristics. This function operates on digital audio data before it is passed to the audio DACs.

Bass control can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.
- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.

Treble control applies a user programmable gain, without any adaptive boost function.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | |
|---|---|---|---|---|---|---|
| R12 (0Ch) Bass Control | 7 | BB | 0 | Bass Mode<br>0 = Linear bass control<br>1 = Adaptive bass boost | | |
| | 6 | BC | 0 | Bass Filter Characteristic<br>0 = Low Cutoff (130 Hz at 48kHz sampling)<br>1 = High Cutoff (200 Hz at 48kHz sampling) | | |
| | 3:0 | BASS | 1111 (OFF) | Bass Intensity | | |
| | | | | Code | BB=0 | BB=1 |
| | | | | 0000 | +9dB | 15 (max) |
| | | | | 0001 | +9dB | 14 |
| | | | | 0010 | +7.5dB | 13 |
| | | | | … | (1.5dB steps) | … |
| | | | | 0111 | 0dB | 8 |
| | | | | … | (1.5dB steps) | … |
| | | | | 1011-1101 | -6dB | 4-2 |
| | | | | 1110 | -6dB | 1 (min) |
| | | | | 1111 | Bypass (OFF) | |
| R13 (0Dh) Treble Control | 6 | TC | 0 | Treble Filter Characteristic<br>0 = High Cutoff (8kHz at 48kHz sampling)<br>1 = Low Cutoff (4kHz at 48kHz sampling) | | |
| | 3:0 | TRBL | 1111 (Disabled) | Treble Intensity<br>0000 or 0001 = +9dB<br>0010 = +7.5dB<br>… (1.5dB steps)<br>1011 to 1110 = -6dB<br>1111 = Disable | | |

**Table 4 Tone Control**

**Note:**

All cut-off frequencies change proportionally with the DAC sample rate.

## DIGITAL TO ANALOGUE CONVERTER (DAC)

Treble and linear bass enhancement may produce signals that exceed full-scale. In order to avoid limiting under these conditions, it is recommended to set the DAT bit to attenuate the digital input signal by 6dB. The gain at the outputs should be increased by 6dB to compensate for the attenuation. Cut-only tone adjustment and adaptive bass boost cannot produce signals above full-scale and therefore do not require the DAT bit to be set.

After passing through the tone control filters, digital 'de-emphasis' can be applied to the audio data if necessary (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

The WM8955BL also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. This function is enabled by default. To play back an audio signal, the WM8955BL must first be unmuted by setting the DACMU bit to zero.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R5 (05h)<br>DAC Control | 7 | DAT | 0 | DAC 6dB attenuate enable<br>0 = disabled (0dB)<br>1 = -6dB enabled |
| | 3 | DACMU | 1 | Digital Soft Mute<br>1 = mute<br>0 = no mute (signal active) |
| | 2:1 | DEEMPH | 00 | De-emphasis Control<br>11 = 48kHz sample rate<br>10 = 44.1kHz sample rate<br>01 = 32kHz sample rate<br>00 = No De-emphasis |

**Table 5 DAC Control**

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data are converted to analogue in two separate DACs. However, it is also possible to disable one channel, so that the same signal (left or right) appears on both analogue output channels. Additionally, there is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC, while the other DAC is switched off. The mono-mix signal can be selected to appear on both analogue output channels (see Analogue Outputs).

The DAC output defaults to non-inverted. Setting DACINV will invert the DAC output phase on both left and right channels.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R23 (17h)<br>Additional (1) | 5:4 | DMONOMIX[1:0] | 00 | DAC mono mix<br>00: stereo<br>01: mono ((L+R)/2) into DACL, '0' into DACR<br>10: mono ((L+R)/2) into DACR, '0' into DACL<br>11: mono ((L+R)/2) into DACL & DACR |
| | 1 | DACINV | 0 | DAC phase invert<br>0: non-inverted<br>1: inverted |

**Table 6 DAC Mono Mix Select**

## LINE INPUTS AND OUTPUT MIXERS

The WM8955BL provides the option to mix the DAC output signal with analogue line-in signals from the LINEINL, LINEINR and MONOIN+ and MONOIN- pins. The level of the mixed-in signals can be controlled with PGAs (Programmable Gain Amplifiers).

LINEINL, LINEINR, MONOIN+ and MONOIN- are high impedance, low capacitance AC coupled analogue inputs. They are biased internally to the reference voltage VREF. Whenever these inputs are muted or the device placed into standby mode, the inputs remain biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The mono mixer is designed to allow a number of signal combinations to be mixed, including the possibility of mixing both the right and left channels together to produce a mono output. To prevent overloading of the mixer when full-scale DAC left and right signals are input, the mixer inputs from the DAC outputs each have a fixed gain of -6dB. The bypass path inputs to the mono mixer have variable gain as determined by R38/R39 bits [6:4].

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R34 (22h)<br>Left Mixer (1) | 8 | LD2LO | 0 | Left DAC to Left Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 7 | LI2LO | 0 | LINEINL Signal to Left Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 6:4 | LI2LOVOL | 101<br>(-9dB) | LINEINL Signal to Left Mixer Volume<br>000 = +6dB<br>… (3dB steps)<br>111 = -15dB |
| R35 (23h)<br>Left Mixer (2) | 8 | RD2LO | 0 | Right DAC to Left Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 7 | MI2LO | 0 | MONOIN Signal to Left Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 6:4 | MI2LOVOL | 101<br>(-9dB) | MONOIN Signal to Left Mixer Volume<br>000 = +6dB<br>… (3dB steps)<br>111 = -15dB |

**Table 7 Left Output Mixer Control**

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R36 (24h) Right Mixer (1) | 8 | LD2RO | 0 | Left DAC to Right Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 7 | MI2RO | 0 | MONOIN Signal to Right Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 6:4 | MI2ROVOL | 101 (-9dB) | MONOIN Signal to Right Mixer Volume<br>000 = +6dB<br>… (3dB steps)<br>111 = -15dB |
| R37 (25h) Right Mixer (2) | 8 | RD2RO | 0 | Right DAC to Right Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 7 | RI2RO | 0 | LINEINR Signal to Right Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 6:4 | RI2ROVOL | 101 (-9dB) | LINEINR Signal to Right Mixer Volume<br>000 = +6dB<br>… (3dB steps)<br>111 = -15dB |

**Table 8 Right Output Mixer Control**

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R38 (26h) Mono Mixer (1) | 8 | LD2MO | 0 | Left DAC to Mono Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 7 | LI2MO | 0 | LINEINL Signal to Mono Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 6:4 | LI2MOVOL | 101 (-9dB) | LINEINL Signal to Right Mono Volume<br>000 = 0dB<br>… (3dB steps)<br>111 = -21dB |
| R39 (27h) Mono Mixer (2) | 8 | RD2MO | 0 | Right DAC to Mono Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 7 | RI2MO | 0 | LINEINR Signal to Mono Mixer<br>0 = Disable (Mute)<br>1 = Enable Path |
| | 6:4 | RI2MOVOL | 101 (-9dB) | LINEINR Signal to Mono Mixer Volume<br>000 = 0dB<br>… (3dB steps)<br>111 = -21dB |

**Table 9 Mono Output Mixer Control**

**Note:**

The mono mixer has half the gain of the left and right mixers (i.e. 6dB less), to ensure that the left and right channels can be mixed to mono without clipping.

## DIFFERENTIAL MONO LINE-IN

The WM8955BL can take either a single-ended or a differential mono signal and mix it into the LOUT1/2 and ROUT1/2 outputs. In both cases, LINEINL and LINEINR still remain available as stereo line-in. Differential mono input mode is enabled by setting the DMEN bit, as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R38 (26h) Mono Mixer (1) | 0 | DMEN | 0 | Differential mono line-in enable<br>0 = Single-ended line-in from MONOIN+<br>1 = Differential line-in |

**Table 10 Differential Mono Line-in Enable**

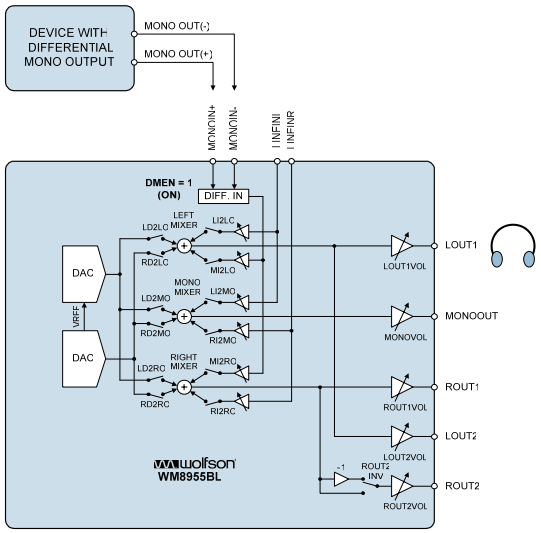



**Figure 8 Differential Mono Line-in Configuration (DMEN=1)**

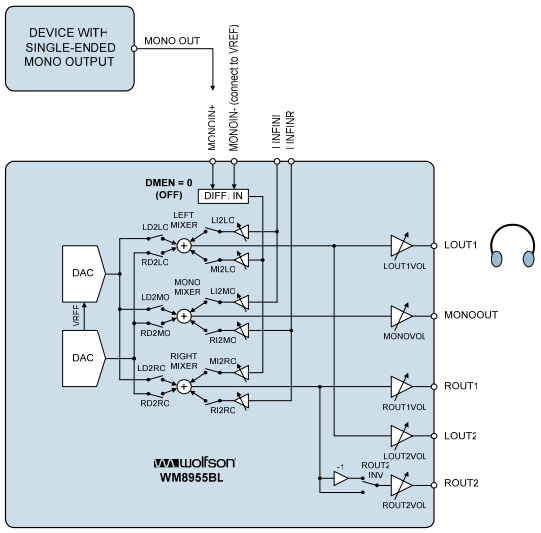



**Figure 9 Single-ended Mono Line-in Configuration (DMEN=0)**

# ANALOGUE OUTPUTS

## ENABLING THE OUTPUTS

Each analogue output of the WM8955BL can be separately enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

Outputs can be enabled at any time, except when the WM8955BL is in OFF mode, as this may cause pop noise (see Minimising Pop Noise at the Analogue Outputs)

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R26 (1Ah) Power Management (2) | 6 | LOUT1 | 0 | 0 = LOUT1 disabled<br>1 = LOUT1 enabled |
| | 5 | ROUT1 | 0 | 0 = ROUT1 disabled<br>1 = ROUT1 enabled |
| | 4 | LOUT2 | 0 | 0 = LOUT2 disabled<br>1 = LOUT2 enabled |
| | 3 | ROUT2 | 0 | 0 = ROUT2 disabled<br>1 = ROUT2 enabled |
| | 2 | MONO | 0 | 0 = MONOOUT disabled<br>1 = MONOOUT enabled |
| | 1 | OUT3 | 0 | 0 = OUT3 disabled<br>1 = OUT3 enabled |

**Table 11 Analogue Output Control**

Whenever an analogue output is disabled, it remains connected to VREF through an internal resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using the VROI bit in register 27. The default is low (1.5kΩ), so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 40kΩ.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R27 (1Bh) Additional (3) | 6 | VROI | 0 | VREF to analogue output resistance<br>0: 1.5 kΩ<br>1: 40 kΩ |

**Table 12 Disabled Outputs to VREF Resistance**

## THERMAL SHUTDOWN

The earpiece and headphone outputs can drive very large currents. To protect the WM8955BL from overheating, a thermal shutdown circuit is included. If the device temperature reaches approximately $150^0$C and the thermal shutdown circuit is enabled (TSDEN = 1) then the output amplifiers (outputs OUT1L/R, OUT2L/R & OUT3) will be disabled.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R23 (17h) Additional (1) | 8 | TSDEN | 0 | Thermal Shutdown Enable<br>0 : thermal shutdown disabled<br>1 : thermal shutdown enabled |

**Table 13 Thermal Shutdown**

### LOUT1/ROUT1 OUTPUTS

The LOUT1 and ROUT1 pins can drive a 16Ω or 32Ω headphone or a line output (see Headphone Output and Line Output sections, respectively). The signal volume on LOUT1 and ROUT1 can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum gain) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

The analogue outputs have a zero cross detect feature to minimize audible clicks and zipper noise when on gain changes (i.e. the updating of the gain value is delayed until the signal passes through zero). By default, this includes a time-out function, which forces the gain to update if no zero crossing occurs within a certain period of time.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R2 (02h) LOUT1 Volume | 6:0 | LOUT1VOL | 1111001 (0dB) | LOUT1 Volume<br>1111111 = +6dB<br>… (80 steps)<br>0110000 = -67dB<br>0101111 to 0000000 = Analogue MUTE |
| | 7 | LO1ZC | 0 | LOUT1 zero cross enable<br>1 = Change gain on zero cross only<br>0 = Change gain immediately |
| | 8 | LO1VU | 0 | Left Volume Update<br>0 = Store LOUT1VOL in intermediate latch (no gain change)<br>1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch) |
| R3 (03h) ROUT1 Volume | 6:0 | ROUT1VOL | 1111001 (0dB) | ROUT1 Volume<br>Similar to LOUT1VOL |
| | 7 | RO1ZC | 0 | ROUT1 zero cross enable<br>Similar to LO1ZC |
| | 8 | RO1VU | 0 | Right Volume Update<br>0 = Store ROUT1VOL in intermediate latch (no gain change)<br>1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL) |
| R23 (17h) | 0 | TOEN | 1 | Time-out enable for zero-cross detectors<br>0 = time-out disabled (i.e. gains are never updated if there is no zero crossing)<br>1 = time-out enabled |

**Table 14 LOUT1/ROUT1 Volume Control**

### LOUT2/ROUT2 OUTPUTS

The LOUT2 and ROUT2 output pins are essentially similar to LOUT1 and ROUT1, but they are independently controlled and can drive an 32Ω BTL earpiece. For BTL drive, the ROUT2 signal must be inverted (ROUT2INV = 1), so that the left and right channel are mixed to mono in the earpiece [L-(-R) = L+R].

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R40 (28h) LOUT2 Volume | 6:0 | LOUT2VOL | 1111001 (0dB) | similar to LOUT1VOL |
| | 7 | LO2ZC | 0 | Left zero cross enable<br>1 = Change gain on zero cross only<br>0 = Change gain immediately |
| | 8 | LO2VU | 0 | similar to LO1VU |
| R41 (29h) ROUT2 Volume | 6:0 | ROUT2VOL | 1111001 (0dB) | similar to ROUT1VOL |
| | 7 | RO2ZC | 0 | Right zero cross enable<br>1 = Change gain on zero cross only<br>0 = Change gain immediately |
| | 8 | RO2VU | 0 | similar to RO1VU |
| R23 (17h) | 0 | TOEN | 1 | as for LOUT1 / ROUT1 |
| R24 (18h) Additional (2) | 4 | ROUT2INV | 0 | ROUT2 Invert<br>0 = No Inversion (0° phase shift)<br>1 = Signal inverted (180° phase shift) |

**Table 15 LOUT2/ROUT2 Control**

### MONO OUTPUT

The MONOOUT pin can drive a mono line output. The signal volume on MONOOUT can be adjusted under software control by writing to MONOOUTVOL.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R42 (2Ah) MONOOUT Volume | 6:0 | MONOOUT VOL | 1111001 (0dB) | MONOOUT Volume<br>1111111 = +6dB<br>… (80 steps)<br>0110000 = -67dB<br>0101111 to 0000000 = Analogue MUTE |
| | 7 | MOZC | 0 | MONOOUT zero cross enable<br>1 = Change gain on zero cross only<br>0 = Change gain immediately |
| R23 (17h) | 0 | TOEN | 1 | as for LOUT1 / ROUT1 |

**Table 16 MONOOUT Volume Control**

### OUT3 OUTPUT

The OUT3 pin can drive a 16Ω or 32Ω headphone or a line output or be used as a DC reference for a headphone output. It can be selected to either drive out an inverted ROUT1 or inverted MONOOUT for e.g. an earpiece drive between OUT3 and LOUT1 or differential output between OUT3 and MONOOUT.

OUT3SW selects the mode of operation required.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R24 (18h) Additional (2) | 8:7 | OUT3SW | 00 | OUT3 select<br>00 : VREF<br>01 : ROUT1<br>10 : MONOOUT<br>11 : right mixer output |

**Table 17 OUT3 Select**

## DIGITAL AUDIO INTERFACE

The digital audio interface is used for feeding audio data into the WM8955BL. It uses three pins:

- DACDAT: DAC data input
- DACLRC: DAC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and DACLRC can be outputs when the WM8955BL operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- $I^2S$
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

### MASTER AND SLAVE MODE OPERATION

The WM8955BL can be configured as either a master or slave mode device. As a master device the WM8955BL generates BCLK and DACLRC and thus controls sequencing of the data transfer on DACDAT. In slave mode, the WM8955BL responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the MS control bit. Master and slave modes are illustrated below.

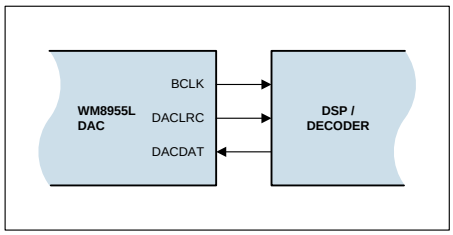



**Figure 10 Master Mode**

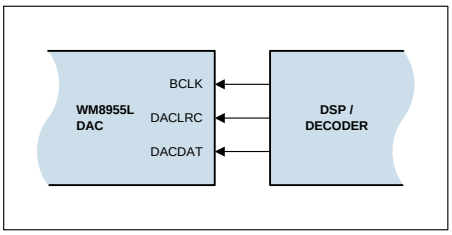



**Figure 11 Slave Mode**

### AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a DACLRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each DACLRC transition.

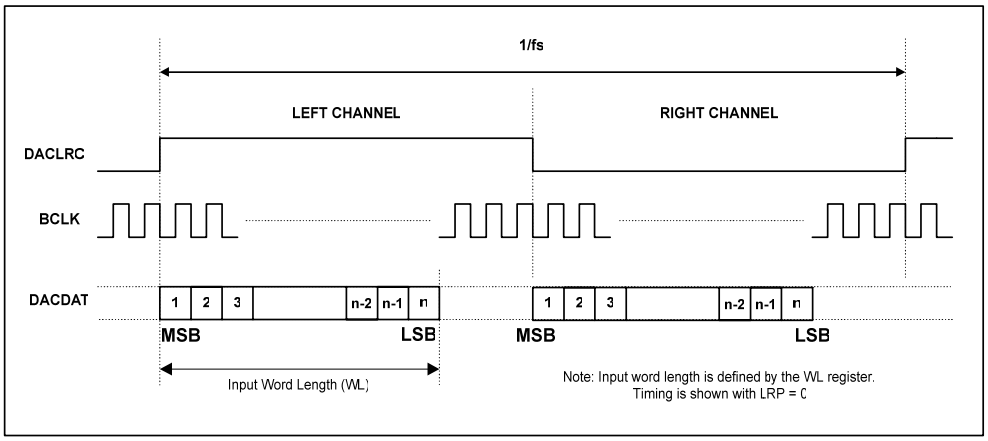



**Figure 12 Left Justified Audio Interface (assuming n-bit word length)**

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a DACLRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each DACLRC transition.

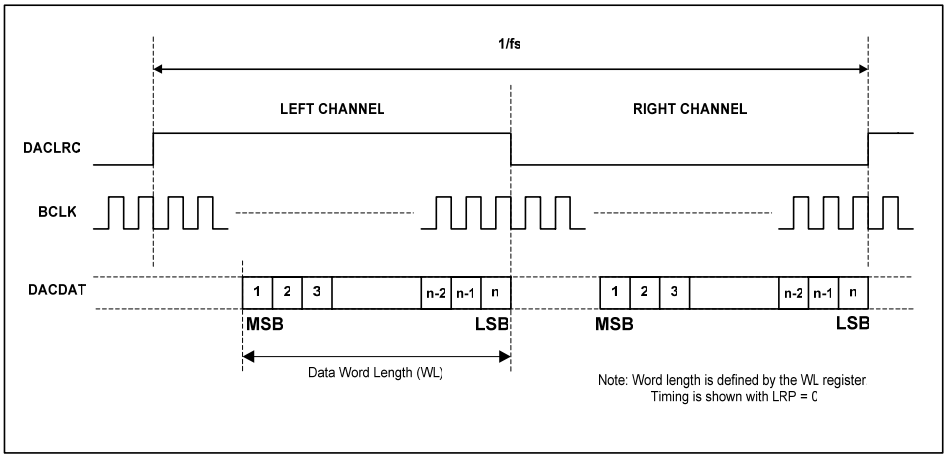



**Figure 13 Right Justified Audio Interface (assuming n-bit word length)**

In $I^2S$ mode, the MSB is available on the second rising edge of BCLK following a DACLRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

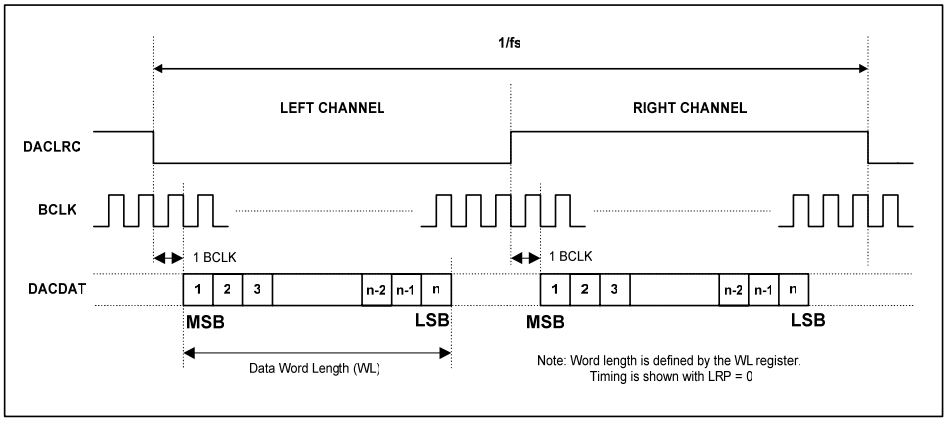



**Figure 14 $I^2S$ Justified Audio Interface (assuming n-bit word length)**

In DSP mode, the left channel MSB is available on either the first or second rising edge of BCLK (selectable by LRP) following a rising edge of DACLRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

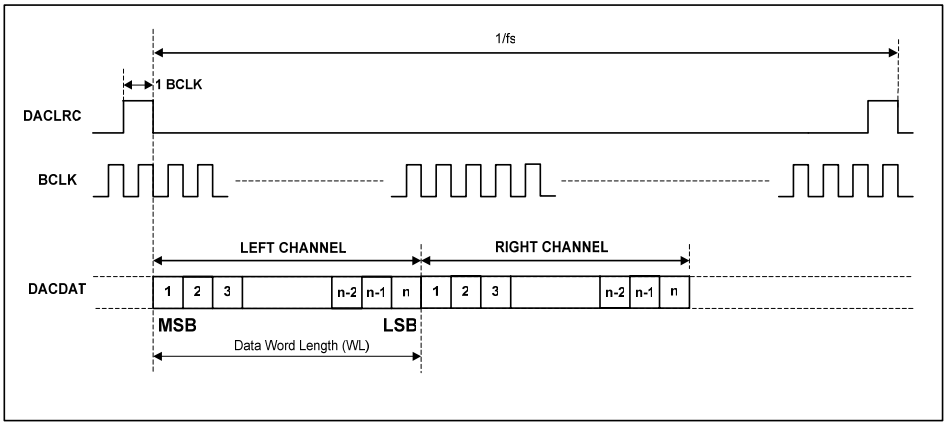



**Figure 15 DSP Mode Audio Interface (Mode A; LRP = 0)**

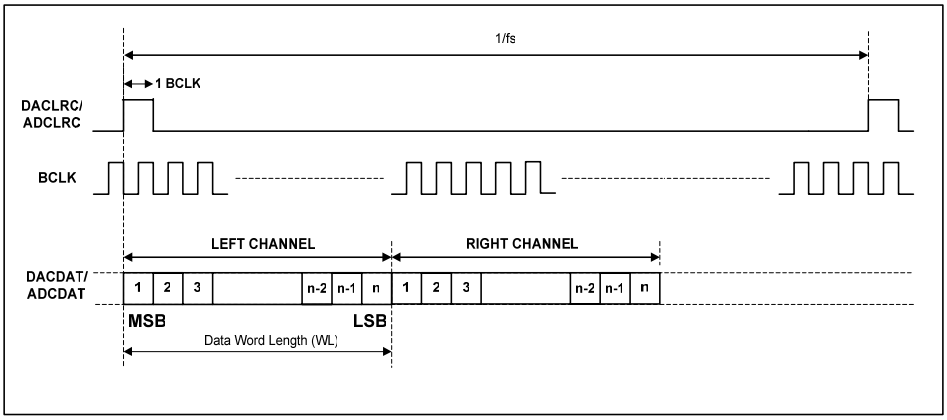



**Figure 16 DSP Mode Audio Interface (Mode B; LRP = 1)**

## AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|---|---|---|---|---|---|
| R7 (07h)<br>Digital Audio Interface Format | 1:0 | FORMAT | 10 | Audio Data Format Select<br>11 = DSP Mode<br>10 = $I^2S$ Format<br>01 = Left justified<br>00 = Right justified | |
| | 3:2 | WL | 10 | Audio Data Word Length<br>11 = 32 bits (see Note)<br>10 = 24 bits<br>01 = 20 bits<br>00 = 16 bits | |
| | 4 | LRP | 0 | $I^2S$, LJ, RJ Formats<br>1: Invert LRCLK polarity<br>0: Normal LRCLK polarity | DSP Format<br>1: MSB available on 1st BCLK rising edge after LRC rising edge<br>0: MSB available on 2nd BCLK rising edge after LRC rising edge |
| | 5 | LRSWAP | 0 | Swap Left and Right Channels<br>0: No swap (L to L, R to R)<br>1: Swap (L to R, R to L) | |
| | 6 | MS | 0 | Master / Slave Mode Control<br>1: Master Mode<br>0: Slave Mode | |
| | 7 | BCLKINV | 0 | BCLK Invert<br>1: BCLK inverted<br>0: BCLK not inverted | |

**Table 18 Audio Data Format Control**

**Note:**
Right Justified mode does not support 32-bit data. If WL=11 in Right justified mode, the actual word length will be 24 bits.

## MASTER CLOCK AND PHASE LOCKED LOOP

The WM8955BL has an on-chip phase-locked loop (PLL) circuit that can be used to:

- generate a master clock for the WM8955BL audio function from another external clock, e.g. in telecoms applications.

The PLL circuit is shown below.

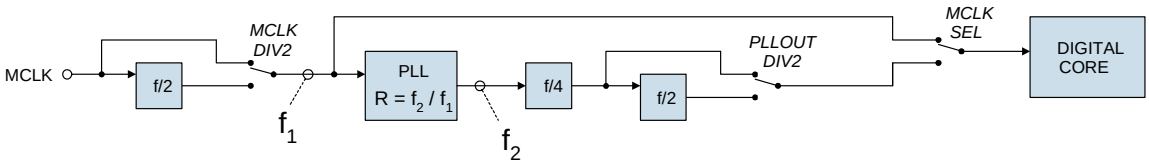



**Figure 17 PLL Circuit**

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R8 (08h) Sample Rates | 6 | MCLKDIV2 | 0 | MCLK Divide by 2<br>0: Divide disabled<br>1: Divide enabled |
| R43 (2Bh) Clocking and PLL | 8 | MCLKSEL | 0 | Select internal master clock<br>0: from MCLK pin<br>1: from PLL (make sure PLLEN=1) |
| | 5 | PLLOUTDIV2 | 0 | PLL Output Divide by 2<br>0: Divide disabled<br>1: Divide enabled |
| | 4 | PLL_RB | 0 | 0: PLL held in reset<br>1: PLL running (if PLLEN=1) |
| | 3 | PLLEN | 0 | PLL Enable<br>0: PLL disabled; 1: PLL enabled. |

**Table 19 PLL and Clocking Control**

The PLL frequency ratio R = $f_2/f_1$ (see Figure 17) can be set using K and N in registers 44 (2Ch) to 46 (2Eh):

N = int (R)

K = int ($2^{22}$ (R-N))

Example:

MCLK = 12MHz required clock = 12.288MHz

R should be chosen to ensure 5<N<13. There is a divide by 4 and selectable divide by 2 after the PLL which should be set to meet this requirement. Enabling the divide by 2 sets the required $f_2$ = 8x 12.288MHz = 98.304MHz.

R = 98.304/12 = 8.192

N = intR = 8

K = int ($2^{22}$ x (8.192-8)) = 805306 = C49BAh.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R44 (2Ch) PLL Control (1) | 8:5 | N | 1000 | Integer part of PLL input/output frequency ratio. Use values greater than 5 and less than 13. |
| | 3:0 | K [21:18] | 0011 | Fractional part of PLL input/output frequency ratio (treat as one 22-digit binary number) |
| R45 (2Dh) PLL Control (2) | 8:0 | K [17:9] | 024h | |
| R46 (2Eh) PLL Control (3) | 8:0 | K [8:0] | 1BAh | |
| R59 (3Bh) | 7 | KEN | 0 | 0: Fractional part (K) disabled<br>1: K enabled |

**Table 20 PLL Frequency Ratio Control**

The PLL performs best when $f_2$ is around 90MHz. Its stability peaks at N=8. Some example settings are shown below.

| MCLK (MHz) | DESIRED OUTPUT (MHz) | F2 (MHz) | MCLK DIV2 | PLL OUT DIV2 | R | F2 (Hex) | K (Hex) |
|---|---|---|---|---|---|---|---|
| 11.91 | 11.2896 | 90.3168 | 0 | 1 | 7.5833 | 7 | 25545C |
| 11.91 | 12.288 | 98.304 | 0 | 1 | 8.2539 | 8 | 103FF6 |
| 12 | 11.2896 | 90.3168 | 0 | 1 | 7.5264 | 7 | 21B089 |
| 12 | 12.288 | 98.304 | 0 | 1 | 8.192 | 8 | C49BA |
| 13 | 11.2896 | 90.3168 | 0 | 1 | 6.9474 | 6 | 3CA2F4 |
| 13 | 12.288 | 98.304 | 0 | 1 | 7.5618 | 7 | 23F548 |
| 14.4 | 11.2896 | 90.3168 | 0 | 1 | 6.272 | 6 | 116872 |
| 14.4 | 12.288 | 98.304 | 0 | 1 | 6.8267 | 6 | 34E818 |
| 19.2 | 11.2896 | 90.3168 | 1 | 1 | 9.408 | 9 | 1A1CAC |
| 19.2 | 12.288 | 98.304 | 1 | 1 | 10.24 | A | F5C28 |
| 19.68 | 11.2896 | 90.3168 | 1 | 1 | 9.1785 | 9 | B6D22 |
| 19.68 | 12.288 | 98.304 | 1 | 1 | 9.9902 | 9 | 3F6017 |
| 19.8 | 11.2896 | 90.3168 | 1 | 1 | 9.1229 | 9 | 7DDCA |
| 19.8 | 12.288 | 98.304 | 1 | 1 | 9.9297 | 9 | 3B8023 |
| 24 | 11.2896 | 90.3168 | 1 | 1 | 7.5264 | 7 | 21B089 |
| 24 | 12.288 | 98.304 | 1 | 1 | 8.192 | 8 | C49BA |
| 26 | 11.2896 | 90.3168 | 1 | 1 | 6.9474 | 6 | 3CA2F4 |
| 26 | 12.288 | 98.304 | 1 | 1 | 7.5618 | 7 | 23F548 |
| 27 | 11.2896 | 90.3168 | 1 | 1 | 6.6901 | 6 | 2C2B30 |
| 27 | 12.288 | 98.304 | 1 | 1 | 7.2818 | 7 | 12089E |

**Table 21 PLL Frequency Examples**

## AUDIO SAMPLE RATES

The WM8955BL supports a wide range of master clock frequencies and can generate many commonly used audio sample rates directly from the master clock.

There are two clocking modes:

- 'Normal' mode supports master clocks of $128f_s$, $192f_s$, $256f_s$, $384f_s$, and their multiples
- USB mode supports 12MHz or 24MHz master clocks. This mode is intended for use in systems with a USB interface, and can run without a PLL.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R8 (08h)<br>Sample Rates | 0 | USB | 0 | Clocking Mode Select<br>1: USB Mode<br>0: 'Normal' Mode |
| | 5:1 | SR [4:0] | 00000 | Sample Rate Control |
| | 6 | MCLK DIV2 | 0 | MCLK Divide by 2<br>0: Divide disabled<br>1: Divide enabled |
| | 7 | BCLKDIV2 | 0 | Divide BITCLK output by 2<br>(use only in USB master mode, i.e. when USB=1, MS=1)<br>1 = BCLK is divided by 2 (Note 1)<br>0 = BCLK is not divided |

**Table 22 Clocking and Sample Rate Control**

**Note:**

1. With BCLKDIV2=1, the LRCLK output produces a non-50:50 duty cycle if BCLK/LRCLK is not an even integer.

The clocking of the WM8955BL is controlled using the MCLKDIV2, USB, and SR control bits. Setting the MCLKDIV2 bit divides MCLK by two internally. The USB bit selects between 'Normal' and USB mode. Each combination of the SR4 to SR0 control bits selects one MCLK division ratio and hence one sample rate (see Table 23). The digital filter characteristics are automatically adjusted to suit the MCLK and sample rate selected (see Digital Filter Characteristics).

Since all sample rates are generated by dividing MCLK, their accuracy depends on the accuracy of MCLK. If MCLK changes, the sample rates change proportionately. Note that some sample rates (e.g. 44.1kHz in USB mode) are approximated, i.e. they differ from their target value by a very small amount. This is not audible, as the maximum deviation is only 0.27% (8.0214kHz instead of 8kHz in USB mode – for comparison, a half-tone step corresponds to a 5.9% change in pitch).

| MCLK MCLKDIV2=0 | MCLK MCLKDIV2=1 | DAC SAMPLE RATE | USB | SR [4:0] | FILTER TYPE | BCLK (MS=1) |
|---|---|---|---|---|---|---|
| **'Normal' Clock Mode ('*' indicates backward compatibility with WM8711 and WM8721)** | | | | | | |
| 12.288MHz | 24.576MHz | 8 kHz (MCLK/1536) | 0 | 00010 * | 1 | MCLK/4 |
| | | 12 kHz (MCLK/1024) | 0 | 01000 | 1 | MCLK/4 |
| | | 16 kHz (MCLK/768) | 0 | 01010 | 1 | MCLK/4 |
| | | 24 kHz (MCLK/512) | 0 | 11100 | 1 | MCLK/4 |
| | | 32 kHz (MCLK/384) | 0 | 01100 * | 1 | MCLK/4 |
| | | 48 kHz (MCLK/256) | 0 | 00000 * | 1 | MCLK/4 |
| | | 96 kHz (MCLK/128) | 0 | 01110 * | 3 | MCLK/2 |
| 11.2896MHz | 22.5792MHz | 8.0182 kHz (MCLK/1408) | 0 | 10010 | 1 | MCLK/4 |
| | | 11.025 kHz (MCLK/1024) | 0 | 11000 | 1 | MCLK/4 |
| | | 22.05 kHz (MCLK/512) | 0 | 11010 | 1 | MCLK/4 |
| | | 44.1 kHz (MCLK/256) | 0 | 10000 * | 1 | MCLK/4 |
| | | 88.2 kHz (MCLK/128) | 0 | 11110 * | 3 | MCLK/2 |
| 18.432MHz | 36.864MHz | 8 kHz (MCLK/2304) | 0 | 00011 * | 1 | MCLK/6 |
| | | 12 kHz (MCLK/1536) | 0 | 01001 | 1 | MCLK/6 |
| | | 16 kHz (MCLK/1152) | 0 | 01011 | 1 | MCLK/6 |
| | | 24 kHz (MCLK/768) | 0 | 11101 | 1 | MCLK/6 |
| | | 32 kHz (MCLK/576) | 0 | 01101 * | 1 | MCLK/6 |
| | | 48 kHz (MCLK/384) | 0 | 00001 * | 1 | MCLK/6 |
| | | 96 kHz (MCLK/192) | 0 | 01111 * | 3 | MCLK/3 |
| 16.9344MHz | 33.8688MHz | 8.0182 kHz (MCLK/2112) | 0 | 10011 * | 1 | MCLK/6 |
| | | 11.025 kHz (MCLK/1536) | 0 | 11001 | 1 | MCLK/6 |
| | | 22.05 kHz (MCLK/768) | 0 | 11011 | 1 | MCLK/6 |
| | | 44.1 kHz (MCLK/384) | 0 | 10001 * | 1 | MCLK/6 |
| | | 88.2 kHz (MCLK/192) | 0 | 11111 * | 3 | MCLK/3 |
| **USB Mode (assumes BCLKDIV2=0. '*' indicates backward compatibility with WM8711 and WM8721)** | | | | | | |
| 12.000MHz | 24.000MHz | 8 kHz (MCLK/1500) | 1 | 00010 * | 0 | MCLK |
| | | 11.0259 kHz (MCLK/1088) | 1 | 11001 | 1 | MCLK |
| | | 12kHz (MCLK/1000) | 1 | 01000 | 0 | MCLK |
| | | 16kHz (MCLK/750) | 1 | 01010 | 0 | MCLK |
| | | 22.0588 kHz (MCLK/544) | 1 | 11011 | 1 | MCLK |
| | | 24kHz (MCLK/500) | 1 | 11100 | 0 | MCLK |
| | | 32 kHz (MCLK/375) | 1 | 01100 * | 0 | MCLK |
| | | 44.118 kHz (MCLK/272) | 1 | 10001 * | 1 | MCLK |
| | | 48 kHz (MCLK/250) | 1 | 00000 * | 0 | MCLK |
| | | 88.235kHz (MCLK/136) | 1 | 11111 * | 3 | MCLK |
| | | 96 kHz (MCLK/125) | 1 | 01110 * | 2 | MCLK |

**Table 23 Master Clock and Sample Rates**

# CONTROL INTERFACE

## SELECTION OF CONTROL MODE

The WM8955BL is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are register bits, corresponding to the 9 bits in each control register. The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE pin selects the interface format.

| MODE | INTERFACE FORMAT |
|---|---|
| Low | 2 wire |
| High | 3 wire |

**Table 24 Control Interface Mode Selection**

## 3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB latches in a complete control word consisting of the last 16 bits.

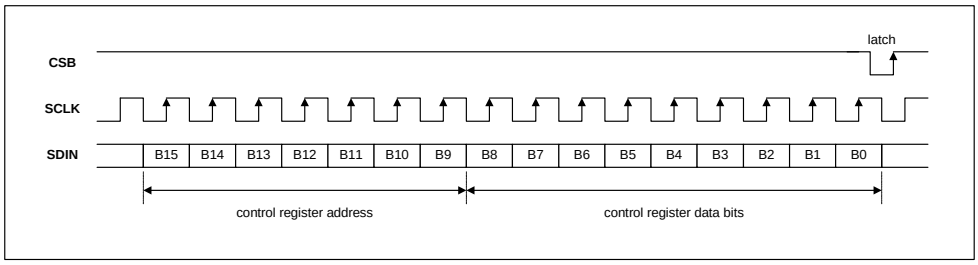



**Figure 18 3-Wire Serial Control Interface**

## 2-WIRE SERIAL CONTROL MODE

The WM8955BL supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8955BL).

The WM8955BL operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8955BL and the R/W bit is '0', indicating a write, then the WM8955BL responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8955BL returns to the idle condition and wait for a new start condition and valid address.

Once the WM8955BL has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8955BL register address plus the first bit of register data). The WM8955BL then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8955BL acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8955BL returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

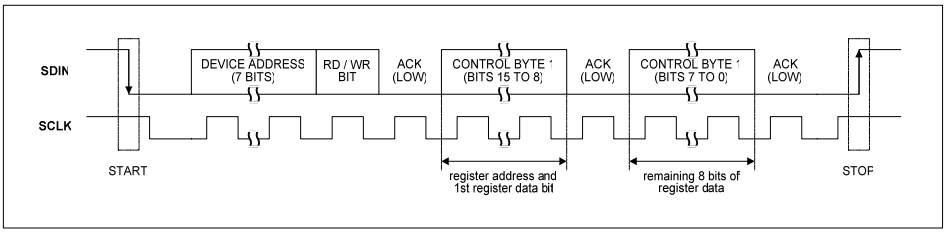



**Figure 19 2-Wire Serial Control Interface**

The WM8955BL has two possible device addresses, which can be selected using the CSB pin.

| CSB STATE | DEVICE ADDRESS |
|---|---|
| Low | 0011010 |
| High | 0011011 |

**Table 25 2-Wire MPU Interface Address Selection**

## POWER SUPPLIES

The WM8955BL can use up to four separate power supplies:

- AVDD / AGND: Analogue supply, powers all analogue functions except the headphone drivers. AVDD can range from 1.8V to 3.6V and has the most significant impact on overall power consumption (except for power consumed in the headphone). A large AVDD slightly improves audio quality.
- HPVDD / HPGND: Headphone supply, powers the headphone drivers. HPVDD is normally tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. If HPVDD is lower than AVDD, the output signal may be clipped.
- DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD can range from 1.42V to 3.6V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD.
- DBVDD: Digital buffer supply, powers the audio and control interface buffers. This makes it possible to run the digital core at very low voltages, saving power, while interfacing to other digital devices using a higher voltage. DBVDD draws much less power than DCVDD, and has no effect on audio quality. The return path for DBVDD is DGND, which is shared with DCVDD.

It is possible to use the same supply voltage on all four. However, digital and analogue supplies should be routed and decoupled separately to keep digital switching noise out of the analogue signal paths.

## POWER MANAGEMENT

The WM8955BL has two control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information)

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R25 (19h) Power Management (1) | 8:7 | VMIDSEL | 00 | VMID resistor divider select<br>00 – VMID disabled<br>01 – 50kΩ divider enabled<br>10 – 500kΩ divider enabled<br>11 – 5kΩ divider enabled (for fast start-up) |
| | 6 | VREF | 0 | VREF (necessary for all other functions) |
| R26 (1Ah) Power Management (2) | 8 | DACL | 0 | DAC Left Enable<br>0=off<br>1=on |
| | 7 | DACR | 0 | DAC Right Enable<br>0=off<br>1=on |
| | 6 | LOUT1 | 0 | LOUT1 Output Buffer* Enable<br>0=off<br>1=on |
| | 5 | ROUT1 | 0 | ROUT1 Output Buffer* Enable<br>0=off<br>1=on |
| | 4 | LOUT2 | 0 | LOUT2 Output Buffer* Enable<br>0=off<br>1=on |
| | 3 | ROUT2 | 0 | ROUT2 Output Buffer* Enable<br>0=off<br>1=on |
| | 2 | MOUT | 0 | MONOOUT Output Buffer and Mono Mixer Enable<br>0=off<br>1=on |
| | 1 | OUT3 | 0 | OUT3 Output Buffer Enable<br>0=off<br>1=on |
| **Note:**<br>* The left mixer is enabled when LOUT1=1 or LOUT2=1. The right mixer is enabled when ROUT1=1 or ROUT2=1. | | | | |

**Table 26 Power Management**

## STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the WM8955BL, the master clock should be stopped in Standby and OFF modes. If this is cannot be done externally at the clock source, the DIGENB bit (R25, bit 0) can be set to stop the MCLK signal from propagating into the device core. However, since setting DIGENB has no effect on the power consumption of other system components external to the WM8955BL, it is preferable to disable the master clock at its source wherever possible.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R25 (19h) Power Management (1) | 0 | DIGENB | 0 | Master clock disable<br>0: master clock enabled<br>1: master clock disabled |

**Table 27 ADC and DAC Oversampling Rate Selection**

NOTE: Before DIGENB can be set, the control bits DACL and DACR must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs and ADCs from re-starting correctly.

## OVERSAMPLING RATE

By default, the oversampling rate of the DAC digital filters is 128x. However, this can be changed to 64x by writing to the DACOSR bit. In the 64x oversampling mode, the digital filters consume less power. However, the signal-to-noise ratio is slightly reduced.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R24 (18h) Additional Control (2) | 0 | DACOSR | 0 | DAC oversample rate select<br>1 = 64x (lowest power)<br>0 = 128x (best SNR) |

**Table 28 Oversampling Rate Selection**

## SAVING POWER AT LOW SUPPLY VOLTAGES

The analogue supplies to the WM8955BL can run from 1.8V to 3.6V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. However, at lower voltages, it is possible to save power by reducing the internal bias currents used in the analogue circuitry. This is controlled as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| R23 (17h) Additional Control(1) | 7:6 | VSEL[1:0] | 11 | Analogue Bias optimization<br>00 : Lowest bias current, optimized for 1.8V<br>01 : Low bias current, optimized for 2.5V<br>10, 11 : Default bias current, optimized for 3.3V |

**Table 29 Analogue Bias Selection**

## REGISTER MAP

| REGISTER | ADDRESS (BIT 15 – 9) | REMARKS | BIT8 | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R0 (00h) | 0000000 | Reserved | 000000000 | | | | | | | | |
| R1 (01h) | 0000001 | Reserved | 000000000 | | | | | | | | |
| R2 (02h) | 0000010 | LOUT1 | LO1VU | LO1ZC | LOUT1VOL | | | | | | |
| R3 (03h) | 0000011 | ROUT1 | RO1VU | RO1ZC | ROUT1VOL | | | | | | |
| R4 (04h) | 0000100 | Reserved | 000000000 | | | | | | | | |
| R5 (05h) | 0000101 | DAC Control | 0 | DAT | 0 | 0 | 0 | DACMU | DEEMPH | | 0 |
| R6 (06h) | 0000110 | Reserved | 000000000 | | | | | | | | |
| R7 (07h) | 0000111 | Audio Interface | 0 | BCLKINV | MS | LRSWAP | LRP | WL | | FORMAT | |
| R8 (08h) | 0001000 | Sample Rates | 0 | BCLK DIV2 | MCLK DIV2 | SR | | | | | USB |
| R9 (09h) | 0001001 | Reserved | 000000000 | | | | | | | | |
| R10 (0Ah) | 0001010 | Left Gain | LDVU | LDACVOL (Right DAC Digital Volume) | | | | | | | |
| R11 (0Bh) | 0001011 | Right Gain | RDVU | RDACVOL (Right DAC Digital Volume) | | | | | | | |
| R12 (0Ch) | 0001100 | Bass | 0 | BB | BC | 0 | 0 | BASS (Bass Intensity) | | | |
| R13 (0Dh) | 0001101 | Treble | 0 | 0 | TC | 0 | 0 | TRBL (Treble Intensity) | | | |
| R14 (0Eh) | 0001110 | Reserved | 000000000 | | | | | | | | |
| R15 (0Fh) | 0001111 | Reset | writing 000000000 to this register resets all registers to their default state | | | | | | | | |
| R16 – R22 | | Reserved | 000000 | | | | | | | | |
| R23 (17h) | 0010111 | Additional (1) | TSDEN | VSEL | | DMONOMIX | | 0 | 0 | DACINV | TOEN |
| R24 (18h) | 0011000 | Additional (2) | OUT3SW | | 0 | 0 | ROUT2INV | 0 | 0 | 0 | DACOSR |
| R25 (19h) | 0011001 | Pwr Mgmt (1) | VMIDSEL | | VREF | 0 | 0 | 0 | 0 | 0 | DIGENB |
| R26 (1Ah) | 0011010 | Pwr Mgmt (2) | DACL | DACR | LOUT1 | ROUT1 | LOUT2 | ROUT2 | MOUT | OUT3 | 0 |
| R27 (1Bh) | 0011011 | Additional (3) | 0 | 0 | VROI | 0 | 0 | 0 | 0 | 0 | 0 |
| R28 – R33 | | Reserved | | | | | | | | | |
| R34 (22h) | 0100010 | Left Mix (1) | LD2LO | LI2LO | LI2LOVOL | | | 0 | 0 | 0 | 0 |
| R35 (23h) | 0100011 | Left Mix (2) | RD2LO | MI2LO | MI2LOVOL | | | 0 | 0 | 0 | 0 |
| R36 (24h) | 0100100 | Right Mix (1) | LD2RO | MI2RO | MI2ROVOL | | | 0 | 0 | 0 | 0 |
| R37 (25h) | 0100101 | Right Mix (2) | RD2RO | RI2RO | RI2ROVOL | | | 0 | 0 | 0 | 0 |
| R38 (26h) | 0100110 | Mono Mix (1) | LD2MO | LI2MO | LI2MOVOL | | | 0 | 0 | 0 | DMEN |
| R39 (27h) | 0100111 | Mono Mix (2) | RD2MO | RI2MO | RI2MOVOL | | | 0 | 0 | 0 | 0 |
| R40 (28h) | 0101000 | LOUT2 | LO2VU | LO2ZC | LOUT2VOL | | | | | | |
| R41 (29h) | 0101001 | ROUT2 | RO2VU | RO2ZC | ROUT2VOL | | | | | | |
| R42 (2Ah) | 0101010 | MONOOUT | 0 | MOZC | MONOOUTVOL | | | | | | |
| R43 (2Bh) | 0101011 | Clocking / PLL | MCLKSEL | 0 | 0 | PLLOUT DIV2 | PLL_RB | PLLEN | 0 | 0 | 0 |
| R44 (2Ch) | 0101100 | PLL Control (1) | N | | | | 0 | K [21:18] | | | |
| R45 (2Dh) | 0101101 | PLL Control (2) | K [17:9] | | | | | | | | |
| R46 (2Eh) | 0101110 | PLL Control (3) | K [8:0] | | | | | | | | |
| R59 (3Bh) | 0111011 | PLL Control (4) | 0 | KEN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## DIGITAL FILTER CHARACTERISTICS

Depending on the MCLK frequency and sample rate selected, 4 different types of digital filter can be used in the DAC, called Type 0, 1, 2 and 3 (see "Master Clock and Audio Sample Rates"). The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the following pages.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **DAC Filter Type 0 (USB mode, 250fs operation)** | | | | | |
| Passband | +/- 0.03dB | 0 | | 0.416fs | |
| | -6dB | | 0.5fs | | |
| Passband Ripple | | | | +/-0.03 | dB |
| Stopband | | 0.584fs | | | |
| Stopband Attenuation | f > 0.584fs | -50 | | | dB |
| **DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)** | | | | | |
| Passband | +/- 0.03dB | 0 | | 0.4535fs | |
| | -6dB | | 0.5fs | | |
| Passband Ripple | | | | +/- 0.03 | dB |
| Stopband | | 0.5465fs | | | |
| Stopband Attenuation | f > 0.5465fs | -50 | | | dB |

**Table 30 Digital Filter Characteristics**

| MODE | GROUP DELAY |
|---|---|
| 0 (250 USB) | 11/FS |
| 1 (256/272) | 16/FS |
| 2 (250 USB, 96k mode) | 4/FS |
| 3 (256/272, 88.2/96k mode) | 3/FS |

**Table 31 DAC Filters**

## TERMINOLOGY

Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)

Pass-band Ripple – any variation of the frequency response in the pass-band region

## DAC FILTER RESPONSES

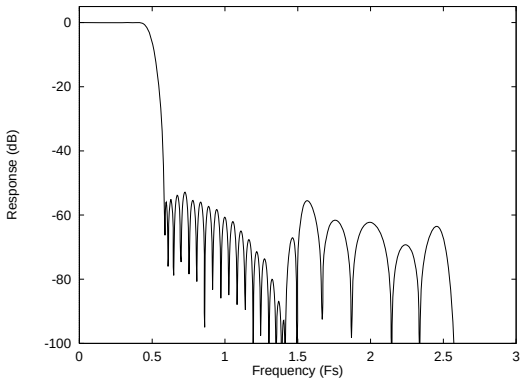



**Figure 20 DAC Filter Frequency Response – Type 0**

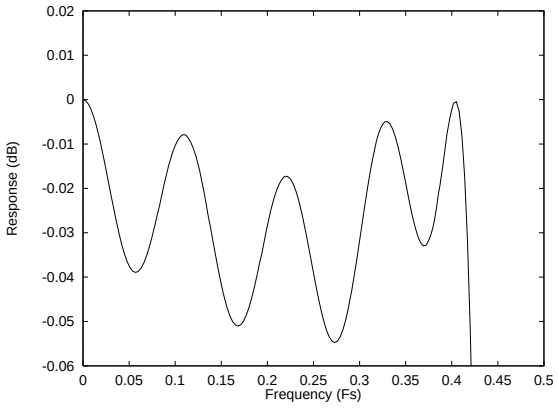



**Figure 21 DAC Filter Ripple – Type 0**

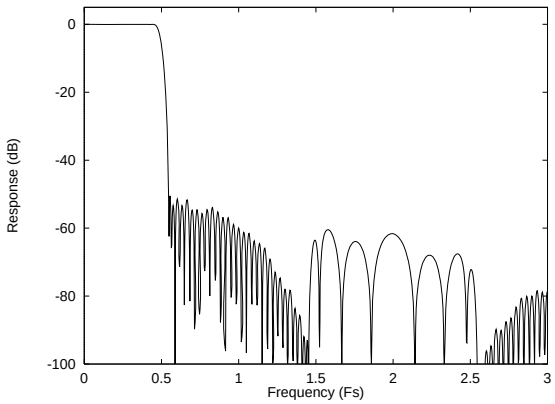



**Figure 22 DAC Filter Frequency Response – Type 1**

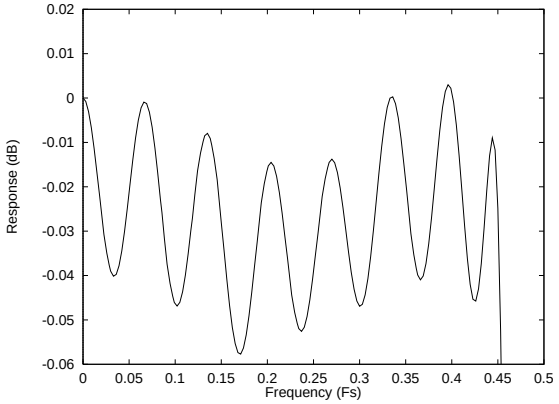



**Figure 23 DAC Filter Ripple – Type 1**

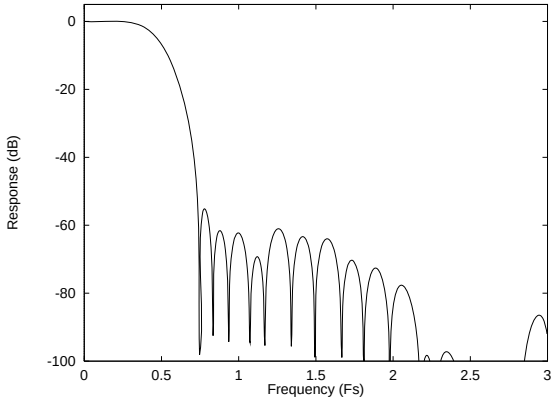



**Figure 24 DAC Filter Frequency Response – Type 2**

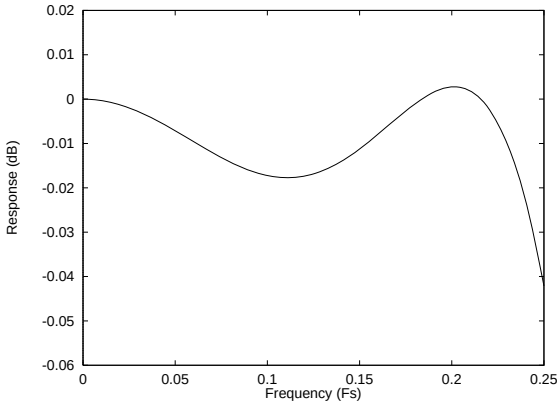



**Figure 25 DAC Filter Ripple – Type 2**

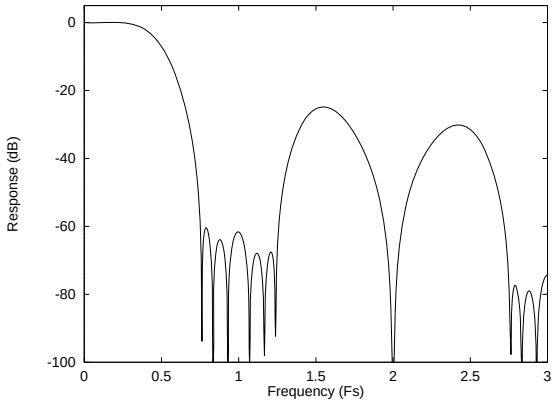



**Figure 26 DAC Filter Frequency Response – Type 3**

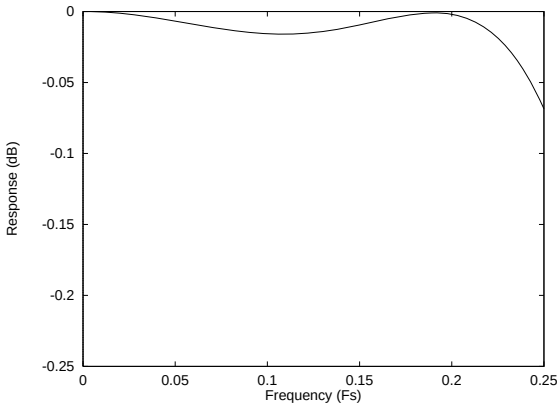
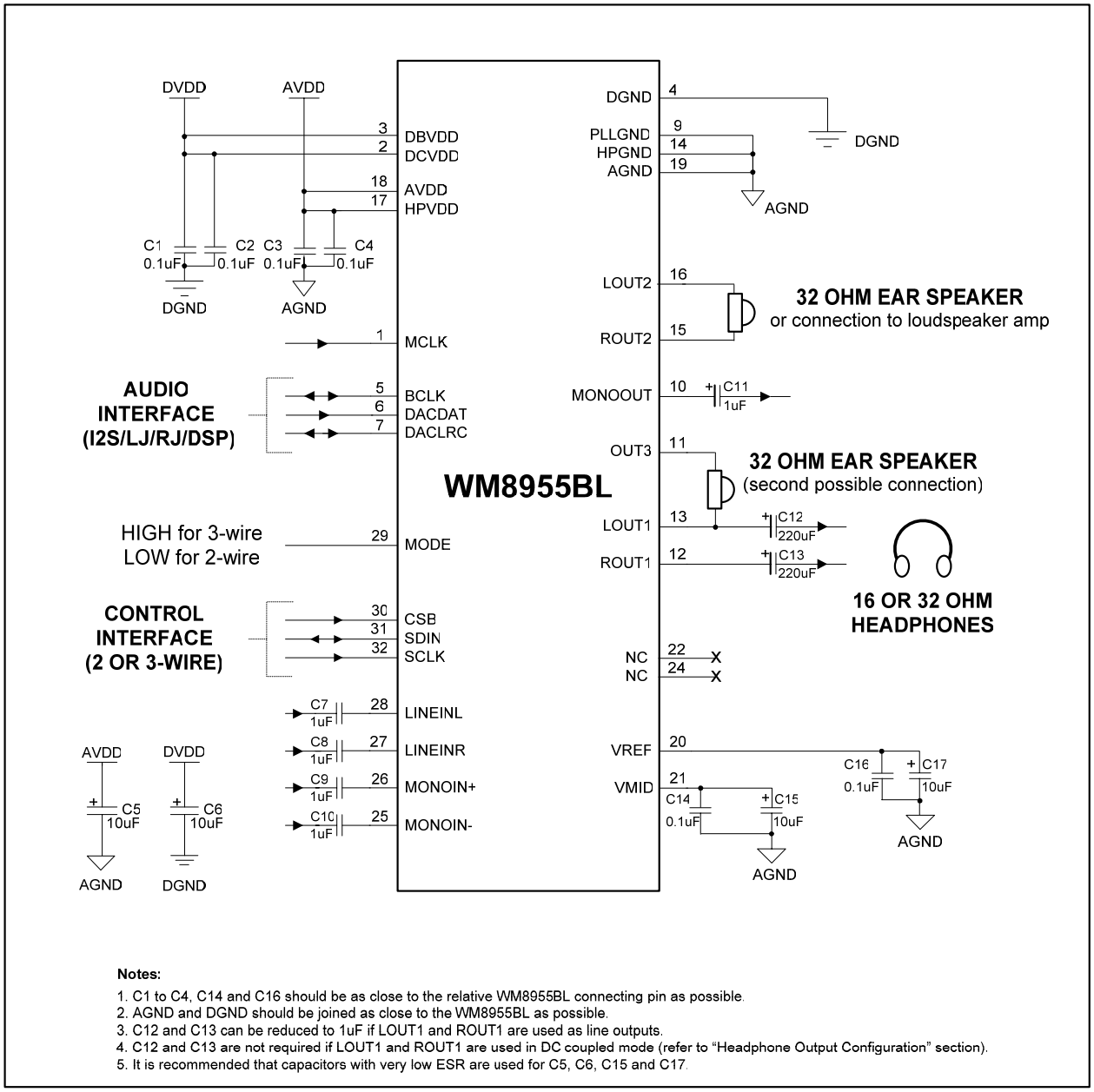



**Figure 27 DAC Filter Ripple – Type 3**

# APPLICATIONS INFORMATION

## RECOMMENDED EXTERNAL COMPONENTS




**Notes:**

1. C1 to C4, C14 and C16 should be as close to the relative WM8955BL connecting pin as possible.
2. AGND and DGND should be joined as close to the WM8955BL as possible.
3. C12 and C13 can be reduced to 1uF if LOUT1 and ROUT1 are used as line outputs.
4. C12 and C13 are not required if LOUT1 and ROUT1 are used in DC coupled mode (refer to "Headphone Output Configuration" section).
5. It is recommended that capacitors with very low ESR are used for C5, C6, C15 and C17.

**Figure 28 Recommended External Component Diagram**

## MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimise any pop or click noise when the system is powered up or down, the following procedures are recommended.

### POWER UP

- Switch on power supplies. By default the WM8955BL is in OFF Mode (i.e. only the control interface is powered up)
- Enable the reference voltage VREF by setting the WM8955BL to Standby mode. DO NOT enable any of the analogue outputs at this point.
- Allow VREF to settle. The settling time depends on the value of the capacitor connected at VMID, and the size of the resistors selected using VMIDSEL ($\tau$ = RC).
- Enable DACs, etc. as required.
- Enable outputs required.
- Set DACMU = 0 to soft-un-mute the audio DACs.

### POWER DOWN

- Set DACMU = 1 to soft-mute the audio DACs.
- Disable outputs.
- Switch off the power supplies.

## LINE OUTPUT CONFIGURATION

All the analogue outputs, LOUT1/ROUT1, LOUT2/ROUT2, and MONOOUT, can be used as line outputs. Recommended external components are shown below.

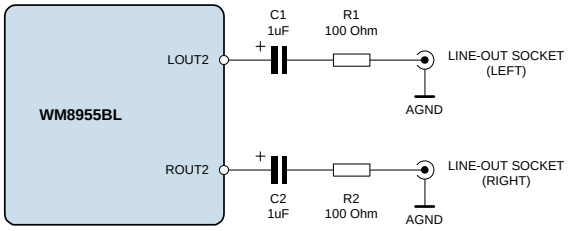



**Figure 29 Recommended Circuit for Line Output**

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, $f_c$. Assuming a 10 k$\Omega$ load and C1, C2 = 1$\mu$F:

$f_c = 1 / 2\pi (R_L+R_1) C_1 = 1 / (2\pi \times 10.1k\Omega \times 1\mu F) = 16$ Hz

Increasing the capacitance lowers $f_c$, improving the bass response. Smaller values of C1 and C2 will diminish the bass response. The function of R1 and R2 is to protect the line outputs from damage when used improperly.

## HEADPHONE OUTPUT CONFIGURATION

The analogue outputs LOUT1/ROUT1, LOUT2/ROUT2, and OUT3 can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.

Headphone Output using DC blocking capacitors

DC Coupled Headphone Output (OUT3SW = 00)

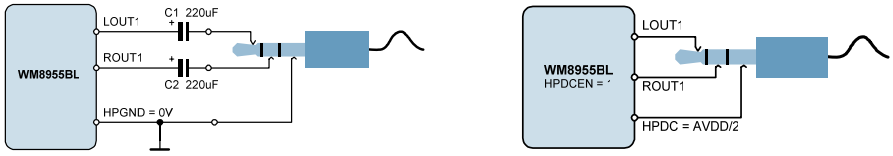



**Figure 30 Recommended Headphone Output Configurations**

When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency, $f_c$. Increasing the capacitance lowers $f_c$, improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 16Ω load and C1 = 220µF:

$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu F) = 45$ Hz

In the DC coupled configuration, the headphone "ground" is connected to the OUT3 pin, which must be enabled by setting OUT3 = 1 and OUT3SW = 00. As the OUT3 pin produces a DC voltage of AVDD/2 (=VREF), there is no DC offset between LOUT1/ROUT1 and OUT3, and therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to connect the DC coupled headphone outputs only to headphones, and not to the line input of another device. Although the built-in short circuit protection will prevent any damage to the headphone outputs, such a connection may be noisy, and may not function properly if the other device is grounded.

## EARPIECE OUTPUT CONFIGURATION

LOUT2 and ROUT2 can differentially drive a mono 32Ω earpiece as shown below.

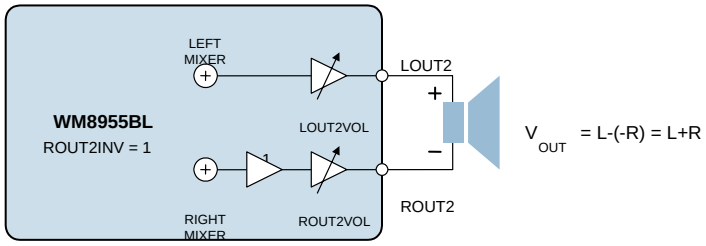
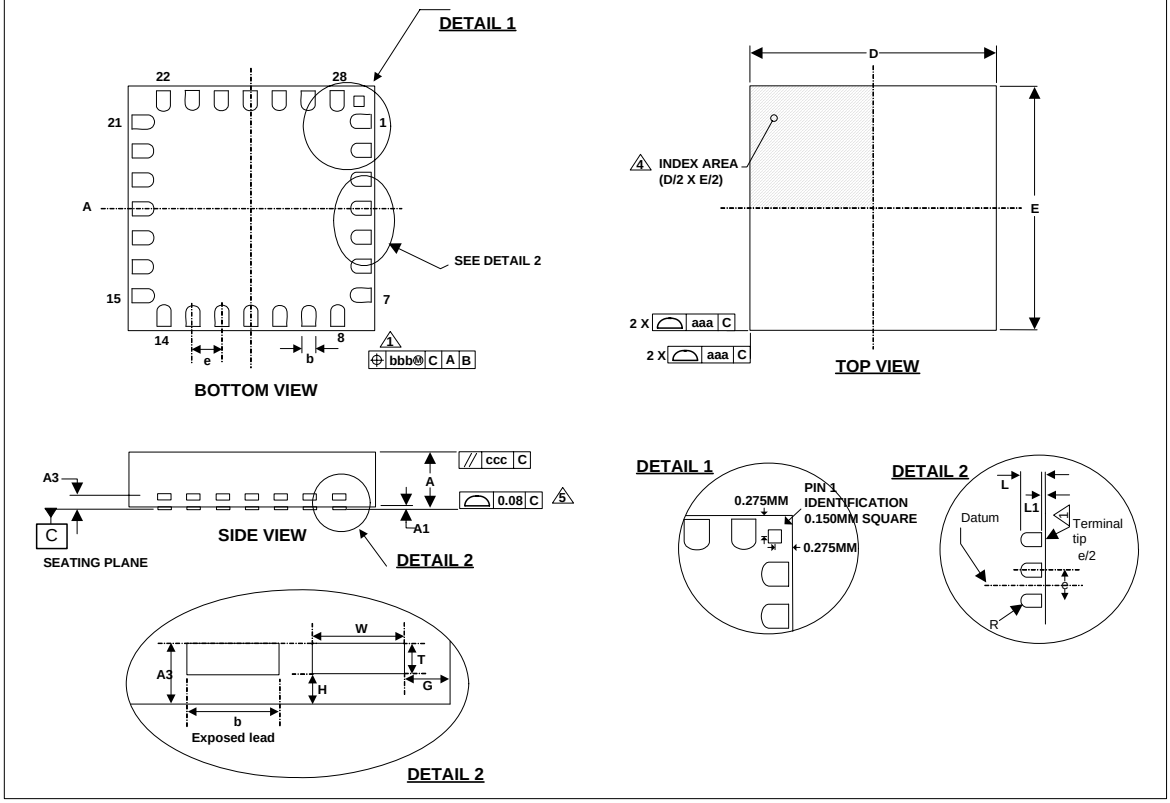



**Figure 31 Earpiece Output Connection**

The right channel is inverted by setting the ROUT2INV bit, so that the signal across the earpiece is the sum of left and right channels.

## PACKAGE DIMENSIONS

**FL: 28 PIN COL QFN PLASTIC PACKAGE 4 x 4 x 0.75 mm BODY, 0.45 mm LEAD PITCH** **DM043.F**




| Symbols | | Dimensions (mm) | | |
|---|---|---|---|---|
| | MIN | NOM | MAX | NOTE |
| A | 0.725 | 0.75 | 0.775 | |
| A1 | 0 | 0.02 | 0.05 | |
| A3 | | 0.203 REF | | |
| b | 0.18 | 0.23 | 0.28 | 1 |
| D | 3.95 | 4.00 | 4.05 | |
| E | 3.95 | 4.00 | 4.05 | |
| e | | 0.45 BSC | | |
| G | | 0.535 REF | | |
| H | | 0.100 REF | | |
| L | | 0.40 REF | | |
| L1 | | 0.05 REF | | 7 |
| T | | 0.100 REF | | |
| W | | 0.230 REF | | |
| Tolerances of Form and Position | | | | |
| aaa | | 0.15 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| REF: | | JEDEC, MO-220 | | |

NOTES:
1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VGGD-2.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULL BACK (L1) MAY BE PRESENT.
8. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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