TDK SEMICONDUCTOR CORP.

73M2921
Advanced Single Chip Modem

Advanced Information

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DESCRIPTION

The 73M2921 is a CMOS integrated circuit which provides all the modem "Data Pump" functions required to implement a V.22bis data modem. It consists of a DSP (Digital Signal Processor) core with RAM and ROM data memory, ROM instruction memory, and register mapped input/output functions including timers, interrupts, ΣΔ ADC and DAC ports and Serial Data I/O.

Once the 73M2921 has been initialized, all call progress and modem handshaking is automatic. The default conditions may be changed as required for country specific or custom applications.

The 73M2921 provides DTMF tone generation and detection, precise call progress detect and ADSI functions such as CAS tone detection.

Other features include a parallel interface control port between the host processor and the 73M2921. A synchronous serial data channel provides synchronizing clocks RXCLK and TXCLK from the modem pump to the controller.

The 73M2921 contains an oscillator and power control features.

The host controller function can be implemented with a 73M2910 communications micro controller or another commercial microcontroller (such as the 68302). The 73M2921 has been optimized to work with the 73M2910 synchronous serial port.

FEATURES

- **Automatic handshaking for all data modes**
- **Data Speeds:**
  - **V.22bis - 2400 b/s**
  - **V.22, Bell 212 - 1200 b/s**
  - **V.21, Bell 103 - 300 b/s**
  - **V.23 1200 b/s - 75 b/s**
  - **Bell 202 1200 b/s**
- **Facsimile Speeds:**
  - **V.29 - 9600, 7200 b/s**
  - **V.27ter - 4800, 2400 b/s**
  - **V.21 ch 2 - 300 b/s**
- **V.8bis applications**
- **Designed for 3.3 and 5-Volt systems.**
- **Low operating power.**
- **Speaker monitor output**
- **Provides 2 tone generators for single tone or DTMF generation**
- **Provides DTMF tone detection**
- **Provides 4 precise and 1 imprecise call progress filters and corresponding detect bits with programmable thresholds and frequencies**
- **Provides CAS tone detection for ADSI and CLASS® feature support**
- **Supports parallel (8 bit) control, and synchronous serial data I/O**
- **73M2921 provides a microcontroller interrupt**
- **Packaging: The 73M2921 is available in a QFP production package. A PGA package is available for prototyping**

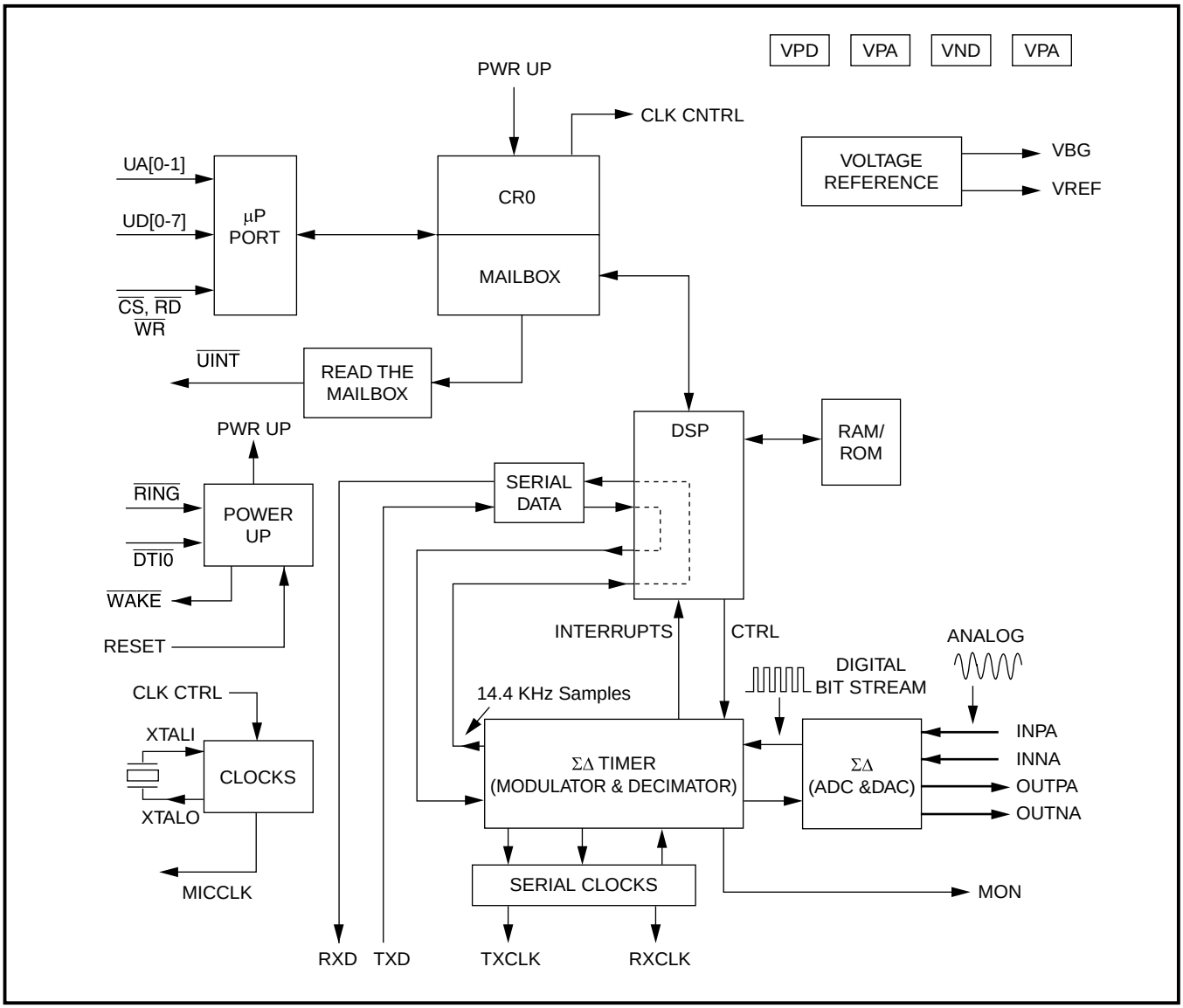


FIGURE 1 - Block Diagram

PIN DESCRIPTION

POWER

NAME	PIN	TYPE	DESCRIPTION
VPD	3, 23, 51, 82	I	DIGITAL POWER: Positive Digital Power.
VND	4, 20, 52, 74	I	DIGITAL POWER: Negative Digital Power.
VPA	29, 36	I	ANALOG POWER: Positive Analog Power.
VNA	27, 37	I	ANALOG POWER: Negative Analog Power.
VREF	32	O	VREF: Analog voltage reference for biasing of off chip analog function. Maximum output current is +/- 20µA.
VBG	33	O	BANDGAP VOLTAGE: Bandgap voltage pin used as a connection point for an external capacitor for noise reduction only.

CLOCKS AND RESETS

NAME	PIN	TYPE	DESCRIPTION
XTALI	22	I	CRYSTAL INPUT: Onboard crystal oscillator input, or the master clock input to the 73M2921 if the crystal oscillator is not used.
XTALO	21	I	CRYSTAL OUTPUT: Onboard crystal oscillator output should be left unconnected if the crystal oscillator on the 73M2921 is not used. Along with XTALI and proper loading capacitors, these pins include an inverter for use with parallel resonant mode crystals.
MICCLK	19	O	MICROCONTROLLER CLOCK: Programmable clock output for use when the system oscillator is on the 73M2921. May be used to drive the system controller. The output frequency is controlled by CR0 bits D11-D9 (MCLK [2:0]).
RESET	40	I	MASTER CHIP RESET: Active High Input with hysteresis. Resets the 73M2921 and the control registers. If not used as a reset source, this pin must be tied low.

PIN DESCRIPTION (continued)

POWER CONTROL

NAME	PIN	TYPE	DESCRIPTION
$\overline{\text{DTI0}}$	26	I	DATA TERMINAL INTERRUPT 0: Active Low Input with hysteresis. Power up signal. The action of this pin can be masked by the PSDIS[1] register bit. This pin would connect to EIA-232 connection DTR in many applications. Requires a 50KΩ external pull up.
$\overline{\text{RING}}$	24	I	RING DETECT: Active Low Input with hysteresis. Power up signal. The action of this pin can be masked by the PSDIS[0] register bit. This pin would connect to the ring detect circuitry or the control microcontroller in many applications. Requires a 50KΩ external pull up.
$\overline{\text{WAKE}}$	39	O	WAKE: Active Low Output. Indicates that a power up pin ($\overline{\text{RING}}$ or $\overline{\text{DTI0}}$) has been activated when the 73M2921 is in slave mode. The latched signal remains true until a reset of the wake function by a write to CR0 LSByte, or a chip reset. Requires a 50KΩ external pull up.

MICROCONTROLLER INTERFACE

NAME	PIN	TYPE	DESCRIPTION
$\overline{\text{CS}}$	15	I	CHIP SELECT: Active Low Input. Enables data transfers on the µP parallel interface. Requires a 50KΩ external pull up.
$\overline{\text{RD}}$	17	I	READ: Active Low Input. Read enable signals for the mailbox/control register interface.
$\overline{\text{WR}}$	16	I	WRITE: Active Low Input. Write enable signals for the mailbox/control register interface.
UA[0:1]	13-14	I	ADDRESS: Address bits that are used by the µP to communicate with the 73M2921 mailbox and CR0.
UD [0:7]	5-12	I/O	DATA: Parallel data bus for the mailbox/CR0 interface.
$\overline{\text{UINT}}$	18	O	INTERRUPT: µC interrupt Active Low Output. Used as an interrupt to the microcontroller indicating that the 73M2921 needs data or has a request for the µC. It is activated when the 73M2921 writes to the mailbox and cleared when the µC reads the mailbox LSByte. Requires a 50KΩ external pull up.

PIN DESCRIPTION (continued)

SERIAL DATA INTERFACE

NAME	PIN	TYPE	DESCRIPTION
RXCLK	45	O	RECEIVE CLOCK: Receive clock for the serial data interface. Data is transferred from the 73M2921 on the rising edge of the clocks.
TXCLK	42	O	TRANSMIT CLOCK: Transmit clock for the serial data interface. Data is transferred to the 73M2921 on the rising edge of the clocks.
RXD	44	O	RECEIVE DATA: Receive Digital Data.
TXD	41	I	TRANSMIT DATA: Transmit Digital Data.

AUXILIARY FUNCTIONS

NAME	PIN	TYPE	DESCRIPTION
MON	38	O	MONITOR: Speaker driver. PCM output under software control. See app note concerning the use of this pin.
PEXT	50	I	EXTERNAL PROGRAM ENABLE: This pin must be tied low for normal operation.

ANALOG I/O

NAME	PIN	TYPE	DESCRIPTION
INPA, INNA	34, 35	I	ANALOG INPUT: Differential analog input to a high resolution ADC.
OUTPA, OUTNA	31, 30	O	ANALOG OUTPUT: Differential analog output from a high resolution DAC.

HARDWARE REQUIREMENTS

The 73M2921 chip is designed for a single +3.3 or 5 Volt supply and for minimum power consumption (~100mW @ 3.3V). It supports power down (idle) mode via microcontroller software control. It will also accept a request for power down from the DTE via hardware control. The device operates from internal ROM/RAM, but may be configured for external ROM operation and external RAM access (for custom applications) using either the prototype or the production packages.

LINE/HYBRID INTERFACE

The 73M2921 chip provides a differential analog input and output. This interface will drive a standard Data Access Arrangement (DAA). The system controller provides additional control such as hook, phone and auxiliary relay, parallel pickup and in-use detect, and ring detect.

The Internal DAC provides a differential output signal with a maximum output swing of 1.2Vpp, capable of driving a 50KΩ load. One output can be used alone for a single ended output (with possible performance degradation).

The internal ADC has a differential input maximum of 1.2Vpp, and provides a biasing resistor to Vref for AC coupling. One input can be driven while leaving the other floating for a single ended input (with possible performance degradation). The signal passes through a passive anti-aliasing filter.

POWER CONTROL

The power control circuit determines the state of the 73M2921 when powered down, and the means for waking up the chip. The function is related to the chip and DSP reset functions and is controlled by various input pins and register bits. The chip pins are $\overline{\text{RING}}$, $\overline{\text{DTI0}}$, and RESET. The CR0 register bits that control power circuit function are RSTCHIP, RSTDSPB, ENOSC, ENDSPCK, ENMCLK, and PSDIS (1:0).

POWER CONTROL CIRCUIT FUNCTION

Power consumption can be reduced by turning off or slowing down specific circuit functions in register CR0.

- EN DSP=0: stops DSP clock.
- EN MCLK=0: turns off *u*C clock. MCLK=000: state gives lowest µC clock frequency.
- EN OSC=0: turns off oscillator and analog bias currents.
- DSPCK=000: state gives lowest DSP clock frequency.

The 73M2921 has a power-down mode. Access to this mode is described below.

Power Down Mode: To achieve power down first set RSTDSP to 0 in CR0 (bit 0). Second, set ENDSPCK, ENMCLK, and ENOSC to 0 in CR0 (bits 12, 8, and 7 respectively). Writing a one to ENDSPCK, ENMCLK, and ENOSC will bring the 73M2921 back to its previous power mode.

Powering up: Toggling the RESET pin, $\overline{\text{DTI0}}$, or $\overline{\text{RING}}$ will power the 73M2921 up to Normal mode. Similar results can be achieved by writing to the reset pin in CR0 (00b, bit 3).

The following is a functionality chart for the power control circuitry. It shows all inputs and describes the effect on various 73M2921 functions.

INPUT	AFFECTED SIGNAL OR FUNCTION
PIN	
$\overline{\text{RING}}$ (Pin 24)	These are the two pins used to bring the chip out of a power down state. Their function can be masked by the PSDIS bits in register CR0.
$\overline{\text{DTI0}}$ (Pin 26)	
CR0 bits	
ENDSPCK (CR0 D12)	Either of these bits in CR0 set to ONE inhibits the generation of a pulse that will reset the DSP.
ENOSC (CR0 D7)	
PSDIS1 (CR0 D2)	Masks $\overline{\text{DTI0}}$ input when set.
PSDIS0 (CR0 D1)	Masks $\overline{\text{RING}}$ when set.

Table 4 - Power Control Functions

POWER CONTROL TIMING

DESCRIPTION	MIN	TYP	MAX	UNIT
Powerup input to active state	250			µs
Powerup input to inactive state	50			µs

Table 5 - Power Control Timing

DCE-DTE INTERFACE

The 73M2921 is designed to interface with a synchronous port such as that found on the TDK 73M2910. It also provides a parallel control interface. This parallel interface appears as an 8 bit memory mapped peripheral to the host controller.

SERIAL DATA INTERFACE

The serial data interface is a four pin bi-directional port. It consists of the TXD and RXD data paths (LSBit shifted in and out first, respectively), the TXCLK and RXCLK serial clock outputs associated with the data pins.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
TXDS	DATA to TXCLK		Tbd		ns
TXDH	TXCLK to Data Hold		Tbd		ns
TRD	RXCLK to RXD Delay		Tbd		ns

Table 3 - Serial Data Interface Timing

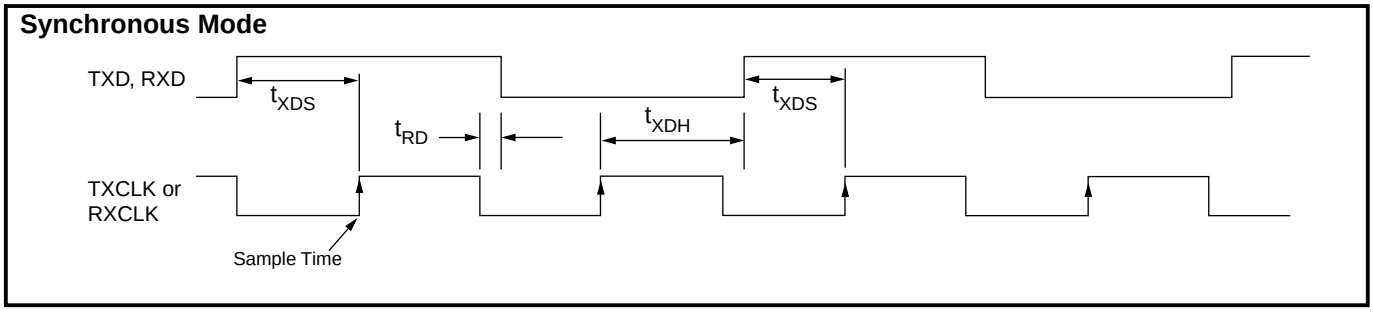


FIGURE 7 - Serial Data Interface Timing Diagram

MICROCONTROLLER TO 73M2921 PARALLEL INTERFACE

The interface between the microcontroller (µC) and the 73M2921 is accomplished through the 2 bit address UA[1:0] and 8 bit data bus UD[7:0], $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$. The 73M2921 chip provides an interrupt output to the µC ($\overline{UINT}$). The 73M2921 and the µC communicate through two 16 bit registers, CR0 and the Mailbox; all µC accesses are 8 bit transfers. All reading and writing functions to and from the 73M2921 internal registers as well

as to internal RAM are performed through these four bytes of memory (see Table 1).

There are 5 separate types of register access possible through the microcontroller interface. These are:

1. Access to CR0.
2. Configuration register access (CR1, CR2), via the Mailbox.
3. Access to the 8-bit General register set via the Mailbox.
4. Unsolicited Response status, via the Mailbox.
5. Memory Block Transfer, via the Mailbox (Not described in this document, please refer to application note "Using the Mailbox on the 73M2921").

The host controller initiates all communications over the data bus by sending a command to either read or write to a location. CR0 is a special case in that it is accessed directly by way of the address bits and does not generate a response from the 73M2921. All other registers are accessed indirectly by way of a "mailbox" register and will generate a response from the 73M2921.

UA [1:0]	ADDRESS	DESTINATION/SOURCE	
0 0	0	Direct hardware control of CR0 (MSB)	Write Only
0 1	1	Direct hardware control of CR0 (LSB)	Write Only
1 0	2	Mailbox function – Control Byte/High Byte	Read/Write
1 1	3	Mailbox function – Data Byte/Low Byte	Read/Write

Table 1 – Interface Register Address

(1) CONTROL REGISTER CR0 DESCRIPTION

Control Register 0 (CR0) is a 16 bit register that defines functions of general importance to the modem system. CR0 can be written to directly from the microcontroller interface, and is read/write accessible by the internal DSP. Control of a number of DSP functions is accomplished by writing two 8 bit bytes to this 16 bit wide register. UA Address 00b accesses bits D15 through D8 and address 01b is for bits D7 through D0. Writing to these locations directly access CR0. Writing to the CR0 Register sets an internal bit notifying the internal DSP firmware that the host microcontroller has issued a command. Access to CR0 does not return a response to the host controller.

Table 2 shows the state of CR0 after various reset conditions. Note that a reset from the register bit D3 (Reset Chip) does not alter the power-up source mask bit D2 and D1 and they remain unchanged from the previous state (U = unchanged).

CONDITION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reset from Reset Pin	1	1	1	1	1	1	1	0	1	0	1	1	0	0	0	1
Reset from CR0 bit D3	1	1	1	1	1	1	1	0	1	0	1	1	0	U	U	1

Table 2 - CR0 State After Reset

State of CR0 after reset from the reset pin and CR0 Reset bit (U = unchanged from previous state)

REGISTER NAME: CR0 ADDRESS: UA00, 01h (WRITE ONLY)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DSPCK (2:0)			EN DSPCK	MCLK (2:0)			EN MCLK	EN OSC	MAINCK (2:0)			RESET	PSDIS (1:0)		$\overline{\text{RSTDSP}}$

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	$\overline{\text{RSTDSP}}$	1	Set to a logic 1 by the RESET pin, the RESET CHIP bit, or by powering up the chip. To enable the DSP, the $\overline{\text{RSTDSP}}$ bit must be high.
		0	Causes a RESET interrupt to be continuously held for the DSP. While low, the DSP will remain at instruction location 0x0000.
D1, D2	Power Up Source Disable[1,0]		Used to mask the external power up source pins, $\overline{\text{DTI0}}$ and $\overline{\text{RING}}$. A logical 1 on PSDIS[1] masks $\overline{\text{DTI0}}$. A logical 1 on PSDIS[0] masks $\overline{\text{RING}}$.
D3	Reset Chip		Resets the state of the 73M2921 putting it into a known state. The function of this bit is similar to that of the RESET pin, except that this bit does NOT change the setting of the POWERUP SOURCE DISABLE bits. See Table 2.
D4, D5, D6	Main Timer Clock Divisor	D6 D5 D4 0 1 1	Must be set to provide 4.608MHz to the timer. Default values shown should be used with the 18.432 MHz oscillator frequency.
D7	Enable Oscillator	1 0	Enables the master oscillator. (Must be set to run) Disables the oscillator and stops all chip activity.
D8	Enable Micro-processor Clock	 1 0	For a clean MICCLK transition when stopping the clock (EN MCLK=0), the EN MCLK bit must be turned off prior to the oscillator (EN OSC) being disabled. MICCLK enabled. MICCLK disabled (Set to 0 if not using MICCLK).
D9, D10, D11	Microcontroller Clock Divisor	D11 D10 D9 1 1 1	Controls the frequency of the MICCLK output as a function of the oscillator frequency. Default values shown should be used with the 18.432 oscillator frequency. Set these to 0 if not using MICCLK (See Table 3).
D12	Enable DSP Clock	 1 0	Set by the RESET pin, the RESET CHIP bit, or by powering up the chip. DSP clock enabled. (Must be set to run) DSP clock disabled.
D13, D14, D15	DSP Clock	D15 D14 D13 1 1 1	Controls the internal DSP clock frequency as a function of the oscillator frequency. Default values shown should be used with the 18.432 MHz oscillator frequency.

For a clean DSPCK transition when stopping the DSP ($\overline{\text{RSTDSP}}$=0), the $\overline{\text{RSTDSP}}$ bit must be set low prior to the oscillator (ENOSC) being disabled.

For a clean DSPCK transition when starting the DSP ($\overline{\text{RSTDSP}}$=1), the $\overline{\text{RSTDSP}}$ bit must be set high after the oscillator (ENOSC) is enabled. This happens automatically after reset or power up.

MCLK [2:0]	Divisor	MICCLK Output
0 0 0	12	1.536
0 0 1	6	3.072
0 1 0	3	6.144
0 1 1	1.5	12.288
1 0 0	8	2.304
1 0 1	4	4.608
1 1 0	2	9.216
1 1 1	1	18.432

Table 4 - µP clock (MHz) vs. Divisor

USING THE MAILBOX REGISTER[1]

The mailbox function uses the same data interface as when accessing CR0 but has a different physical addresses (UA1:0 = 10b, 11b). The Mailbox is configured as two 8-bit bytes which are separated into a Control byte at address 10b and the Data byte at address 11b.

The $\overline{\text{UINT}}$ interrupt is closely coupled to the use of the Mailbox. An interrupt from $\overline{\text{UINT}}$ (DSP to microcontroller interrupt) indicates that the host controller should read the mailbox. This interrupt can be the result of the host accessing the Mailbox or an "unsolicited interrupt" indicating there has been a change in one of the status registers. The µC reads the MSB first, then the LSB. Reading the LSB sets $\overline{\text{UINT}}$ high and clears the 73M2921 internal mail full flag bit, allowing the 73M2921 to write new data to the mailbox. Mailbox data is not explicitly formatted. The microcontroller and 73M2921 firmware define the control exchange format.

(2) CONFIGURATION REGISTER ACCESS (CRA)

The configuration registers, CR1 and CR2 control some of the basic operating conditions. Some of the bits in these registers are for factory use only and should only be set to zero. Others, as noted, must be set to one for normal operation. Descriptions of CR1 and CR2 follow the programming section.

For Configuration Register Access, the Mailbox Control byte must be set up as follows:

Mailbox Control Byte for Configuration Register Access

D7	D6	D5	D4	D3	D2	D1	D0
RES	WT/$\overline{\text{BT}}$	R/$\overline{\text{W}}$					
0	1	1/0	1	0	0	0	1

- Res = Reserved for DSP use.
- WT/BT = Word Transfer/Byte Transfer. Should be 1 (word transfer) for CRA.
- R/$\overline{\text{W}}$ = Read/Write. Read = 1, Write = 0

For Configuration Register Access, the Mailbox Data byte specifies CR1 or CR2 as follows:

Mailbox Data Byte for CR1 Access

[1] Reading and writing through the Mailbox Register should be limited to once per millisecond while in idle mode and once per ten milliseconds otherwise.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0

Mailbox Data Byte for CR2 Access

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0

Reading and writing to the Configuration registers is a four step process for the host processor.

(1) The host processor writes to the Mailbox Control byte:
   (a) When writing data to the configuration registers the control byte 051h should be written to UA address 10b.
   (b) When reading data from the configuration registers the control byte 071h should be written to UA address 10b.

(2) The Host writes to the Mailbox Data byte (at UA address 11b, write either B0h to access CR1 or D0h to access CR2). Order is important as the writing of the Data byte triggers an internal interrupt in the DSP indicating that new mail is present. The 73M2921 will respond through the mailbox. The contents of the response are not important to the host.

(3) The host reads/writes the high byte of CR1/CR2 at UA address 10b.

(4) The host reads/writes the low byte of CR1/CR2 at UA address 11b.

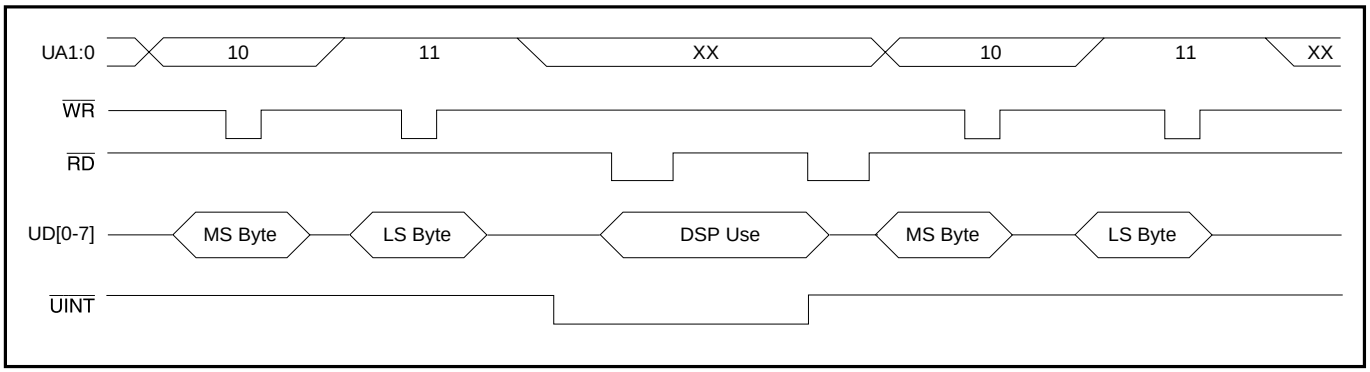


FIGURE 2: Interface Bus Activity for Configuration Register Access

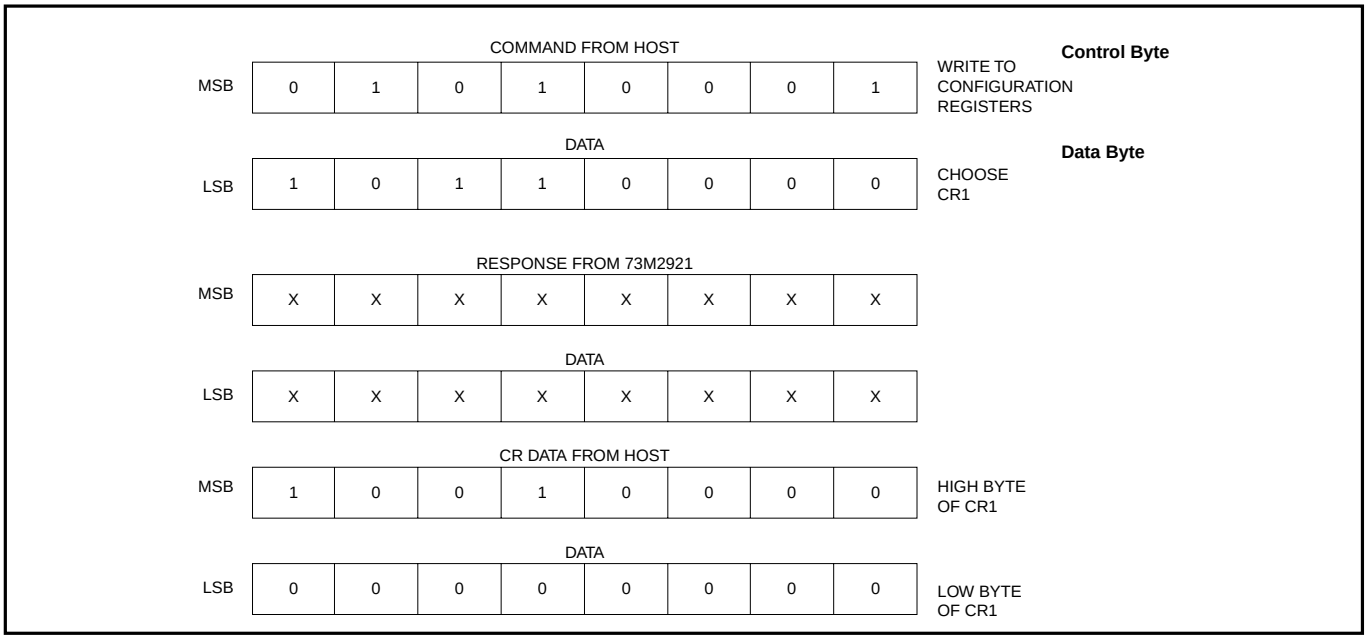


FIGURE 3: Write Command and Response

An example of a Configuration Register write cycle is shown in figures 2 and 3. Figure 2 shows the activity on the interface register data pins and $\overline{\text{UINT}}$. First there are two command bytes sent by the host processor. The 73M2921 responds (the contents of this response are not important to the host). Then the host writes the high and low byte of the Configuration register to the 73M2921.

An example of the Control and Data bytes for a CRA write is shown in Figure 3. In this example we will write 90 00h to Configuration register one (CR1). This turns on the digital portion of the 73M2921.

The Control byte shows D6 set to indicate that a word size transfer will take place. D5 is zero to indicate a write will occur. D4 is set to specify Configuration Register Access. D0 of the Control byte is always 1h for Configuration Register Access. The data byte shows D7 and D5 set to indicate that CR1 is to be accessed. D4 is always set for configuration register access. D3:0 are always zero for configuration register access.

The response from the 73M2921 will not be defined.

The word size transfer of CR1 data is also shown in figure 3. The MS byte is 90h. This enables the digital portion of the 73M2921. The LS byte is 0h. Refer to the configuration register description on pages 10 and 11 for further information.

REGISTER NAME: **CR1 Configuration Register 1** **ADDRESS: 05H (101b)**

CR1 controls Diagnostic modes, data wait, 5V power supply detect, speaker volume, ADC/DAC sampling rate, slave sync, digital loopback, digital interface loopback, enable digital interface, and enable timer. It also has bits that are reserved for test modes.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EN TIMER	TEST 3	TEST 2	EN DIGI	TDK	TDK	0	0	SLAVE SYNC	16 KHZ	SPKR VOL (1:0)		0	5V DETECT	DATA WAIT	DIAG MODE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Diagnostic Mode (Test Mode)	Always 0	DIAGNOSTIC MODE: Must be zero.
D1	Data Wait (Test Mode)	Always 0	Must be zero.
D2	5V Detect (output)		This is a logical 1 if the power supply to the 73M2921 is in the 5V range. Note, this signal is valid only when EN ANALOG (CR2: D10) is enabled.
D3	0		Not Used.
D4,D5	Speaker Volume (1:0)[2]	1 1 1 0 0 1 0 0	High Volume Medium Volume Low Volume Speaker off
D6	16KHz	1	The ADC/DAC sampling rates are 16.0KHz
		0	The ADC/DAC sampling rates are 14.4KHZ (Default)
D7	Slave Sync (modem test mode)	1	The phase error register measures the time between the rising edge of RXC and the rising edge of TXC
		0	The phase error register measures the time between the rising edge of EXC and the rising edge of TXC
D8,D9	0		Not Used
D10	TDK	Always 0	TDK proprietary.
D11	TDK	Always 0	TDK proprietary.
D12	Enable Digital Interface	1	Enables the digital serial interface. Pins TXCLK, RXCLK, TXD, and RXD are enabled. Must be set to one for normal operation.
		0	Tri-states pins TXCLK and RXCLK (with a weak pull-down to 0). RXD pin is driven to a 1, TXD is disabled at the input pin, and the timer baud clocks are forced low.
D13	Test 2	0	Must be zero.
D14	Test 3	0	Must be zero.
D15	Enable Timer	1	When set to 1, sample, bit, and clocks for transmit and receive are running. Baud (provided that EN DIGI is true).

[2] Volume PCM output on pin 38, MON, under software control. See application note concerning the use of this pin.

REGISTER NAME: CR2 Configuration Register 2 ADDRESS: 06H (110b)

CR2 controls analog port enable, analog loopback, ADC receive gain, VREF voltage, charge pump, and wide transmit bandwidth. It also has bits that are reserved for test modes.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WIDE TX BW	N/A	VREF	N/A	TDK	EN ANALOG	TEST 5	TEST 4	0	0	0	0	0	0	0	0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0 – D7	N/A	0	Not Used.
D8	Test 4	0	Must be zero.
D9	Test 5	0	Must be zero.
D10	Enable Analog	1	Analog port turned on. The timer must also be enabled (CR1:D15). NOTE: When the analog port is enabled and the timer is disabled, the ADC output is looped to the DAC input.
		0	Analog port turned off. All analog currents are off, including the bandgap generator. The setting of the ENOSC register bit to the disabled state also forces all analog power to be turned off.
D11	TDK		TDK proprietary.
D12	N/A	0	Not used.
D13	VREF	Set to 0	Selects the voltage reference voltage 1.25V DSP detectors require this setting on this version.
D14	N/A	1	Not used.
D15	Wide Transmit Bandwidth	1	Sets the transmit filter to pass 10KHz
		0	Sets the transmit filter to pass 3KHz (default)

(3) GENERAL REGISTER ACCESS (GRA)

For General Register Access (GRA), the mailbox the Control byte from the host controller is broken down into bit segments as follows:

General Register Access Control Byte: Microcontroller to 73M2921

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Res	WT/$\overline{BT}$	R/$\overline{W}$	---------- Register Address Bits ----------				
0	0	1/0					

Res = Reserved
WT/$\overline{BT}$ = Word Transfer/Byte Transfer. Should be 0 (byte transfer) for GRA.
R/$\overline{W}$ = Read / Write. 1 = Read, 0 = Write

Register Address Bits = 5 bit address for the register being accessed. See General Register descriptions in the following section.
(Register address 00000b is reserved CR0 location)

Reading and writing to the General Registers via the Mailbox is a four step process for the µC.

(1) The µC writes a Control byte (UA1:0 = 10b) to the mailbox with the R/$\overline{W}$ bit in the appropriate state for a read or a write.

(2) Then the µC writes a Data byte (UA1:0 = 11b). The Data byte contains the data to be written or null (00h) if a read is performed. Order is important as the Data byte triggers an internal interrupt in the 73M2921 firmware indicating new mail present. The 73M2921 then:

   (a) reads the mailbox
   (b) writes back to the mailbox register the Control Byte.
   (c) writes a response code (if R/$\overline{W}$ = 0) or data (if R/$\overline{W}$ = 1) to the Data Byte. The response code will be 00h for OK and 01h for ERROR
   (d) Lowers $\overline{UINT}$ to interrupt the µC indicating that data is in the Mailbox from the 73M2921.

The response from the 73M2921 can either be polled by the host controller or interrupt-driven. In the interrupt-driven response, an interrupt is issued by the 73M2921 from $\overline{UINT}$ when the response data is available, at which time the microcontroller reads two bytes (Control, Data) from the 73M2921. Reading valid Data clears the $\overline{UINT}$ interrupt for the next command. All reads and writes to the General registers will get an immediate response. In a polled mode of operation, if data is not ready, the Control and Data byte will both be zero. When the Control byte is non-zero, data is available.

(3) The µC reads the Control byte (UA1:0 = 10b).

(4) The µC reads the Data byte (UA1:0 = 11b). The data is the response code if the µC had requested a write, or the contents of the General Register in the Control address field if the µC had requested a read. This clears the $\overline{UINT}$ to a high state. The ERROR indicator byte should never be received when communications between the µC and the 73M2921 are working properly.

The Control byte returned by the 73M2921 is broken down into bit segments as follows:

Control byte 73M2921 to Microcontroller

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UR	WT/$\overline{BT}$	R/$\overline{W}$	---------- Register Address Bits ----------				
1/0	0	1/0					

UR = Unsolicited Response. Set if data is not response to last command.
WT/$\overline{BT}$ = Word Transfer/Byte Transfer. Should be 0 (byte transfer) for GRA.
R/$\overline{W}$ = Read = 1, Write = 0.

Register Address shadows last operation.

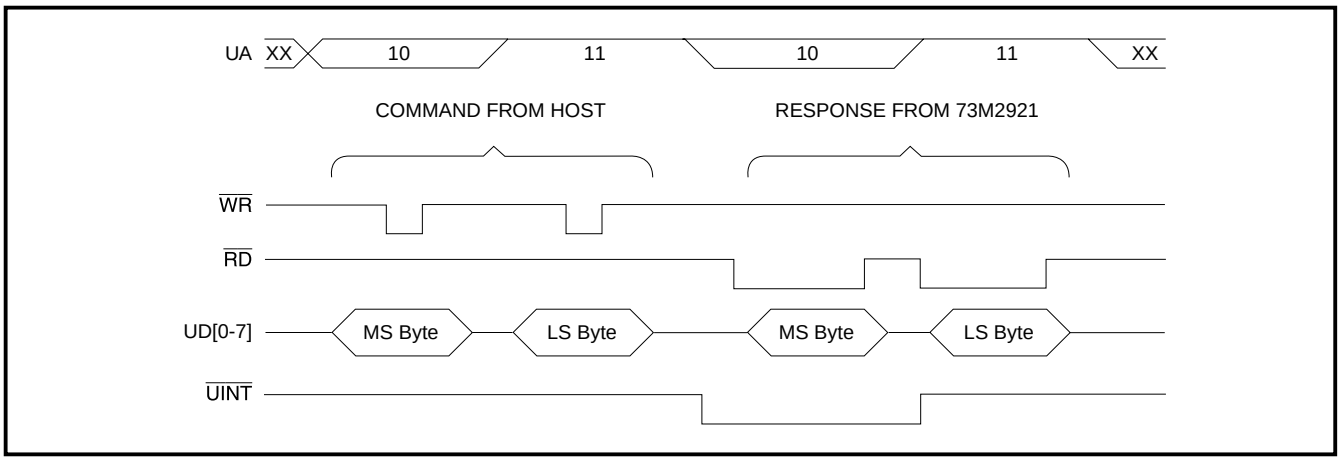


FIGURE 4 – Interface Bus Data Activity

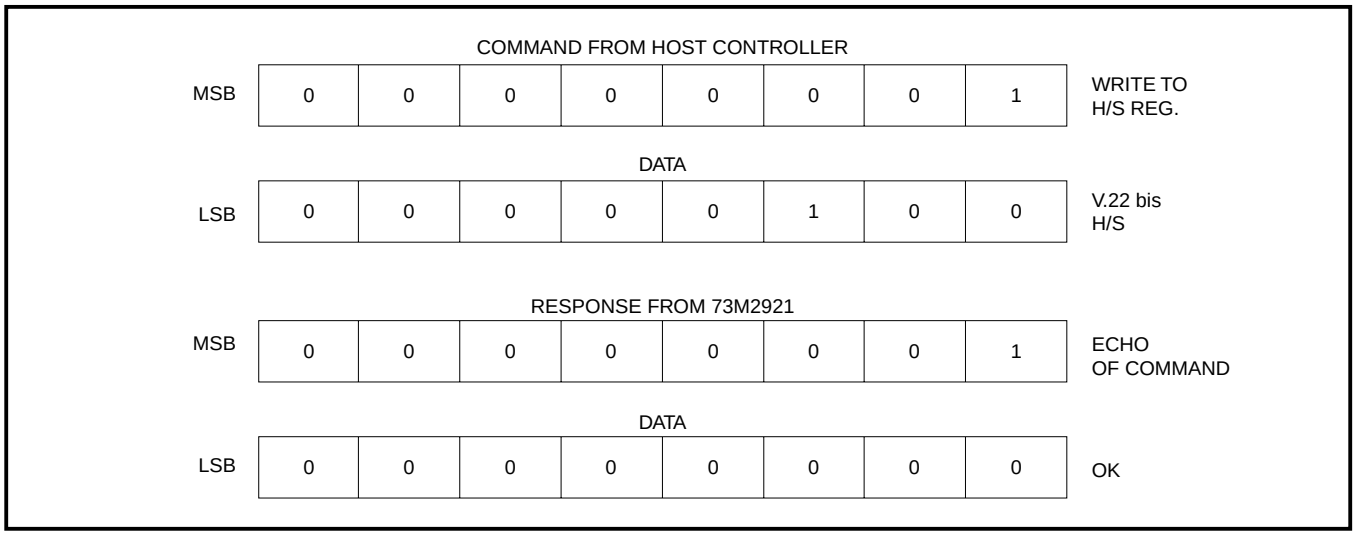


FIGURE 5 – Write Command and Response

An example of a write cycle is shown in Figure 4 and 5. Figure 4 shows the activity on the interface data pins and $\overline{\text{UINT}}$. First there are two command bytes sent by the host controller, then an interrupt is generated in $\overline{\text{UINT}}$ telling the host to read the response data, then the controller reads back the response from the 73M2921. The $\overline{\text{UINT}}$ interrupt is reset when the LS byte is read.

An example of the Control and Data register data in a write command process is shown in Figure 5. In this example we will write data to the Handshake Register telling it to perform a V.22bis handshake. The Control byte shows bit 5 low indicating a write process and the lower 5 address bits are set to address 00001b, the Handshake register. The Data byte contains the new contents for the Handshake register, in this case 04h, indicating a V.22 handshake will be performed. The 73M2921 processes this command and generates an interrupt on $\overline{\text{UINT}}$. The host then reads the data from the Control register, which echoes the command sent and the Data register which contain all zeros, or a successful operation. $\overline{\text{UINT}}$ is cleared when the Data byte is read.

UNSOLICITED RESPONSE

A $\overline{UINT}$ (low) interrupt can be the result of the µC doing a General register access (GRA, previously described), or an Unsolicited Response indicating there has been a change in one of the status registers. An Unsolicited Response is defined as any response or information sent from the 73M2921 to the mailbox, which was the result of an unsolicited interrupt from the internal DSP. The general register set $\overline{UINT}$ interrupt service routine must always check bit 7 of the Control byte to determine whether the interrupt was the result of a GRA in progress or an Unsolicited Response from the General register set status registers. An Unsolicited Response must always be serviced first, then the GRA in progress can be resumed. The data received from the 73M2921 is broken into Control and Data fields. Address 10b is the Control byte and Address 11b is the Data byte.

As an example, the user can enable each individual bit in each Detect Register to create an interrupt every time a detect bit has changed state. Once a detect bit is enabled, any change in state for that bit will trigger an Unsolicited Interrupt which sets bit 7 of the control byte to a one and the address bits of the Control byte to the address of the register which contains the bit that changed state. The Data byte will contain the contents of that register. Reading the mailbox clears the interrupt from the 73M2921 and allows further interrupts to occur.

The Control byte is broken down into bit segments as follows:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UR	WT/$\overline{BT}$	R/$\overline{W}$	---------- General Register Address ----------				

UR = Unsolicited Response. Set if data is not response to last command.
WT/$\overline{BT}$ = Word Transfer/Byte Transfer. Will always be zero (byte transfer) during Unsolicited Interrupt.
R/$\overline{W}$ = Read/Write. Shadows last command. (Don't care).
The General Register Address holds detect register address which triggered the interrupt.

In the example shown in Figure 6, the UR bit 7 will be set informing the microcontroller that this is an unsolicited response. The WT/$\overline{BT}$ bit is clear as this is a byte transfer. The address bits hold the address of Detect Register 1 (09h), which generated the interrupt. The Data byte contains the Detect register information. In this case an S1 signal is being received.

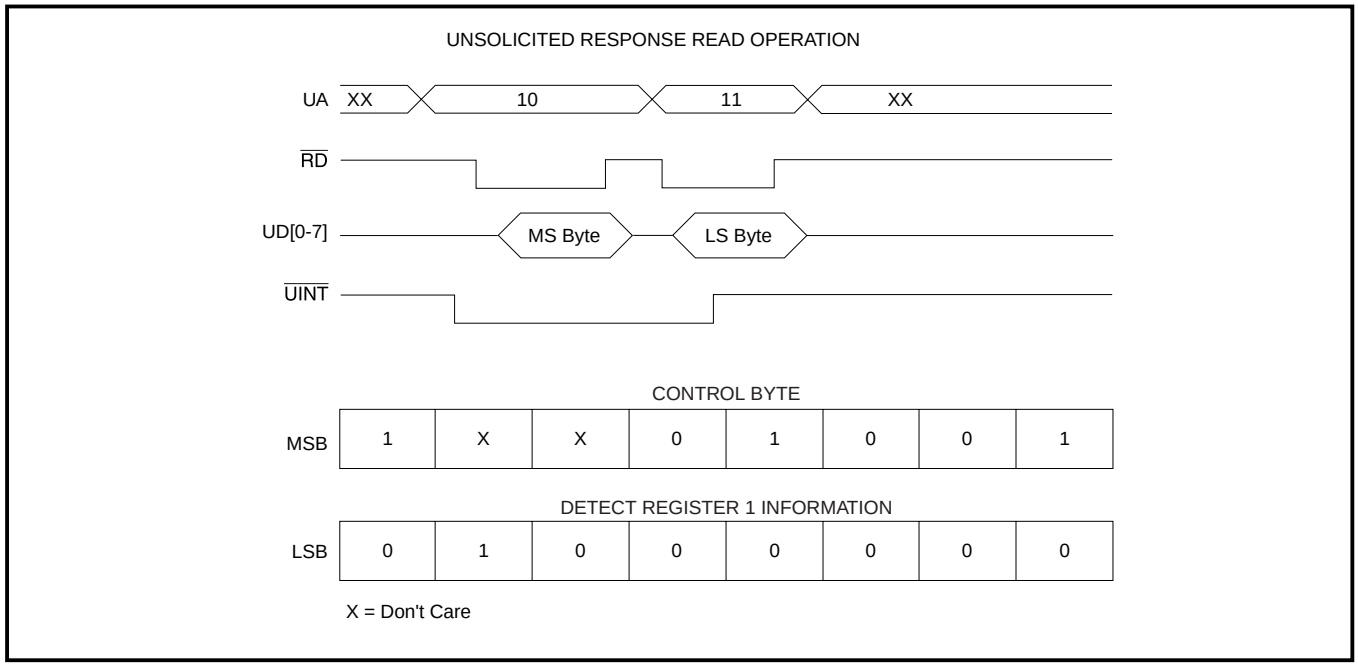


FIGURE 6 – Unsolicited Interrupt Example

2921 GENERAL REGISTER SET SUMMARY

NAME	R/W	FIVE BIT ADDRESS (HEX)	COMMENT
Data Mode Handshake	R/W	01h	Selects automatic handshake to be performed
Connection Detect	R	02h	Read Only, indicates successful handshake in Data mode
DTMF Dial	R/W	03h	Sets DTMF digit and twist for transmission
DTMF Detect	R	04h	Read only, indicates DTMF digit received
Data Mode Control	R/W	05h	Selects answer/originate and retrain modes allowed
Test Control	R/W	06h	Selects test patterns, test mode handshaking, scrambler/descrambler operation.
Version	R	07h	Read only, revision level of the 73M2921
Detect 1 Enable	R/W	08h	Enables interrupts on changes of state from Detect Reg. 1 status bits.
Detect Register 1	R	09h	Read only, indicates status of detectors used during handshaking for various modes.
Detect 2 Enable	R/W	0Ah	Enables interrupts on changes of state from Detect Reg. 2 status bits.
Detect Register 2	R	0Bh	Read only, indicates status of detectors used during handshaking for various modes.
Transmit Control	R/W	0Ch	Selects data format or FSK, carrier transmission in DATA mode or DTMF transmit enable in CALL PROGRESS mode.
General Control	R/W	0Dh	Controls transmit power level, idle mode power consumption, receive gain boost, clock out enable
Fax Handshake	R/W	0Eh	Controls Fax speed and transmit or receive mode
Reserved	X	0Fh	Reserved
Mode Control	R/W	010h	Controls Call Progress, Data or Idle Mode selection. Also controls method of initialization and modification of default settings. Affects operation of all registers.
MSE0	R	011h	Read only, Least Significant Byte of the DSP error signal. Indication of signal quality.
MSE1	R	012h	Read only, Most Significant Byte of the DSP error signal. Indication of signal quality.
CPTX	R/W	014h	Controls Call Progress transmit functions.
PCPD Detect Enable	R/W	018h	Enables interrupts on changes of state from PCPD detect bits.
PCPD Detect	R	019h	Read only, indicates detection of precise call progress tones.

Note: Reserved bits should never be programmed to a 1 state.

HANDSHAKE REGISTER ADDRESS: 01H (01d, 00001b) MODE: DATA

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
V.23	V.21	Bell 103	Bell 212	V.22	V.22bis	Bell 202	Res.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Reserved	1	Reserved for future use.
D1	Bell 202	1	Instructs the modem to attempt a Bell 202 handshake
D2	V.22bis	1	Instructs the modem to attempt a V.22bis handshake
D3	V.22	1	Instructs the modem to attempt a V.22 handshake
D4	Bell 212	1	Instructs the modem to attempt a Bell 212 handshake
D5	Bell 103	1	Instructs the modem to attempt a Bell 103 handshake
D6	V.21	1	Instructs the modem to attempt a V.21 handshake
D7	V.23	1	Instructs the modem to attempt a V.23 handshake

Note: The Handshake register defines the handshake methods allowed during the connection phase of a communication session. Only one bit can be set at a given time except for automatic V.22bis fallback to V.22 or Bell 212A which requires both BIT D2 and BIT D3 to be set. The master transmit enable, TXEN, BIT D7 of the TRANSMIT CONTROL REGISTER (0CH) must be set for the handshake transmit functions to operate.

CONNECTION DETECT REGISTER (READ ONLY) ADDRESS: 02h (02d, 00010b) MODE: DATA, FAX

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
V.23 (data) V.29 (fax)	V.21 (data) V.21 CH2 (fax)	Bell 103	Bell 212	V.22 (data) V.27ter (fax)	V.22bis	Bell 202	Res.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Reserved		Reserved for future use.
D1	Bell 202		Informs processor Bell 202 was detected.
D2	V.22bis		Informs processor of a successful V.22bis connection.
D3	V.22 V.27ter	Data Mode Fax Mode	Informs processor of a successful V.22 connection. Informs processor of a successful V.27ter connection.
D4	Bell 212		Informs processor of a successful Bell 212A connection.
D5	Bell 103		Informs processor of a successful Bell 103 connection.
D6	V.21 V.21 CH2	Data Mode Fax Mode	Informs processor of a successful V.21 connection. Informs processor of a successful V.21 CH2 connection.
D7	V.23 V.29	Data Mode Fax Mode	Informs processor of a successful V.23 connection. Informs processor of a successful V.29 connection.

Note: All bits are zero until a successful connection has been established (carrier detect valid, data mode active). Then the appropriate bit will be set. This register is shared between fax and data modes. Only bits D3, D6, and D7 are valid when in fax mode.

DTMF DIAL REGISTER **ADDRESS: 03h (03d, 00011b)** **MODE: CALL PROGRESS**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
RES	TWIST2	TWIST1	TWIST0	DTMF3	DTMF2	DTMF1	DTMF0

BIT NO.	NAME	CONDITION				DESCRIPTION
D3, D2, D1, D0	DTMF 3-0					
	Digit	D3	D2	D1	D0	
	1	0	0	0	1	Transmits 697 Hz & 1209 Hz
	2	0	0	1	0	Transmits 697 Hz & 1336 Hz
	3	0	0	1	1	Transmits 697 Hz & 1477 Hz
	4	0	1	0	0	Transmits 770 Hz & 1209 Hz
	5	0	1	0	1	Transmits 770 Hz & 1336 Hz
	6	0	1	1	0	Transmits 770 Hz & 1477 Hz
	7	0	1	1	1	Transmits 852 Hz & 1209 Hz
	8	1	0	0	0	Transmits 852 Hz & 1336 Hz
	9	1	0	0	1	Transmits 852 Hz & 1477 Hz
	0	1	0	1	0	Transmits 941 Hz & 1336 Hz
	*	1	0	1	1	Transmits 941 Hz & 1209 Hz
	#	1	1	0	0	Transmits 941 Hz & 1477 Hz
	A	1	1	0	1	Transmits 697 Hz & 1633 Hz
	B	1	1	1	0	Transmits 770 Hz & 1633 Hz
	C	1	1	1	1	Transmits 852 Hz & 1633 Hz
	D	0	0	0	0	Transmits 941 Hz & 1633 Hz
	Twist 2-0	D6	D5	D4		Relative Level
		0	0	0		0 dB (Same levels)
		0	0	1		1 dB Low tone below the high tone
		0	1	0		2 dB Low tone below the high tone (Default)
		0	1	1		3 dB Low tone below the high tone
		1	0	0		4 dB Low tone below the high tone
		1	0	1		5 dB Low tone below the high tone
		1	1	0		6 dB Low tone below the high tone
		1	1	1		7 dB Low tone below the high tone
D7	Reserved					Reserved for future use.

The TXDT BIT 3 of the TRANSMIT CONTROL REGISTER (0Ch) must be set for DTMF tone transmission. TXDT is gated on and off during the transmission of tones when dialing DTMF digits.

DTMF DETECT REGISTER **ADDRESS: 04h (04d, 00100b)** **MODE: CALL PROGRESS**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
Det. Valid	RES.	RES.	RES.	DTDET 3	DTDET 2	DTDET 1	DTDET 0

BIT NO.	NAME	CONDITION				DIGIT	DESCRIPTION
D3, D2, D1, D0	DTMF Detect 3-0	D3	D2	D1	D0		
		0	0	0	1	1	Detects 697 Hz & 1209 Hz
		0	0	1	0	2	Detects 697 Hz & 1336 Hz
		0	0	1	1	3	Detects 697 Hz & 1477 Hz
		0	1	0	0	4	Detects 770 Hz & 1209 Hz
		0	1	0	1	5	Detects 770 Hz & 1336 Hz
		0	1	1	0	6	Detects 770 Hz & 1477 Hz
		0	1	1	1	7	Detects 852 Hz & 1209 Hz
		1	0	0	0	8	Detects 852 Hz & 1336 Hz
		1	0	0	1	9	Detects 852 Hz & 1477 Hz
		1	0	1	0	0	Detects 941 Hz & 1336 Hz
		1	0	1	1	*	Detects 941 Hz & 1209 Hz
		1	1	0	0	#	Detects 941 Hz & 1477 Hz
		1	1	0	1	A	Detects 697 Hz & 1633 Hz
		1	1	1	0	B	Detects 770 Hz & 1633 Hz
		1	1	1	1	C	Detects 852 Hz & 1633 Hz
		0	0	0	0	D	Detects 941 Hz & 1633 Hz
D4, D5, D6	Reserved					Reserved for future use	
D7	Valid DTMF Detect	1				Indicates a valid DTMF detection	
		0				Indicates no detect for polled applications	

DATA MODE CONTROL REGISTER ADDRESS: 05h (05d, 00101b) MODE: DATA

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
RESERVED	ANS	GTEN	GTONE	RESERVED	RESERVED	RESERVED	RT FORCE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Retrain Force	1	Forces a retrain request. Cleared by 73M2921.
D1	Reserved		Reserved
D2	Reserved		Reserved
D3	Reserved		Reserved
D4	Guard Tone	1 0	Sets the guard tone to 550 Hz Sets the guard tone to 1800 Hz
D5	Guard Tone Enable	1	Enables the guard tones
D6	Answer/ Originate (Main Channel Selection)	1 0	Sets the modem to be in Answer mode. When Modulation is set for V.23, the 73M2921 transmits in main channel @ 1200 b/s and Receives in back channel @ 75 bps. When Modulation is set for Bell 202, the 73M2921 transmits @ 1200 bps. Sets the modem into Originate mode. When Modulation is set for V.23, the 73M2921 receives in main channel @ 1200 bps and Transmits in back channel @ 75 bps. When Modulation is set for Bell 202, the 73M2921 receives at 1200 bps.
D7	Reserved		Reserved for future use

TEST CONTROL REGISTER **ADDRESS: 06h (06d, 00110b)** **MODE: DATA***

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
ALB	RDLB	DSD1	SCD1	SDP3	SDP2	SDP1	SDP0

BIT NO.	NAME	CONDITION				DESCRIPTION
D3, D2, D1, D0	Send Data Pattern	D3	D2	D1	D0	
		0	0	0	0	Send Data
		0	0	0	1	Send Marks
		0	0	1	0	Send Space
		0	0	1	1	Send Dotting Pattern (Not valid for FSK)
		0	1	0	0	Send S1 (Not valid for FSK)
		0	1	0	1	Send S0 (Not valid for FSK)
		0	1	1	0	Reserved
		0	1	1	1	Reserved
		1	X	X	X	Reserved
D4	Scrambler Disable	1				Disables the scrambler (V.22bis, V.22, Bell212)
D5	Descrambler Disable	1				Disables the Descrambler (V.22bis, V.22, Bell212)
D6	Remote Digital Loopback	1				Instructs the modem to perform a Remote Digital Loopback connection (V.22bis, V.22, Bell212)
D7	Analog Loopback	1				Instructs the modem to perform an Analog Loopback connection (V.22bis, V.22, Bell212, Bell 103, V.21)

VERSION REGISTER (READ ONLY) **ADDRESS: 07h (07d, 00111b)** **MODE: ALL MODES**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
0	**1**	**0**	**1**	**1**	**0**	**0**	**0**

This register contains 8 bit firmware version number.

* Changes can be made to this register during DATA MODE. Changes will be activated immediately.

DETECT 1 ENABLE REGISTER **ADDRESS: 08h (08d, 01000b)** **MODE: SEE DET REG 1**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
CAS	S1	RES	EGY	HIP	CAR	RDLBD	RES

This is the enable register for Detect 1. Setting bits TO 1 in this register enables the unsolicited interrupt feature. These bits have a 1 to 1 correspondence with Detect Register 1. The default value is "0". See Detect Register 1.

DETECT REGISTER 1 (READ ONLY) **ADDRESS: 09h (09d, 01001b)** **MODE: SEE BELOW**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
CAS	S1	RES	EGY	HIP	CAR	RDLBD	RES

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Reserved		Reserved.
D1	RDLBD	Valid in Data Mode	RDLB Detect
D2	Carrier Detect	Valid in Data Mode	This bit will be set when conditions for V.24 circuit 104 are met by the modulation mode being used (Modem in data mode).
D3	Handshake in progress	Valid in Data Mode	This bit will be set if a handshake is currently in progress. This bit is cleared by the 73M2921 when either a handshake has been successful and the 73M2921 has entered DATA mode, or when a handshake has been aborted and the 73M2921 is placed into IDLE mode.
D4	Energy Detect	Valid in call Progress Mode	This bit will be set if receive level is above a predetermined threshold.
D5	Reserved		Reserved.
D6	S1 Detect	Valid in Data Mode	This bit will be set if S1 (Unscrambled 1100 @ 1200b/s) is detected. This bit is also used to detect a Retrain request if connected V.22bis or V.22 and S1 is detected.
D7	CAS Tone Detect	Valid in All Modes	This bit will be set if the CAS tone (2130Hz + 2750 Hz) is detected.

DETECT 2 ENABLE REGISTER ADDRESS: 0Ah (010d, 01010b) MODE: SEE DET REG 2

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
2250Hz	V21	2225Hz	2100Hz	1100Hz	1300Hz	RES.	CPD1

This is the enable register for Detect 2. Setting bits in this register enables the unsolicited interrupt feature. These bits have a 1 to 1 correspondence with Detect Register 2. A "1" in each bit location would enable the detect register bit of the same name. The default value is "0". See Detect Register 2.

DETECT REGISTER 2 (READ ONLY) ADDRESS: 0Bh (011d, 01011b) MODE: SEE BELOW

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
2250Hz	V21	2225Hz	2100Hz	1100Hz	1300Hz	RES.	CPD1

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Call Progress Filter 1	Valid in Call Progress Mode	Imprecise call progress detector, energy detected in the 350-600 Hz band.
D1	Reserved		Reserved for future use.
D2	1300 Hz Detect	Valid in Call Progress Mode Answer Only	This bit will be set if 1300 Hz Data Modem Calling Tone is detected.
D3	1100 Hz Detect	Valid in Call Progress Mode Answer Only	This bit will be set if 1100 Hz Fax Modem Calling Tone is detected.
D4	2100 Hz Detect	Valid in Call Progress Modes Originate Only	This bit will be set if 2100 Hz Answer Tone is detected.
D5	2225 Hz Detect	Valid in Call Progress Modes Originate Only	This will be set if 2225 Hz Answer Tone is detected.
D6	V21 Detect (High Band)	Valid in Call Progress Modes Originate Only	This bit will be set if V.21 channel 2 tone is detected.
D7	2250 Hz Detect	Valid in Call Progress Modes Originate Only	This bit will be set if the 2250Hz component of S0 (unscrambled mark) is detected.

TRANSMIT CONTROL REGISTER **ADDRESS: 0Ch (012d, 01100b)** **MODE: SEE BELOW**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
TXEN	Res.	Res.	Res.	TXDT	MOD2	MOD1	MOD0

	NAME	CONDITION	DESCRIPTION
D0, D1,D2	Modulation Type	D2 D1 D0	Valid in Data Modes
		0 0 0	Internal Sync
		0 0 1	Reserved
		0 1 0	Slave Sync
		0 1 1	Reserved
		1 0 0	Reserved
		1 0 1	Reserved
		1 1 0	Reserved
		1 1 1	FSK
D3	Transmit DTMF Tones	Valid in Call Progress Mode	Transmits tone set in DTMF Dial Register.
D4,D5,D6	Reserved		Reserved for future use.
D7	Master Transmit Enable	Valid in Data Mode	Enables Transmitter in Data Mode. Must be set prior to Data Mode. The DSP ignores bit changes after Data Mode transitions.

GENERAL CONTROL REGISTER **ADDRESS: 0Dh (013d, 01101b)** **MODE: ALL MODES**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
Res.	Res.	Res.	RESERVED	TXAT3	TXAT2	TXAT1	TXAT0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D1,D2, D3	Transmit Attenuation	D3 D2 D1 D0	Allows for 16 levels in all transmit modes
		0 1 1 1	+ 7 dB
		0 1 1 0	+ 6 dB
		0 1 0 1	+ 5 dB
		0 1 0 0	+ 4 dB
		0 0 1 1	+ 3 dB
		0 0 1 0	+ 2 dB
		0 0 0 1	+ 1 dB
		0 0 0 0	Nominal
		1 1 1 1	- 1 dB
		1 1 1 0	- 2 dB
		1 1 0 1	- 3 dB
		1 1 0 0	- 4 dB
		1 0 1 1	- 5 dB
		1 0 1 0	- 6 dB
		1 0 0 1	- 7 dB
		1 0 0 0	- 8 dB
D4	Reserved		Reserved
D5	Reserved		Reserved
D6	Reserved		Reserved
D7	Reserved	-	Reserved for future use

FAX HANDSHAKE REGISTER **ADDRESS: E0h (014d, 01110b)** **MODE: FAX**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
T/$\overline{R}$	Res.	Res.	Res.	FM3	FM2	FM1	FM0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D1,D2, D3	Fax Connect Mode	D3 D2 D1 D0	Defines Modulation for transmit or receive
		0 0 0 0	V.21 channel 2 connection
		0 0 0 1	V.27ter 2400 b/s connection
		0 0 1 0	V.27ter 4800 b/s connection
		0 0 1 1	V.29 7200 b/s connection
		0 1 0 0	V.29 9600 b/s connection
		1 x x x	Reserved for future use
D4,D5,D6	Reserved		Reserved for future use
D7	Transmit	1	Indicates a transmit operation
		0	Indicates a receive operation

MODE CONTROL REGISTER **ADDRESS: 010h (016d, 10000b)** **MODE: ALL MODES**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
RES	HINIT	SRUN	SINIT	ICMP	FAX	DATA	CP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2, D1, D0	DSP Mode[3]	D2 D1 D0	
		0 0 0	DSP in IDLE Mode
		0 0 1	DSP in Call Progress Mode
		0 1 0	DSP in Data Mode
		1 0 0	DSP in Fax Mode
		Any other	DSP Error
D3	Initialization Complete (Read Only)	1[4]	Indicates the completion of the initialization routines in call progress, and data modes.
		0	Initialization not complete.
D5, D4	Soft Init / Soft Run[5]	D5 D4	Used with MBT
		0 0	Perform both init and run functions.
		0 1	Perform only the INITIALIZATION functions. This allows the µP to go back to idle and modify any initialization parameters.
		1 0	Perform only the RUN functions assuming the init function are complete. DO NOT attempt to run without initialization.
		1 1	Perform init and run functions. This will init all functions to their default values and then perform the run functions.
D6	Hard Init[4]	1	Forces a hard initialization of all state machine timing and control variables.
		0	Allows normal operation.
D7	Reserved		Reserved
		0	Allows normal operation. Valid for V.22 and V.22 bis only

[3] Only one bit of D0, D1, D2 are allowed at any one time. The 73M2921 will return ERROR if the µP tries to set more than one bit or if a bit is set while another bit is already set. When all three bits (D0,D1,D2) are set to 0, it defines IDLE mode. All transition must return to IDLE mode before setting another mode. i.e. In order to switch from Data mode to Call Progress mode, the mode must be set to 000 (IDLE mode) first before setting to 001(CALL PROGRESS mode).

[4] The ICMP bit does not correctly reflect completion of the initialization routine (depending on mode). Wait 2 baud periods and the initialization will be done regardless.

[5] Refer to application notes for information on Memory Block Transer (MBT); set to zero. Only used with Memory Block Transfers.

MSE0 REGISTER (LSB) **ADDRESS: 011h (017d, 10001b)** **MODE: ALL MODES**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0

This register returns the Least Significant Byte of the Mean Squared Error number from the DSP. Used to determine Signal Quality.

MSE1 REGISTER (MSB) **ADDRESS: 012h (018d, 10010b)** **MODE: ALL MODES**

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0

This register returns the Most Significant Byte of the Mean Squared Error number from the DSP. Used to determine Signal Quality.

CALL PROGRESS TRANSMIT REGISTER ADDRESS: 014 h (020d, 10100b) MODE: CALL PROGRESS

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
CPDIR	Res.	Res.	TX2225	TX2100	TX1300	TX1100	CPTE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Call Progress Transmit Enable	1	Enables Call Progress Transmit. This bit must be set to transmit a tone.
D1	Transmit 1100 Hz	D7 = 0	Transmits 1100 Hz Fax Calling Tone. Only active when D7 = 0
D2	Transmit 1300 Hz	D7 = 0	Transmits 1300 Hz Modem Calling Tone. Only active when D7 = 0
D3	Transmit 2100 Hz	D7 = 1	Transmits 2100 Hz CCITT Answer Tone.
D4	Transmit 2225 Hz	D7 = 1	Transmits 2225 Hz Bell Answer Tone.
D5,D6	Reserved	-	Reserved for future use
D7	Call Progress Direction	1 0	Call Progress Answer. D1 & D2 are disabled Call Progress Originate. D3 & D4 are disabled

NOTE: When using bits D1-D4, only one may be active at a time.

PRECISE CPD ENABLE REGISTER ADDRESS: 18h (024d, 11000b) MODE: CALL PROG.

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0

This register enables the precise CPD register. Setting bits in this register enables the unsolicited interrupt feature. These bits have a 1 to 1 correspondence with the Precise CPD register. The default value is "0". See Precise CPD register.

PRECISE CPD REGISTER ADDRESS: 19h (025d, 11001b) MODE: CALL PROG. ORIGINATE ONLY

BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
Res.	Res.	2750 Hz	2130 Hz	620 Hz	480 Hz	440 Hz	350 Hz

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Detect 350 Hz	1	Indicates detection of 350 Hz tone
D1	Detect 440 Hz	1	Indicates detection of 440 Hz tone
D2	Detect 480 Hz	1	Indicates detection of 480 Hz tone
D3	Detect 620 Hz	1	Indicates detection of 620 Hz tone
D4	Detect 2130 Hz	1	Indicates detection of 2130 Hz tone (component of CAS tone)
D5	Detect 2750 Hz	1	Indicates detection of 2750 Hz tone (component of CAS tone)
D6, D7	Reserved	-	Reserved for future use

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Applied Voltage	-0.3 to (VDD + 0.3V)
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS (TA = -40°C to 85°C VDD 3.3V ± .3V except as noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply Voltage (VPD, VPA)	VNA & VND = 0V	3.0	3.3	3.6	V
Supply Current (IPA+IPD)	VPA & VPD = 3.3V Outputs unloaded CMOS input levels Running internal code		18	30	mA
	In power down mode, CR0 CLK turned off		6	50	µA

RECOMMENDED OPERATING CONDITIONS (TA = -40°C TO 85°C VDD 5V ± .5V except as noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply Voltage (VPD, VPA)	VNA & VND = 0V	4.5	5.0	5.5	V
Supply Current (IPA+IPD)	VPA & VPD = 5.0V Outputs unloaded CMOS input levels Running internal code		30	40	mA
	In power down mode, CR0 CLK turned off		6	50	µA
VIH Input High		0.75* VP			V
VIL Input Low				0.25*VP	V
Input Current (digital)	0 < VIN < VP	-1		1	µA
Input Current	0 < VIN < VP	-100	1	100	µA
VOL Output Low	IOL = +3mA	0		0.5	V
VOH Output High	IOH = -3mA	VP-0.5		VP	V
Clock Variation	Crystal or external clock	-0.01		+0.01	%
TA, Operating Temperature		-40		85	°C

ANALOG VOLTAGE REFERENCE AND REGULATION (TA = -40°C to 85°C VDD 5V ± .5V except as noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Vbg			1.25		V
Vref	VPA, VPD = 5V, VREF HIGH = 0	1.1	1.25	1.4	V

ANALOG VOLTAGE REFERENCE AND REGULATION (TA = -40°C to 85°C VDD 5V ± .5V except as noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Impedance	INPA & INNA	50			KΩ
Offset Voltage	DAC min scale	-100	0	100	mV
DC Gain	DAC max scale Output load = 50 KΩ	-0.5	0	0.5	dB
Input Level Differential analog INPA, INNA	Vref = 1.25V 1 KHz sine wave			0.450	V pk
Analog Output Level (OUTPA-OUTNA or OUTNA-OUTPA)	Vref = 1.25V DAC max scale Output load = 50 KΩ	0.5	0.55	0.6	V pk-pk
Idle Channel Noise	0.3KHz - 3.0KHz		-65		dBm
Output THD (OUTPA-OUTNA)	1KHz sine max scale into DAC Output load = 50 KΩ			-50	dB
Input THD (INPA-INNA)	1KHz sine at 1.25V=Vref &1V pk-pk			-50	dB
Intermodulation Distortion	1.0KHz & 1.2KHz at ±18,876 counts (full scale signal) into DAC, Output load = 50 KΩ			-50	dB

DYNAMIC CHARACTERISTICS AND TIMING (TA = -40°C to 85°C VDD 5V ± .5V,differential mode, except as noted)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
QAM/DPSK Modulator	Output load 50KΩ max				
Output Amplitude	TX scrambled marks (Vcc = 5V) Transmit Attenuator set to 0000		-10.0	-9.0	dBm0
FSK Modulator					
Transmit Level	Transmit Dotting Pattern (Vcc = 5V, Vref = 1.25V)		-10.0	-9.0	dBm0

ANSWER TONE GENERATOR (2100 or 2225 Hz)	CONDITION	MIN	NOM	MAX	UNIT
Output Amplitude	Vcc = 5V	11.5	-10.0	-9.0	dBm0
Output Distortion	Distortion products in receive band			-40	dB

DTMF GENERATOR[6]	CONDITION	MIN	NOM	MAX	UNIT
Frequency Accuracy		-0.1		0.1	%
Output Amplitude Low Band	Vcc = 5V		-9		dBm
Output Amplitude High Band	Vcc = 5V		-7		dBm
Twist	Adjustable in firmware		2		dB

IMPRECISE CALL PROGRESS DETECTOR	IN CALL PROGRESS MODE 350 - 600 Hz	MIN	NOM	MAX	UNIT
Detect Level	460 Hz test signal	-53.0			dBm
Reject Level	460 Hz test signal			-53.0	dBm
Delay Time	-70 dBm0 to -30 dBm0 level change		60		ms
Hold Time	-30 dBm0 to -70 dBm0 level change		70		ms

CARRIER DETECT	CONDITION	MIN	NOM	MAX	UNIT
Threshold	All Modes	-48.0		-43.0	dBm
Hysteresis	All Modes	2.0			dBm
Delay Time All Modes	-70 dBm0 to -6 dBm0 level change		40		ms
Hold Time All Modes	-70 dBm0 to -6 dBm0 level change		40		ms

ANSWER TONE DETECTOR	CALL PROGRESS MODE	MIN	NOM	MAX	UNIT
Detect Level Threshold		-48.0		-43.0	dBm
Detect Time	2100 or 2225 Hz		60		ms
Hold Time			100		ms

[6] Do not transmit DTMF levels higher than -3.0dBm600.

MAXIMUM OUT OF BAND ENERGY TRANSMIT	CONDITION	MIN	NOM	MAX	UNIT
	4 kHz, Guard Tones Off			-35	dBm
	10 kHz, Guard Tones Off			-55	dBm
	12 kHz, Guard Tones Off			-65	dBm

GUARD TONE GENERATOR	CONDITION	MIN	NOM	MAX	UNIT
Tone Level (Below QAM/DPSK Output)	550 Hz	-4.5	-3	-1.5	dB
	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion (700 to 2900 Hz)	550 Hz and 1800Hz			-50	dB

CONTROL INTERFACE TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tCW	$\overline{CS}$ to $\overline{WR}$ Low	50			ns
tWC	$\overline{WR}$ High to $\overline{CS}$ High	20			ns
tWH	Write Hold Time	20			ns
tWS	Write Setup Time	150			ns
tWW	$\overline{WR}$ width	185			ns
tRC	$\overline{RD}$ High to $\overline{CS}$ High	20			ns
tRW	$\overline{RD}$ width	185			ns
tRH	Read Hold Time	5			ns
tRZ	Read High-Z Time			20	ns

Table 6 - µC Parallel Interface Timing

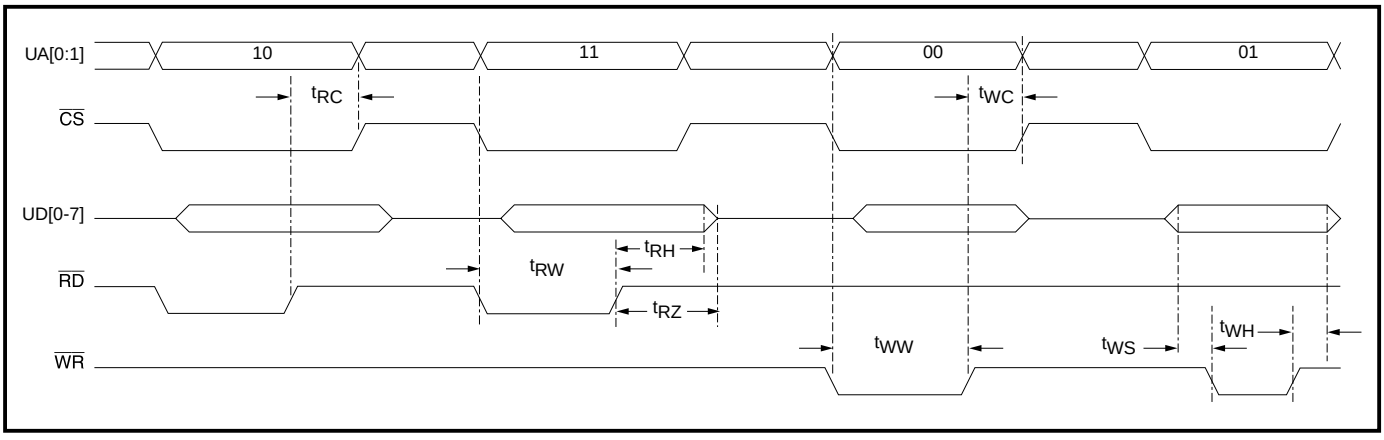


FIGURE 8 - µC Parallel Interface Timing Diagram

DESIGN CONSIDERATIONS

TDK Semiconductor's single chip modem solutions include all the basic modem functions. This makes these devices adaptable to a variety of applications, and as easy to control as conventional digital bus peripherals.

Unlike digital logic circuitry, modem designs must contend with precise frequency tolerances and verify low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. The crystal oscillator should be held to a 50ppm tolerance. Following are additional recommendations that should be taken into consideration when starting new designs. Additional information is available in the 73M2921 Design Guide.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain high performance in modem designs. The more digital circuitry present on the PC board, the more attention to noise control is needed.

The 73M2921 should be considered a high performance analog device. A 10µF electrolytic capacitor in parallel with a 0.1µF Ceramic capacitor should be placed between VPD and VND as well as between VPA and VNA. A 0.1µF ceramic capacitor should be placed between VREF and VNA as well as VBG and VNA. Liberal use of ground planes and large traces on power are also highly recommended. High speed, digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations.

To accomplish this, high speed, digital devices should be locally bypassed, and the telephone line interface and the modem should be located next to each other near where the telephone line connection is accessed. To avoid problems, power supplies and ground traces should be routed separately to the analog and digital portions on the board. Digital signals should not be routed near low level analog or high impedance analog traces.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions typical of those encountered over public service telephone lines.

BER vs. SNR (see Figure 9)

This test represents the ability of the modem to operate over noisy lines with a minimum amount of data transfer errors. Since some noise is generated in the best dial up lines, the modem must operate with the lowest signal to noise ratio (SNR) possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically a DPSK modem will exhibit better BER performance test curves receiving in the low band (answer mode) than in the high band (originate mode).

BER vs. RECEIVE LEVEL

This test measures the dynamic range of the modem. Because signal levels vary widely over dial up lines, the widest possible dynamic range possible is desirable. The minimum Bell specification calls for 36dB of dynamic range. The SNR is held constant at the indicated values as the Receive level is lowered from very a very high to a very low signal level. The width of the bowl of these curves, taken at the BER point is the measure of the dynamic range.

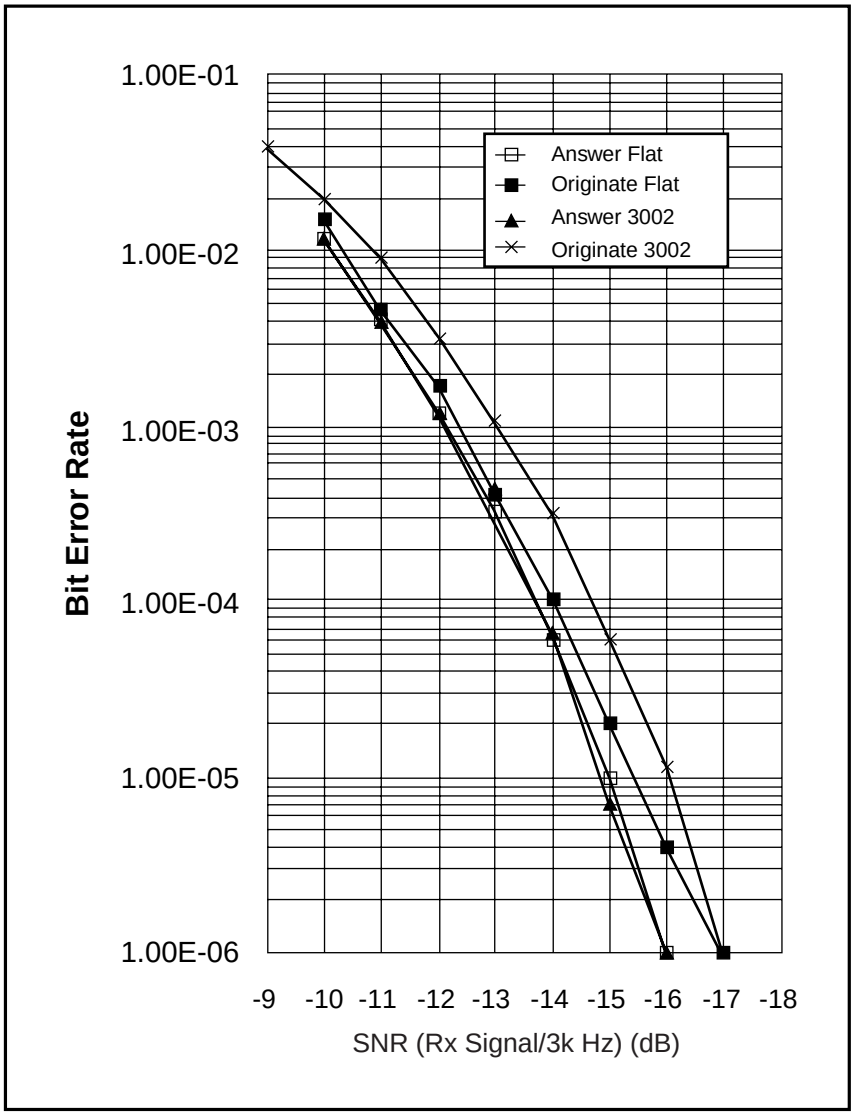


FIGURE 9 - 2400 BPS QAM SNR vs. BER

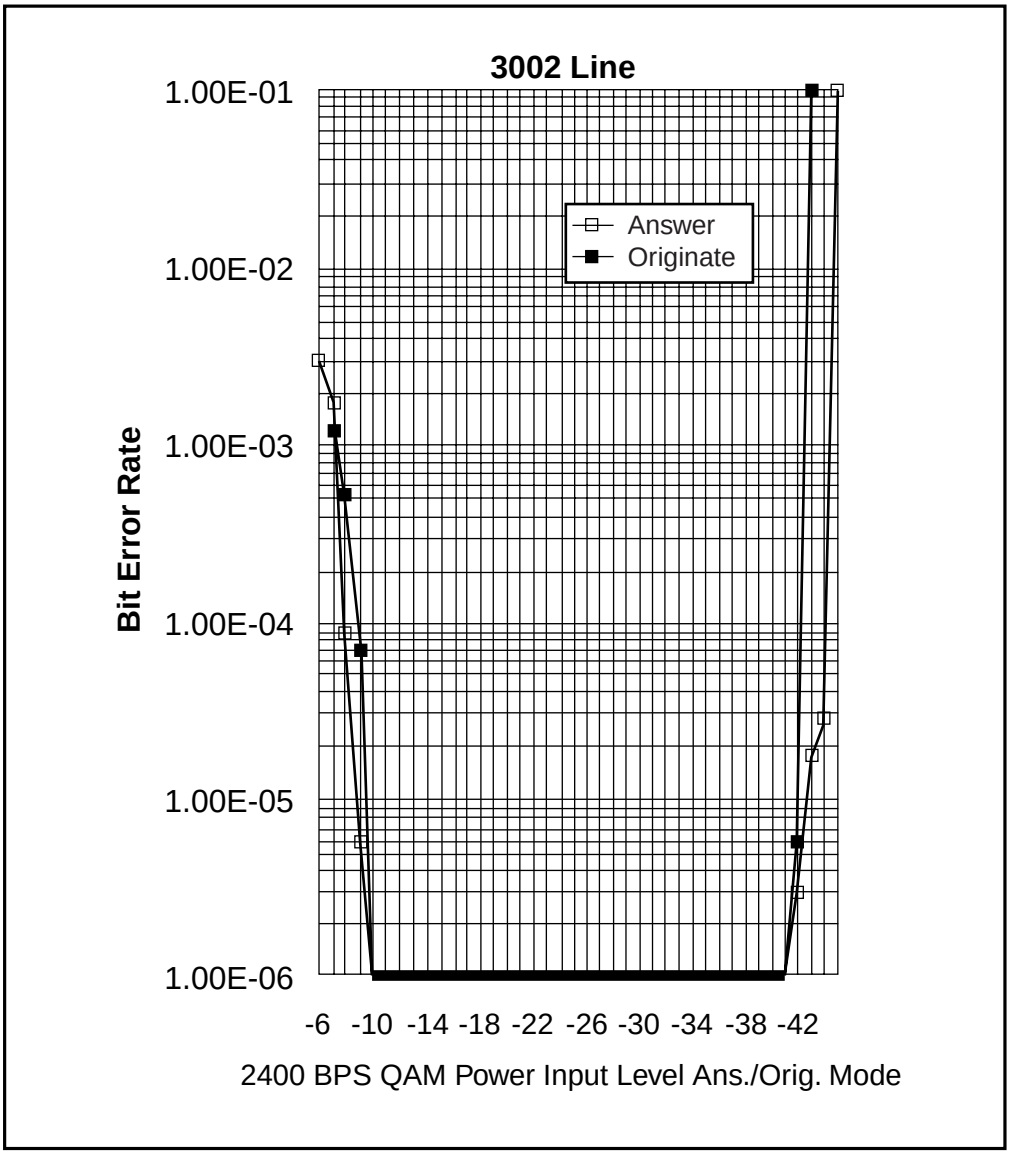


FIGURE 10 – Power Input Level vs. BER

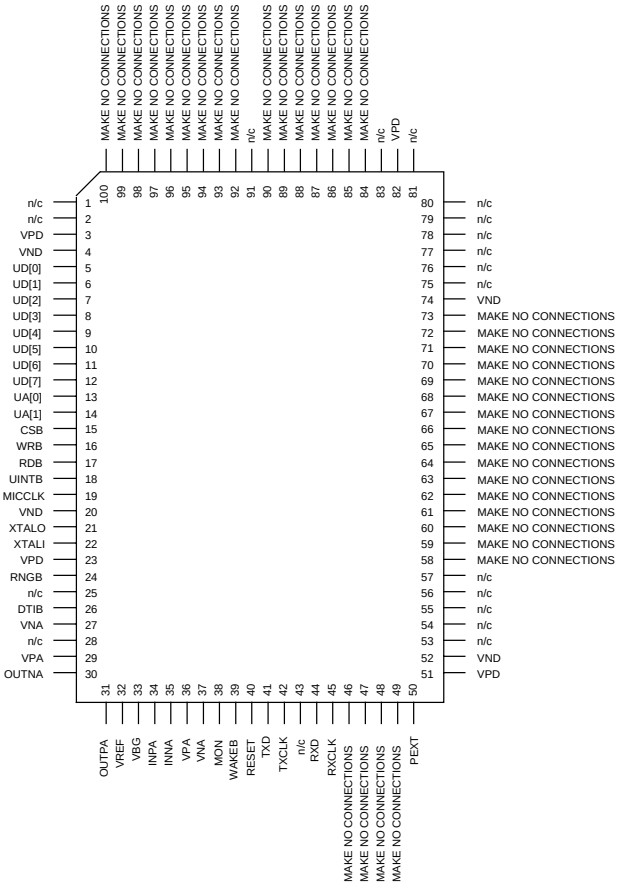
PINOUT

100 PIN QFP - PRODUCTION PACKAGE PINOUT

QFP Pin	Pin Name	Pin Description	QFP Pin	Pin Name	Pin Description
1	n/c		35	INNA	analog negative input
2	n/c		36	VPA	analog positive power supply
3	VPD	digital positive power supply	37	VNA	analog negative power supply
4	VND	digital negative power supply	38	MON	speaker driver output
5-12	UD[0-7]	8 bit microcontroller data bus, bidirectional	39	$\overline{\text{WAKE}}$	microcontroller wake-up output
13,14	UA[0, 1]	2 bit microcontroller address	40	RESET	reset chip input
15	$\overline{\text{CS}}$	microcontroller chip select input	41	TXD	transmit serial data input
16	$\overline{\text{WR}}$	µP write enable input	42	TXCLK	transmit data clock output
17	$\overline{\text{RD}}$	µP read enable input	43	n/c	
18	$\overline{\text{UINT}}$	µP interrupt output	44	RXD	receive serial data output
19	MICCLK	microcontroller clock output	45	RXCLK	receive data clock output
20	VND	digital negative power supply	46-49		for factory use, make no connections
21	XTALO	crystal oscillator output	50	PEXT	for factory use; tie to ground
22	XTALI	crystal oscillator (clock) input	51	VPD	digital positive power supply
23	VPD	digital positive power supply	52	VND	digital negative power supply
24	$\overline{\text{RING}}$	ring detect input	53-57	n/c	
25	n/c		58-73		for factory use, make no connections
26	$\overline{\text{DTI0}}$	data transition 0 input	74	VND	digital negative power supply
27	VNA	analog negative power supply	75-81	n/c	
28	n/c		82	VPD	digital positive power supply
29	VPA	analog positive power supply	83	n/c	
30	OUTNA	analog negative output	84-90		for factory use, make no connections
31	OUTPA	analog positive output	91	n/c	
32	VREF	analog voltage reference output	92-100		for factory use, make no connections
33	VBG	bandgap bypass point			
34	INPA	analog positive input			

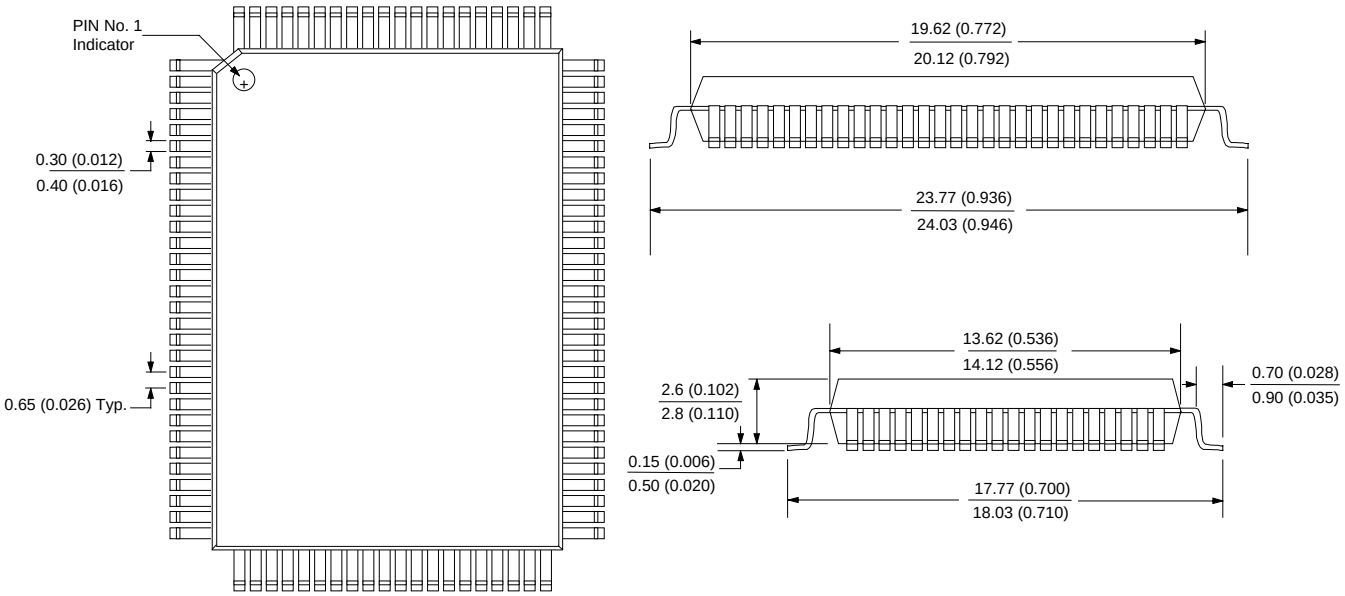
PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100 Pin QFP
73M2921-IG

MECHANICAL SPECIFICATIONS



ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGING MARK
73M2921	100-Pin QFP	73M2921-IG	73M2921-IG

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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