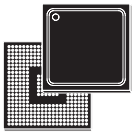
SPEAR-09-H122

SPEAr™ Head600

Preliminary Data

Features

- ARM926EJ-S core @333MHz.
- 600KByte reconfigurable logic array with 88 dedicated General purposes I/Os, 9 LVDS channels and 128KByte configurable internal memory pool.
- Multilayer AMBA 2.0 compliant Bus with f_{MAX} 166MHz
- 32KByte Rom.
- 8KByte common Static Ram.
- Dynamic Power saving features.
- High performance 8 channels DMA.
- Ethernet 10/100/1000 MAC with GMII/MII Interface to external PHY.
- USB2.0 device with integrated PHY.
- 2 USB2.0 Host with integrated PHY.
- Ext. SDRAM memory interface:
  - 8/16bit (DDR1@200MHz)
  - 8/16bit (DDR2@333MHz)
- Flashes interface:
  - Nand 8/16bit
  - Serial (up to 50Mbps).
- 3-SPI Master/Slave up to 40Mbps.
- I^2C Master/Slave mode - High, Fast and Slow speed.
- 2 independent UART up to 460.8 Kbps with Software Flow Control mode.
- IrDA (Fir-Mir-Sir) from 9.6Kbps to 4Mbps speed-rate.
- Colour LCD controller:
  - up to 1024x768 resolutions.



PBGA420

  - 24bpp true colour TFT panel.
  - 16bpp DSTN panel.
- 10 GPIOs bidirectional signals with interrupt capability.
- 88 RAS-GPIOs user customizable bidirectional signals (up to 4 clocks).
- ADC 10 bit, 1MSPS, 8 analog inputs.
- JPEG codec accelerator.
- 10 independent Timers with programmable prescaler.
- Real Time Clock.
- WatchDog
- System Controller
- MISC internal control registers.
- JTAG (IEEE1149.1) interface

Description

SPEAr Head600 is a powerful digital engine belonging to SPEAr family, the innovative customizable System on chip.
The device integrates an ARM 926 core with a large set of proven IPs and a big configurable logic block that allow very fast customization of unique and/or proprietary solution.

Table 1. Device summary

Part number	Op. temp. range, °C	Package	Packing
SPEAR-09-H122	-40 to 85	PBGA420(23x23x1.81mm)	Tray

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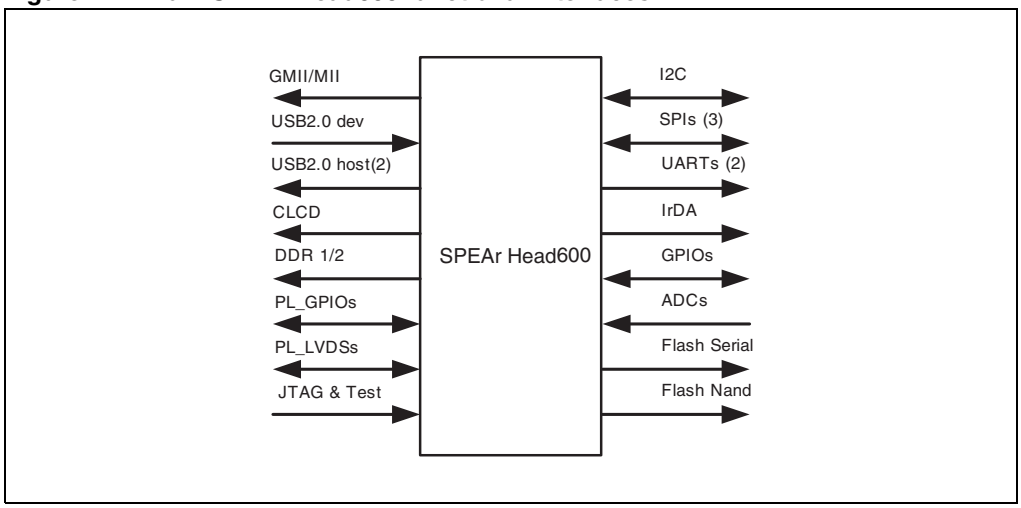
Reference documentation

1. ARM926EJ-S - Technical Reference Manual
2. AMBA 2.0 Specification
3. EIA/JESD8-9 Specification
4. USB2.0 Specification
5. OHCI Specification
6. EHCI Specification
7. USB Specification
8. IEEE 802.3 Specification
9. I^2C - Bus Specification

1 Product Overview

An outline picture of the main SPEAr Head600 functional interfaces is shown in *Figure 1*.

Figure 1. Main SPEAr Head600 functional interfaces



1.1 Features

The following main functionalities are implemented in the SPEAr Head600 SoC device:

- ARM926EJ-S core @333MHz, 16KB-I/D cache, configurable TMC-I/D size, MMU, TLB, JTAG and ETM trace module (multiplexed interfaces).
- 600KByte reconfigurable logic array (programmable through 4Metal and 4Vias).
- 128KByte configurable internal memory pool (Single and Dual port memory).
- 32KByte Rom (code customizable) 8KByte common SRam.
- Dynamic Power save features.
- High performance linked list 8 channels DMA.
- Ethernet GMII/MII (IEEE802.3/3x/1Q), management i/f.
- USB2.0 Device (High-Full-Slow speed); integrated PHY transceiver.
- 2-USB2.0 Host (High-Full-Slow speed); integrated PHY transceiver.
- Ext. memory i/f: 8/16bit DDR1@200Mhz/DDR2@333Mhz.
- Flash interface: Nand 8/16bit and Serial (up to 50Mbps).
- 3-SPI Master/Slave (Motorola-Texas-National) up to 40Mbps.
- I^2C (High-Fast-Slow speed) Master/Slave.
- 2-Uart (speed rate up to 460.8Kbps).
- IrDA (Fir-Mir-Sir) from 9.6Kbps to 4Mbps speed-rate.
- Color LCD up to 1024x768 resolutions; 24bpp true colour; STN/TFT display panel.
- 10 GPIOs bidirectional signals with interrupt capability.
- 9 LVDS (8 out and 1 input) signals; customizable interface through programmable logic.
- 88 RAS-GPIOs user customizable bidirectional signals (up to 4 clocks).

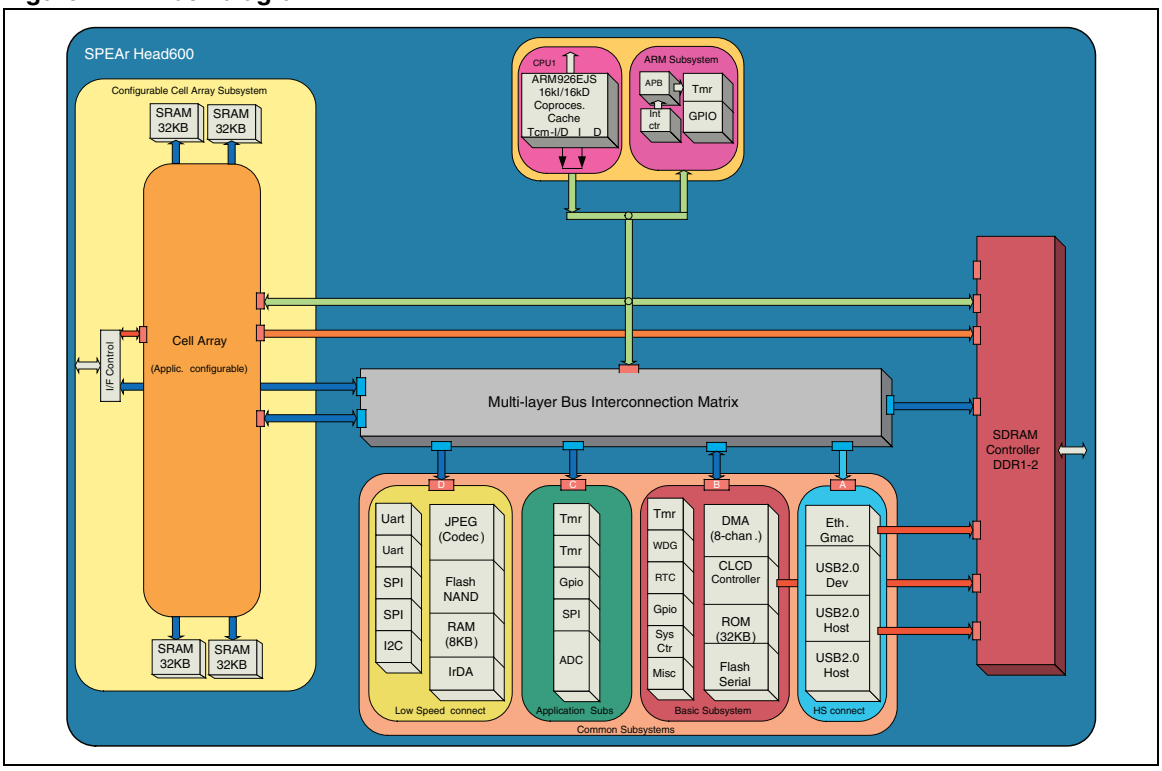
- ADC (1us/1MSPS) 8 analog input channel; 10bit approximation.
- JPEG codec accelerator 1clock/pixel.
- 10 independent Timers with programmable prescaler.
- RTC - WDOG - SYSCTR - MISC internal control registers.
- JTAG (IEEE1149.1) interface.

1.2 Architecture properties

- Power save features:
  - Operating frequency SW programmable.
  - Clock gating functionality.
  - Low frequency operating mode.
  - Automatic power saving controlled from application activity demands.
- Customizable logic to embed the customer real 'core competence':
  - 600Kgate standard cell array.
  - Internal memory pool (128Kbyte) full configurable.
  - Up to 16 external/internal source clock (some of these programmable).
  - Three memory path toward the SDRAM controller to ensure a good bandwidth.
- Architecture easily extensible.
- External memory bandwidth of each master tuneable to meet the target performances of different applications.

1.3 Block diagram

Figure 2. Block diagram



2 Pin description

2.1 Functional pin group

With reference to figure package schematic in *Section 6*, here follows the pin list, sorted by their belonging IP. All supply and ground pins are classified as power signals and gathered in the *Table 3*.

Table 2. Pin description by functional group

Group	Signal name	Ball	Direction	Function	Pin Type
ADC	AIN_0	W11	Input	ADC analog input channel	Analog buffer 2.5V tolerant
	AIN_1	V11			
	AIN_2	V12			
	AIN_3	W12			
	AIN_4	W13			
	AIN_5	V13			
	AIN_6	V14			
	AIN_7	W14			
	ADC_VREFN	W15		ADC negative voltage reference	
	ADC_VREFP	V15		ADC positive voltage reference	
DEBUG	TEST_0	E15	Input	Test Configuration ports. For functional mode they have to be set to zero.	TTL input buffer, 3.3 V tolerant, PD
	TEST_1	D14			
	TEST_2	E14			
	TEST_3	E13			
	TEST_4	D13			
	TEST_5	D12			
	nTRST	D17	Input	Test Reset Input	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDO	E17	Output	Test Data Output	TTL output buffer, 3.3V capable,4 mA
	TCK	E16	Input	Test Clock	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDI	D16	Input	Test Data Input	
	TMS	D15	Input	Test Mode Select	
PL	PL_GPIO_0	P4	I/O	Programmable Logic I/O	TTL BIDIR buffer, 3.3V capable, 4mA 3.3V tolerant, PU

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
PL	PL_GPIO_1	N4	I/O	Programmable Logic I/O	TTL BIDIR buffer, 3.3V capable, 4mA 3.3V tolerant, PU
	PL_GPIO_2	N5			
	PL_GPIO_3	N6			
	PL_GPIO_4	M5			
	PL_GPIO_5	M4			
	PL_GPIO_6	M3			
	PL_GPIO_7	M2			
	PL_GPIO_8	M1			
	PL_GPIO_9	L1			
	PL_GPIO_10	L2			
	PL_GPIO_11	L3			
	PL_GPIO_12	L4			
	PL_GPIO_13	L5			
	PL_GPIO_14	K6			
	PL_GPIO_15	K5			
	PL_GPIO_16	K4			
	PL_GPIO_17	K3			
	PL_GPIO_18	K2			
	PL_GPIO_19	K1			
	PL_GPIO_20	J1			
	PL_GPIO_21	J2			
	PL_GPIO_22	J3			
	PL_GPIO_23	J4			
	PL_GPIO_24	J5			
	PL_GPIO_25	H5			
	PL_GPIO_26	H4			
	PL_GPIO_27	H3			
	PL_GPIO_28	H2			
	PL_GPIO_29	H1			
	PL_GPIO_30	G1			
	PL_GPIO_31	G2			
	PL_GPIO_32	G3			
	PL_GPIO_33	G4			
	PL_GPIO_34	G5			
	PL_GPIO_35	F5			

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
PL	PL_GPIO_36	F4	I/O	Programmable Logic I/O	TTL BIDIR buffer, 3.3V capable, 4mA 3.3V tolerant, PU
	PL_GPIO_37	F3			
	PL_GPIO_38	F2			
	PL_GPIO_39	F1			
	PL_GPIO_40	E4			
	PL_GPIO_41	E3			
	PL_GPIO_42	E2			
	PL_GPIO_43	E1			
	PL_GPIO_44	D3			
	PL_GPIO_45	D2			
	PL_GPIO_46	D1			
	PL_GPIO_47	C2			
	PL_GPIO_48	C1			
	PL_GPIO_49	B1			
	PL_GPIO_50	A1			
	PL_GPIO_51	B2			
	PL_GPIO_52	A2			
	PL_GPIO_53	C3			
	PL_GPIO_54	B3			
	PL_GPIO_55	A3			
	PL_GPIO_56	B4			
	PL_GPIO_57	C4			
	PL_GPIO_58	D4			
	PL_GPIO_59	E5			
	PL_GPIO_60	D5			
	PL_GPIO_61	C5			
	PL_GPIO_62	B5			
	PL_GPIO_63	B6			
	PL_GPIO_64	C6			
	PL_GPIO_65	D6			
	PL_GPIO_66	E6			
	PL_GPIO_67	F6			
	PL_GPIO_68	F7			
	PL_GPIO_69	E7			
	PL_GPIO_70	D7			

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
PL	PL_GPIO_71	C7	I/O	Programmable Logic I/O	TTL Output buffer 3.3V capable, 4mA TTL Input Buffer 3.3V tolerant, PU
	PL_GPIO_72	B7			
	PL_GPIO_73	E8			
	PL_GPIO_74	D8			
	PL_GPIO_75	C8			
	PL_GPIO_76	B8			
	PL_GPIO_77	A8			
	PL_GPIO_78	C9			
	PL_GPIO_79	D9			
	PL_GPIO_80	E9			
	PL_GPIO_81	E10			
	PL_GPIO_82	D10			
	PL_GPIO_83	C10			
	PL_CLK_1	A7		Programmable Logic External Clock	TTL BIDIR buffer, 3.3V capable, 8mA 3.3V tolerant, PU
	PL_CLK_2	A6			
	PL_CLK_3	A5			
	PL_CLK_4	A4			
Ethernet	GMII_TXCLK	F22	Output	Transmit clock (GMII)	TTL Output Buffer 3.3V capable, 8mA
	GMII_TXCLK125	E22	Input	Ext. Clock	TTL Input Buffer, 3.3V tolerant, PD
	MII_TXCLK	D22		Transmit Clock MII	
	TXD_0	F21	Output	Transmit data	TTL Output buffer 3.3V capable, 8mA
	TXD_1	E21			
	TXD_2	F20			
	TXD_3	E20			
	GMII_TXD_4	D21	I/O		TTL BIDIR buffer 3.3V capable, 8mA 3.3V tolerant, PD
	GMII_TXD_5	D20			
	GMII_TXD_6	C22			
	GMII_TXD_7	C21			
	TX_ER	D18	Output	Transmit Error	TTL Output buffer 3.3V capable, 8mA
	TX_EN	D19		Transmit Enable	
	RX_ER	C20	Input	Receive Error	TTL Input buffer 3.3V tolerant, PD
	RX_DV	C19		Receive Data Valid	
	RX_CLK	A22		Receive Clock	
	RXD_0	B22		Receive Data	

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
Ethernet	RXD_1	B21	Input	Receive Data	TTL Input buffer 3.3V tolerant, PD
	RXD_2	A21			
	RXD_3	B20			
	GMII_RXD_4	A20	I/O		TTL BIDIR buffer 3.3V capable, 8mA 3.3V tolerant, PD
	GMII_RXD_5	B19			
	GMII_RXD_6	A18			
	GMII_RXD_7	A19			
	COL	A17	Input	Collision Detect	TTL Input buffer 3.3V tolerant, PD
	CRS	B17		Carrier sense	
	MDIO	B18	I/O	Management Data I/O	TTL BIDIR buffer 3.3V capable, 4mA 3.3V tolerant, PD
	MDC	C18	Output	Management Data Clock	TTL Output buffer 3.3V capable, 8mA
GPIO	GPIO_0	W18	I/O	General purpose I/O	TTL BIDIR Buffer 3.3V capable, 8mA 3.3V tolerant, PU
	GPIO_1	V18			
	GPIO_2	U18			
	GPIO_3	T18			
	GPIO_4	W19			
	GPIO_5	V19			
	GPIO_6	U19			
	GPIO_7	T19			
	GPIO_8	R19			
	GPIO_9	R18			
LCD I/F	CLD_0	Y20	Output	LCD Data	TTL Output buffer 3.3V capable, 8mA
	CLD_1	Y21			
	CLD_2	Y22			
	CLD_3	W22			TTL Output buffer 3.3V capable, 8mA
	CLD_4	W21			
	CLD_5	W20			
	CLD_6	V20			
	CLD_7	V21			
	CLD_8	V22			
	CLD_9	U22			
	CLD_10	U21			

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
LCD I/F	CLD_11	U20	Output	LCD Data	TTL Output buffer 3.3V capable, 8mA
	CLD_12	T20			
	CLD_13	T21			
	CLD_14	R21			
	CLD_15	R20			
	CLD_16	P19			
	CLD_17	P20			
	CLD_18	P21			
	CLD_19	N21			
	CLD_20	N20			
	CLD_21	N19			
	CLD_22	M20			
	CLD_23	M21			
	CLAC	T22		STN AC bias drive TFT Data Enable	
	CLCP	R22		LCD Panel Clock	
	CLFP	P22		STN Frame Pulse TFT Vertical Sync	
	CLLP	N22		STN Line Pulse TFT Horizontal Sync	
	CLLE	M22		Line End	
	CLPOWER	M19		LCD Power Enable	
DDR I/F	DDR_ADD_0	AB3		Address Line	SSTL_2/SSTL_18
	DDR_ADD_1	AB4			
	DDR_ADD_2	AA4			
	DDR_ADD_3	Y4			
	DDR_ADD_4	W4			
	DDR_ADD_5	W5			
	DDR_ADD_6	Y5			
	DDR_ADD_7	AA5			
	DDR_ADD_8	AB5			
	DDR_ADD_9	AB6			
	DDR_ADD_10	AA6			
	DDR_ADD_11	Y6			
	DDR_ADD_12	W6			
	DDR_ADD_13	W7			

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
DDR I/F	DDR_ADD_14	Y7	Output	Address Line	SSTL_2/SSTL_18
	DDR_BA_0	Y9		Bank select	
	DDR_BA_1	W9			
	DDR_BA_2	W10		Bank select	
	DDR_RAS	AB7		Row strobe	
	DDR_CAS	AA7		Column Strobe	
	DDR_WE	AA8		Write Enable	
	DDR_CLKEN	AB8		Clock Enable	
	DDR_CLK_P	AA9		Differential Clock	Differential SSTL_2/SSTL_18
	DDR_CLK_N	AB9			
	DDR_CS_0	Y8		Chip Select	SSTL_2/SSTL_18
	DDR_CS_1	W8		Chip Select	SSTL_2/SSTL_18
	DDR_ODT_0	AB2		On-die Termination Enable lines	
	DDR_ODT_1	AB1			
	DDR_DATA_0	AB11	I/O	Data Lines (Lower byte)	
	DDR_DATA_1	AA10			
	DDR_DATA_2	AB10			
	DDR_DATA_3	Y10			
	DDR_DATA_4	Y11			
	DDR_DATA_5	Y12			
	DDR_DATA_6	AB12			
	DDR_DATA_7	AA12			
	DDR_DQS_0	AB13		Differential lower Data Strobe	Differential SSTL_2/SSTL_18
	DDR_nDQS_0	AA13			
	DDR_DM_0	AA11	Output	Lower Data Mask	SSTL_2/SSTL_18
	DDR_GATE_0	Y13	I/O	Lower Gate Open	
	DDR_DATA_8	AB15		Data Lines (Upper byte)	
	DDR_DATA_9	AA16			
	DDR_DATA_10	AB16			
	DDR_DATA_11	Y16			
	DDR_DATA_12	Y15			
	DDR_DATA_13	Y14			
	DDR_DATA_14	AB14			

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
DDR I/F	DDR_DATA_15	AA14	I/O	Data Lines (Upper byte)	SSTL_2/SSTL_18
	DDR_DQS_1	AB17		Differential upper Data Strobe	Differential SSTL_2/SSTL_18
	DDR_nDQS_1	AA17			
	DDR_DM_1	AA15	Output	Upper Data Mask	SSTL_2/SSTL_18
	DDR_GATE_1	Y17	I/O	Upper Gate Open	
	DDR_VREF	V10	Input	Reference Voltage	Analog
	DDR_COMP_2V5	V9	Output	Ext. Resistor 2.5V	Analog
	DDR_COMP_GND	V8	-	Common Return for Ext. Resistors	Power
	DDR_COMP_1V8	V7	Output	Ext. Resistor 1.8V	Analog
	DDR2_EN	D11	input	Configuration	TTL Input Buffer 3.3V tolerant, PU
USB	DEV_DP	V1	I/O	USB Device D+	Bidirectional Analog Buffer 5V tolerant
	DEV_DM	V2		USB Device D-	
	DEV_VBUS	R4	Input	USB Device VBUS	TTL Input Buffer 3.3V tolerant, PD
	HOST1_DP	T1	I/O	USB HOST1 D+	Bidirectional Analog Buffer 5V tolerant
	HOST1_DM	T2		USB HOST1 D-	
	HOST1_VBUS	P5	Output	USB HOST1 VBUS	TTL Output Buffer 3.3V capable, 4mA
	HOST1_OVRC	P6	Input	USB Host1 Over-current	TTL Input Buffer 3.3V tolerant, PD
	HOST2_DP	P1	I/O	USB HOST2 D+	Bidirectional Analog Buffer 5V tolerant
	HOST2_DM	P2		USB HOST2 D-	
	HOST2_VBUS	R5	Output	USB HOST2 VBUS	TTL Output Buffer 3.3V capable, 4mA
	HOST2_OVRC	R6	Input	USB Host2 Over-current	TTL Input Buffer 3.3V tolerant, PD
	USB_RREF	U4	Output	Reference resistor	Analog
Master Clock	MCLK_XI	Y1	Input	30 MHz Crystal I	Oscillator 2.5V capable
	MCLK_XO	Y2	Output	30 MHz Crystal O	
RTC	RTC_XI	A9	Input	32KHz Crystal I	Oscillator 1V capable
	RTC_XO	B9	Output	32 KHz Crystal O	
SMI	SMI_DATAIN	L21	Input	Serial Flash Input Data	TTL Input Buffer 3.3V tolerant, PU

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
SMI	SMI_DATAOUT	L20	Output	Serial Flash Output Data	TTL Output Buffer 3.3V capable, 4mA
	SMI_CLK	L22		Serial Flash Clock	
	SMI_CS_0	L19		Serial Flash Chip Selects	
	SMI_CS_1	L18			
SPI	SSP_1_MOSI	AA21	I/O	Master Out Slave In	TTL BIDIR buffer 3.3V capable, 8mA 3.3V tolerant, PU
	SSP_1_MISO	AB21	I/O	Master In Slave Out	
	SSP_1_SCLK	AB22	I/O	Serial Clock	
	SSP_1_SS	AA22	I/O	Slave Select	
	SSP_2_MOSI	K20	I/O	Master Out Slave In	
	SSP_2_MISO	K21	I/O	Master In Slave Out	
	SSP_2_SCLK	K22	I/O	Serial Clock	
	SSP_2_SS_0	K19	I/O	Slave Select	
	SSP_2_SS_1	K18	I/O	Slave Select	
	SSP_3_MOSI	J20	I/O	Master Out Slave In	
	SSP_3_MISO	J21	I/O	Master In Slave Out	
	SSP_3_SCLK	J22	I/O	Serial Clock	
	SSP_3_SS	J19	I/O	Slave Select	
UART	UART1_TXD	AA19	Output	Serial data Out	TTL Output Buffer 3.3V capable, 4mA
	UART2_TXD	AA20	Output		
	UART1_RXD	AB19	Input	Serial Data In	TTL Input Buffer 3.3V tolerant, PD
	UART2_RXD	AB20	Input		
FIRDA	FIRDA_TXD	AA18	Output	Serial data Out	TTL Output Buffer 3.3V capable, 4mA
	FIRDA_RXD	AB18	Input	Serial Data In	TTL Input Buffer 3.3V tolerant, PU
I^2C	SDA	Y18	I/O	Serial data In/Out	TTL BIDIR Buffer 3.3V capable, 4mA 3.3V tolerant, PU
	SCL	Y19	I/O	Serial Clock	
NAND FLASH I/F	NF_IO_0	H19	I/O	Data	TTL BIDIR Buffer 3.3V capable, 4mA 3.3V tolerant, PU

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
NAND FLASH I/F	NF_IO_1	H18	I/O	Data	TTL BIDIR Buffer 3.3V capable, 4mA 3.3V tolerant, PU
	NF_IO_2	G19			
	NF_IO_3	G18			
	NF_IO_4	F19			
	NF_IO_5	F18			
	NF_IO_6	E18			
	NF_IO_7	E19			
	NF_CE	G20	Output	Chip Enable	TTL Output Buffer 3.3V capable, 4mA
	NF_RE	G22		Read Enable	
	NF_WE	H20		Write Enable	
	NF_ALE	H21		Address Latch Enable	
	NF_CLE	G21		Command Latch Enable	
	NF_WP	J18		Write Protect	
	NF_RB	H22	Input	Read/Busy	TTL Input Buffer 3.3V tolerant PU
	MRESET	C17	Input	Main Reset	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
LVDS I/F	PH0	A16	Output	General purpose I/O with LVDS transceiver	LVDS Driver
	PH0n	B16			
	PH1	C16			
	PH1n	C15			
	PH2	A15			
	PH2n	B15			
	PH3	A14			
	PH3n	B14			
	PH4	C14			
	PH4n	C13			
	PH5	A13			
	PH5n	B13			
	PH6	A12			
	PH6n	B12			
	PH7	C12			
	PH7n	C11			
	PH8	A11	Input		LVDS Receiver

Table 2. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
LVDS I/F	PH8n	B11	Input	General purpose I/O with LVDS transceiver	LVDS Receiver
	DIGITAL_REXT	E11	Output	Configuration	Analog 3.3V capable

Note: PU means Pull Up and PD Means Pull Down

Table 3. Power supply

Signal name	Ball	Value
GND	J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, M18, N18, P18, T5, V6, N2, R1, U2, T4, W3, W2, Y3, AA3, V5, U5, V17, U17, A10, E12	0 V
AGND	V16	0 V
VDD3	J6, H6, F8, F9, F16, H17, K17, L17, N17, P17, M6, F17	3.3 V
VDD	G6, L6, G17, M17, R17, F10, F13, F15, J17, T6, U13, U10, U16	1.0 V
HOST2_VDDbc	N1	2.5 V
HOST2_VDDbs	N3	1.0 V
HOST2_VDDb3	R3	3.3 V
HOST1_VDDbc	P3	2.5 V
HOST1_VDDbs	R2	1.0 V
HOST1_VDDb3	R3	3.3 V
DEVICE_VDDbc	U1	2.5 V
DEVICE_VDDbs	U3	1.0 V
DEVICE_VDDb3	T3	3.3 V
USB_PLL_VDDp	V3	1.0 V
USB_PLL_VDDp2v5	W1	2.5 V
MCLK_VDD	AA1	1.0 V
MCLK_VDD2v5	AA2	2.5 V
DITH_VDD2v5	V4	2.5 V
DITH_VDD	U6	1.0 V
SSTL_VDDe	U7, U8, U9, U11, U12, U14, U15	1.8/2.5 V
ADC_AVDD	W16	2.5 V
DDR_PLL_AVDD	W17	2.5 V
DDR_PLL_VDD	T17	1.0 V
LVDS_VDD	F11, F12, F14	2.5 V
RTC_VDD	B10	1.0 V

2.2 Special IOs

2.2.1 USB 2.0 Transceiver

SPEAr Head600 has three USB 2.0 Multimode ATX transceivers. One transceiver will be used by the USB Device controller, and two will be used by the Hosts. These are all integrated into a single USB three-PHY macro.

2.2.2 SSTL_2/SSTL_18

T.B.D.

2.2.3 LVDS

T.B.D.

3 Memory map

3.1 Main memory map

Table 4. Main memory map

START ADDRESS	END ADDRESS	PERIPHERAL	NOTES
0x0000.0000	0x3FFF.FFFF	External SDRAM	DDR1 or DDR2
0x4000.0000	0xBFFF.FFFF	RAS_N/M	Programmable Logic Array
0xC000.0000	0xCFFF.F7FF	AHB_EH2H exp. Interface	
0xCFFF.F800	0xCFFF.FFFF	AHB_EH2H registers	
0xD000.0000	0xD7FF.FFFF	ICM1	Low Speed connection
0xD800.0000	0xDFFF.FFFF	ICM2	Application Subsystem
0xE000.0000	0xE7FF.FFFF	ICM4	High Speed Connection
0xE800.0000	0xEFFF.FFFF	Reserved	
0xF000.0000	0xF7FF.FFFF	ML1,2	Multi Layer CPU subsystem
0xF800.0000	0xFFFF.FFFF	ICM3	Basic Subsystem

3.2 ICM1 - Low speed connection

Table 5. ICM1 - Low speed connection

START ADDRESS	END ADDRESS	PERIPHERAL	NOTES	BUS
0xD000.0000	0xD007.FFFF	UART 1		APB
0xD008.0000	0xD00F.FFFF	UART 2		APB
0xD010.0000	0xD017.FFFF	SPI 1		APB
0xD018.0000	0xD01F.FFFF	SPI 2		APB
0xD020.0000	0xD027.FFFF	I2C		APB
0xD028.0000	0xD07F.FFFF	-	Reserved	-
0xD080.0000	0xD0FF.FFFF	JPEG codec		AHB
0xD100.0000	0xD17F.FFFF	IrDA		AHB
0xD180.0000	0xD1FF.FFFF	FSMC	NAND Flash Controller	AHB
0xD200.0000	0xD27F.FFFF	FSMC	NAND Flash Memory	AHB
0xD280.0000	0xD7FF.FFFF	SRAM	Static Ram Shared memory (8KB)	AHB

3.3 ICM2 - Application subsystem

Table 6. ICM2 - Application subsystem

START ADDRESS	END ADDRESS	PERIPHERAL	NOTES	BUS
0xD800.0000	0xD807.FFFF	Timer 1		APB
0xD808.0000	0xD80F.FFFF	Timer 2		APB
0xD810.0000	0xD817.FFFF	GPIO		APB
0xD818.0000	0xD81F.FFFF	SPI 3		APB
0xD820.0000	0xD827.FFFF	ADC		APB
0xD828.0000	0xDFFF.FFFF	-	Reserved	

3.4 ICM4 - High speed connection

Table 7. ICM4 - High speed connection

START ADDRESS	END ADDRESS	PERIPHERAL	NOTES	BUS
0xE000.0000	0xe07F.FFFF	-	Reserved	APB
0xE080.0000	0xE0FF.FFFF	Ethernet ctrl	GMAC	AHB
0xE100.0000	0xE10F.FFFF	USB2.0 Device	FIFO	AHB
0xE110.0000	0xE11F.FFFF	USB2.0 Device	Configuration Registers	AHB
0xE120.0000	0xE12F.FFFF	USB2.0 Device	Plug Detect	AHB
0xE130.0000	0xE17F.FFFF	-	Reserved	AHB
0xE180.0000	0xE18F.FFFF	USB2.0 EHCI 1		AHB
0xE190.0000	0xE19F.FFFF	USB2.0 OHCI 1		AHB
0xE1A0.0000	0xE1FF.FFFF	-	Reserved	AHB
0xE200.0000	0xE20F.FFFF	USB2.0 EHCI 2		AHB
0xE210.0000	0xE21F.FFFF	USB2.0 OHCI 2		AHB
0xE220.0000	0xE2FF.FFFF	-	Reserved	AHB
0xE280.0000	0xE280.FFFF	ML USB ARB	Configuration Register	AHB
0xE290.0000	0xE7FF.FFFF	-	Reserved	AHB

3.5 ML1, 2 - Multi layer CPU subsystem

Table 8. ML1, 2 - Multi layer CPU subsystem

START ADDRESS	END ADDRESS	PERIPHERAL	NOTES	BUS
0xF000.0000	0xF00F.FFFF	Timer		APB
0xF010.0000	0xF01F.FFFF	GPIO		APB
0xF020.0000	0xF0FF.FFFF	-	Reserved	AHB
0xF100.0000	0xF10F.FFFF	ITC Secondary		AHB
0xF110.0000	0xF11F.FFFF	ITC Primary		AHB
0xF120.0000	0xF7FF.FFFF	-	Reserved	AHB

3.6 ICM3 - Basic subsystem

Table 9. ICM3 - Basic subsystem

START ADDRESS	END ADDRESS	PERIPHERAL	NOTES
0xF800.0000	0xFBFF.FFFF	Serial Flash Memory	
0xFC00.0000	0xFC1F.FFFF	Serial Flash Controller	
0xFC20.0000	0xFC3F.FFFF	LCD Controller	
0xFC40.0000	0xFC5F.FFFF	DMA Controller	
0xFC60.0000	0xFC7F.FFFF	SDRAM Controller	
0xFC80.0000	0xFC87.FFFF	Timer	
0xFC88.0000	0xFC8F.FFFF	Watch Dog Timer	
0xFC90.0000	0xFC97.FFFF	Real Time Clock	
0xFC98.0000	0xFC9F.FFFF	General Purpose I/O	
0xFCA0.0000	0xFCA7.FFFF	System Controller	
0xFCA8.0000	0xFCAF.FFFF	Miscellaneous Registers	
0xFCB0.0000	0xFEFF.FFFF	-	Reserved
0xFF00.0000	0xFFFF.FFFF	Internal Rom	Boot

4 Main Blocks

4.1 7.1 CPU subsystem

4.1.1 Overview

The CPU sub-system includes the following blocks:

- ARM 926EJS
- Two timer channels
- One GPIO block (8 I/O lines)
- Two Interrupt Controller (32 IRQ lines)

4.1.2 CPU ARM 926EJ-S

The processor is the powerful ARM926EJ-S, targeted for multi-tasking applications.

Belonging to ARM9 general purposes family microprocessor, it principally stands out for the Memory Management Unit, which provides virtually memory features, making it also compliant with WindowsCE, Linux and SymbianOS operating systems.

The ARM926EJ-S supports the 32 bit ARM and 16 bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

Besides, it has the ARM debug architecture and includes logic to assist in software debug.

Its main features are:

- CORE f_{MAX} 333 MHz independent programmable for each CPU
- Memory Management Unit
- 16 KB of instruction CACHE
- 16 KB of data CACHE
- Configurable **T**ightly **C**oupled **M**emory (I/D) size trough the configurable logic array
- ARM-V5TEJ instructions set architecture:
  - ARM (32 bit), Thumb® (16 bit)
  - DSP extensions
  - JAVA™ (8 bit) instructions.
- AMBA Bus interface
- Coprocessor interface
- EmbeddedICE-RT
  - Single mode (two connectors)
  - Two processor daisy chained
- ETM9 (Embedded Trace Macro-cell)
  - Single ETM mode (single or double packet configurable)
  - Dual ETM mode (both processors ETM are available in single packet mode)

4.2 Clock and Reset System

The Clock System block is a fully programmable block able to generate all clocks necessary at the chip.

The clocks, at default operative frequency, are:

- clock @ 333 MHz for the CPUs. (note 1)
- clock @ 166 MHz for AHB Bus and AHB peripherals. (note 1)
- clock @ 83 MHz for, APB Bus and APB peripherals. (note 1)
- clock @ 100-333 MHz for DDR memory interface. (note 2)

The frequencies are the maximum allowed value and the user can modify them by programming dedicated registers.

The Clock System consists of 2 main parts: a Multi-Clock Generator block and an two internal PLL.

The Multi-Clock Generator block, starting from a reference signal (which generally is delivered from the PLL), generates all clocks for the IPs of SPEAr Head600 according to dedicated programmable registers.

Each PLL, starting from the oscillator input of 30 MHz, generates a clock signal at a frequency corresponding at the highest of the group, which is the reference signal used by the Multi-Clock Generator block to obtain all the other requested clocks for the group. Its main features is the Electro-Magnetic Interference reduction capability: user has the possibility to set up the PLL in order to modulate with a triangular wave to the VCO clock; the resulting signal will have the spectrum (and the power) spread on a small range (programmable) of frequencies centered on F0 (VCO Freq.), obtaining minimum electromagnetic emissions. This method replace all the other traditional methods of E.M.I. reduction, as filtering, ferrite beads, chokes, adding power layers and ground planets to PCBs, metal shielding etc., allowing sensible cost saving for customers.

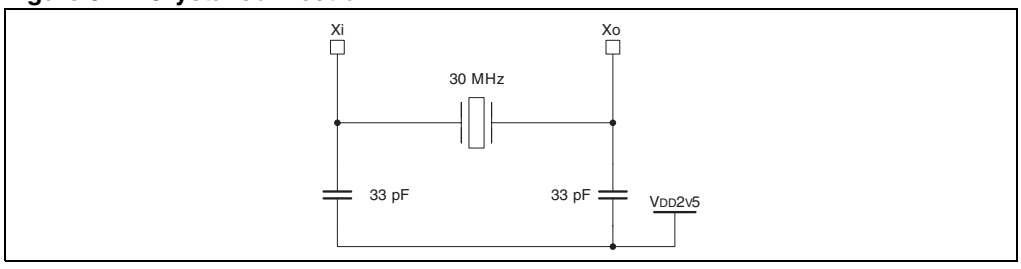
Note: 1 This frequency is based on the PLL1.

2 This frequency is based on the PLL2.

4.3 Main oscillator

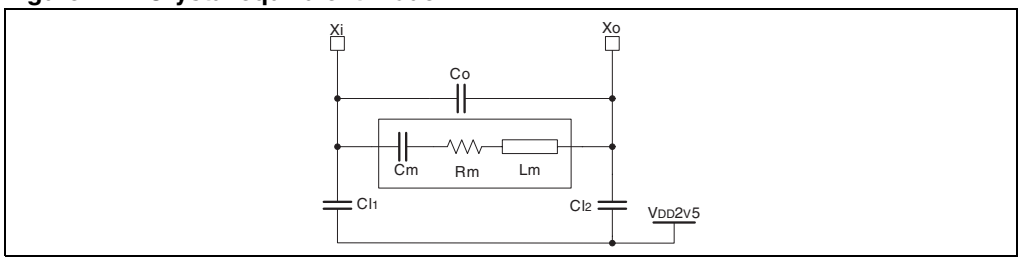
4.3.1 Crystal connection

Figure 3. Crystal connection



4.3.2 Crystal equivalent model

Figure 4. Crystal equivalent model



1. Co is the parasitic capacitance of the crystal package
2. Cl1 and Cl2 are the capacitance on each resonator PAD

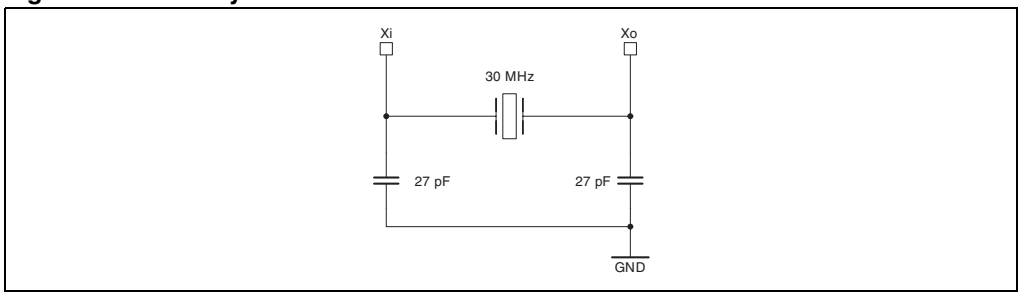
Table 10. Main oscillator characteristics

Supplier	Rm(Ohms)	Lm(mH)	Cm(fF)	Co(pF)	Q(K)
Epson (E31821)	9.3	5.9	4.8	1.7	120
Raltron (M3000)	9.6	2.6	10.8	3.5	45
KSS (KSS3KF)	5	3.2	8.7	2.7	121

4.4 RTC oscillator

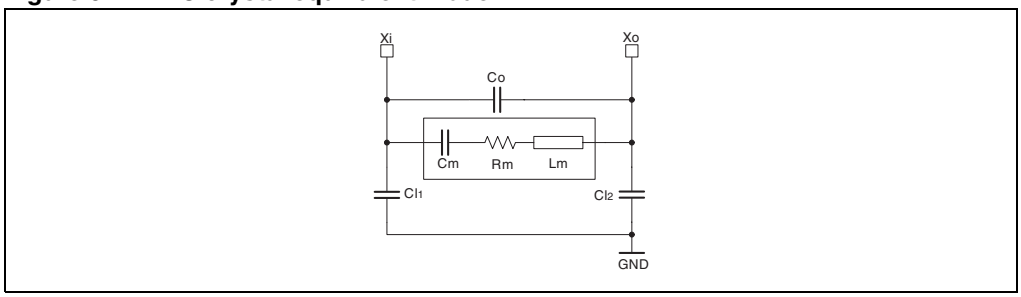
4.4.1 RTC crystal connection

Figure 5. RTC crystal oscillator



4.4.2 RTC crystal equivalent model

Figure 6. RTC crystal equivalent model



1. Co is the parasitic capacitance of the crystal package
2. Cl1 and Cl2 are the capacitance on each resonator PAD

Table 11. RTC oscillator characteristics

Supplier	Rm(KOhms)	Lm(mH)	Cm(fF)	Co(pF)
Ecliptek	<65	10	1.9	0.85

4.5 Ethernet controller

- Compliant with the IEEE 802.3-2002 standard.
- GMII or MII Interface to the external PHY.
- It supports 10/100/1000 Mbps data transfer rates with any one or a combination of the PHY interfaces above;
- Local FIFO available (4Kbyte RX, 2Kbyte TX).
- It supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided for, as well as packet bursting and frame extension at 1000 Mbps.
- Programmable frame length to support both Standard and Jumbo Ethernet frames with size up to 16 Kbytes.
- A variety of flexible addresses filtering modes are supported.
- A set of control and status registers (CSRs) to control GMAC Core operation.
- Native DMA with single-channel Transmit and Receive engines, providing 32/64/128-bit data transfers.
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining.
- An AHB slave acting as programming interface to access all CSRs, for both DMA and GMAC Core subsystems.
- An AHB master for data transfer to system memory.
- 32-bit AHB master bus width, supporting 32, 64, and 128-bit wide data transactions.

4.6 USB2 Host Controller

SPEAr Head600 has two fully independent USB 2.0 Hosts and each one is constituted with 5 major blocks:

- EHCI able to manage the High Speed transfer (HS - 480 Mbits).
- OHCI that manages the Full and the Low Speed transfer (12 and 1.5 Mbits).
- Local FIFO having size of 2 Kbyte
- Local DMA
- Integrated USB2 Transceiver (PHY).

Both the hosts are capable to manage an external Power Switch providing the control line to enable or disable the power and also having an input line to sense the over-current condition detected by the external switch.

4.7 USB2 Device Controller

- It supports the 480 Mbps high-speed (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the low-speed (LS) for USB 1.1.
- It supports 16 physical endpoints and proper configurations to achieve logical endpoints.

EP0	Control (IN/OUT)
EP1~15	Software configurable to: – Bulk In – Bulk Out – Interrupt In – Interrupt Out – Isochronous.

- Integrated USB transceiver (PHY)
- Local FIFO having size of 4 Kbyte shared among all the endpoints.
- Both DMA mode and Slave-Only mode supported.
- In DMA mode, the UDC supports descriptor-based memory structures in application memory.
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs);
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus.
- A USB Plug Detect (UPD) which detects the connection of a cable.

4.8 Low jitter PLL

Within the USB Hosts and device a local Low Jitter PLL is provided to meet the USB2.0 specification requirements.

4.9 Reconfigurable logic array

4.9.1 Overview

The Configurable Logic array consists of an embedded macro where it is possible to implement a custom project by mapping up to 600K equivalent gates.

This macro is interfaced with the rest of the system by some AHB bus, some memory channels and has a direct connection to the 1st ARM processor internal bus. In this way is also possible to customize the TCM memory or add a coprocessor using this macro.

The following memory cuts are available to this block:

- 4 cuts single port with size of 8kB each
- 8 cuts single port with size of 4kB each
- 16 cuts single port with size of 2kB each
- 8 cuts dual port with size of 2kB each
- 4 cuts dual port with size of 4kB each

The array is also connected to 88 I/O (3.3V capable/tolerant and 4 mA sink/source) plus 9 lvds lines (one input and 8 outputs).

The following clocks can be used in the integrated logic:

- 5 different coming from the external balls
- 4 different coming from the integrated frequency synthesizer
- PLL1 frequency
- PLL2 Frequency
- 48 MHz (USB PLL)
- 30 MHZ (MAIN Oscillator)
- 32.768 KHz (RTC Oscillator)
- APB clock (programmable)
- AHB clock (programmable)

4.9.2 Custom project development

The flow to develop a custom project to embed in the SPEAr Head600 is similar to the standard ASIC flow.

The Configurable Logic is an empty module of the whole System on Chip. Pin out and maximum gates are fixed. The HDL project is synthesized using dedicated library and post synthesis simulation is possible to verify the custom net-list.

Regarding the back end flow, after the place and route phase the verification procedure is the same as a standard ASIC flow.

4.9.3 Customization process

The layers used for the IP configuration range from 2 metals - 1 via up to 4 metals - 4 vias. Diffusion and remaining metal/vias are invariant across multiple custom designs. Density and performance scale with number of customization layers.

The Configurable Logic included in the SPEAr Head600 Chip is a 600Kgates equivalent array when customized using 4 metals - 4 vias.

4.9.4 ADC Controller

- Successive approximation ADC;
- 10 bit resolution;
- Up to 1 Msps;
- analog input (AIN) channels, ranging from 0 to 2.5 V;
- INL ± 1 LSB, DNL ± 1 LSB;
- Programmable conversion speed, (min conversion time is 1 µs).
- Programmable average results from 1 (No average) up to 128.

4.10 Other interfaces

4.10.1 UART

Two UART are provided with the following features:

- Separate 16x8 (16 location deep x 8-bit wide) transmit and 16x12 receive FIFOs to reduce CPU interrupts;
- Speed up to 560.8 Kbps.

4.10.2 SPI

Three SPI are provided. The main features are:

- Max speed of 40 Mbps
- Programmable choice of interface operation SPI, Microwire or TI synchronous serial
- Programmable data frame size from 4 to 16 bit.
- The SPI controllers can deal with Master and slave mode.
- A connection with general purpose DMA is provided to reduce the CPU load.

5 Electrical characteristics

5.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages; however it is advisable to take normal precaution to avoid application of any voltage higher than the specified maximum rated voltages.

Table 12. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD} core	Supply Voltage core	1.6	V
V_{DD} I/O	Supply Voltage I/O	4.8	V
V_{DD} PLL	Supply Voltage PLL		V
V_{DD} DDR1	Supply Voltage DRAM I/F (DDR1)	4.8	V
V_{DD} DDR2	Supply Voltage DRAM I/F (DDR2)	4.8	V
V_{DD} RTC	Supply Voltage RTC	1.6	V
T_J	Junction temperature	-40 ~ 125	°C
T_{STG}	Storage temperature	-55 ~ 150	°C

The average chip-junction temperature, Tj, can be calculated using the following equation:

$T_j = T_A + (P_D \cdot \Theta J_A)$

where:

- T_A is the ambient temperature in °C
- ΘJ_A is the package Junction-to-Ambient thermal resistance, which is 34 °C/W
- $P_D = P_{INT} + P_{PORT}$
  - P_{INT} is the chip internal power
  - P_{PORT} is the power dissipation on Input and Output pins; user determined

If P_{PORT} is neglected, an approximate relationship between PD is:

$P_D = K / (T_j + 273\ °C)$

And, solving first equations:

$K = P_D \cdot (T_A + 273\ °C) + \Theta J_A \times P_D^2$

K is a constant for the particular, which can be determined through last equation by measuring P_D at equilibrium, for a know T_A

Using this value of K, the value of P_D and T_J can be obtained by solving first and second equation, iteratively for any value of T_A.

5.2 DC electrical characteristics

Supply voltage specifications

The recommended operating conditions are listed in the following table:

Table 13. DC electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD} core	Supply voltage core	0.95	1	1.05	V
V_{DD} I/O	Supply voltage I/O	3	3.3	3.6	V
V_{DD} PLL	Supply voltage PLL	2.25	2.5	2.75	V
V_{DD} OSC	Supply voltage oscillator	2.25	2.5	2.75	V
V_{DD} DDR1	Supply voltage DRAM I/F (DDR1)	2.25	2.5	2.75	V
V_{DD} DDR2	Supply voltage DRAM I/F (DDR2)	1.7	1.8	1.9	V
V_{DD} RTC	Supply voltage RTC	0.95	1	1.05	V
T_{OP}	Operating temperature	-40		85	°C

6 Package information

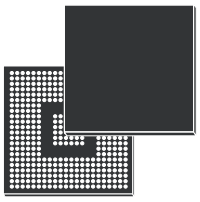
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

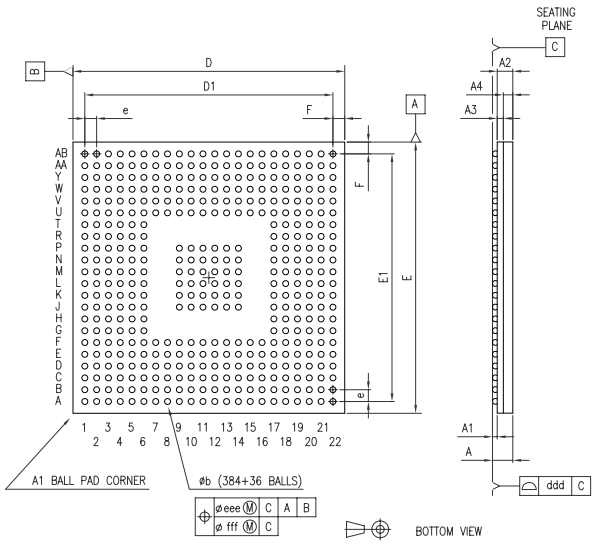
Figure 7. PBGA420 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.81			0.0713
A1	0.27			0.0106		
A2		1.305			0.0514	
A3		0.52			0.0205	
A4		0.785			0.0309	
b	0.45	0.50	0.55	0.0177	0.0197	0.0217
D	22.80	23.00	23.20	0.8976	0.9055	0.9134
D1		21.00			0.8268	
E	22.80	23.00	23.20	0.8976	0.9055	0.9134
E1		21.00			0.8268	
e		1.00			0.0394	
F		1.00			0.0394	
ddd			0.20			0.0079
eee			0.25			0.0098
fff			0.10			0.0039

OUTLINE AND MECHANICAL DATA



PBGA420 (23x23x1.81mm)
Ball **G**rid **A**rray **P**ackage



7 Revision history

Table 14. Document revision history

Date	Revision	Changes
28-Feb-2007	1	Initial release.

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