Integrated Circuit Systems, Inc.

# AV9107C-19
# AV9107C-20

# Frequency Generator for Fibre Channel Systems

## General Description

The **AV9107C-19** and **AV9107C-20** are high-speed clock generators designed to support fibre channel system requirements. The **AV9107C-19** generates a single copy of the 106.25 MHz from a 17 MHz crystal. The **AV9107C-20** provides a second copy of the 106.25 MHz clock with output skew less than ±100ps.

An exact frequency multiplying ratio ensures better than ±100 ppm frequency accuracy using a standard AT crystal with external load capacitors (typically 33pF±5% for an 18pF load crystal). Achieving ±100 ppm over four years requires the crystal to have a ±20 ppm initial accuracy, ±30 ppm tempera-ture and ±5 ppm/year aging coefficients.

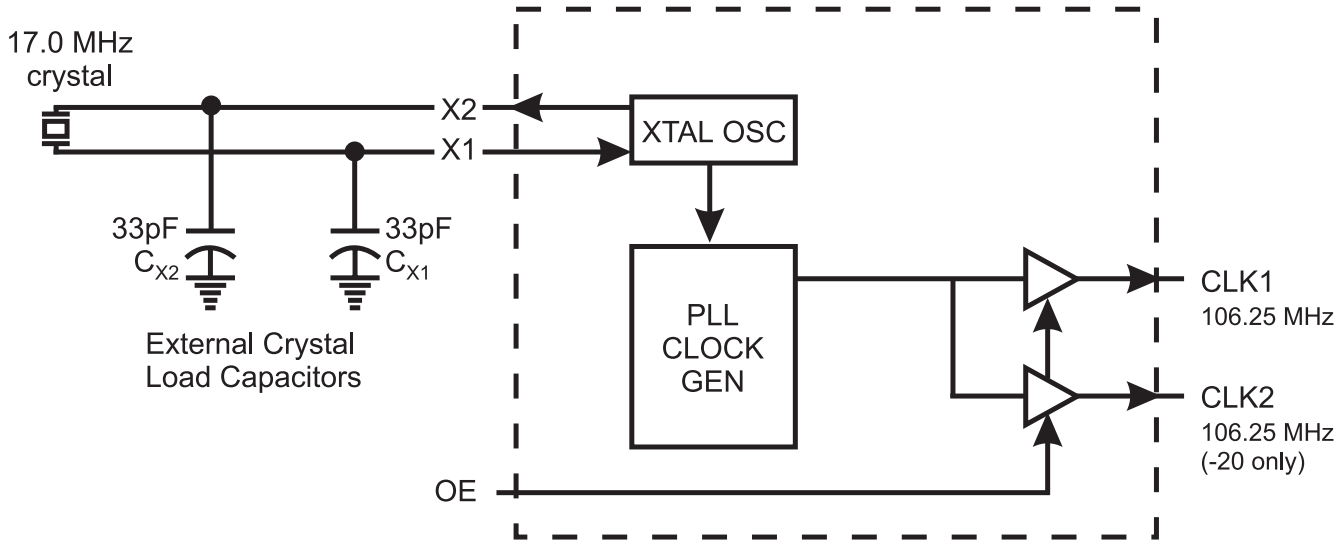
## Features

- Generates one or two 106.25 MHz clocks from a 17 MHz crystal
- Less than 60ps one sigma jitter
- Less than ±200ps absolute jitter
- Output skew less than ±100ps on two channel version (-20)
- Rise/fall times less than 4ns driving 15pF
- On-chip loop filter components
- 3.0V-5.5V supply range
- 8-pin, 150-mil SOIC package

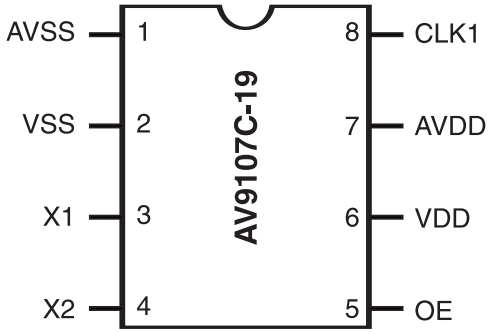
## Applications

- Specifically designed to support the high-speed clocking requirements of fibre channel systems

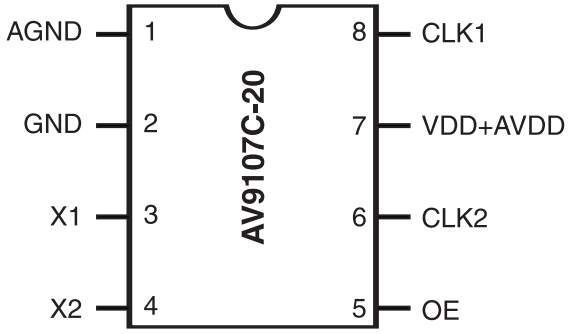
## Block Diagram



## Pin Configurations




8-Pin SOIC




8-Pin SOIC

## Functionality

| OE | X1, X2 (MHz) | FOUT (MHz) |
|---|---|---|
| 1 | 17.00 | 106.25 |
| 0 | X | Tristate |

## Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | AVSS | PWR | Analog ground. |
| 2 | VSS | PRW | Digital Ground. |
| 3 | X1 | IN | Crystal or clock input to device; nominally 17.0 MHz. Requires external load capacitors. |
| 4 | X2 | IN | Crystal drive output from device. Requires external load capacitors. |
| 5 | OE | IN | Output enable causes all outputs to tristate when at a logic low level; has a pull-up. |
| 6 | VDD<br>CLK2 | PWR<br>OUT | +3.3 or +5.0 volt supply (-19).<br>106.25 MHz clock output (-20). |
| 7 | AVDD<br>VDD+AVDD | PWR<br>PWR | Analog power. (Must equal digital power voltage) (-19).<br>Digital and analog power, +3.3 or +5.0 volt supply (-20). |
| 8 | CLK1 | OUT | 106.25 MHz clock output. |

## Absolute Maximum Ratings

AVDD, VDD referenced to GND . . . . . 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics at 5.0V

Operating $V_{DD}$ = +4.5V to +5.5V; $T_A$ =0°C to 70°C unless otherwise stated

| DC Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| Input Low Voltage | $V_{IL}$ | | - | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | 2.0 | - | - | V |
| Input Low Current | $I_{IL}$ | $V_{IN}$=0V (Pull-up input) | -16.0 | -6.0 | - | µA |
| Input High Current | $I_{IH}$ | $V_{IN}=V_{DD}$ | -2.0 | - | 2.0 | µA |
| Output Low Voltage[1] | $V_{OL}$ | $I_{OL}$=10mA | - | 0.15 | 0.40 | V |
| Output High Voltage[1] | $V_{OH}$ | $I_{OH}$=-30mA | 2.4 | 3.25 | - | V |
| Output Low Current[1] | $I_{OL}$ | $V_{OL}$=0.8V | 22.0 | 35.0 | - | mA |
| Output High Current[1] | $I_{OH}$ | $V_{OH}$=2.0V | - | -50.0 | -35.0 | mA |
| Supply Current | $I_{DD}$ | Unloaded | - | 22.0 | 45.0 | mA |
| Pull-up Resistor[1] | $R_{pu}$ | | - | 380.0 | 700.0 | k ohms |
| **AC Characteristics** | | | | | | |
| Rise Time[1] | $T_{r1}$ | 15pF load, 0.8 to 2.0V | - | 0.8 | 1.4 | ns |
| Fall Time[1] | $T_{f1}$ | 15pF load, 2.0 to 0.8V | - | 0.7 | 1.2 | ns |
| Rise Time[1] | $T_{r2}$ | 15pF load, 20% to 80% | - | 1.5 | 2.0 | ns |
| Fall Time[1] | $T_{f2}$ | 15pF load, 80% to 20% | - | 1.0 | 1.5 | ns |
| Duty Cycle[1] | $D_t$ | 15pF load @ 1.4V | 42.0 | 49.0 | 55.0 | % |
| Jitter, One Sigma[1] | $T_{i1s}$ | 15pF load | - | 30.0 | 60.0 | ps |
| Jitter, Absolute[1] | $T_{jab}$ | 15pF load | -200.0 | | 200.0 | ps |
| Output Skew,[1] Clock 1 to 2 | $t_{sk1}$ | 15pF load @ 1.4V (-20 only) | -100.0 | -20.0 | 100.0 | ps |
| Input Frequency[1] | $F_i$ | | 11.0 | 17.0 | 19.0 | MHz |
| Output Frequency[1] | $F_o$ | | 2.0 | 106.25 | 120.0 | MHz |
| Power-up Time[1] | $T_{pu}$ | | - | 7.58 | 18.0 | ms |
| Transition Time[1] | $T_{ft}$ | 8 to 66.6 MHz | - | 6.0 | 13.0 | ms |
| Crystal Input Capacitance[1] | $C_{inx}$ | X1 (Pin 3)<br>X2 (Pin 4) | - | 5.0 | - | pF |

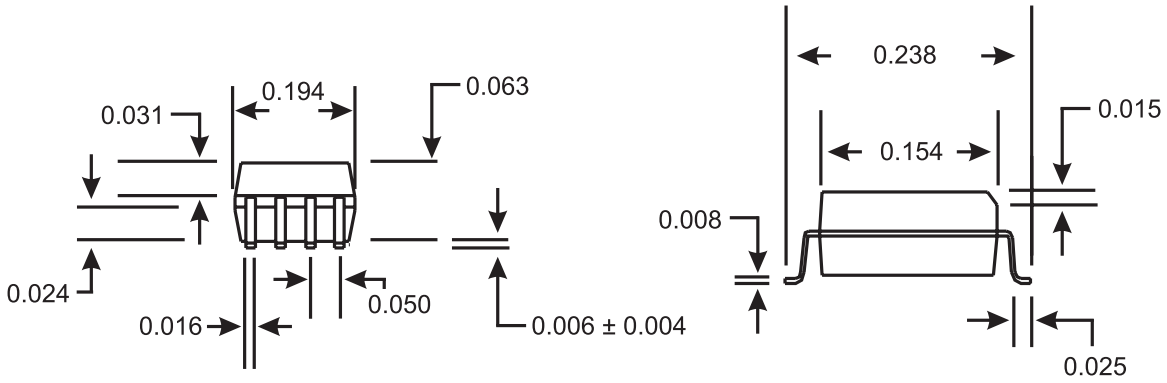
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Electrical Characteristics at 3.3V

Operating $V_{DD}$ = +3.0V to +3.7V; $T_A$ =0°C to 70°C unless otherwise stated

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | - | - | $0.20V_{DD}$ | V |
| Input High Voltage | $V_{IH}$ | | $0.7V_{DD}$ | - | - | V |
| Input Low Current | $I_{IL}$ | $V_{IN}$=0V (Pull-up input) | -7.0 | -2.5 | - | µA |
| Input High Current | $I_{IH}$ | $V_{IN}=V_{DD}$ | -2.0 | - | 2.0 | µA |
| Output Low Voltage[1] | $V_{OL}$ | $I_{OL}$=6mA | - | $0.05V_{DD}$ | $0.1V_{DD}$ | V |
| Output High Voltage[1] | $V_{OH}$ | $I_{OH}$=-5mA | $0.85V_{DD}$ | $0.92V_{DD}$ | - | V |
| Output Low Current[1] | $I_{OL}$ | $V_{OL}=0.2V_{DD}$ | 15.0 | 22.0 | - | mA |
| Output High Current[1] | $I_{OH}$ | $V_{OH}=0.7V_{DD}$ | - | -17.0 | -10.0 | mA |
| Supply Current | $I_{DD}$ | Unloaded | - | 14.0 | 30.0 | mA |
| Pull-up Resistor[1] | $R_{pu}$ | | - | 550.0 | 900.0 | k ohms |
| **AC Characteristics** | | | | | | |
| Rise Time[1] | $T_{r1}$ | 15pF load, 0.8 to 2.0V | - | 1.6 | 3.5 | ns |
| Fall Time[1] | $T_{f1}$ | 15pF load, 2.0 to 0.8V | - | 0.9 | 1.5 | ns |
| Rise Time[1] | $T_{r2}$ | 15pF load, 20% to 80% | - | 1.8 | 2.5 | ns |
| Fall Time[1] | $T_{f2}$ | 15pF load, 80% to 20% | - | 1.1 | 2.5 | ns |
| Duty Cycle[1] | $D_t$ | 15pF load @ 1.4V | 30.0 | 40.0 | 50.0 | % |
| Jitter, One Sigma[1] | $T_{j1s}$ | 15pF load | - | 30.0 | 80.0 | ps |
| Jitter, Absolute[1] | $T_{jab}$ | 15pF load | -200.0 | - | 200.0 | ps |
| Output Skew,[1] Clock 1 to 2 | $t_{sk1}$ | 15pF load @ 1.4V (-20 only) | -100.0 | -25.0 | 100.0 | ps |
| Input Frequency[1] | $F_i$ | | 11.0 | 17.0 | 19.0 | MHz |
| Output Frequency[1] | $F_o$ | | 2.0 | 106.25 | 120.0 | MHz |
| Power-up Time[1] | $T_{pu}$ | | - | 7.58 | 18.0 | ms |
| Transition Time[1] | $T_{ft}$ | 8 to 66.6 MHz | - | 6.0 | 13.0 | ms |
| Crystal Input Capacitance[1] | $C_{inx}$ | X1 (Pin 3)<br>X2 (Pin 4) | - | 5.0 | - | pF |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.




**8-Pin Plastic SOIC Package**

## Ordering Information

**AV9107C-19CS08 orAV9107C-20CS08**

Example:

**XXX XXXX-PPP M X#W**

**Lead Count & Package Width**
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

**Package Type**
S=SOIC

**Pattern Number (2 or 3 digit number for parts with ROM code patterns)**

**Device Type (consists of 3 or 4 digit numbers)**

**Prefix**
ICS, AV=Standard Device