PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83940-02

LOW SKEW, 1-TO-18 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

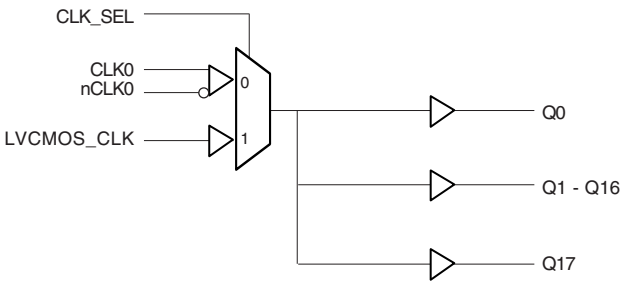
The ICS83940-02 is a low skew, 1-to-18 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The 83940-02 has two selectable clock inputs. The CLK0, nCLK0 pair can accept most standard differential input levels. The single ended clock input accepts LVCMOS or LVTTL input levels.The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 18 to 36 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83940-02 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940 ideal for those clock distribution applications demanding well defined performance and repeatability.

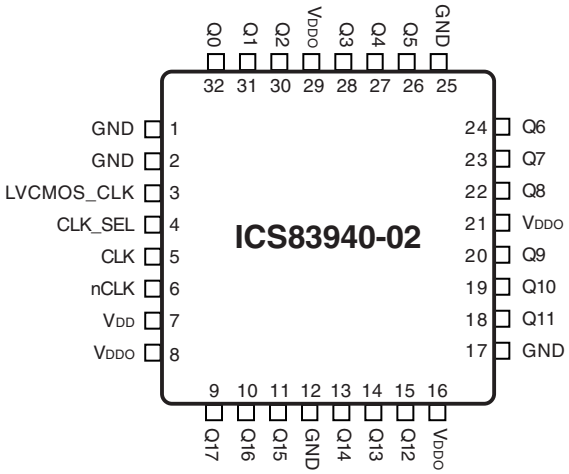
FEATURES

- 18 LVCMOS outputs, 7Ω typical output impedance
- Selectable LVCMOS clock or CLK0, nCLK0 input pair
- LVCMOS_CLK supports the following input types: LVCMOS or LVTTL
- CLK0, nCLK0 pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maxmim output frequency up to 200MHz
- Output skew: 150ps (maximum)
- Part-to-part skew: TBDps (maximum)
- Full 3.3V, 2.5V or mixed 3.3V, 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Pin compatible with the MPC940L in single supply applications

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Pacakge
7mm x 7mm x 1.4mm package body
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Output power supply ground. Connect to ground.
3	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK0, nCLK0 inputs when LOW.
5	CLK0	Input	Pulldown	Non-inverting differential clock input.
6	nCLK0	Input	Pullup	Inverting differential clock input
7	V_{DD}	Power		Positive supply pin. Connect to 3.3V or 2.5V.
8, 16, 21, 29	V_{DDO}	Power		Output supply pins. Connect to 3.3V or 2.5V.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. 7Ω typical output impedance. LVCMOS interface levels

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V				pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V				pF
		V_{DD}, V_{DDO} = 2.625V				pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	**CLK0, nCLK0**	**LVCMOS_CLK**
0	Selected	De-selected
1	De-selected	Selected

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK-SEL	LVCMOS_CLK	CLK0	nCLK0	Q0 thru Q17		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section on page 13, Figure 8, which discusses wiring the differential input to accept single ended levels.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD}+0.5 V
Outputs, V_O	-0.5V to V_{DDO}+0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, Tstg	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				70	mA
I_{DDO}	Output Supply Current					mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		V_{DD} + 0.3	V
		CLK_SEL					
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	LVCMOS_CLK, CLK_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	LVCMOS_CLK, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.4			V
V_{OL}	Output Low Voltage; NOTE 1					0.6	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See page 10, Figure 1A, 3.3V Output Load Test Circuit.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK0	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK0	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK0	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay; NOTE 1	0 ≤ f ≤ 200MHz	2.3		4	ns
tp_{HL}	Propagation Delay; NOTE 1	0 ≤ f ≤ 200MHz				ns
*t*sk(o)	Output Skew; NOTE 2, 4	Measured on rising edge @V_{DDO}/2			150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4	Measured on rising edge @V_{DDO}/2			TBD	ps
t_R	Output Rise Time	20% to 80% @ 50MHz				ns
t_F	Output Fall Time	20% to 80% @ 50MHz				ns
odc	Output Duty Cycle		45	50	55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Uusing the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%; V_{DDO} = 2.5V±5%, TA = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Input Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current					mA
I_{DDO}	Output Supply Current					mA

TABLE 4E. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5%; V_{DDO} = 2.5V±5%, TA = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		V_{DD} + 0.3	V
		CLK_SEL					
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	LVCMOS_CLK, CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	LVCMOS_CLK, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.6	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See page 10, Figure 1B, 3.3V/2.5V Output Load Test Circuit.

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%; V_{DDO} = 2.5V±5%, TA = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0	V_{DD} = V_{IN} = 3.465V			150	µA
		nCLK0	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK0	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK0	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%; V_{DDO} = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay; NOTE 1	0 ≤ f ≤ 200MHz				ns
tp_{HL}	Propagation Delay; NOTE 1	0 ≤ f ≤ 200MHz				ns
*t*sk(o)	Output Skew; NOTE 2, 4	Measured on rising edge @V_{DDO}/2				ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4	Measured on rising edge @V_{DDO}/2				ps
t_R	Output Rise Time	20% to 80% @ 50MHz				ns
t_F	Output Fall Time	20% to 80% @ 50MHz				ns
odc	Output Duty Cycle		45	50	55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Uusing the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Input Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current					mA
I_{DDO}	Output Supply Current					mA

TABLE 4H. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		2.96	V
		CLK_SEL					
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
		CLK_SEL					
I_{IH}	Input High Current	LVCMOS_CLK, CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	LVCMOS_CLK, CLK_SEL	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See page 11, Figure 1C, 2.5V Output Load Test Circuit.

TABLE 4I. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0	$V_{DD} = V_{IN} = 2.625V$			150	µA
		nCLK0	$V_{DD} = V_{IN} = 2.375V$			5	µA
I_{IL}	Input Low Current	CLK0	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
		nCLK0	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay; NOTE 1	0 ≤ f ≤ 200MHz				ns
tp_{HL}	Propagation Delay; NOTE 1	0 ≤ f ≤ 200MHz				ns
*t*sk(o)	Output Skew; NOTE 2, 4	Measured on rising edge @$V_{DDO}/2$				ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4	Measured on rising edge @$V_{DDO}/2$				ps
t_R	Output Rise Time	20% to 80% @ 50MHz				ns
t_F	Output Fall Time	20% to 80% @ 50MHz				ns
odc	Output Duty Cycle		45	50	55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Uusing the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

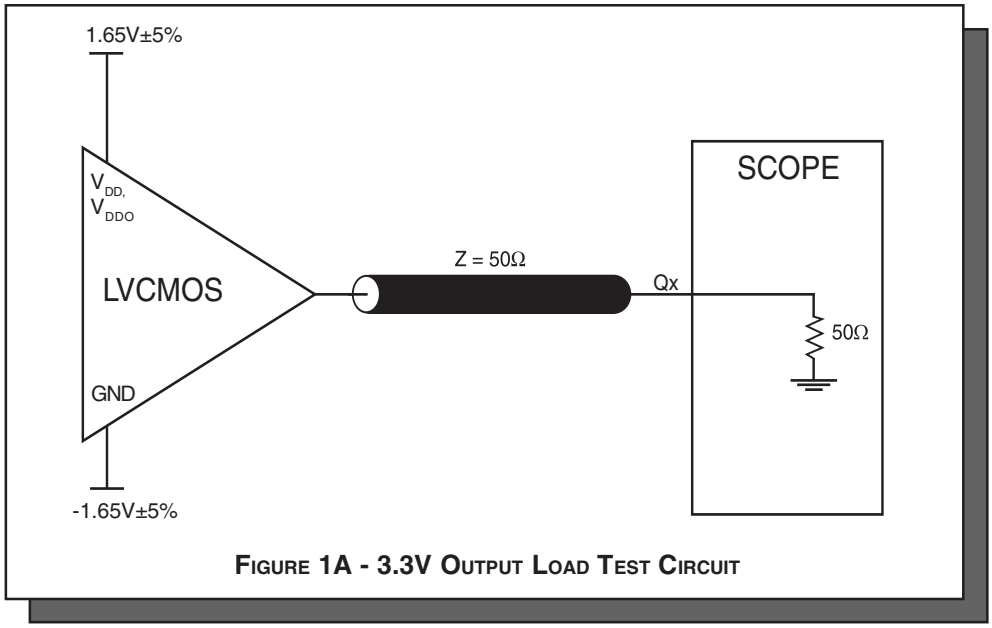


FIGURE 1A - 3.3V OUTPUT LOAD TEST CIRCUIT

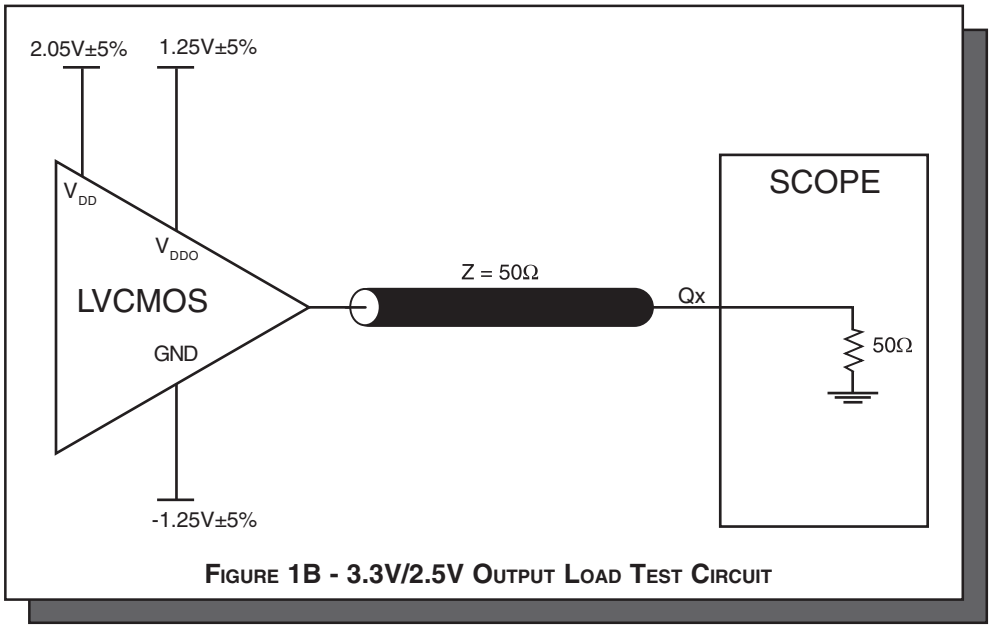


FIGURE 1B - 3.3V/2.5V OUTPUT LOAD TEST CIRCUIT

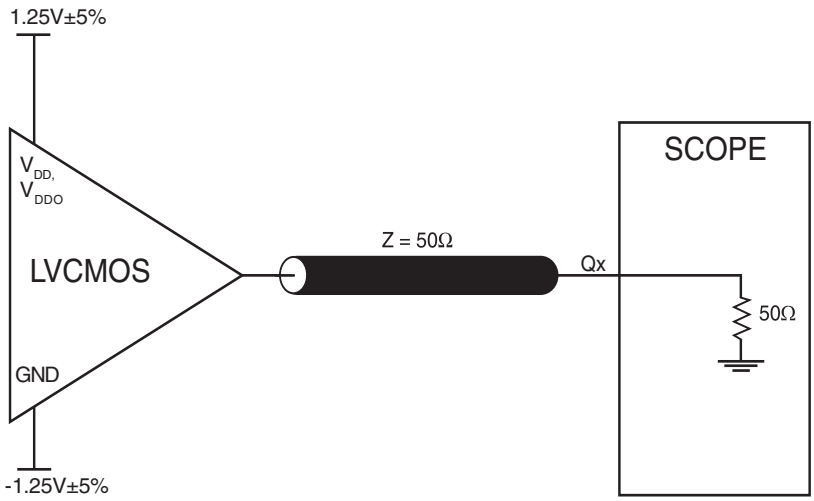


FIGURE 1C - 2.5V OUTPUT LOAD TEST CIRCUIT

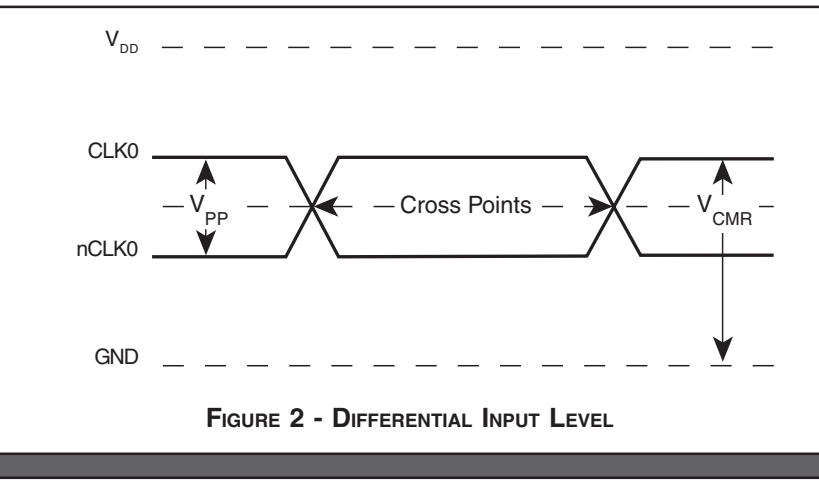


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

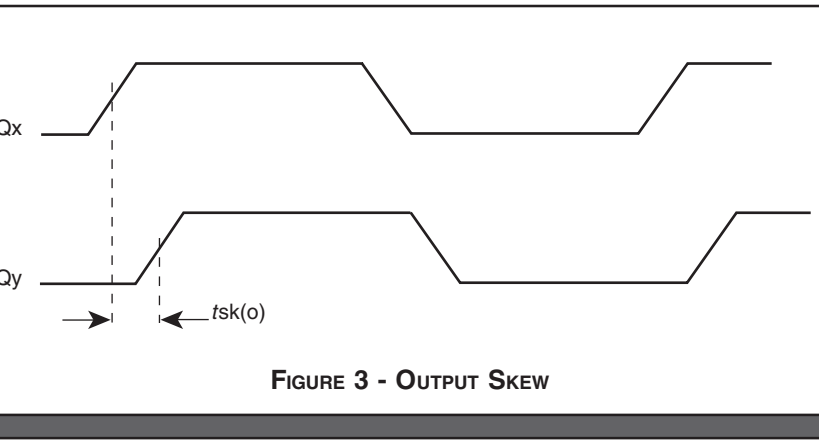


FIGURE 3 - OUTPUT SKEW

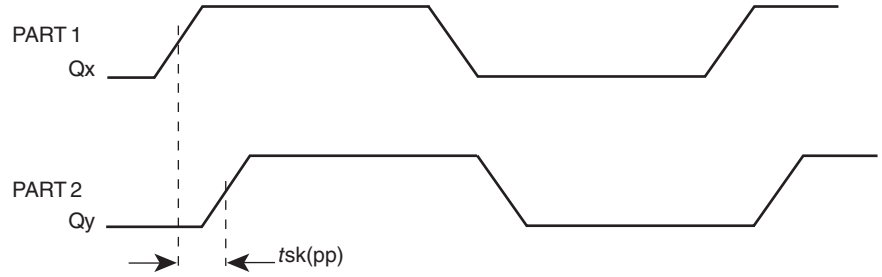


FIGURE 4 - PART-TO-PART SKEW

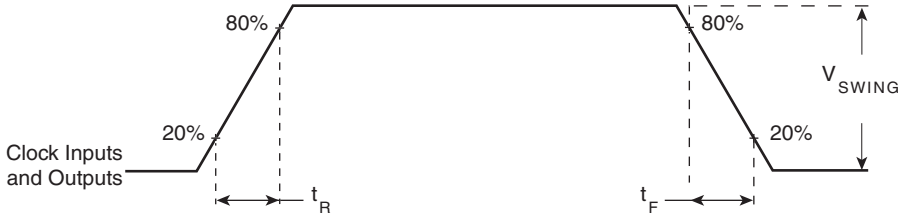


FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

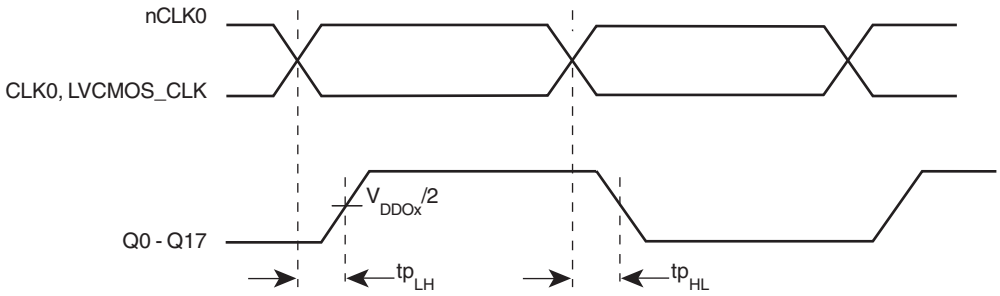


FIGURE 6 - PROPAGATION DELAY

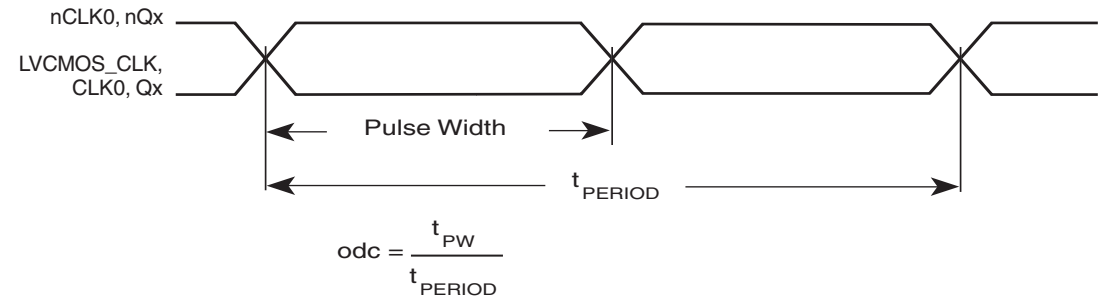


FIGURE 7 - odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

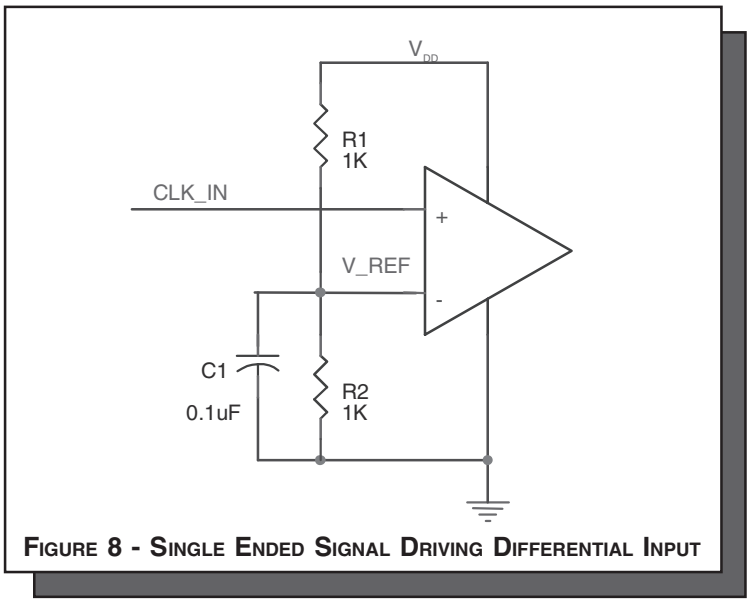


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83940-02 is: 4270

PACKAGE OUTLINE - Y SUFFIX

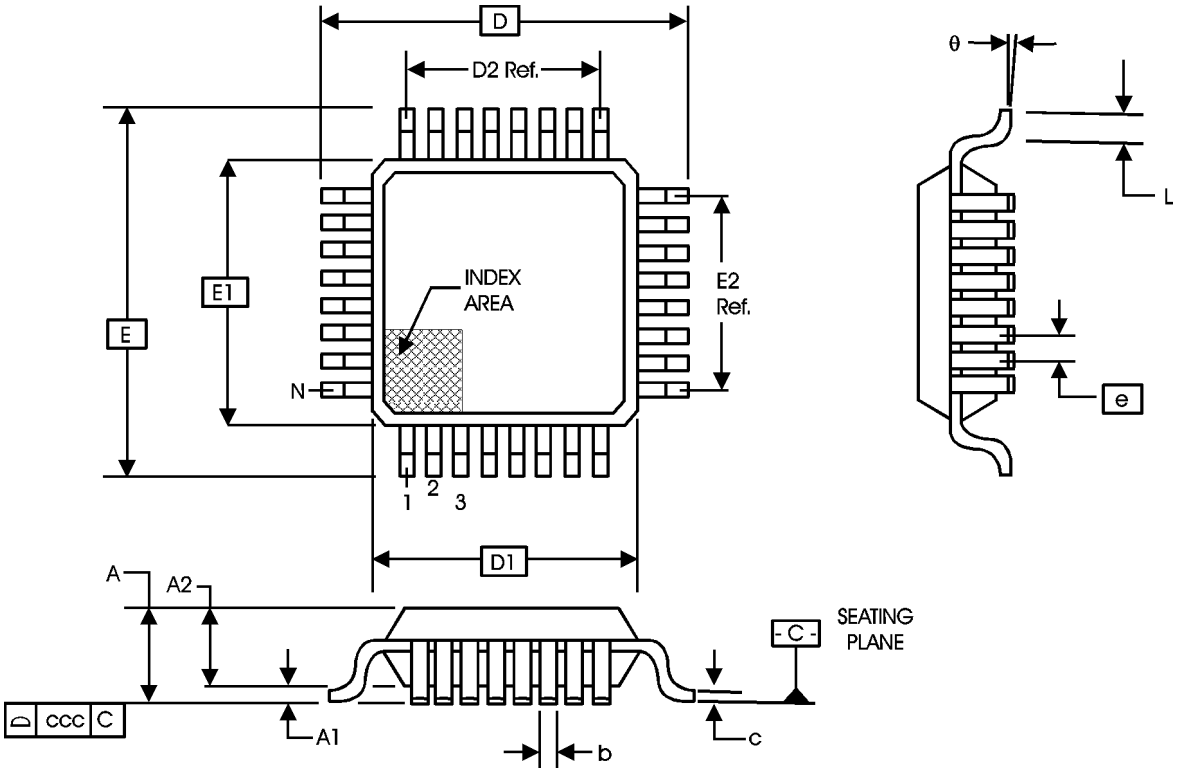


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83940AY-02	ICS83940AY-02	32 Lead LQFP	250 per tray	0°C to 70°C
ICS83940AY-02T	ICS83940AY-02	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C