Features

- Compatible with ST-BUS
- 8 full duplex, 32-channel time-division multiplexed (TDM) data streams
- 256 ports non-blocking switch
- Power supply: 5V (8980) and 3.3V (8980L)
- Microprocessor interface
- Tri-state serial output port

Applications

- PBX
- Central office
- Access Switch

Ordering Information

Part Number	Package
PT7A8980P	40-Pin DIP
PT7A8980J	44-Pin PLCC
PT7A8980LJ	44-Pin PLCC
PT7A8980JE	Lead free 44-Pin PLCC
PT7A8980LJE	Lead free 44-Pin PLCC

Description

PT7A8980/8980L is designed to handle data in ST-BUS format. It interfaces with a microprocessor to switch PCM-encoded voice or data in application areas such as modern digital exchange, PBX and Central Office.

PT7A8980/8980L can simultaneously connect up to 256 channels of 64 kbit/s each. It has 8 data stream inputs and 8 data stream outputs. Each data stream consists of 32 multiplexed 64 kbit/s channels which is compatible to 2048 kbit/s ST-BUS format.

Its microprocessor interfaces not only allow access to the internal registers and memory, but also provide means to read from the input channels or to write to the output channels.

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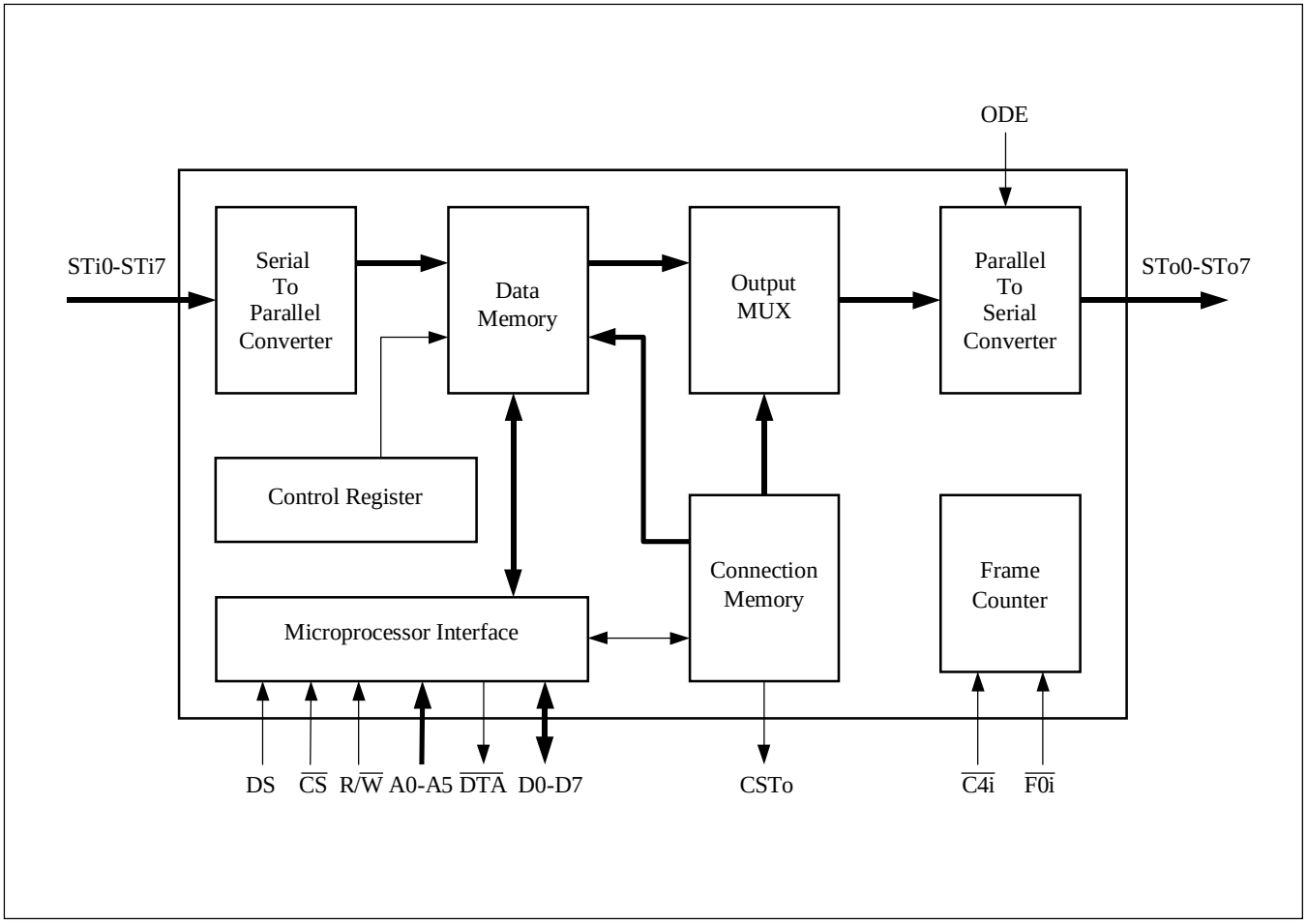
Block Diagram

Figure.1 Block Diagram



Pin Information

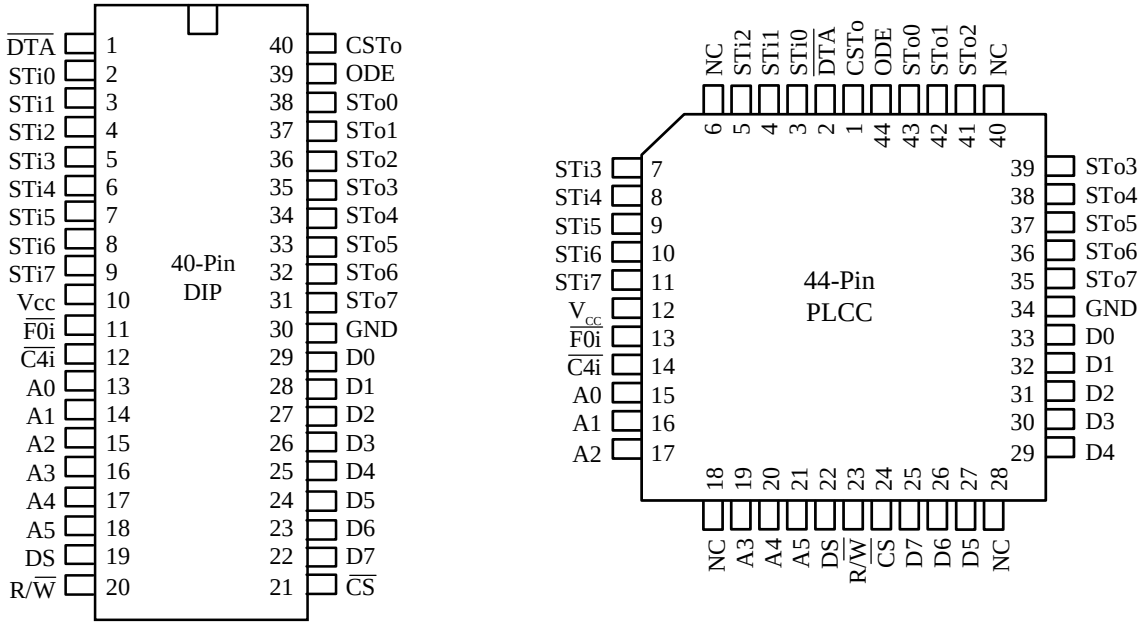
Pin Assignment

Table1. Pin Assignment

Group	Symbol	Function
Chip Clock	$\overline{C4i}$, $\overline{F0i}$	Clock
Power & Ground	GND, Vcc	Power
Microprocessor Interface	$\overline{CS}$, DS, $\overline{DTA}$, ODE, CSTo, R/$\overline{W}$, A0~A5	Control or Data
I/O Interface	D0-D7, STi0-STi7, STo0-STo7	Data

Pin Configuration

Figure 2. Pin Configuration



Pin Description

Table 2. Pin Description

Pin		Name	Type	Description
PDIP	PLCC			
1	2	$\overline{DTA}$	O	**Data Acknowledgement (Open Drain Output).** This pin, when pulled low, acknowledges the microprocessor that the chip has processed the data. Using 1kΩ 1/4W pull-up resistor is recommended.
2-4	3-5	STi0-STi2	I	**0~2 ST-BUS data stream input**. Input pin of 2048 kbit/s ST-BUS data stream.
5-9	7-11	STi3-STi7	I	**3~7 ST-BUS data stream input**. Input pin of 2048kbit/s ST-BUS data stream.
10	12	Vcc	Power	**Power supply.**
11	13	$\overline{F0i}$	I	**Framing signal, active low.** It is the input pin that provides the frame synchronization pulse for 2048kbit/s ST-BUS data stream. A low level on this input pin causes the internal counter to reset on the next negative transition of $\overline{C4i}$ signal.
12	14	$\overline{C4i}$	I	**4.096 MHz clock**. The bit cell boundaries of operating ST-BUS data stream are aligned with every other falling edges of this clock.
13-15	15-17	A0-A2	I	**Address line 0~2**. Address pins of the control interface.
16-18	19-21	A3-A5	I	**Address line 3~5**. Address pins of the control interface.
19	22	DS	I	**Data Strobe.** Data strobe pin of the control interface, active high.
20	23	R/$\overline{W}$	I	**Read or Write Signal.** The read or write signal pin of the control interface, high level for read, low level for write.
21	24	$\overline{CS}$	I	**Chip select signal.** Chip selects signal pin of the control interface, active low.
22-24	25-27	D5-D7	I/O	**Data Buses 5~7**. Bi-directional data pins of the control interface.
25-29	29-33	D0-D4	I/O	**Data Buses 0~4.** Bi-drectional data pins of the control interface.
30	34	GND	Power	**Connected to ground.**
31-35	35-39	STo3-STo7	O	**ST-BUS Data Stream Output 3~7.** Output pins of 2048 kbit/s ST-BUS data stream.
36-38	41-43	STo0-STo2	O	**ST-BUS Data Stream Output 0~2**. Output pins of 2048 kbit/s ST-BUS data stream.
39	44	ODE	I	**Output Drive Enable**. If its input is held high, STo0~STo7 outputs behave normally. If its input is held low, STo0~STo7 outputs are forced into high impedance state. [Note]: Even when ODE is high level, certain channels of STo0~STo7 output stream can also enter into high impedance state under software control.
40	1	CSTo	O	**Supplement ST-BUS Output.** This pin also outputs serial data stream of ST-BUS format. Each frame has 256 bits, containing the values of bit 1 in all Connection Memory High (256 locations).

Functional Description

ST-BUS (Serial Telecom Bus) is widely used in bus architecture. It supports digital voice, data switching and inter-processor communication within the Telecommunication Switch or Access System. The ST-BUS data stream has a bit rate of 2048 kbit/s. It' s organized in frames of 125 µs. Each frame contains 32 channels, and each channel contains one byte of serial data.

The PT7A8980/8980L is designed to handle data in the ST-BUS format. It combines data switching function and inter-processor communication function into one device. Therefore, it' s suitable for use in distributed processing systems to switch digitized voice or data in ST-BUS format.

The PT7A8980/8980L can perform the data switching between channels on ST-BUS input and channels on ST-BUS output. The microprocessor can read the data from any ST-BUS input channel or write the data to any ST-BUS output channel via the microprocessor interface . The microprocessor communicates with the PT7A8980/8980L in the same way as with its external memory. By writing to the PT7A8980/8980L, the microprocessor can either establish switched connections between one ST-BUS input channel and one ST-BUS output channel or transmit specific messages to ST-BUS output channels. On the other hand, by reading from the PT7A8980/8980L, the microprocessor can receive messages from ST-BUS input channel or check which switching connections have been already established.

Input and Output Control

2048 kbit/s ST-BUS data goes to the chip through 8 ST-BUS inputs (STi0-STi7) of the PT7A8980/8980L. Each ST-BUS input data stream contains 32 channels, each channel contains 8 bits. After entering into the chip, the 8 bit data is converted into parallel form, and is stored in one of the 256 x 8 Voice or Data Memory locations. Each byte location in the Data Memory is associated with a channel on one of the 8 ST-BUS input data streams.

Similarly, each location of 256 x 11 Connection Memory is also associated with a channel on one of the ST-BUS output data streams . The Connection Memory is divided into two parts, high and low. In each memory location, the high part contains 3 bits, the low part contains 8 bits. When a data is due to be transmitted to a ST-BUS output, the data of the channel can either be switched from a ST-BUS input channel or can originate from the microprocessor. If the data is switched from an channel, the contents of the Connection Memory Low Location associated with the output channel will be used to address the Data Memory. Since this Data Memory address corresponds to a specific channel on a ST-BUS input stream, the data from this input channel is switched to be put out to the proper output channel. If the data to an output channel originates from the microprocessor (Message Mode), the contents of the Connection Memory Low Location associated with the output channel are output directly, and this data is output repetitively on the channel every frame until the microprocessor intervenes.

Microprocessor Interface and Address Selection

The Microprocessor Interface consists of data lines D7-D0, address lines A5-A0 and control signals $\overline{CS}$, $\overline{DTA}$. The microprocessor can access the Control Register as well as the memory inside the chip via the Microprocessor Interface. There are two parts of any address of the Data Memory and Connection Memory. The higher 3 bits come from the Control Register, and the lower 5 bits come from the address lines directly.

Table 3. Address Memory Map

A5	A4	A3	A2	A1	A0	Hex Address	Location
0	x	x	x	x	x	00-1F	Control Register*
1	0	0	0	0	0	20	Channel 0**
1	0	0	0	0	1	21	Channel 1**
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	3F	Channel 31**

* Writing to the Control Register is the only fast transaction.
** Memory and Data Stream are specified by the contents of the Control Register.

As shown in Table 3 above, whether the processor access the Control Register or the internal memory depends on the status of address line A5. If A5 is 0, the Control Register is addressed regardless of the value of the other address lines. If A5 is 1, the internal memory is addressed. In this case, the contents of the Control Register bits 4~3 determine whether Connection Memory High or Low or Data Memory is accessed. The Control Register bits 2~0 select the memory address associated with the particular data stream, while address lines A4~A0 select the memory location corresponding to the channel of this data stream.

ST-BUS Timing Reference

All ST-BUS timing is referenced to the $\overline{C4i}$ and $\overline{F0i}$ inputs. These two clock signals must be synchronized to each other, and compliant with the timing requirements specified in Figure 9. The $\overline{C4i}$ is a 4.096 MHz clock, and the $\overline{F0i}$ at 8 kHz is the frame synchronization signal of data stream.

Control Register

The data in the Control Register consists of Mode Control bits, Memory Select bits and Data Stream Address bits (see Figure 3 and Table 4). The Mode Control bits consist of bits 6~7. Bit 7 of the Control Register can put the chip in the Split Read and Write mode where reads are from the Data Memory and writes are to the Connection Memory Low.

Bit 6, when 1, sets all the 256 output channels of the chip into Message Mode. In this mode, the Contents of all Connection Memory Low are output on the ST-BUS output data streams every frame unless the ODE pin is low. The chip behaves as if the bits 2 and 0 of every Connection Memory High location were 1.

Bits 4~3 are the Memory Select bits that determine the accessed location is in the Connection Memory High, Low or Data Memory.

The Data Stream Select bits, Bits 0~2, specify which memory location of the eight input and output data streams is addressed.

Figure 3. Control register Bits

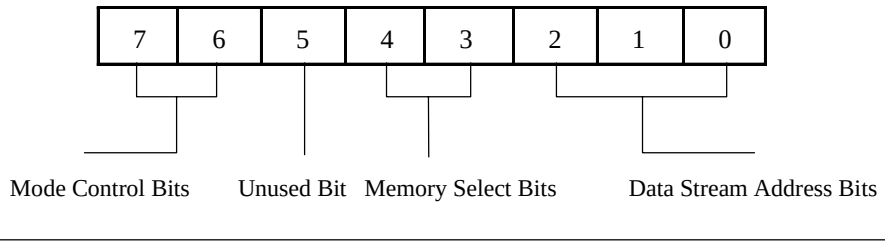


Table 4. Control Register Bits

Bit	Name	Description
7	Split Read & Write Mode Bit	When 1, the microprocessor interface is in split read and write mode where subsequent reads are from the Data Memory and writes are to the Connection Memory Low except that the Control Register is accessed again. When 0, the Memory Selection bits specify the memory for subsequent operations.
6	Message Mode Bit	When 1, entering into Message Mode. The contents of the Connection Memory Low of all Channels are output on the ST-BUS output channel except that the ODE pin is low. When 0, the bits of each Connection Memory corresponding to the output channel determine which input channel to be switched out.
5	Unused	
4-3	Memory Selection Bits	0-0 Not used 0-1 Data Memory (read only from the microprocessor port) 1-0 Connection Memory Low location 1-1 Connection Memory High location
2-0	Data Stream Address Bits	Specify which memory location of the eight input and output data streams is addressed.

Normal Mode

The PT7A8980/8980L mainly has two modes of operation, Normal Mode and Message Mode. In Normal Operation Mode, data on the ST-BUS output comes from the ST-BUS input. The microprocessor can decide which channel inputs and which channel outputs. It establishes switching connections between input channels and output channels by programming the Connection Memory Low. Note that the contents of Connection Memory Low locations are used to address the Data Memory locations associated with the input channels (see Figure 5 and Table 6). This relationship allows an input channel to be switched to its destined output channel (refer to Input and Output Control section).

Message Mode

In Message mode, the contents of the Connection Memory Low location associated with the output channel are driven out directly on this output channel. The processor can put out specific message to any output channel by writing the message data to its Connection Memory Low location.

An output channel can be put into Message Mode in two ways, i.e.,
1) Bit 6 of the Control Register is set 1, or
2) Bit 2 of the Connection Memory High location associated with the channel is set 1.

If Bit 6 of the Control Register is 1, all 256 output channels are in Message Mode no matter what value of Bit 2 in each Connection Memory High location is. If Bit 2 of the associated Connection Memory High location is 1 and the Bit 6 of the Control Register is 0, only this output channel is in Message Mode. Therefore, the Control Register overrides the Connection Memory High in setting the channels to Message Mode.

When a ST-BUS output channel is in Message Mode, the data byte in its connection Memory Low location is output on the corresponding channel slot of output data stream.

ST-BUS Output High Impedance

If the ODE pin of the chip is low, all the ST-BUS output pins will be in high impedance state regardless of operation mode of PT7A8980/8980L.

Each output channel can also be set in high impedance respectively by writing a 0 to the Output Enable bit (Bit 0) of the corresponding Connection Memory High location (see Figure 4 and Table 5). However, this is possible only when the ODE pin is high and Bit 6 in the Control memory High location is 0. Otherwise, the Output Enable bit has no effect on the output channel. This feature is useful when constructing switching matrices.

CSTo Output

the CSTo Bit (Bit 1) of each Connection Memory High location (see Figure 4 and Table 5) is output on the CSTo pin every frame. The order of these bits on the CSTo output pin is as follows.

All the 8 CSTo Bits corresponding to the same channel numbers on the 8 data streams STo0~7 are grouped together for output via the CSTo pin in one-channel time-slot . The CSTo Bit for data stream STo0 always comes out first within the time-slot, then the bits STo1, STo2,..., STo7.

To account for the possible delay in the external control circuitry, each group of the CSTo Bits is output in one-channel time-slot before data on the corresponding channel comes out to the ST-BUS data stream (see Figure 13). The CSTo Bits for channel 0, for example, are output on the CSTo during the channel 31 time-slot of the last frame, and CSTo Bits for channel 1 are output during the channel 0 time-slot of the same frame.

Figure 4. Connection Memory High Bits

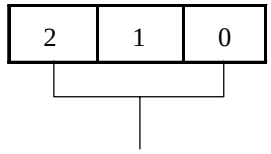


Table 5. Connection Memory High Bits

Bit	Name	Description
2	Message Channel	When 1, the contents of the corresponding location in Connection Memory Low are output on the output data stream of the corresponding channel. When 0, the contents of the corresponding location in Connection Memory Low are used as address for the Data Memory to determine the location of input data stream of the corresponding channels.
1	CSTo Bit	This bit is output on the CSTo pin one channel early. The CSTo bit for 0 channel of the data stream 0 is output first.
0	Output Enable	If the ODE pin is high and bit 6 of the Control Register is 0, this bit will enable driver of the output data stream of the corresponding channels. When 1, enables the driver and when 0 disables it.

Figure 5. Connection Memory Low Bits

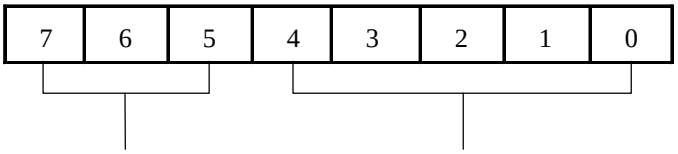


Table 6. Connection Memory Low Bits

Bit	Name	Description
7-5	Data Stream Address	The number expressed in binary notation on these 3 bits indicates the location of the input data stream to be connected. Bit 7 is the most significant bit, e.g., if bit 7 is 1, bit 6 is 0 and bit 5 is 1, the input data stream to be connected is on the channels in STi5.
4-0	Channel Address	The number expressed in binary notation on these 5 bits indicates the channel location of the ST-BUS Bits of input data stream to be connected (Which input data stream this channel belongs to is defined by bit 7, 6 and 5). Bit 4 is the most significant bit, e.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 0 and bit 0 is 1, the channel to be connected is 17.

Detailed Specifications

Absolute Maximum Ratings

PT7A8980

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc)	-0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +7.0V
DC Input Voltage	-0.3V to +7.0V
DC Input and Output Current	120mA
Power Dissipation	1W

PT7A8980L

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc)	-0.3V to +5.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +5.0V
DC Input Voltage	-0.3V to +5.0V
DC Input and Output Current	120mA
Power Dissipation	1W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Sym	Characteristics	Test Conditions	Min	Typ	Max	Units
Vcc	Supply Votage for PT7A8980		4.5	5.0	5.5	V
	Supply Votage for PT7A8980L		3.0	3.3	3.6	V
V_{IH}	Input HIGH Voltage		2.4		Vcc	V
V_{IL}	Input LOW Voltage		0		0.4	V
T_A	Operating Temperature		-40	25	85	°C

Note:

Typical figures are at 25°C and are for design aid only; not production tested.

DC Electrical, Power Supply and Capacitance Characteristics

(Voltages are with respect to ground unless otherwise stated.)

Table 8. DC Electrical, Power Supply and Capacitance Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	F0i, $\overline{C4i}$ = 0V			1	mA
	Supply Current - 8980	F0i = 8kHz, $\overline{C4i}$ = 4.096MHz			10	mA
	Supply Current - 8980L				5	mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IL}	Input Leakage Current	V_I between GND and V_{CC}			±5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 10mA			0.8	V
V_{OH}	Output HIGH Voltage - 8980	I_{OH} = -10mA	2.4			V
	Output HIGH Voltage- - 8980L		2.0			V
I_{OL}	Output LOW Current	V_{OL}=0.4V	5	10		mA
I_{OH}	Output HIGH Current - 8980	V_{OH} = 2.4V	-10	-20		mA
	Output HIGH Current - 8980L	V_{OH} = 2.0V	-10	-15		mA
I_{OZ}	Output High Impedance Leakage	V_O between GND and V_{CC}			±5	µA
C_{IN}	Input Pin Capacitance			8	10	pF
C_{OUT}	Output Pin Capacitance			8	10	pF

Note:

1. For $\overline{DTA}$ pin, I_{OZ} is measured, but I_{OH} and V_{OH} are not applicable.
2. Typical figures are at 25ºC and are for design aid only; not production tested.

AC Electrical Characteristics

Clock Timing

Table 9. Timing Characteristics of Clock

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{CP}	Clock Period		220	244		ns
t_{CTT}	Clock Transition Time			20		ns
t_{CPL}	CP Pulse Width Low		110	122	150	ns
t_{CPH}	CP Pulse Width High		95	122	150	ns
t_{FSW}	Frame Pulse Width			244		ns
t_{FSS}	Frame Signal Setup Time		20			ns
t_{FSH}	Frame Signal Hold Time		20			ns
t_{CFH}	CP Pulse Hold Time for Frame		20			ns
t_{CFS}	CP Pulse Setup Time for Frame		20			ns

Note:
1. Contents of Connection Memory are not lost if the clock stops.
2. Typical figures are at 25°C and are for design aid only; not production tested.

Figure 8. Timing Diagram of Frame

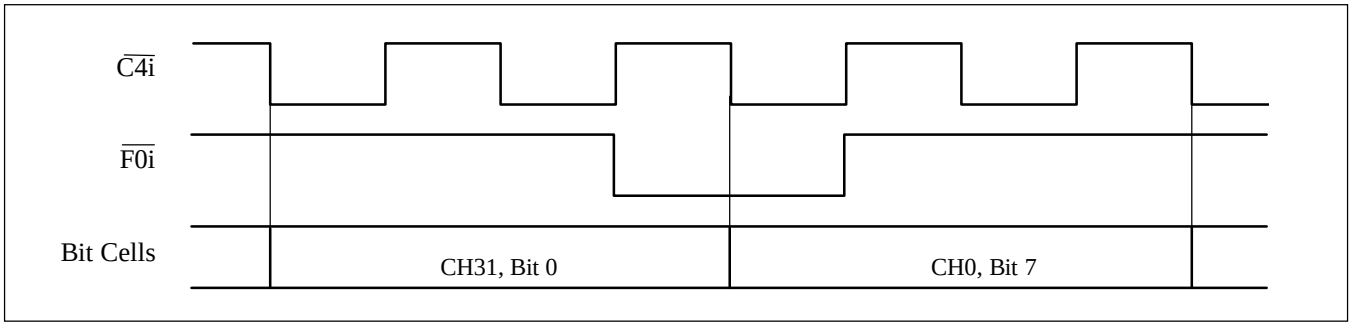
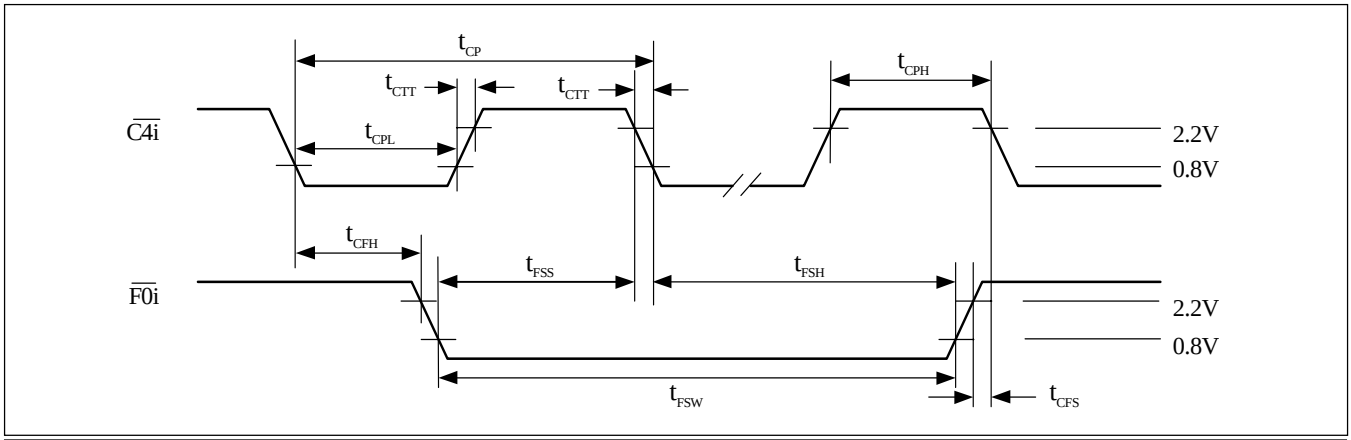


Figure 9. Timing Diagram of Clock



Serial Streams

Table 10. Timing Characteristics of Serial Streams

Sym	Description	Test Condition	Min	Typ	Max	Units
t_{SAZ}	STo0/7 Delay-Active to High Z	R_L=1kΩ C_L=150pF		25	80	ns
t_{SZA}	STo0/7 Delay-High Z to Active	C_L=150pF		30	125	ns
t_{SAA}	STo0/7 Delay-Active to Active	C_L=150pF		25	125	ns
t_{SOH}	STo0/7 Hold Time	R_L=1kΩ C_L=150pF	10			ns
t_{OED}	Output Driver Enable Delay	C_L=150pF		20	125	ns
t_{XCH}	External Control Hold Time	C_L=150pF	0	25		ns
t_{XCD}	External Control Delay			25	110	ns
t_{SS}	Serial Input Setup Time		10	-10		ns
t_{SH}	Serial Input Hold Time - 8980		25	20		ns
	Serial Input Hold Time - 8980L		30	25		ns

Note: Typical figures are at 25°C and are for design aid only; not production tested.

Figure 10. Timing Diagram of Serial Output and External Clock

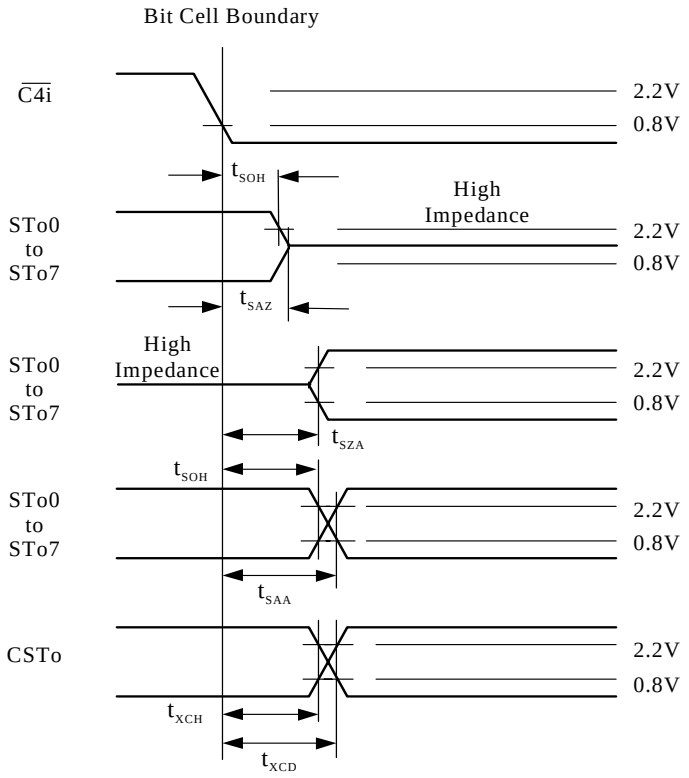


Figure 11. Timing Diagram of Output Driver Enable

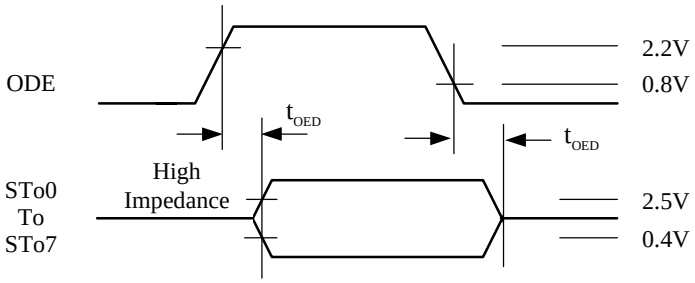


Figure 12. Timing Diagram of Serial Input

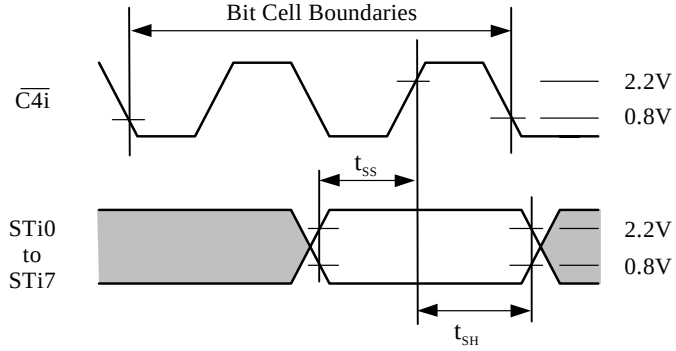
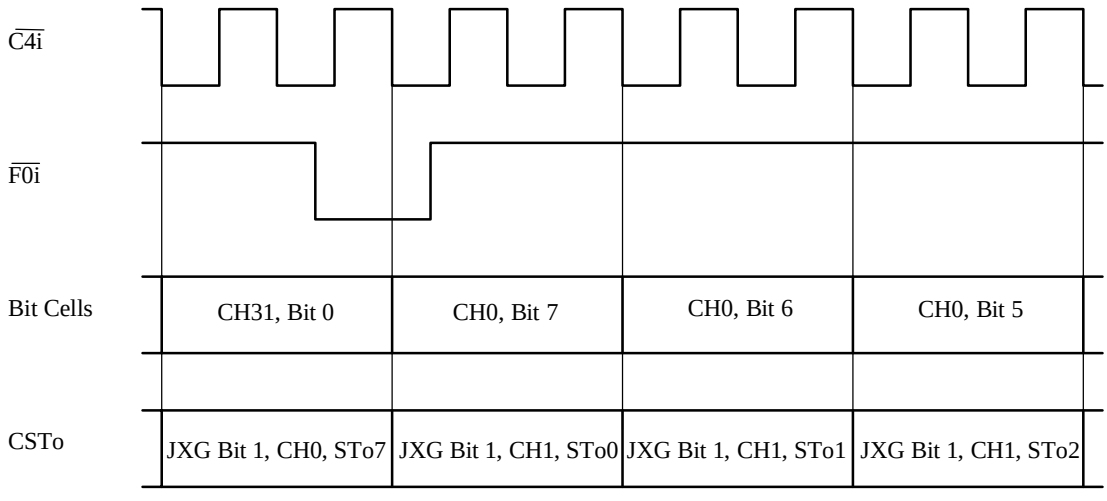


Figure 13. Timing Diagram of CSTo and Output Data Stream



* CH – channel, JXG – Connection Memory High Location

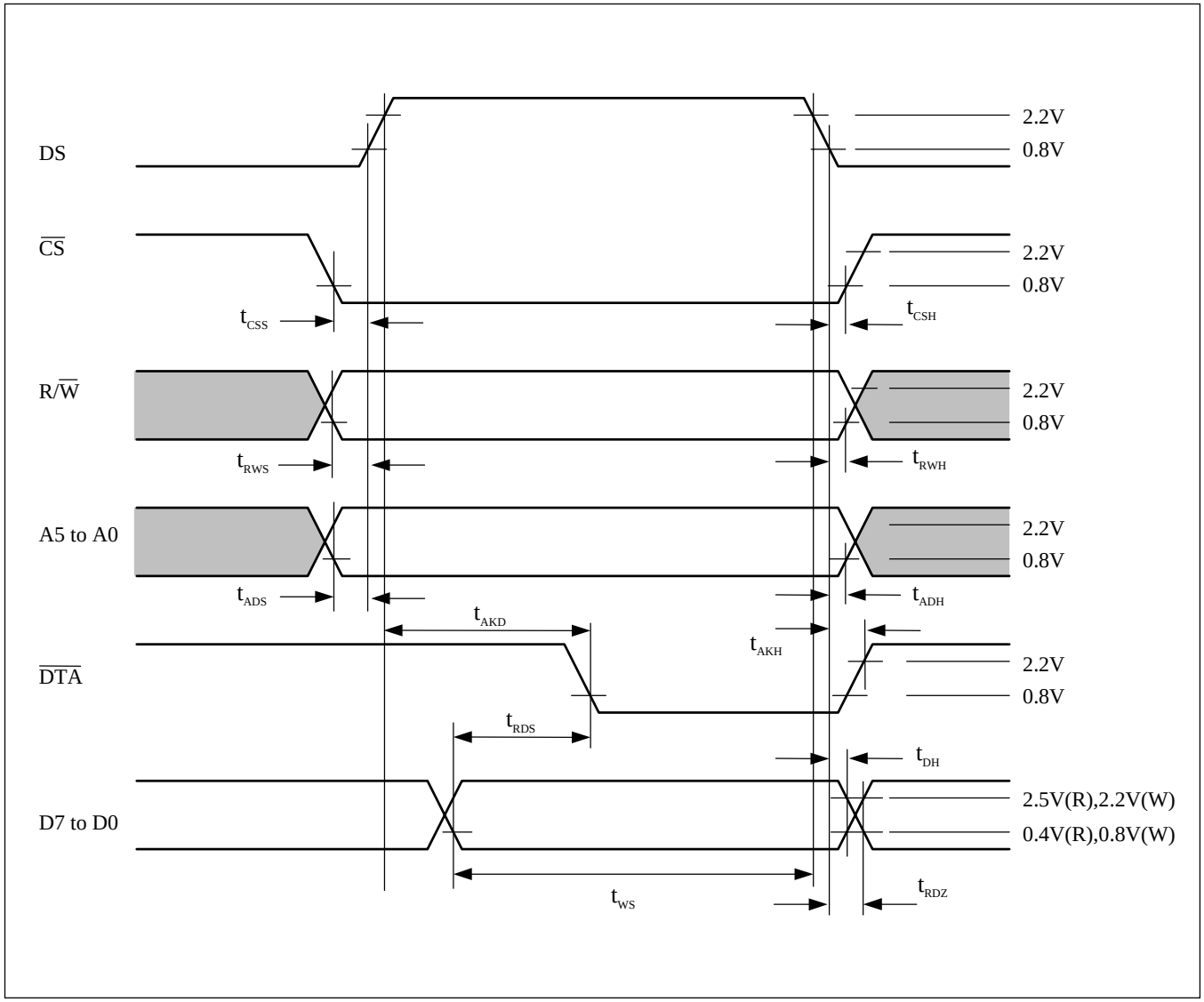
Processor Bus

Table 11. Timing Characteristics of Processor Bus

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{CSS}	Chip Select Setup Time		0	20		ns
t_{RWS}	Read/Write Setup Time		10	25		ns
t_{ADS}	Address Setup Time		10	25		ns
t_{AKD}	Data Acknowledge Delay:	C_L=150pF				
	- Access Connection Memory/Control Registers (8980)			50	100	ns
	- Access Connection Memory/Control Registers (8980L)			70	120	ns
	- Access Data Memory			560	1200	ns
t_{WS}	Write Data Setup Time		20			ns
t_{RDS}	Read Data Setup Time	C_L=150pF	10			ns
t_{DH}	Data Hold Time Read	R_L=1kΩ, C_L=150pF		20		ns
	Write		10			ns
t_{RDZ}	Read Data to High Impedance	R_L=1kΩ, C_L=150pF		50	90	ns
t_{CSH}	Chip Select Hold Time		0	20		ns
t_{RWH}	Read/Write Hold Time		10	20		ns
t_{ADH}	Address Hold Time		10	20		ns
t_{AKH}	Acknowledge Hold Time - 8980	R_L=1kΩ, C_L=150pF		40	80	ns
	Acknowledge Hold Time - 8980L			60	100	ns

Note:
Typical figures are at 25°C and are for design aid only; not production tested.

Figure 14. Timing Diagram of Processor Bus



Mechanical Information

Figure 15.P(40-Pin DIP)

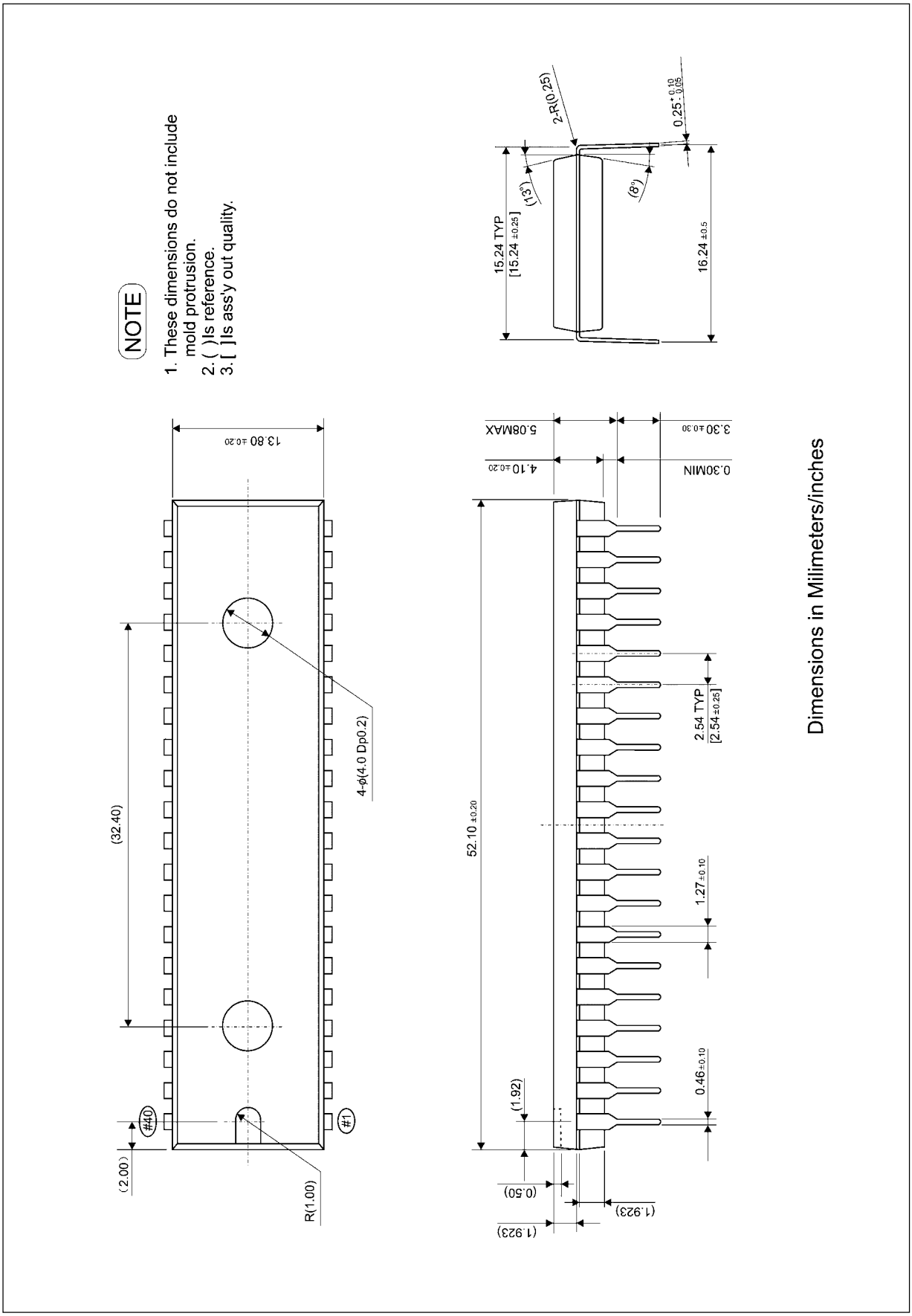
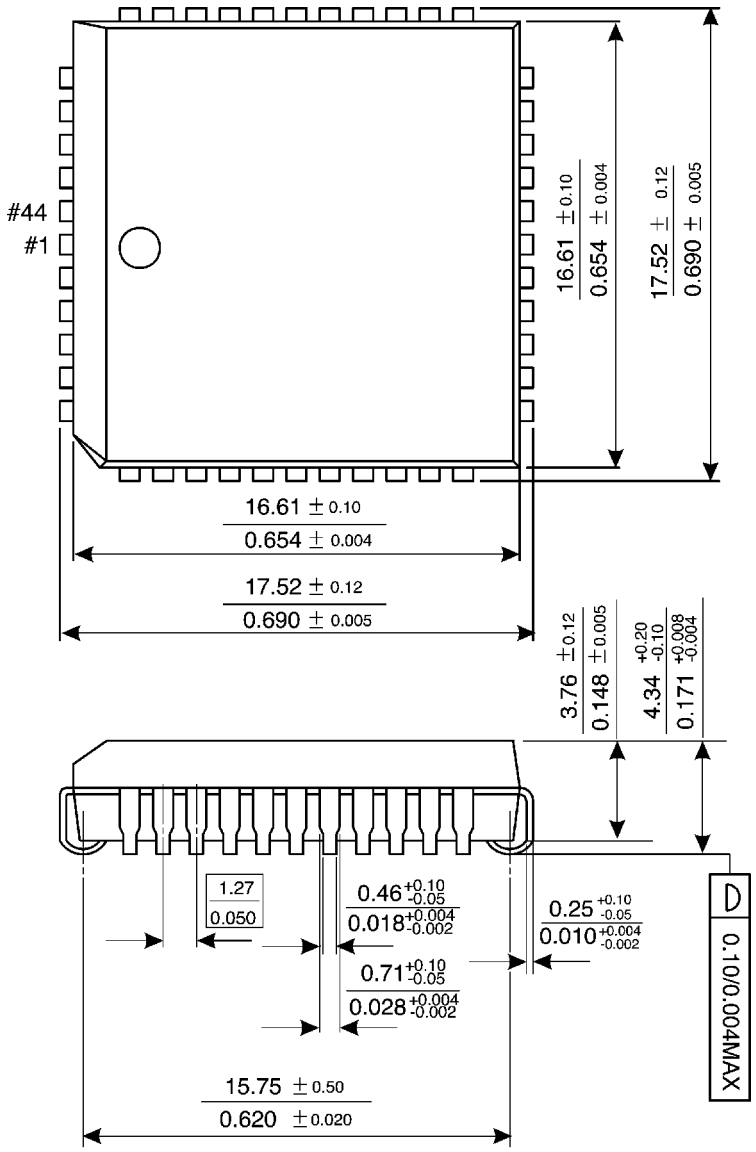


Figure 16. J/JE (44-Pin PLCC)



Dimensions in Milimeters/Inches

Notes

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