Features

- Provides up to 32 full-duplex HDLC/SDLC channels
- Compatible with 1.544 Mb/s T1 and 2.048Mb/s CEPT PCM-30 carrier format
- Provides on-board buffer memory management
- Supports standard hyperchannel configuration and fully programmable hyperchannel configuration
- Provides on-board CRC-16, automatic flag and zero insertion and deletion functions in HDLC format
- Provides programmable tri-state outputs to T1/E1 serial interface and FILL/MASK, thus enabling up to 8 devices connecting to a TDM bus
- Provides data rate adaptation functions
- Compatible with HDLC, SNA SDLC, X.25, X.75, LAPB, and LAPD protocols
- Support non-HDLC signaling channels
- Single +5V power supply
- Package: 68-pin PLCC

Applications

- Primary rate interfaces
- Basic-rate D-channel controller
- Multi-channel HDLC interfaces

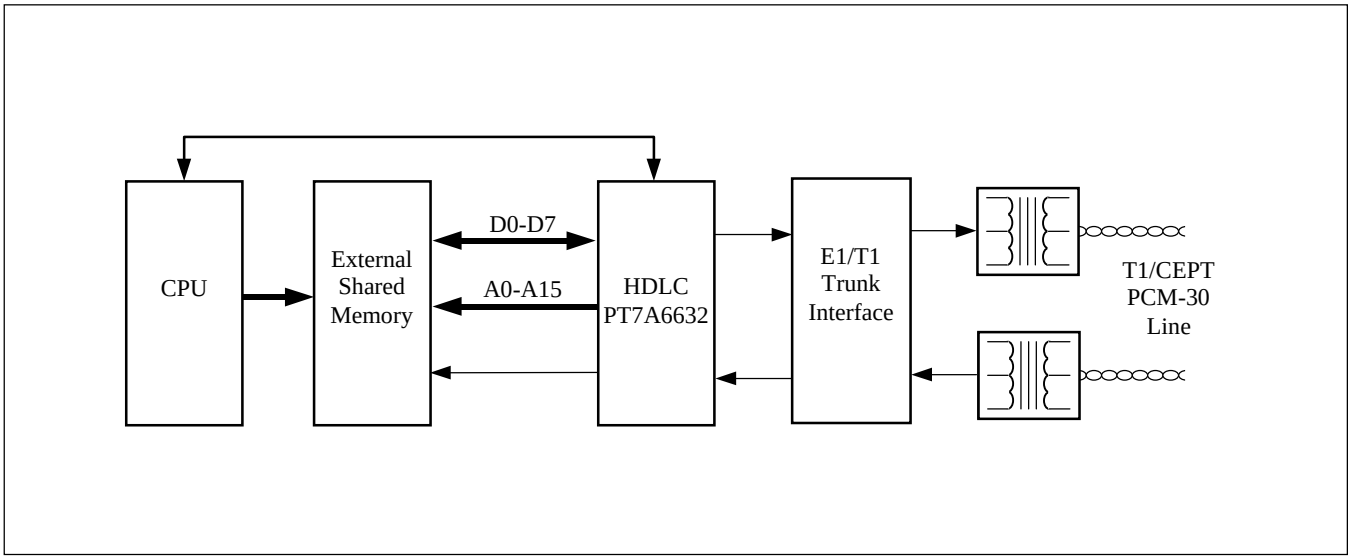
Introduction

The PT7A6632 HDLC controller operates at layer 2 (data link protocol level) of the Open Systems Interconnection (OSI) reference model. It supports HDLC and ISDN implementations.

The PT7A6632 processes data transmitting and receiving on a T1 or E1 communication link. It connects between the T1/E1 serial bus and an external memory shared with CPU(s), multiplexing / demultiplexing up to 32 fully-duplex high-speed data channels.

It provides additional functions that support X.30 and X.31 rate adaptation and fully flexible hyperchannels.

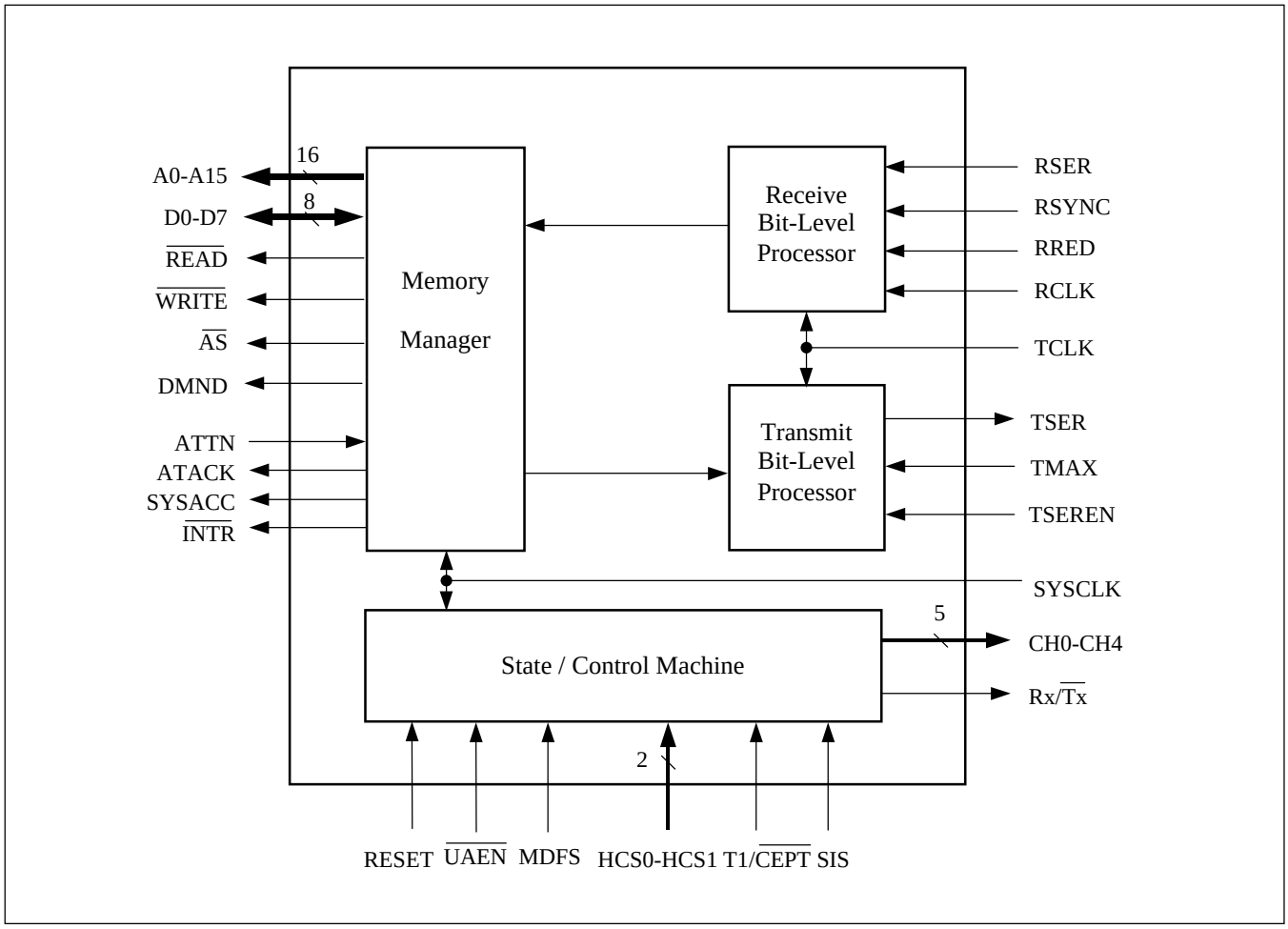
Figure 1. Application Diagram of PT7A6632



Contents

Block Diagram

Figure 2. Block Diagram of PT7A6632



Pin Information

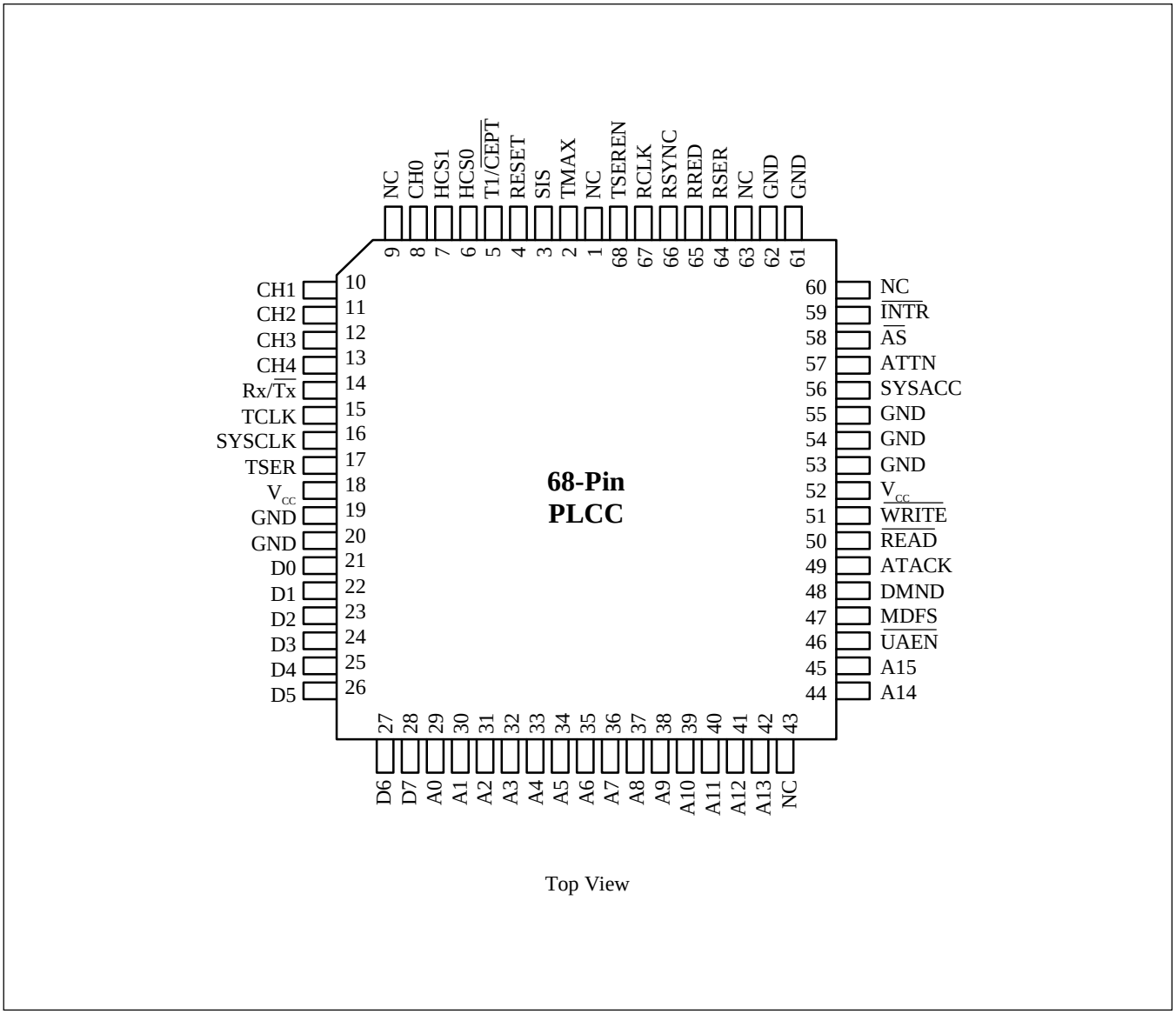
Pin Assignment

Table 1. Pin Assignment

Group	Symbol	Function
Memory Interface	D0-D7, A0-A15, READ, WRITE, AS, DMND	Data, Addresses & Signals with Shared Memory
Serial Interface	RSER, RSYNC, RRED, TSER, TMAX, SYSCLK, TCLK, RCLK, TSEREN	Data & Timing with Serial Interface
CPU Interface	ATTN, ATACK, SYSACC, INTR	Signals with CPU
State & Control	SIS, T1/CEPT, HCS0, HCS1, MDFS, UAEN, RESET, CH0-CH4, Rx/Tx	Device Status & Control Signals
Power	V_{CC}, GND	Power & Ground

Pin Configuration

Figure 3. Pin Configuration



Pin Description

Table 2. Pin Description

Pin	Name	Type	Description
1, 9, 43, 60, 63	NC		**No connection**
2	TMAX	I	**Transmit multiframe sync:** pulse input from T1/E1 Trunk Interface, active HIGH. Getting to high indicates the begining of a multiframe.
3	SIS	I	**Serial interface select:** decides the effective edge of TCLK and RCLK. See Table 25. SIS = 1, falling edge of TCLK and RCLK effective. SIS = 0, rising edge effective.
4	RESET	I	**Reset:** input for initializing the PT7A6632, active HIGH. The initialization will be completed within 90 SYSCLK periods after RESET changes to LOW. The RESET sets the device in the following state: - HDLC mode, - all the FILL/MASK bits are zeros, - all channels deactivated, - transmit channels output all ones.
5	T1/$\overline{\text{CEPT}}$	I	**Select T1 or CEPT mode: a** HIGH sets the device in T1 framing mode, a LOW sets in CEPT PCM-30 framing mode.
6 7	HCS0 HCS1	I	**Hyperchannel select:** set standard hyperchannel patterns in T1 or CEPT mode: - In T1 mode (T1/$\overline{\text{CEPT}}$ = 1), HCS0 HCS1 = 01, four channels of 384 kb/s (H0), = 10, single channel of 1.536Mb/s (H11). - In CEPT PCM-30 mode (T1/$\overline{\text{CEPT}}$ = 0): HCS0 HCS1 = 01, single channel of 1.92Mb/s, time-slot 0 and 16 are 64kb/s (H12), = 10, reserved. - In any of T1 or CEPT PCM-30 mode, HCS0 HCS1 = 00, all channels are 64kb/s, = 11, reserved.
8 10 11 12 13	CH0 CH1 CH2 CH3 CH4	O	**Channel number:** indicates current active channel's number (binary). CH0 is the LSB and CH4 is the MSB.
14	Rx/$\overline{\text{Tx}}$	O	**Receive/transmit channel:** indicates direction of current active channel. HIGH means receive and LOW means transmit.
15	TCLK	I	**Transmit clock:** Square wave input from T1/E1 Trunk Interface. Used for PT7A6632 transmit interface clock. Its phase must be aligned with that of SYSCLK and frequency is one half of SYSCLK.

Table 2. Pin Description (Continued)

Pin	Name	Type	Description
16	SYSCLK	I	**System clock:** Provides timing reference for all external memory interface. Frequency = 3.088MHz for T1 or 4.096MHz for CEPT PCM-30.
17	TSER	O	**Transmitted serial data:** Serial data output line, tri-state output to T1/E1 interface, carries transmitter data bit stream.
18, 52	V_{CC}	I	**Power supply (+5V)**
19, 20, 53, 54, 55, 61, 62	GND	I	**Ground**
21-28	D0-D7	I/O	**Memory Data lines:** Bidirectional data bus between the PT7A6632 and the shared memory. D0 is the LSB and D7 is the MSB.
29-42, 44-45	A0-A15	O	**Memory Address lines:** Output address lines to the external memory. A0 is the LSB and A15 is the MSB.
46	$\overline{\text{UAEN}}$	I	**Upper Address Enable**: Sets the upper address bus lines (A8-A15) state: $\overline{\text{UAEN}}$ = 1: PT7A6632 sets A8-A15 in high impedance during Activation Memory access with SYSACC asserted. $\overline{\text{UAEN}}$ = 0: PT7A6632 sets A8-A15 LOW when SYSACC asserted.
47	MDFS	I	**Memory Data Format Select:** MDFS = 1: the most significant bytes of next buffer start address, buffer size and data length are at even addresses respectively in the external memory, and their least significant bytes at odd addresses (68000MPU). MDFS = 0: inverse with the above, i.e., the most significant bytes of next buffer start address, buffer size and data length are at odd addresses respectively in the external memory, and their least significant bytes at even addresses (8080 MPU).
48	DMND	O	**Memory Demand:** A HIGH informs other devices on the memory bus that the PT7A6632 will access the external memory one TCLK period after DMND assertion (rising edge). The DMND will be deasserted at completion of the memory access.
49	ATACK	O	**Attention Acknowledge:** Active HIGH. 6632 responds to the ATTN to access Activation Memory. After completion of the access, 6632 asserts ATACK. ATACK is deasserted in response to deassertion of ATTN (falling edge).
50	$\overline{\text{READ}}$	O	**Memory Read:** Active LOW. Output to the external memory for data reading. When it is LOW, data from memory is latched to the PT7A6632 on the rising edge of SYSCLK.
51	$\overline{\text{WRITE}}$	O	**Memory Write:** Active LOW. Output to the external memory for data writing.
56	SYSACC	O	**System Access:** Active HIGH. A HIGH indicates the PT7A6632 is accessing Activation Memory locations for channel activation byte or channel buffer pointers.

Table 2. Pin Description (Continued)

Pin	Name	Type	Description
57	ATTN	I	**Attention**: Active HIGH. A HIGH requires PT7A6632 to process the Channel Activation Byte (CAB) at Activation Memory location xx00H in the shared memory. ATTN will be deasserted in response to assertion of ATACK.
58	$\overline{AS}$	O	**Memory Address strobe:** active LOW. Its falling edge will make a valid memory address be on the memory address lines.
59	$\overline{INTR}$	O	**Interrupt:** active LOW. A LOW indicates that the buffer status byte is under update. Its pulse duration is equal to one SYSCLK period.
64	RSER	I	**Received Serial Data:** Serial data input line, receiving data bit stream from the T1/E1 Interface.
65	RRED	I	**Receive Red Alarm:** A HIGH indicates the received data is invalid due to loss of frame alignment or similar reason. If so, PT7A6632 stops processing in all receive channels until the reception synchronization restored.
66	RSYNC	I	**Receive Synchronization:** active HIGH. Level or pulse input for receive frame synchronization.
67	RCLK	I	**Receive Clock:** Clock for serial data receiving. Input from the T1/E1 interface / clock recovery circuit. Frequency is 1.544MHz for T1 or 2.048MHz for CEPT PCM-30.
68	TSEREN	I	**TSER Enable:** active HIGH, decides TSER line status along with FILL/MASK bit in descriptor. When TSEREN = 1, FILL/MASK = 1, send data on TSER, FILL/MASK = 0, send a 1 on TSER. When TSEREN = 0, FILL/MASK = 1, Send data on TSER, FILL/MASK = 0, high impedance on TSER.

Functional Description

General Description

The PT7A6632 HDLC Controller is applied between an external memory and T1/E1 trunk interface to perform data transmission and reception. See Figure 1. Its signal attributes are shown in Figure 4.

PT7A6632 reads the data to be transmitted from the external memory in 8-bit parallel way, formats them and adapts data rate, then transmits the data to the T1/E1 trunk interface.

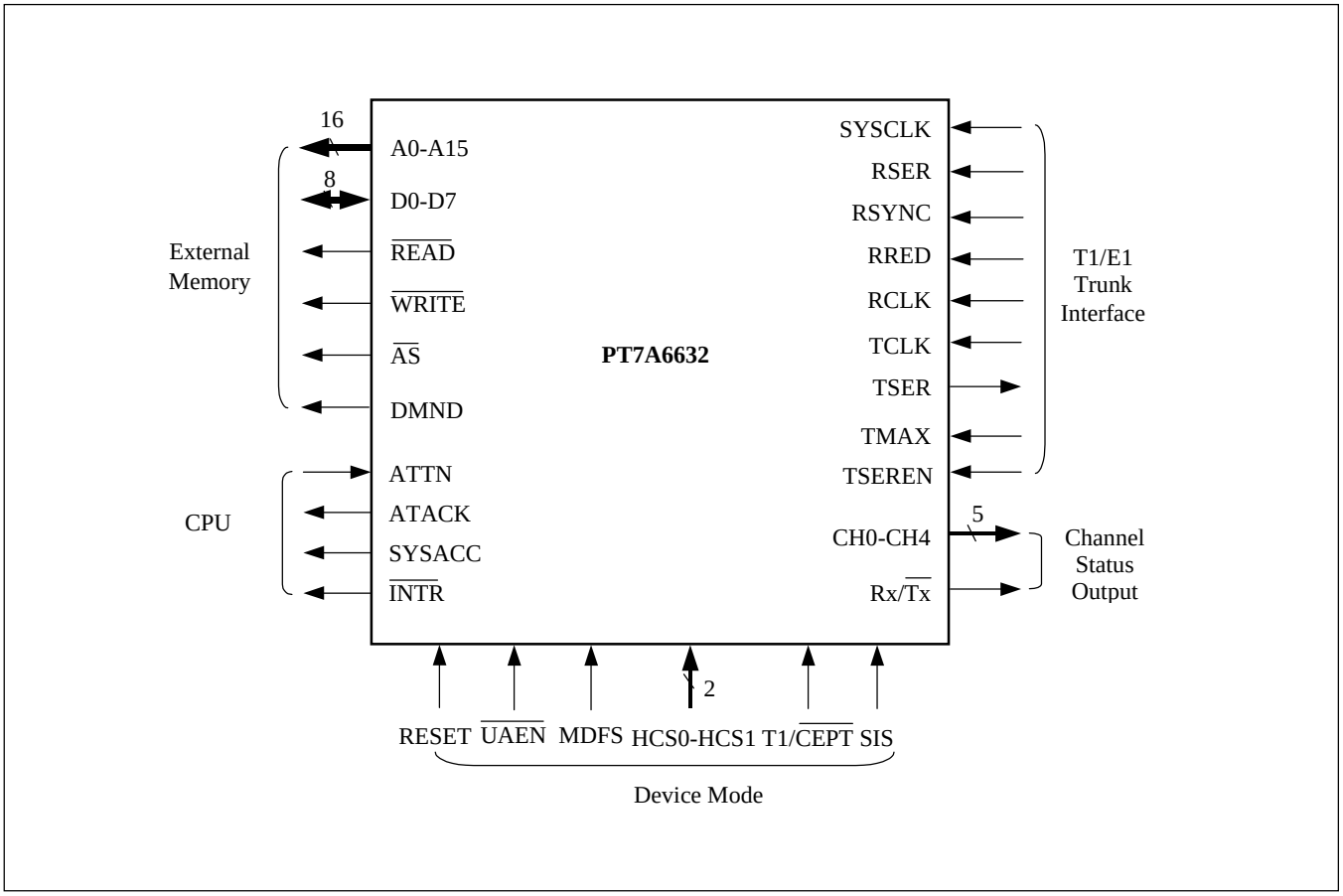
PT7A6632 receives serial data from the T1/E1 trunk interface, deformats them and adapts data rate, then stores the data into the external memory.

The channel operation modes are set up in the external memory by CPU. PT7A6632 reads the commands from the external memory and process data channel by channel, totally 64 channels (32 for transmission and 32 for receive). Each channel mode can be set up in external memory independently by CPU.

PT7A6632 consists of 4 functional blocks as shown in Figure 2. There are:

- Transmit Bit-Level Processor,
- Receive Bit-Level Processor,
- Memory Manager, and
- State/Control Machine.

Figure 4. PT7A6632 Interface Signals



Transmit Bit-Level Processor

The block diagram of the Transmit Bit-Level Processor is shown in Figure 5. The external memory stores data to be transmitted and the channel operation modes in a set of linked buffers (referred as Transmit Data/Command Buffers) in the external memory. Refer to Figure 23 and 24 in the External Memory Organization and Definition.

For transmit, the PT7A6632 reads the data from external memory, formats it in HDLC format (generates flags, abort and idle code, inserts zero-bit, counts the Frame Check Sequences), non-HDLC signaling format or non-HDLC data format, adapts data rate, and sends the processed data to TSER output via the Transmit Interface.

Timing

TCLK clocks data bit stream out at its falling edge. TMAX is multiframe synchronization signal from the T1/E1 trunk interface. SIS decides the TMAX is sampled in rising or falling edge of TCLK . PT7A6632 processes data channel by channel for the data transmission under control of channel counter in the Transmit Interface. See Figure 7-10.

Data Rate Adaptation

The PT7A6632 can adapt the data rate of sub-64kb/s (n x 8kb/s, n = 1 - 8) to the standard 64kb/s bearer rate. A FILL/MASK byte in the transmit command buffer is applied to the data bit by bit to perform data rate adaptation. An example is shown in the Figure 6.

Figure 5. Block Diagram of Transmit Bit-Level Processor

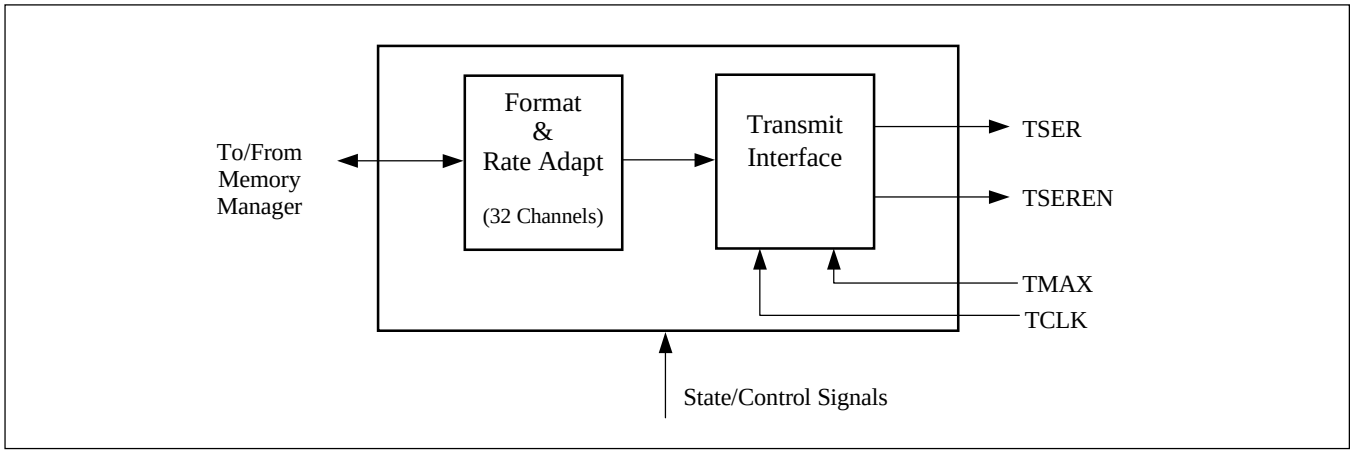


Figure 6. 32kb/s Subrate Operation - Single Transmit Channel

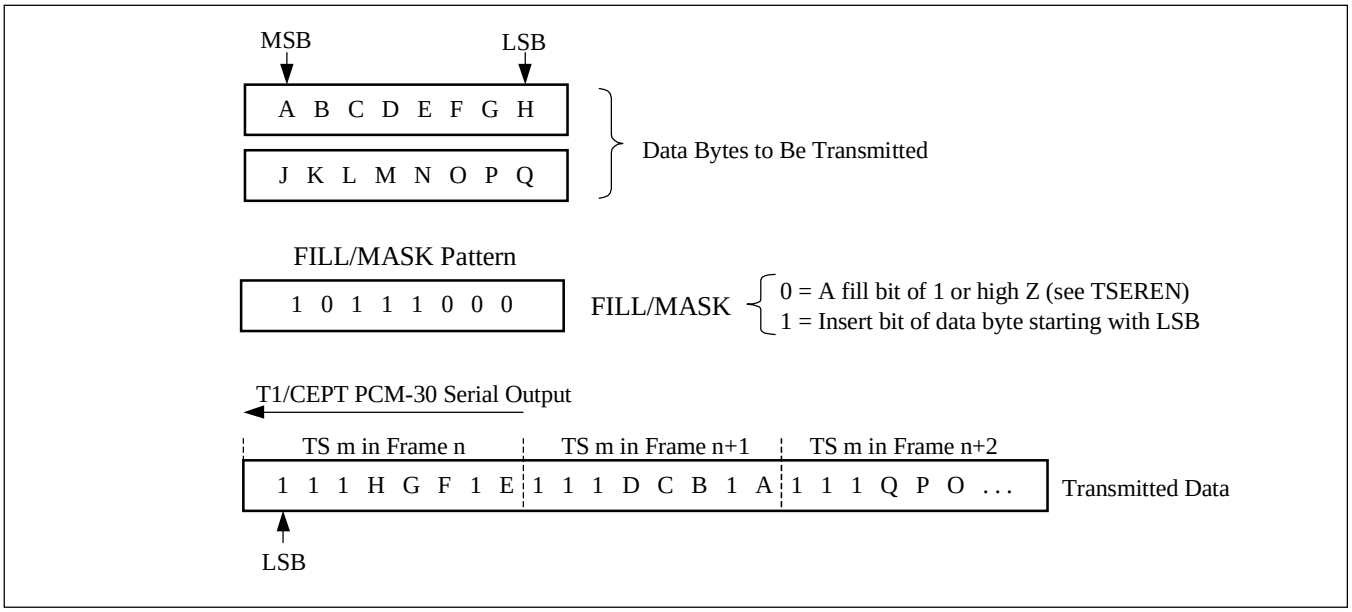
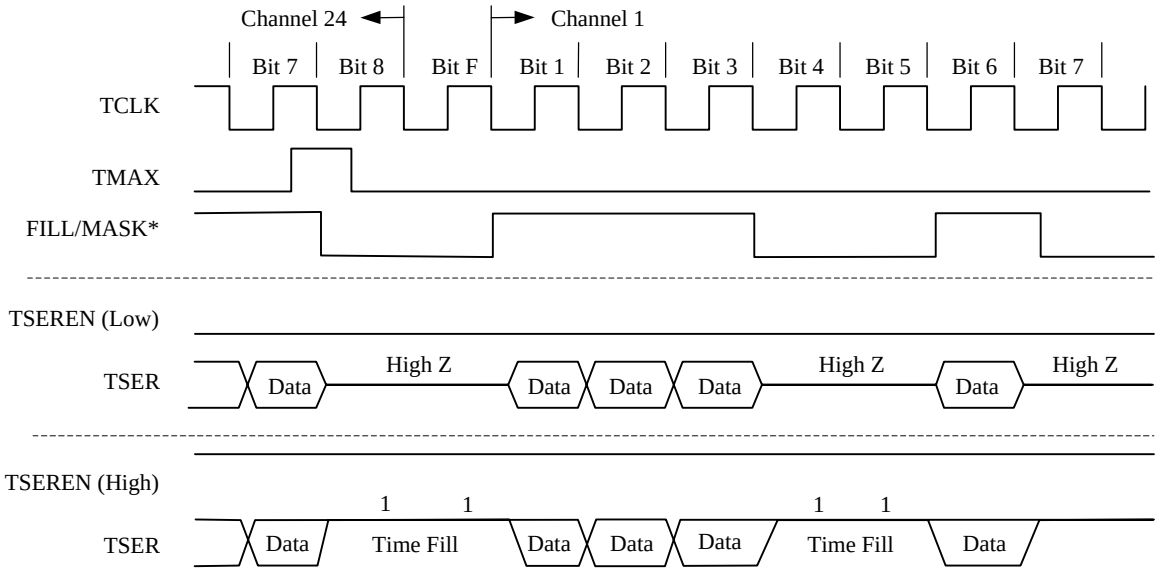


Figure 7. Transmit Frame Synchronization Timing - T1 Mode, SIS = 1



* The F-bit time is processed as if the FILL/MASK = 0. However, this actual FILL/MASK does not apply to the F-bit.

Figure 8. Transmit Frame Synchronization Timing - CEPT PCM-30 Mode, SIS = 1

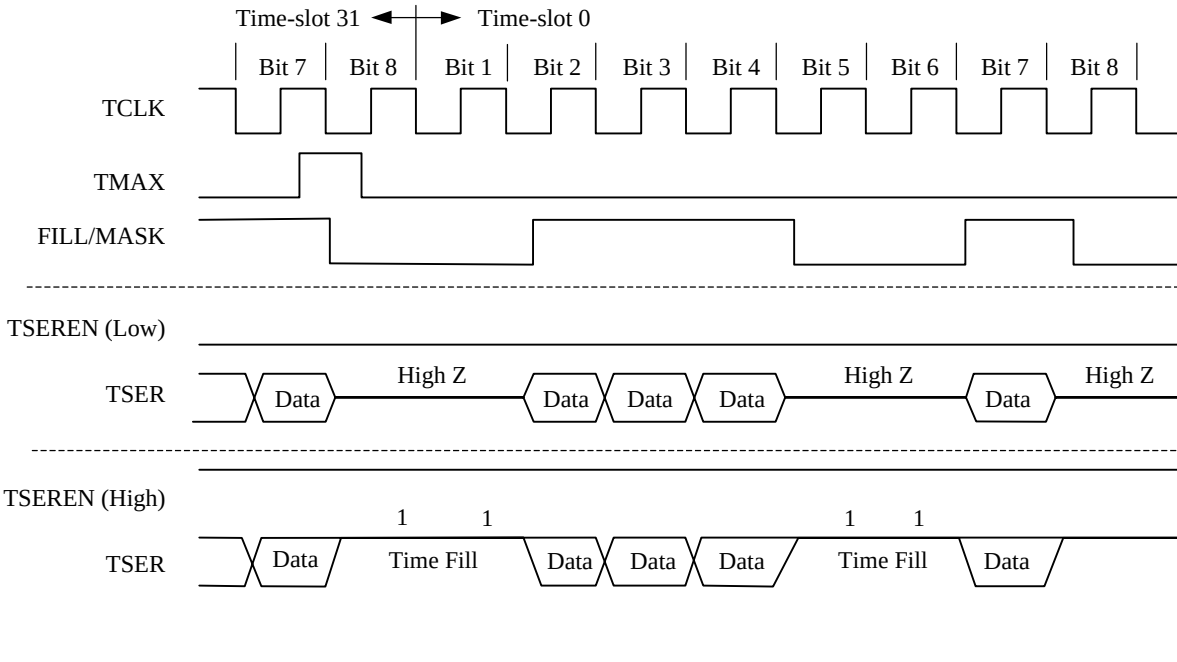
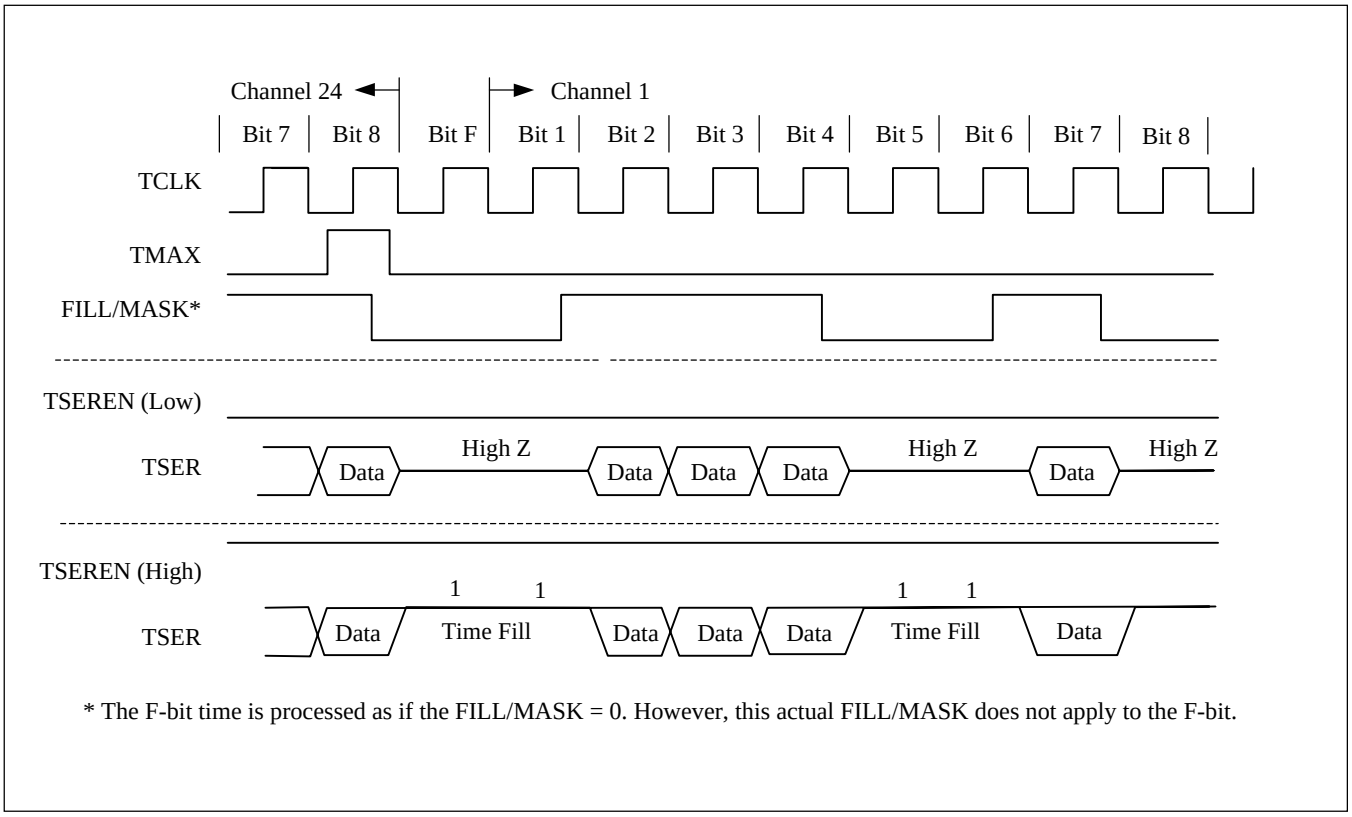
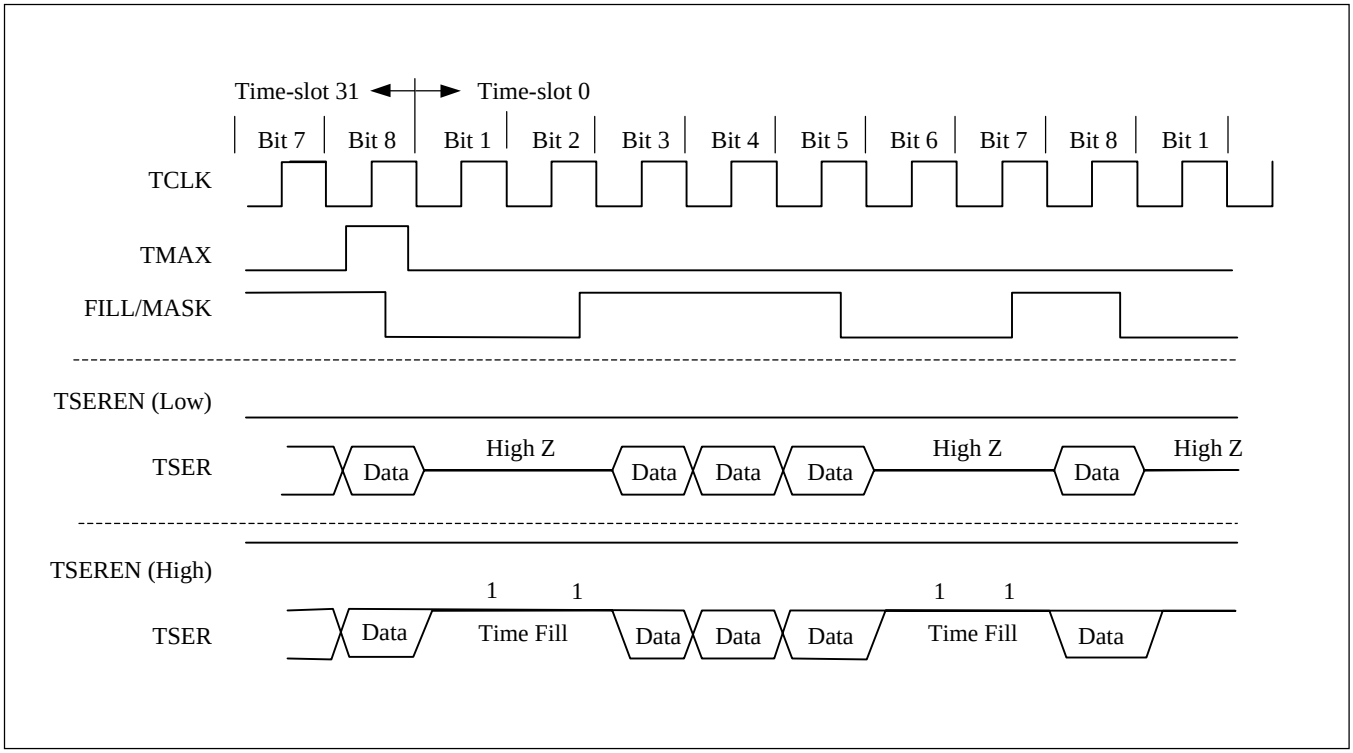


Figure 9. Transmit Frame Synchronization Timing - T1 Mode, SIS = 0



* The F-bit time is processed as if the FILL/MASK = 0. However, this actual FILL/MASK does not apply to the F-bit.

Figure 10. Transmit Frame Synchronization Timing - CEPT PCM-30 Mode, SIS = 0



Hyperchannel

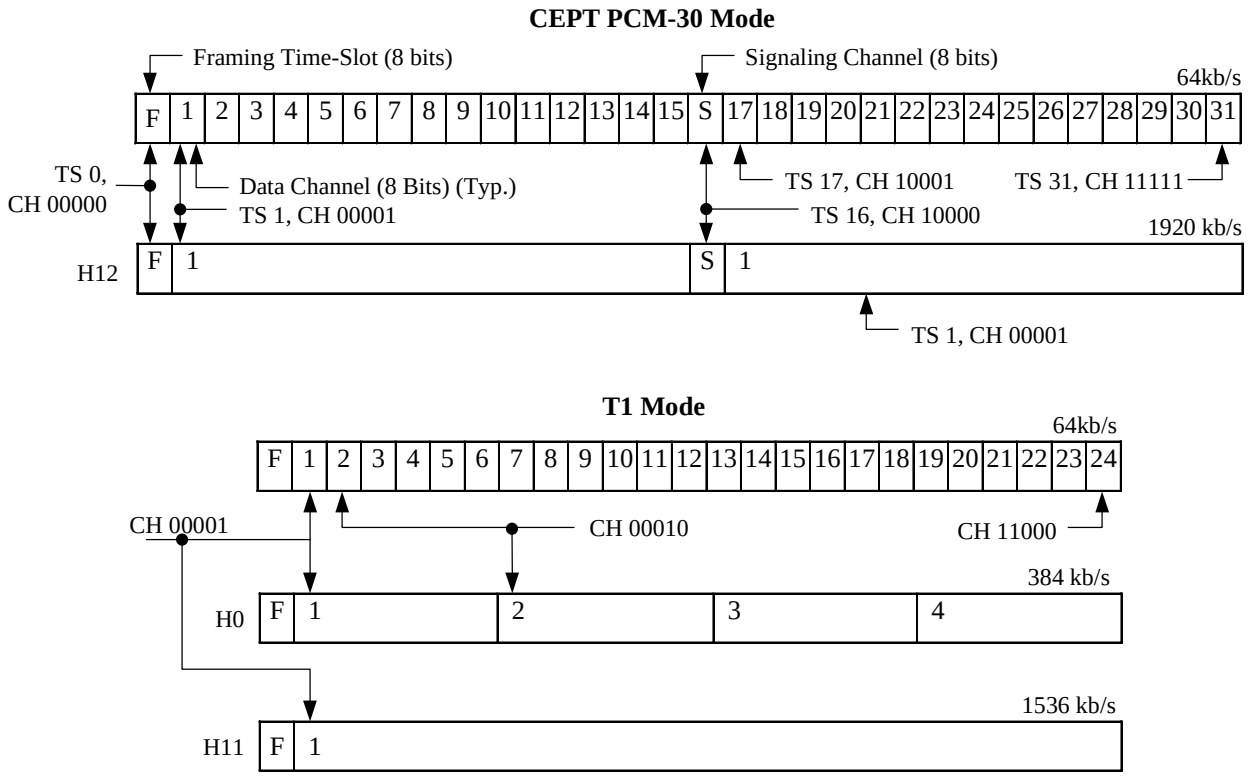
Three standard ISDN hyperchannel options (two for T1, one for CEPT PCM-30) are available by setting HCS0 and HCS1 as well as T1/$\overline{\text{CEPT}}$ pins. See Table 3 and Figure 11.

All channels can also be randomly grouped into flexible hyperchannel (with HCS0 HCS1 = 00). A hyperchannel can contains any number of 64kb/s channels. Details is illustrated in "External Memory Organization and Definition" and Table 10.

Table 3. Hyperchannel Selection

T1/$\overline{\text{CEPT}}$	HCS1	HCS0	Channel Selection
x	0	0	All channels are 64kb/s. (Flexible hyperchannel can be programmed)
1	1	0	Four channels of 384kb/s (H0). Valid for T1 only.
1	0	1	Single channel of 1.538Mb/s (H11). Valid for T1 only.
0	1	0	Single channel of 1.92Mb/s (H12). Time-slots 0 and 16 are 64kb/s. Valid for CEPT only.
x	1	1	Reserved.
0	0	1	Reserved.

Figure 11. Standard Hyperchannel Provisory



Note:
Grouping of 64kb/s channels into standard hyperchannels is fixed as shown. Time-slot assignments can be changed (when HCS1 HCS0 = 00) to create flexible hyperchannels by programming command buffers.

Tri-State Serial Data Output TSER

The TSER can be set to different state by setting TSEREN pin and FILL/MASK byte in the transmit command buffer. See Table 4.

Table 4. Output Selection on TSER

TSEREN	FILL/MASK	Output on TSER
1	0	Send a 1
0	0	High-impedance output
1	1	Send data
0	1	Send data

When TSEREN = 0, and FILL/MASK bit = 0, the TSER output line is in high impedance. This feature allows to connect up to eight PT7A6632 devices together to realize subrate TDM transmission.

Channel Operation Modes

The transmit channels can be set in the following operation modes by CPU in transmit command buffer. See MODE byte in the transmit command buffer for details (Figure 24).

- HDLC Mode

In HDLC mode, the Transmit Processor generates flags, abort and idle code, inserts zero-bit, count the Frame Check Sequences (FCS) for the data.

In HDLC mode, it is programmable to attach a number of flags to the end of HDLC frame as time-fill sequence. The number of flags is specified in the transmit data buffer.

The PT7A6632 counts the intentionally inserted zeroes based on HDLC format. These intentionally inserted zeroes may be counted as intraframe time-fill bits. In this case, the programmed flag number will be adjusted according to the counting result.

Reset the device will make all channels in HDLC mode.

- Non-HDLC Data Mode

In non-HDLC data mode, the data from memory directly transmit on TSER.

In non-HDLC data channel mode (DMI mode 0 or 1), CF/P bit of STATUS byte of allocated data buffer should be reset to ensure uninterrupted data transmit.

- Non-HDLC Signaling Mode

The non-HDLC signaling requires no special consideration in transmit data processing.

In non-HDLC signaling mode, CF/$\overline{P}$ bit of STATUS byte of allocated data buffer should be reset to ensure uninterrupted data transmit. The PT7A6632 assumes that no more than 2 linked data buffers are allocated to the signaling channel by the CPU. Details are shown in Section “External Memory Organization and Definition” and Tables 8 and 14.

- Loop Mode

When a transmit channel is specified in Loop Mode, the PT7A6632 will send the data of this channel into an intermediate buffer in PT7A6632 in channel period while sends the data to TSER output. The data then will be sent back to the external memory via a receive channel in Loop Mode. Each time only one transmit and one receive channel can be specified in Loop Mode. The transmit loop channel number and receive loop channel number are not necessarily identical. The Loop Mode does not support hyperchannel.

If only a transmit loop channel is defined without a receive loop channel defined, the loop operation can not be performed. Reset the device will delete all Loop Mode.

- Logical Inversion

If a transmit channel is set in inversion mode, data including flag, ABORT and FCS bits will be inverted bit by bit when transmit processing. Device reset sets all channel in inversion mode.

Data Transmission Order

The PT7A6632 transmits data bytes in the same time sequence as they are arranged in ascending addresses in the external buffers. For a certain channel, the data at byte address m is transmitted first, the data at address m+1 is transmitted next, and so on while the data bytes are in the same buffer. After the data in a data buffer is exhausted, the PT7A6632 starts to transmit the next byte from the next buffer whose address is specified in the current buffer. The transition to the next buffer is transparent to the CPU while the flow of actual data is maintained. This natural sequence of data flow is maintained for flexible hyperchannels, as well.

The PT7A6632 transmits the LSB (D0) of a data byte first; then the next LSB second; and the MSB (D7) last. The only exception is that the MSB of the HDLC FCS (CRC-CCITT) is transmitted first; the LSB transmitted last.

Receive Bit-Level Processor

The block diagram of the Receive Bit-Level Processor is shown in Figure 12. The receive bit-level processor accept serial data from the T1/E1 trunk interface, perform HDLC deformat (processes flags, abort, deletes zeroes, checks FCS, filters time-fill bits), or other non-HDLC functions and assemble the processed bit, including HDLC header, into bytes and sends them into the external memory. The CPU sets up the channel operation in a set of linked buffers (referred as receive command/data buffer) in the external memory. Refer to Figure 26 and 27 in the Section "External Memory Organization and Definition".

Timing

Generally, the starting of a data frame received from the T1/E1 trunk interface is not correlated with that of a transmit frame. As PT7A6632 uses same 8-bit memory bus for data writing and reading, an elastic buffer is adopted to coordinate the data access on the bus.

The received data stream is clocked into the elastic buffer by the RCLK and then clocked out to the Deformat and Rate Adapt circuit by the TCLK. In this way, the data flow on the memory bus is simple and coordinated. The data is sampled and processed in rising edge (SIS = 0) or falling edge (SIS = 1) of the RCLK. See Figure 14-17.

The RSYNC is used for receive frame synchronization.

Data Rate Adaptation

Reverse process of data rate adaptation of transmission. Illustrated in Figure 13.

Receive Mornitor

The PT7A6632 monitors the Receive Red Alarm (RRED) input. Once the PT7A6632 detects RRED high, it will stop data processing in all receive channels and reports by writing the Status byte. The synchronization will be restored by TMAX and RSYNC signals.

The PT7A6632 performs data validity check (checks CRC) for the received data. Once the PT7A6632 finds any errors in the CRC, the receive interface will stop data processing in current channel until detects a new HDLC flag byte. The situation is reported to the external memory. Details are shown in Table 11 for STATUS byte, ABRT, FCER and SHER bits in Section "External Memory Organization and Definition".

Hyperchannel

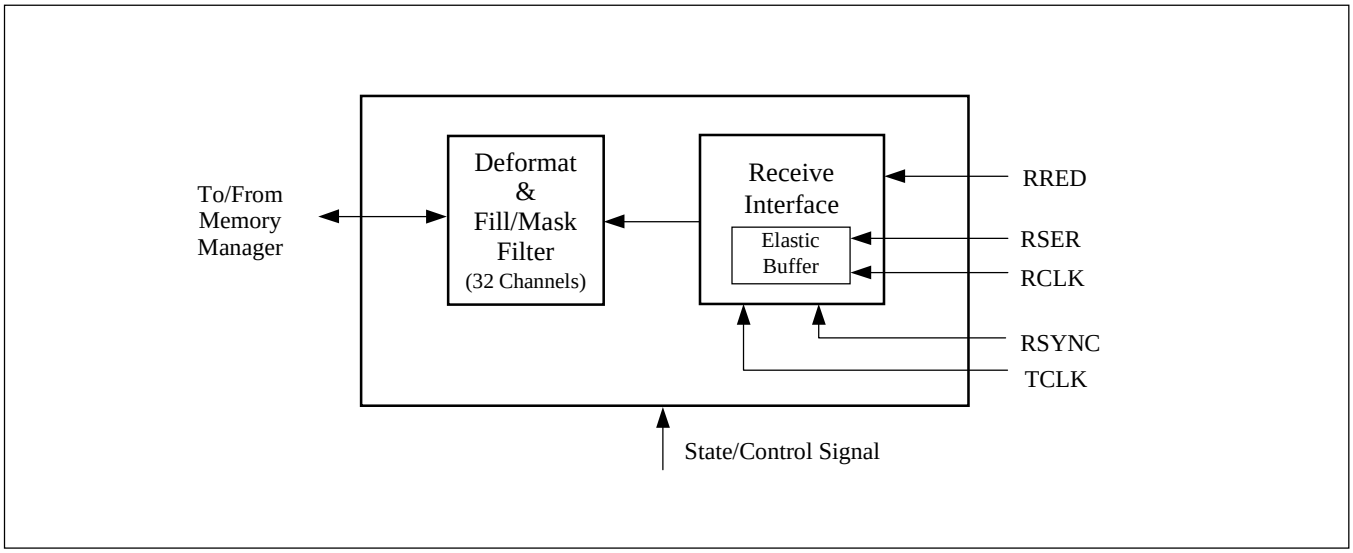
Three standard ISDN hyperchannel options (two for T1, one for CEPT PCM-30) are available by setting HCS0 and HCS1 as well as T1/$\overline{\text{CEPT}}$ pins. See Table 3 and Figure 11.

The channels can also be randomly grouped into flexible hyperchannel (with HCS0 HCS1 = 00). A hyperchannel can contains any number of 32 64kb/s channels. Details is illustrated in Section "External Memory Organization and Definition" and Table 10.

Channel Operation Modes

See receive command buffer in Section "External Memory Organization and Definition" for details (Figure 27).

Figure 12. Block Diagram of Receive Bit-Level Processor



- HDLC Mode

In HDLC mode, the Receive Processor detects flags, abort, delete zero-bit, check the Frame Check Sequences (FCS), and filters the time-fill bits by applying FILL/MASK byte to the received data.

Reset the device will make all channels in HDLC mode.

- Non-HDLC Data Mode

In this mode, received data are directly written into external memory without deformating.

- Non-HDLC Signaling Mode

In non-HDLC signaling mode, PT7A6632 detects the multiframe alignment sequence. If the alignment sequence is valid, the received data will be sent to the external memory; if not, the data will not be sent to external memory until a valid alignment sequence is detected. The loss of the multiframe alignment will be reported to external memory. Any channel(s) can be specified to receive bit-oriented signaling. This feature is very useful in central office switching applications.

Figure 13. 32kb/s Subrate Operation - Single Receive Channel

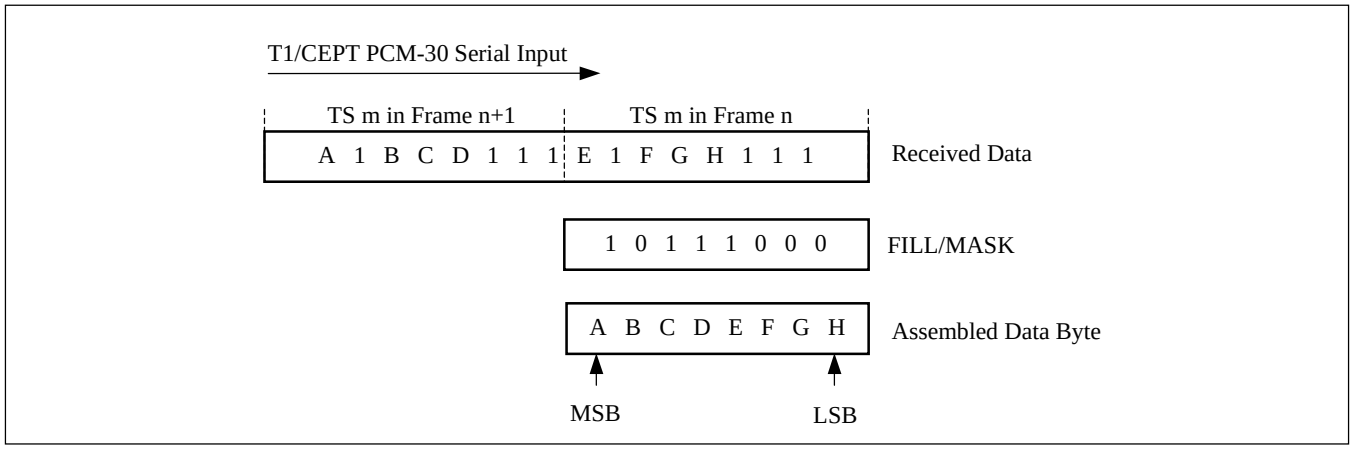


Figure 14. Receive Frame Synchronization Timing - T1 Mode, SIS = 1

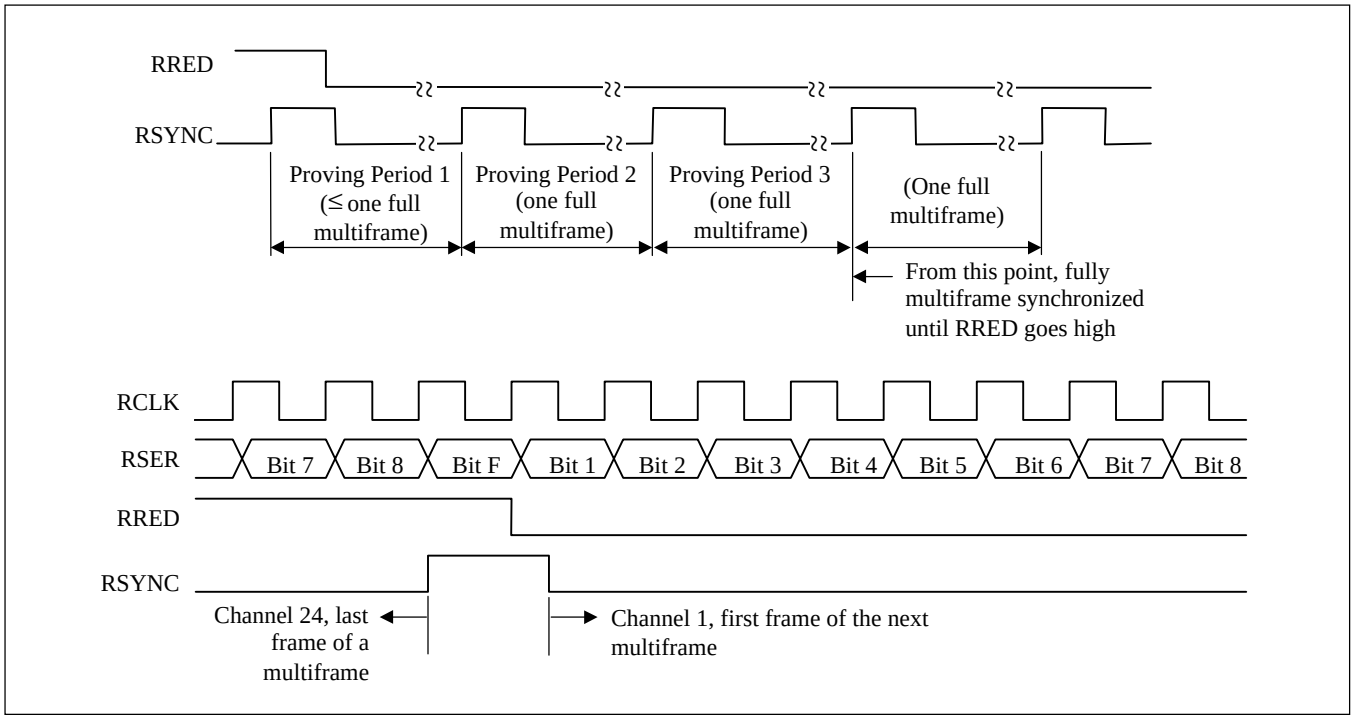


Figure 15. Receive Frame Synchronization Timing - CEPT PCM-30 Mode, SIS = 1

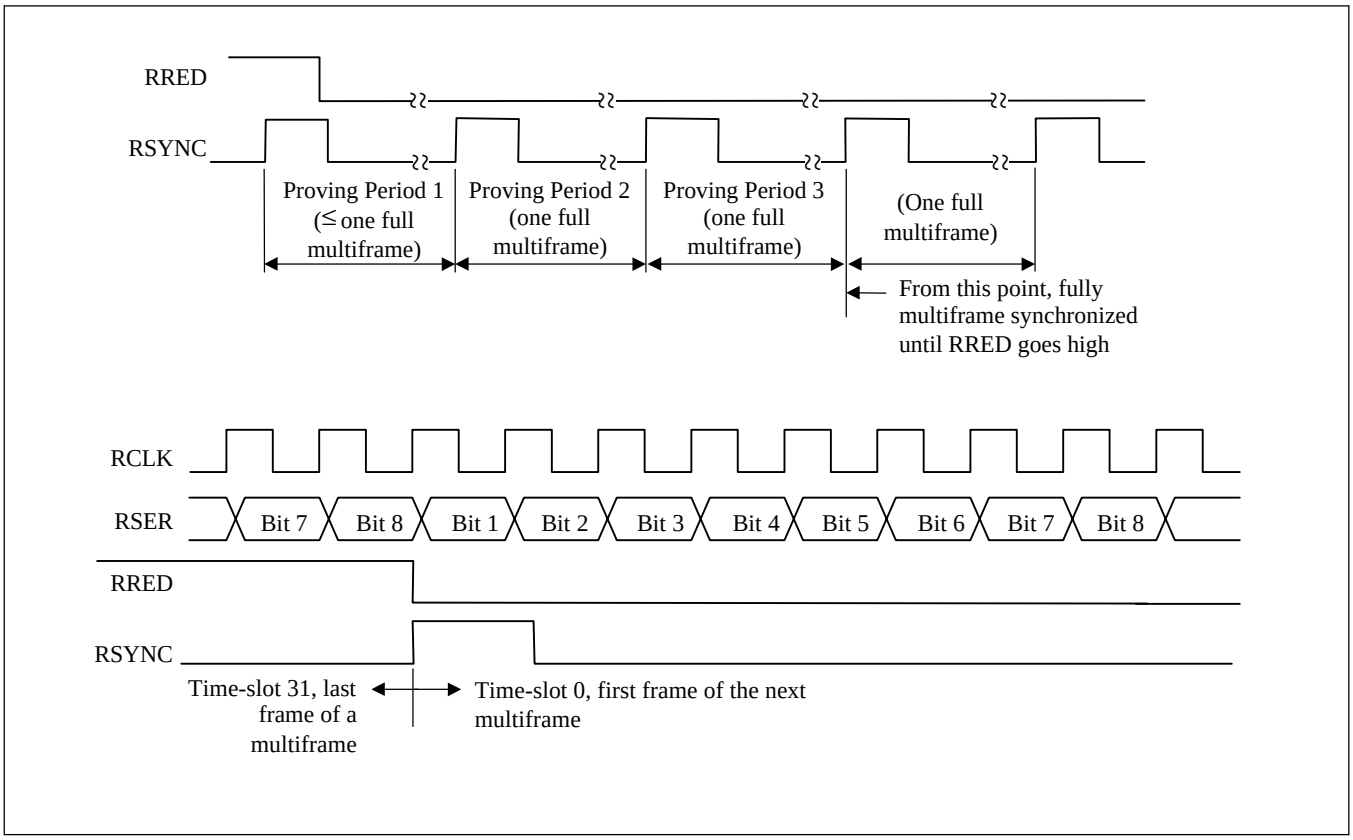


Figure 16. Receive Frame Synchronization Timing - T1 Mode, SIS = 0

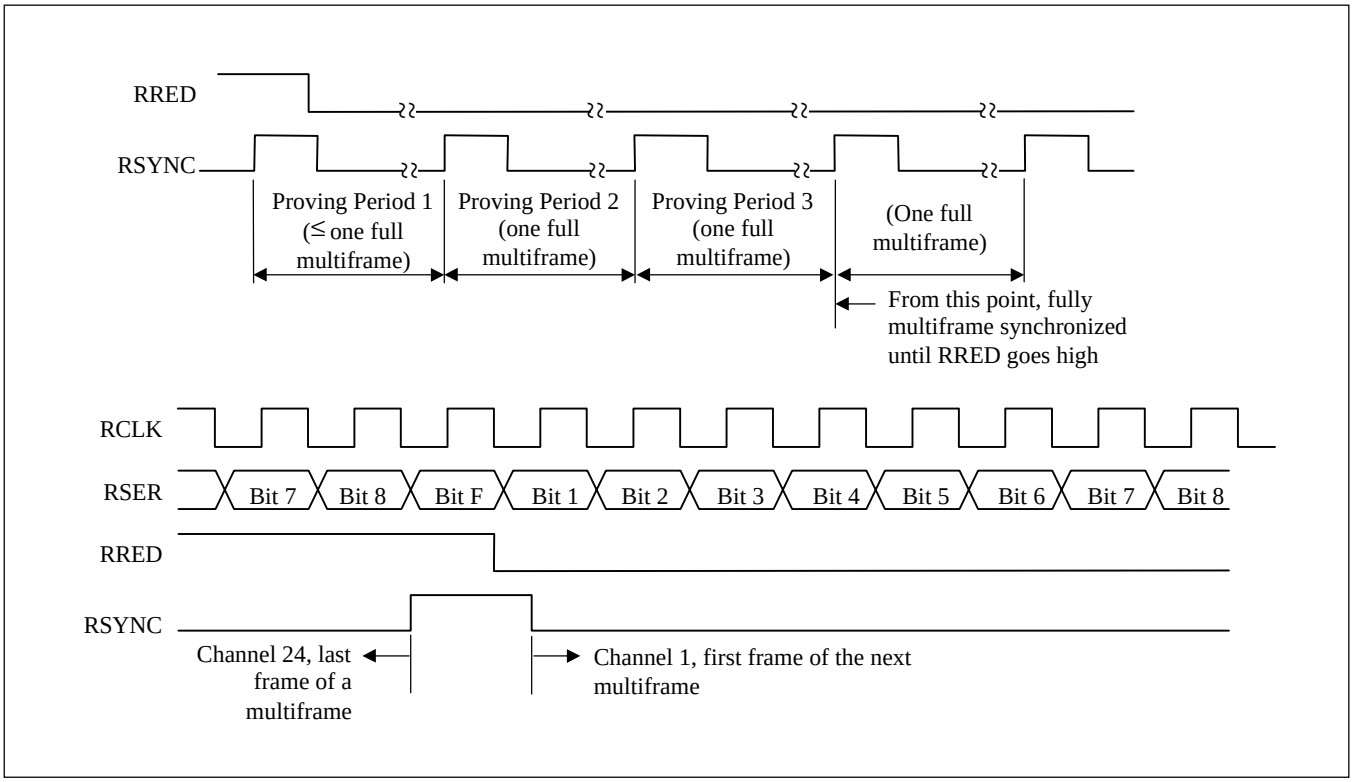
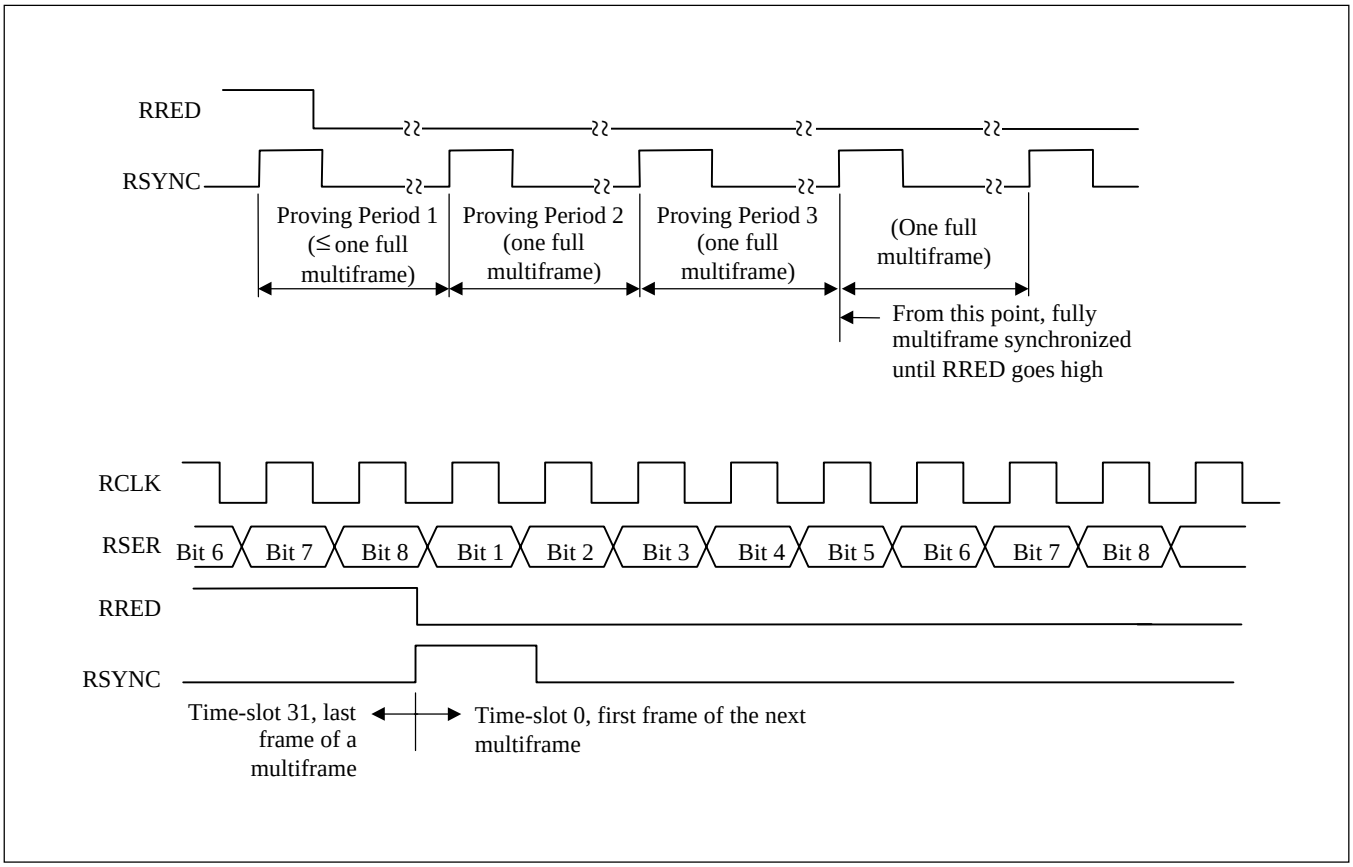


Figure 17. Receive Frame Synchronization Timing - CEPT PCM-30 Mode, SIS = 0



- Loop Mode

When a receive channel is specified in Loop Mode, data to be sent to the external memory is not from the external T1/E1 trunk interface, instead, it is fetched internally from an intermediate buffer in the PT7A6632, in which the data was from a loop mode transmit channel. Thus the data from the external memory is feedback to external memory. Each time only one transmit and one receive channel can be specified in Loop Mode to guarantee normal operation. The transmit loop channel No. and receive loop channel No. are not necessarily identical. The Loop Mode does not support hyperchannel.

Reset the device will delete all Loop Mode.

- Logical Inversion

If a receive channel is set in inversion mode, the received data will be inverted bit by bit when being processed, including flag, ABORT and FCS bits.

Reset the device will make all channel in inversion mode.

Data Reception Order

The PT7A6632 writes received data bytes in the external memory in the same order in which they are received in time. For a certain channel, the first received byte is written at byte address m, the second received at byte address m+1, and so on as long as the buffer is not completely filled or an end-of-frame is not reached. After the end of the frame or the end of the buffer (whichever occurs first) is detected, the PT7A6632 writes the next received data byte at the first allocated address of the next available buffer.

The PT7A6632 writes the first received data bit of an octet at the LSB (D0) position of the external buffer byte, the second received data bit at the next to LSB position, and so on. The last (8th) received data bit of an octet is written at the MSB (D7) position of the data byte.

Memory Manager

The Memory Manager controls data flow between Transmit Processor/Receive Processor and the external memory as shown in Figure 18. CPU assigns the external memory into several parts for activation information (Activation Memory) and data processing information (Data Processing Memory) as shown in Figure 20 in Section "External Memory Organization and Definition".

The Data Processing Memory is allocated to each transmit and receive channel for data, command and status storage. The CPU allocated enough memory in the buffers for the real-time operation of transmit and receive with no data underrun or overrun. The external memory is managed with minimal intervention from the CPU.

The CPU sends out an ATTN signal to command PT7A6632 to access the Activation Memory that contains channel number and channel starting address. The SYSACC signal is asserted by PT7A6632 during accessing the Activation Memory. After the access, the ATACK will be asserted.

The Data Processing Memory contains such information as next buffer address, operation mode, buffer size, data length, buffer status and HDLC frame completion status. They are set up by CPU. PT7A6632 accesses the buffers and processes data and update the status in the buffers after processing. DMND is asserted by the PT7A6632 to inform other devices using the memory bus that PT7A6632 will access the external memory one TCLK period after rising edge of the DMND. $\overline{INTR}$ asserted when PT7A6632 updates the status byte in buffers.

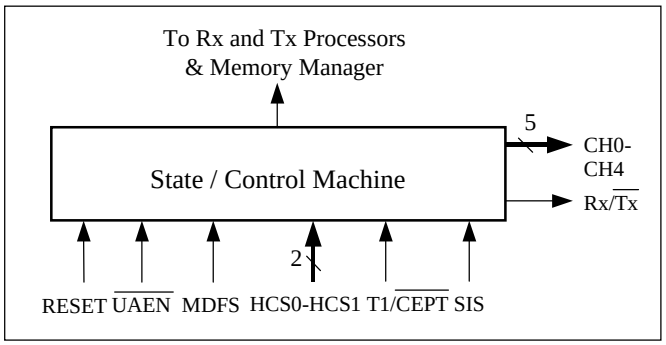
The memory manager responds to CPU-initiated changes in the operational modes of a channel or relocation of the allocated buffers without affecting the operation of the other channels.

The timing for the memory access is generated from SYSCLK.

State/Control Machine

The State/Control Machine processes the device mode and status. MDFS sets the memory location pattern, i.e., the even addresses in external memory are for higher bytes (MDFS = 1) or for lower bytes (MDFS = 0) of the Next Buffer Starting Address, Buffer Size and Data Length respectively.

Figure 19



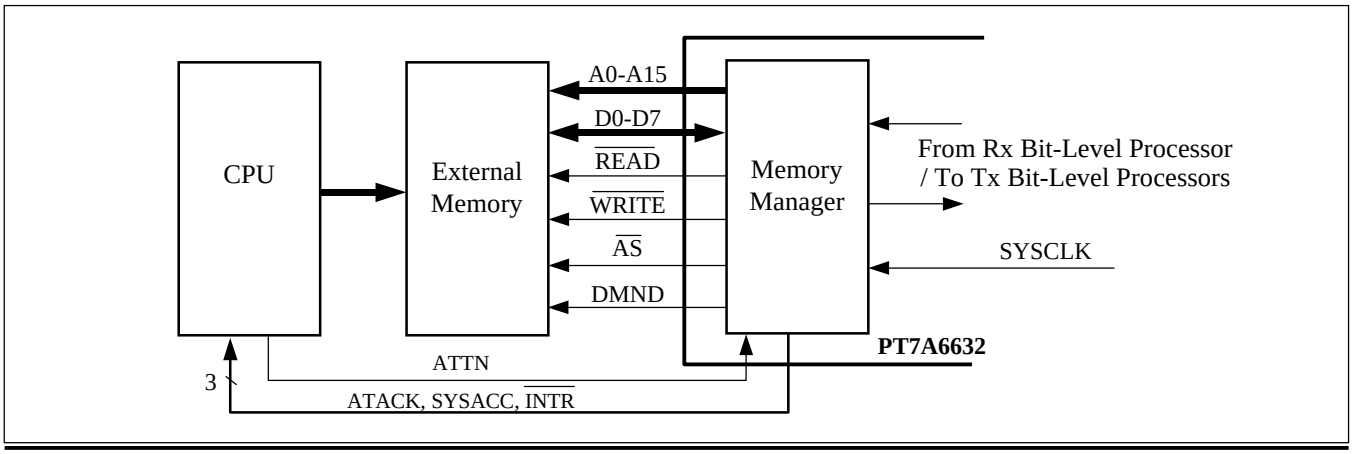
$\overline{UAEN}$ sets the Upper address lines (A8 - A15) in high impedance ($\overline{UAEN}$ = 1) or in Low state ($\overline{UAEN}$ = 0) when accessing Activation Memory. When the upper address lines in high impedance, the CPU can drive them to any state during accessing activation memory.

HCS0, HCS1 and T1/$\overline{CEPT}$ select T1 or CEPT PCM-30 mode and hyperchannel (Table 3). SIS selects trigger edge of RCLK and TCLK. TSEREN sets TSER output line state, i.e., sending data, sending "1" or in high impedance (Table 4).

CH0 to CH4 and Rx/$\overline{Tx}$ are status outputs indicating the current active channel number and direction. CH0 is LSB, CH4 is MSB.

The main clock for PT7A6632 is generated by the State/Control Machine from SYSCLK.

Figure 18. Diagram of Memory Manager with External Memory and CPU



External Memory Organization and Definition

General Structure

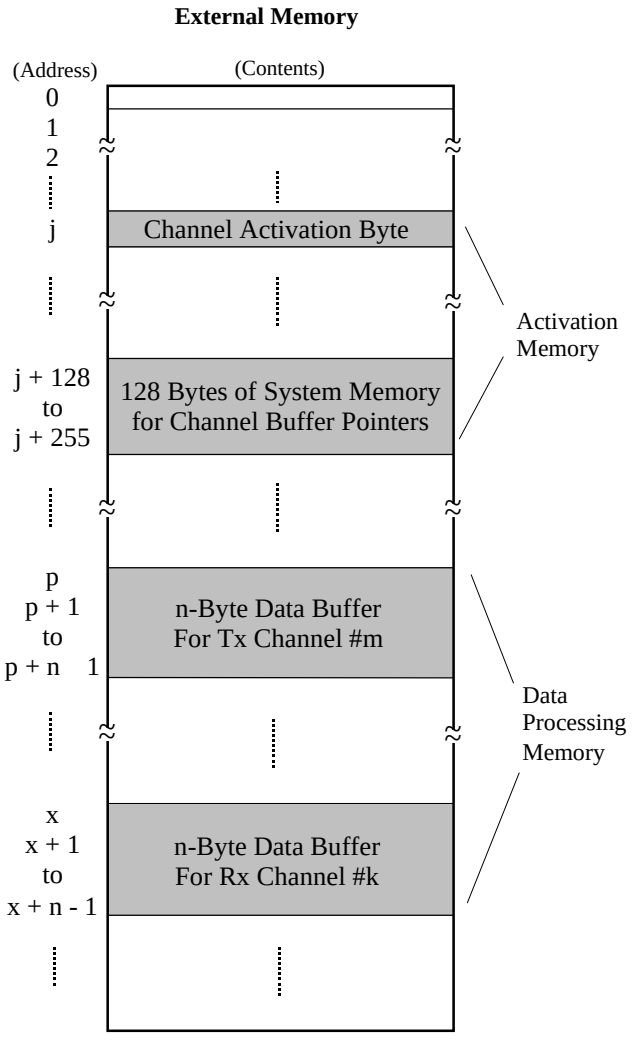
The external memory is divided by the CPU into two functional blocks for channel activation and data processing, referred as Activation Memory and Data Processing Memory.

The Activation Memory contains Channel Activation Byte and Channel Buffer Pointers, providing PT7A6632 such information as channel activation/deactivation, channel direction (transmit or receive) and channel starting addresses. CPU allocates the Channel Starting Pointer for each receive and transmit channel.

The Data Processing Memory contains data/command buffers storing descriptors, user's data received or to be transmitted, channel operation mode and status. CPU allocates a set of linked data/command buffers for each receive and transmit channel.

Details are shown in Figures 20-22.

Figure 20. External Memory Map - Top Level



Activation Memory

The Activation Memory map is shown in the Figure 21.

Channel Activation Byte

The Channel Activation Byte are illustrated in the following table 5. The PT7A6632 reads this byte so that gets the channel number, the channel state (active or inactive) and the channel direction (transmit or receive). The PT7A6632 asserts SYSACC when it accesses the Activation Memory.

Channel Buffer Pointers

Channel Buffer Pointers provide PT7A6632 the channel starting address (16-bit) for each channel, 64 channels totally, guiding to a link of buffers containing data and command. The relative location of the upper and lower bytes of the 16-bit start address word is determined by the MDFS input (see Figure 17). The upper address lines (A8-A15) are placed in the high-impedance state or LOW by the PT7A6632 during the Activation Memory accesses.

Table 5. Channel Activation Byte

Bit 7		Bit 6	Bit 5		Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Active bit			Rx/$\overline{Tx}$ bit		Channel Number 0 ~ 31 (Binary)				
1	0	Unused	1	0	0 0 0 0 0 - channel 0, 0 0 0 0 1 - channel 1, 0 0 0 1 0 - channel 2, etc.				
The channel activated	The channel deactivated		Receive	Transmit					

Figure 21a. Activation Memory Map Locations (MDFS = HIGH)

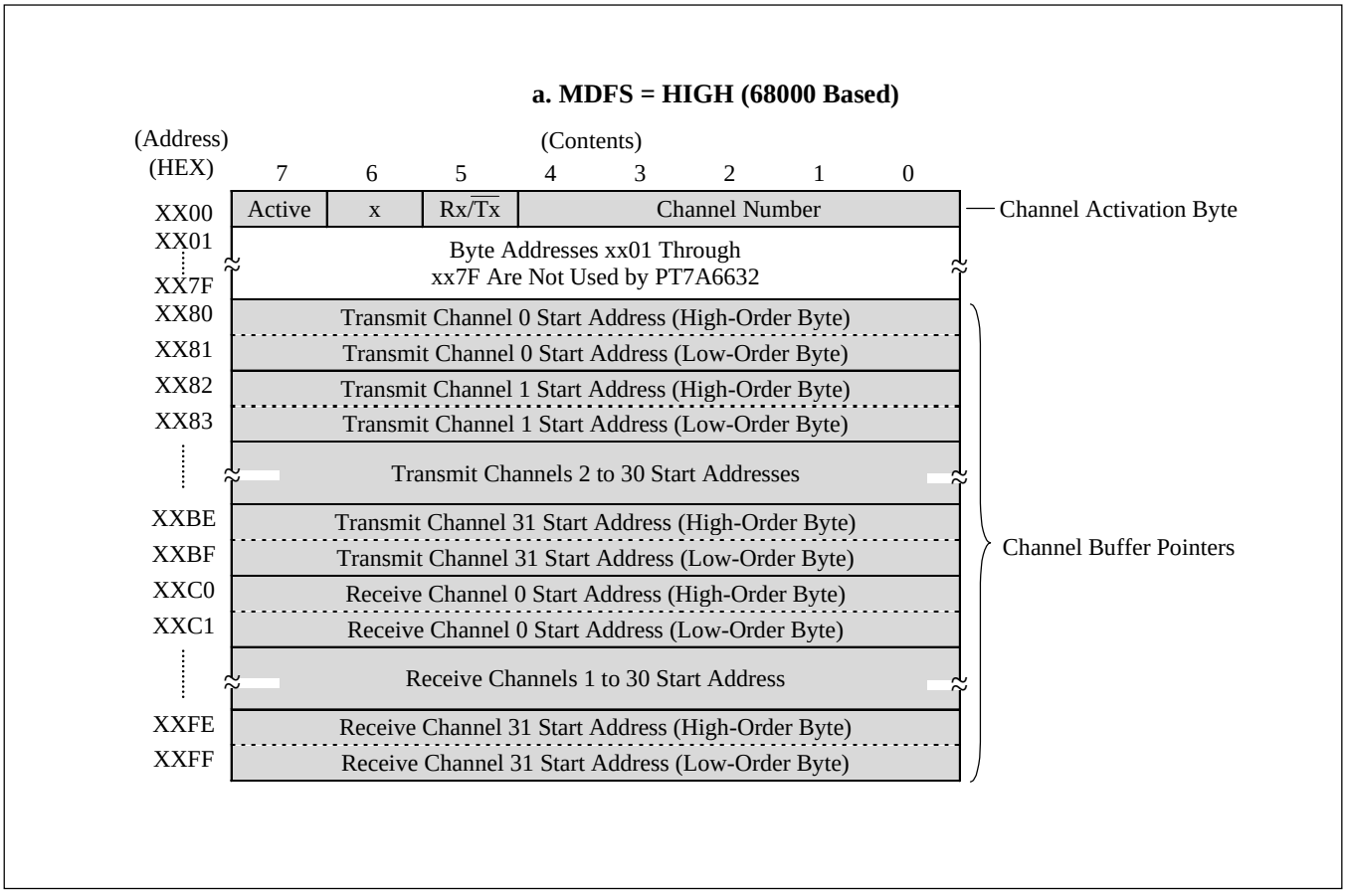


Figure 21b. Activation Memory Map Locations (MDFS = LOW)

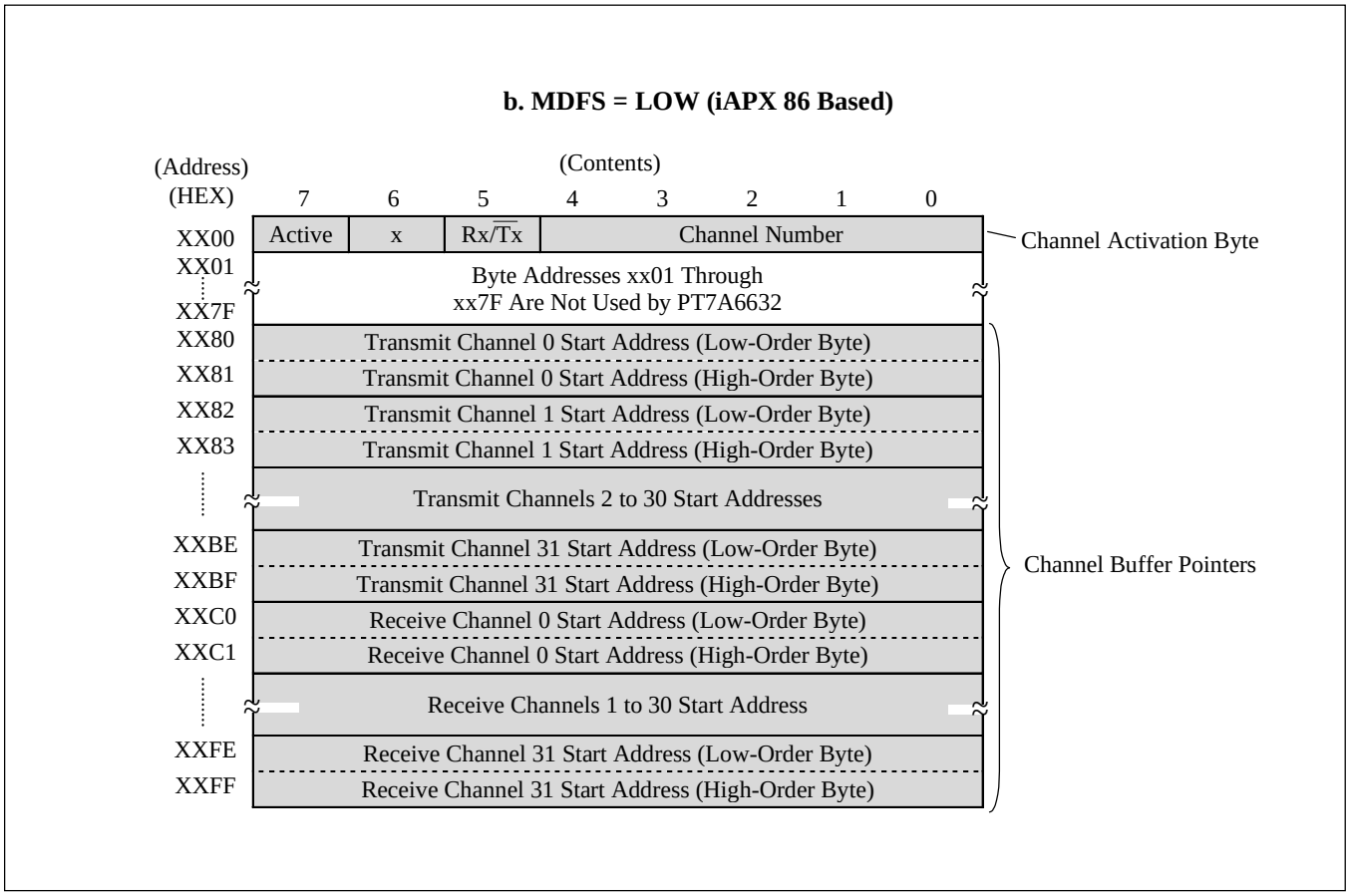
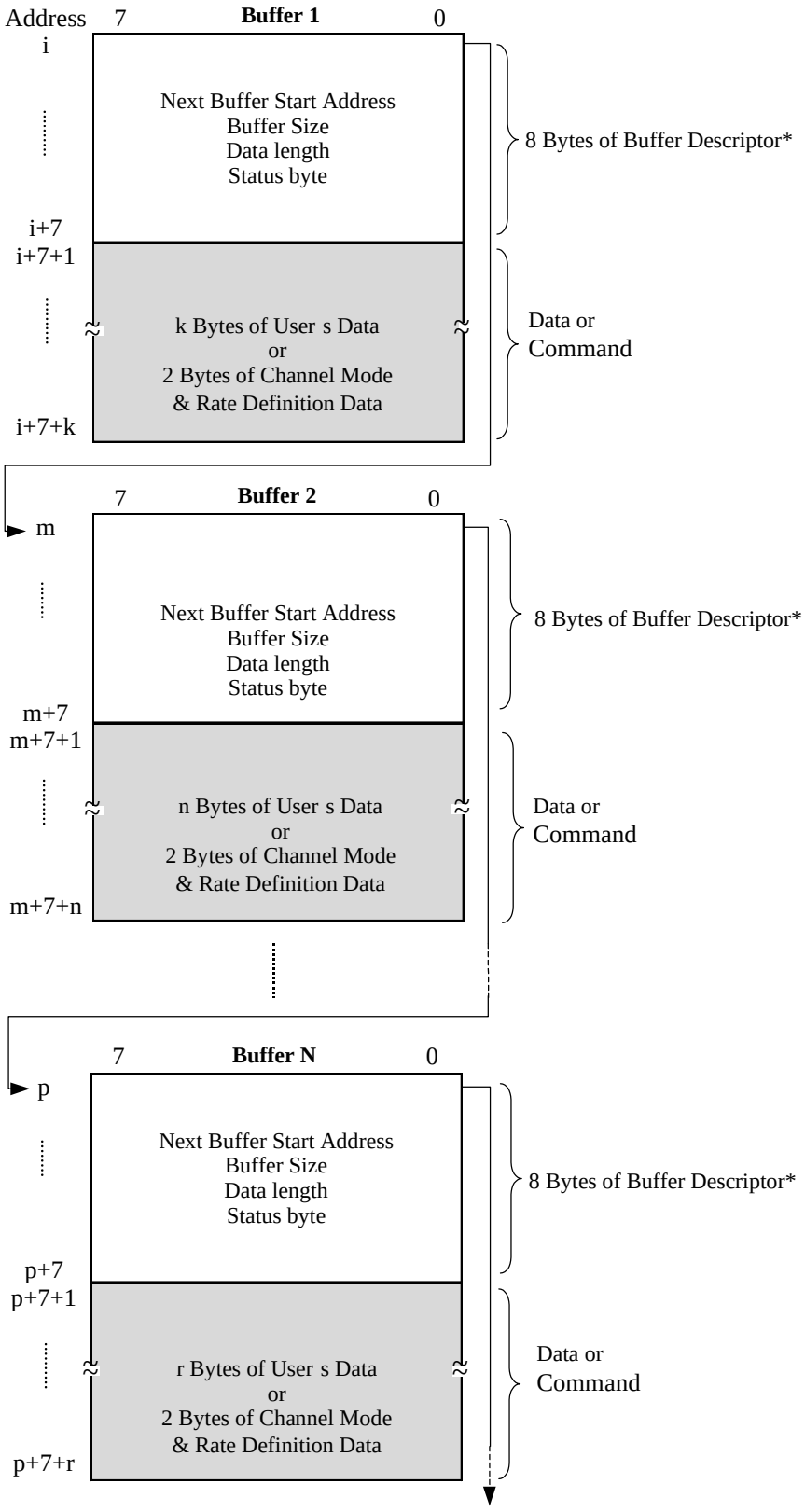


Figure 22. Organization and Linking of Data or Command Buffers



* Formats are different for Data buffer and Command buffer, and differs with MDFS

Data Processing Memory

General

The Data Processing Memory refers to Data or Command buffers which are linked each other. The PT7A6632 accesses the Data Processing Memory for transmit/receive data and operation commands. Each buffer has following configuration (see Figure 22):

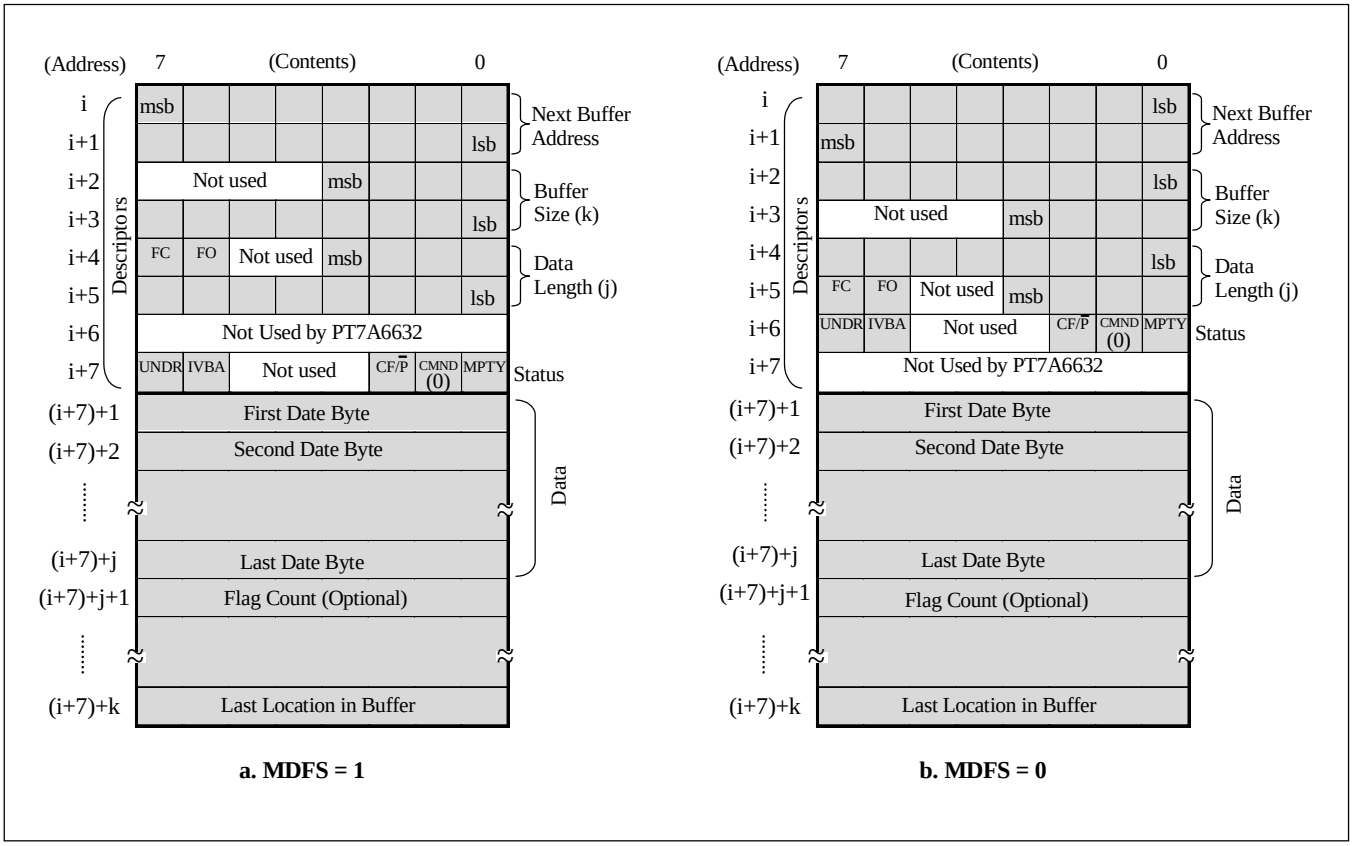
- 8-Byte Descriptors
- Data bytes to be transmitted or received or Command

There are 4 kinds of buffers, Transmit Data Buffer and Transmit Command Buffer for transmit channels, and Receive Data Buffer and Receive Command Buffer for receive channels.

Transmit Data Buffer

The Transmit Data Buffer contains 8 bytes of descriptors and j bytes of user's data as shown in Figure 23. The MDFS pin decides the most significant byte and least significant byte locations (in even and odd addresses).

Figure 23. Transmit Data Buffer



- Descriptors

The first 8 bytes in the transmit Data Buffer is Descriptors that specifies Next Buffer Address, Buffer Size, Data Length and Status respectively. See Table 6 for the definition.

- Data Bytes

Following the Descriptors are the data to be transmitted. The number of bytes are specified by Data Length (for complete data buffer) or Buffer Size (for partial data buffer). The buffer may contains last byte of a frame (CF/$\overline{P}$ = 1) or partial data of a frame (CF/$\overline{P}$ = 0) in HDLC mode. The CF/$\overline{P}$ should be reset for other modes.

- Flag Count Byte (Optional)

Specifies the additional flags to be added after "CRC + one Flag" of a frame. It will be read only when Flag Control bit in the MS byte of Data Length is set (FC = 1).

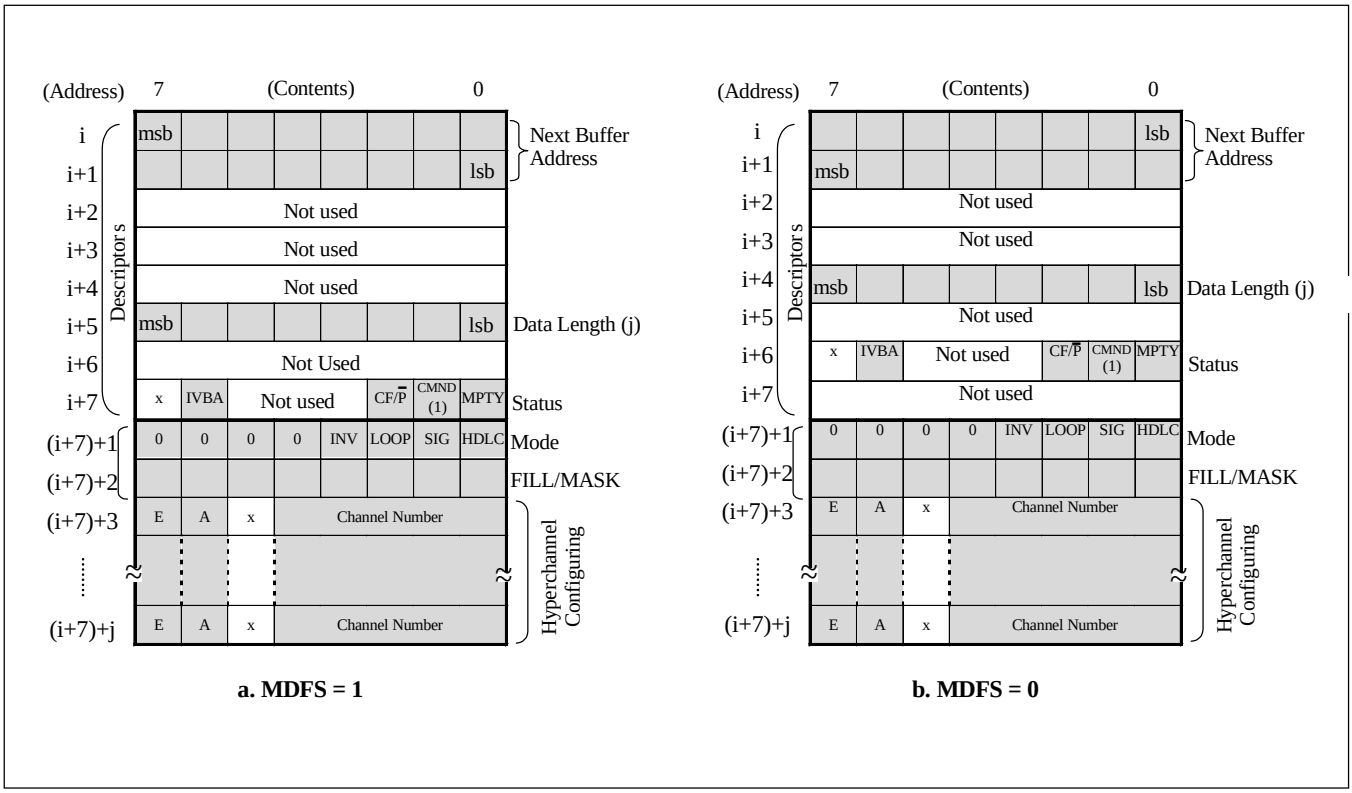
Table 6. Descriptors in Transmit Data Buffer

Name	Description
Next Buffer Address	16-bit address word, pointing to next buffer for 6632 to access
Buffer Size	12-bit, specifies byte number of memory locations allocated by the CPU for current buffer. The 6632 reads the Buffer Size only when the Status (CF/$\overline{P}$ = 0) shows that the data buffer contains partial data. The 6632 will convert the Buffer Size to the actual number of data bytes in this buffer.
FC	**Flag Control**: 1-bit, indicates if any additional flags (except the minimum one flag followed CRC for HDLC format) to be appendixed after the (CRC+1 FLAG) of the HDLC data. If FC is reset by the CPU, it means no additional flag to be added. If set by the CPU, it means there will be additional flag(s) to be added to the data. The number of the additional flag(s) is specified in the optional FLAG COUNT byte in the Tx Data Buffer.
FO	**Flag Offset Count**: 1-bit, meaningful only when FC = 1. If FO is set by the CPU, the Tx channel counts the total number of intentionally inserted zeros based on HDLC protocol, then divides the counted results by 8.The quotient (called "Flag Offset") represents the number of non-data byte inserted in the data. The 6632 subtracts the Flag Offset from the FLAG COUNT, which was set without knowledge of the inserted zeros. The resultant is the actual number of additional flags to be added to the data.
Data Length	12-bit, specifies the actual number of data bytes to be transmitted in the Tx Data Buffer. The 6632 reads the Data Length only if the Status shows that the buffer contains the last byte of a frame (CF/$\overline{P}$ = 1).
MPTY	**Empty**: 1-bit, if set by the CPU, it means the buffer is empty, i.e., data is not ready for transmission. The 6632 will keep polling this bit until it is reset. The CPU resets this bit when the data is ready. 6632 sets the bit to 1 once it completes data transmission in the buffer, and the CPU can reuses the empty locations.
CMND	**Command**: 1-bit, when set by the CPU, it means the buffer is a Command Buffer. If reset by the CPU, it is a Data Buffer.
CF/$\overline{P}$	**Complete Frame/Partial Data Buffer:** 1-bit, set by the CPU to show that the data buffer contains the last byte of an HDLC framed data. Actual number of data bytes is specified by the Data Length (Max. Data Length: 4095). If it is reset by the CPU, it means the buffer contains partial data of a frame, and the rest data is in succeeding buffer(s). The 6632 automatically turns to the next successding buffer. Actual number of data bytes is specified by the Buffer Size (Max. Buffer Size: 4095). For non-HDLC data, the bit should be 0 for continuously data transmission, otherwise data transmission will be interrupted.
IVBA	**Invalid Buffer Address**: 1-bit, the 6632 sets the bit if it finds an invalid Next Buffer Address, i.e., such as address of 16 zeros or in form of FFFx. In this case, the Tx channel will be deactivated and all-one bytes be transmitted until the channel is re-activated by the CPU.
UNDR	**Underrun**: 1-bit, the 6632 sets the bit if the current Tx channel runs out of data, e.g., when the 6632 finds an invalid buffer address, an empty buffer, or a command buffer following a partial data buffer. If so, the 6632 will send out an ABORT code followed by Flags until the condition is cleared (if in HDLC mode), or the 6632 will send out all-ones bytes repeatedly until the CPU sets up a valid non-empty data buffer (if in non-HDLC mode).

Transmit Command Buffer

The Transmit Command Buffer contains 8 bytes of descriptors and 2 bytes of Channel Mode & Rate Definition Data (and maybe the Hyperchannel Configuring Bytes) as shown in Figure 24. The MDFS pin decides the MS byte and LS byte locations (in even and odd addresses).

Figure 24. Transmit Command Buffer



a. MDFS = 1

b. MDFS = 0

- Descriptors

The first 8 bytes in the Transmit Command Buffer are Descriptors that specify Next Buffer Address, Data Length and Status respectively. See Table 7 for the definition.

Table 7. Descriptors in Transmit Command Buffer

Name	Description
Next Buffer Address	16-bit address word, pointing to next buffer for 6632 to access
Data Length	8-bit, decides the non-flexible-hyperchannel process or flexible hyperchannel process. Data Length = 0, 1 or 2, only non-hyperchannel process, Data Length > 2, there is hyperchannel process.
MPTY	**Empty**: 1-bit, the CPU sets it to show that the buffer is empty, i.e., command data is not ready. In this case the 6632 will keep polling this bit until it is reset.The CPU resets this bit when the command data is ready. 6632 sets the bit to inform the CPU completion of command processing in the buffer.
CMND	**Command**: 1-bit, set by the CPU to indicate the buffer is a Command Buffer.
CF/$\overline{P}$	**Complete Command Buffer/Partial Command Buffer:** 1-bit, set by the CPU to indicate that the command buffer is a Complete Command Buffer. During the Complete Command Buffer processing, the 6632 will transmit an HDLC ABORT if it is in HDLC mode. The CPU resets the CF/$\overline{P}$ bit to indicate a Partial Command Buffer (CF/$\overline{P}$=0, CMND=1). In this case the 6632 will send HDLC flag or non-HDLC all-ones byte(s), then continue to process next buffer.
IVBA	**Invalid Buffer Address**: 1-bit, the 6632 sets the bit if it finds an invalid Next Buffer Address, such as address of 16 zeros or in form of FFFx. In this case, the Tx channel will be deactivated and all-one bits be transmitted until the channel is re-activated by the CPU.

- MODE Byte (Channel Mode)

The MODE byte is set up by the CPU to specify channel modes of HDLC, non-HDLC signaling, non-HDLC data, loop, non-loop, inversion or non-inversion.

The details are shown in Table 8.

Table 8. MODE Byte in Transmit Command Buffer

MODE	Name	Description	
Bits 7 - 4		Not used	
Bit 3	INV	1	Invertion
		0	Non-invertion
Bit 2	LOOP	1	Loop channel
		0	Non-loop channel
Bit 1, Bit 0	SIG, HDLC	00	**Non-HDLC data channel mode**: used in modes 0 and 1 of DMI application. CF/$\overline{P}$ should be reset to get uninterrupted data transmission, otherwise the 6632 will transmit all-one byte repeatedly following the last byte in the buffer. The channel time fill and the idle codes are the same.
		01	**HDLC data channel mode:** The channel is an HDLC channel or an LAPD message-oriented channel. Information field is in integral bytes, 16-bit CRC-CCITT polynomial is used to calculate FCS, and ABORT sequence satisfies SDLC and HDLC requirements.
		10	**Non-HDLC signaling channel mode:** The channel carries bit-oriented signaling data. 6632 assumes that no more than 2 linked data buffers are allocated to the signaling channel by the CPU. The last data buffer (even if it is the only buffer) is assumed to be a recirculating buffer.
		11	Reserved

- FILL/MASK Byte (Rate Definition)

The FILL/MASK byte is used as a masking pattern on the HDLC-formatted (including FLAG, header, data, CRC, and ABORT code) or non-HDLC-formatted data in order to adapt subrates that are multiples of 8kb/s to the 64kb/s rate. The 8-bit sequence is applied to data on a bit by bit basis to insert 1 (FILL/MASK bit = 0) for time fill, or insert data bit (FILL/MASK = 1). See an example in Figure 6 in Section "Transmit Bit-Level Processor" and Table 9.

For bit-oriented signaling mode, the FILL/MASK should be set as 1111 1111. If not, the PT7A6632 will not override any other FILL/MASK pattern.

Table 9. Examples of FILL/MASK Options

Option Number	Data Rate	Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Remarks
0 *	0 kb/s	0	0	0	0	0	0	0	0	No data will be sent. Eight 1s for time fill will be sent if TSEREN=1.
1	8 kb/s	0 0	0 0	0 1	0 0	0 0	0 0	0 0	1 0	Arbitrary-user defined; a 1 in any one bit position, but only one 1.
2	16 kb/s	0 0 0 1	0 0 0 1	1 0 0 0	0 0 1 0	0 1 0 0	0 1 1 0	1 0 0 0	0 0 0 0	User defined pattern; a 1 in any two bit positions, but only two 1s.
3	24 kb/s	0 0	0 1	0 0	0 1	0 0	1 1	1 0	1 0	A total of three 1s anywhere as defined by user.
4	32 kb/s	0 1 1	0 1 0	0 1 1	0 1 0	1 0 1	1 0 0	1 0 1	1 0 0	A total of four 1s anywhere as defined by user.
5	40 kb/s	0	0	0	1	1	1	1	1	A total of five 1s anywhere as defined by user.
6	48 kb/s	0	0	1	1	1	1	1	1	A total of six 1s anywhere as defined by user.
7	56 kb/s	0 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	Standard rate in digital data service, restricted version of 64 kb/s. A total of seven 1s anywhere as defined by user.
8	64 kb/s	1	1	1	1	1	1	1	1	

* A special purpose mode in which the transmitter operates as if it is at 64 kb/s, including when it is fetching data from the external memory, even though no data is transmitted.

- Flexible Hyperchannel Configuring Byte (Optional)

The byte follows the FILL/MASK byte if any. It is used to configure flexible hyperchannel. Bits 0 - 4 specify number of a channel to be grouped into or removed from a hyperchannel. Bits 6 and 7 is for hyperchannel enable and add/delete respectively. See Table 10 for details.

Table 10

Bit 7 (E)	Bit 6 (A)	Description
0	x	Hyperchannel assignment remains unchanged.
1	0	Delete channel number in bits 0-4 from hyperchannel.
1	1	Add channel number in bits 0-4 to hyperchannel.

Data Length is used to specify flexible hyperchannel. When Data Length = 0, 1 or 2, only normal channel process. When Data Length > 2, there is hyperchannel process.

- Flexible Hyperchannel

The Flexible Hyperchannel mode allows the PT7A6632 to group any number of 32 64kb/s channels into a hyperchannel. The Data Length (>2) is read to decide the number of additional channels to be added to a hyperchannel. If a previously activated channel is assigned to a flexible hyperchannel, it will suspend the original buffer process, and the process will be restored once the channel is released from the hyperchannel. It may take one frame time. A channel can be assigned to one hyperchannel only.

The channel map may be updated in one cycle of channel counting. In flexible hyperchannel mode, the HCS0 and HCS1 should be set as “0 0”, otherwise the standard hyperchannel will override the flexible hyperchannel.

- Partial Command Buffer

If the CPU can not make next buffer ready before the PT7A6632 completes data transmission of a channel, the CPU will reset the CF/$\overline{P}$ bit to indicate that it is a Partial Command Buffer (CF/$\overline{P}$=0, CMND=1). In this case the PT7A6632 will read Next Buffer Address and send a HDLC flag(s) or a non-HDLC octet all-ones to fill the gap, then the PT7A6632 turns to a new buffer chain as if it complete a normal buffer process by setting the MPTY and CF/$\overline{P}$ bits.

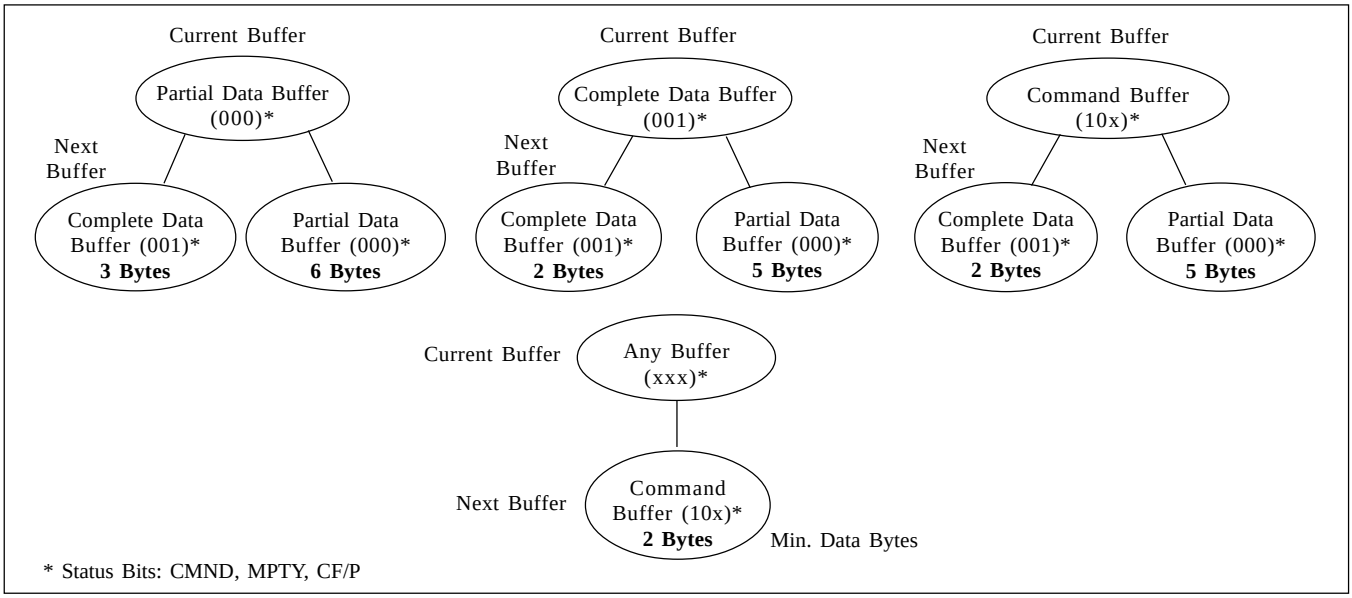
The PT7A6632 sends out flags or all-ones until it is informed to resume data transmission by the CPU again. One Partial Command Buffer sends one flag or one all-ones byte, a chain of Partial Command Buffer sends multiple flags or ones. The Partial Command Buffer processing will not change the MODE and FILL/MASK.

If a Partial Command Buffer is processed after a partial data buffer, the HDLC ABORT or non-HDLC all-ones will be sent.

Minimum Number of Data Bytes in a Tx Buffer

For Transmit Data Buffers and Transmit Command Buffers, minimum number of data bytes is required for buffer maintenance and buffer transition. The minimum numbers depend on the current buffer type and next buffer type. Refer to Figure 25.

Figure 25. Minimum Data Bytes for Transmit Buffer



Receive Data Buffer

The Receive Data Buffer contains 8 bytes of descriptors and j bytes of user's data as shown in Figure 26. The MDFS pin decides the MS byte and LS byte locations (in even and odd addresses).

- Descriptors

The first 8 bytes in the Receive Data Buffer are Descriptors that specify Next Buffer Address, Buffer Size, Data Length and Status respectively. See Table 11 for the definition.

- Data Bytes

Following the Descriptors are received data. The number of data bytes are indicated by Data Length which is written by the PT7A6632 after it receives the last byte of an HDLC frame or the HDLC ABORT code, upon the loss of multiframe alignment error from a non-HDLC signaling channel, or when Receiver Bit-Level Processor detects receive synchronization error caused by RSYN, elastic buffer error or RRED. When it is a partial data buffer, the number of data bytes is indicated by the Buffer Size.

Figure 26. Receive Data Buffer

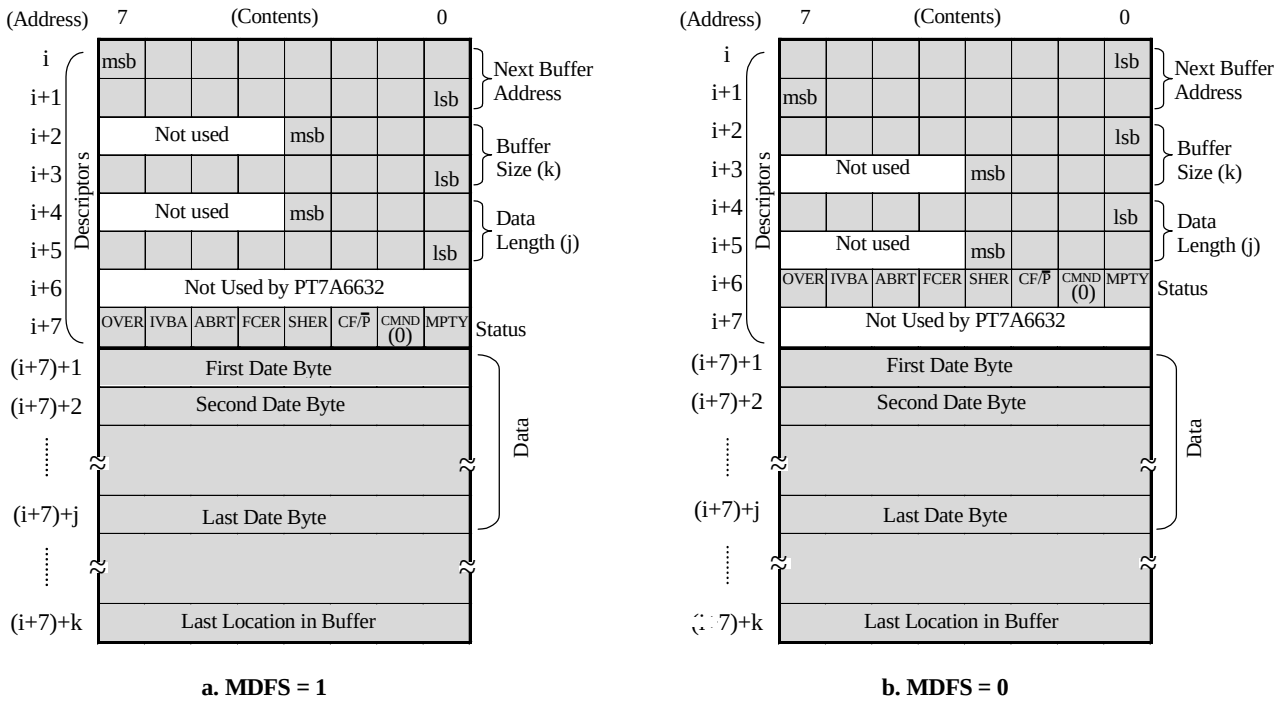


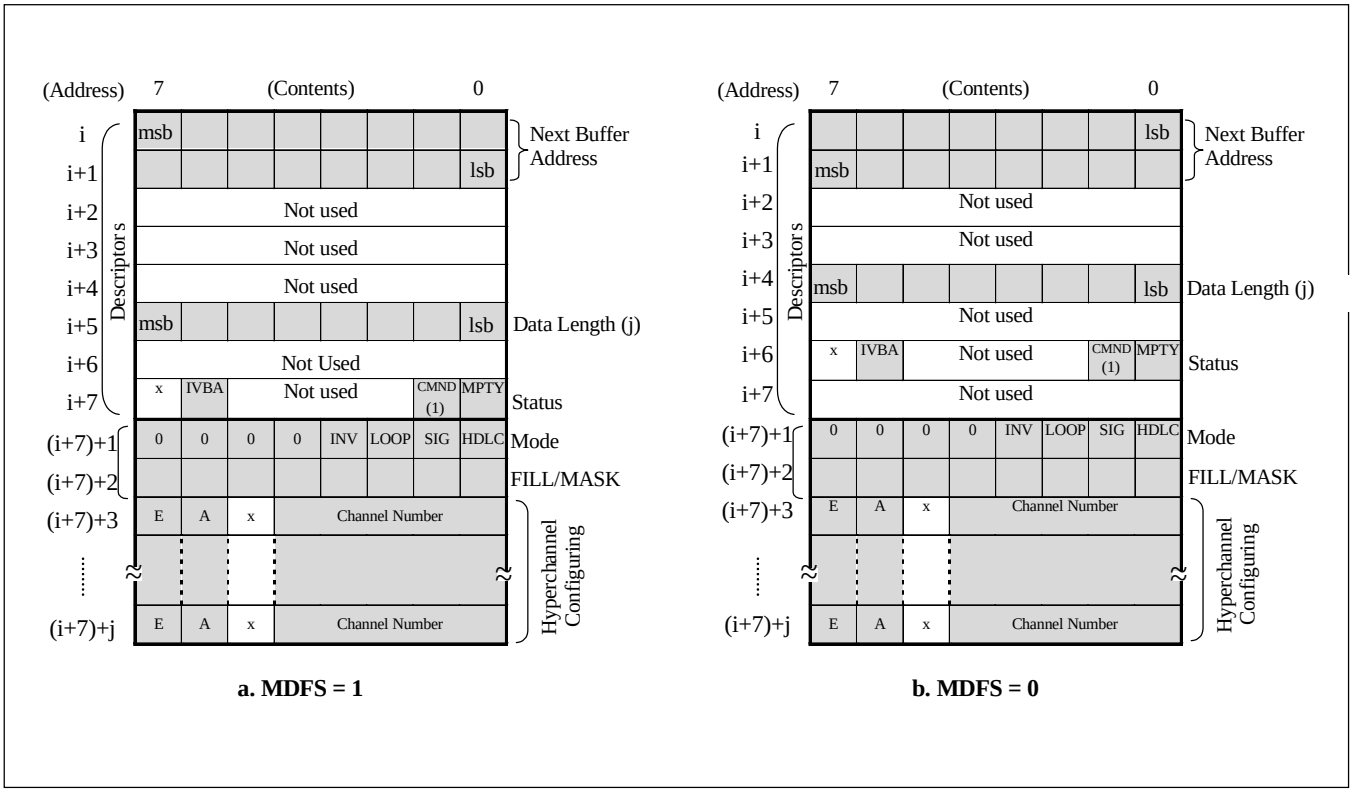
Table 11. Descriptors in Receive Data Buffer

Name	Description
Next Buffer Address	16-bit address word, pointing to next buffer for 6632 to access
Buffer Size	12-bit, specifies byte number of memory locations allocated by the CPU for current buffer. The 6632 reads the Buffer Size when writes data into the buffer.
Data Length	12-bit, the actual number of data bytes received by 6632, written by the 6632 after it receives the last byte of an HDLC frame or the HDLC ABORT code, or upon the loss of multiframe alignment error from a non-HDLC signaling channel. DATA LENGTH is not written if the end of the allocated buffer is reached before the last byte is received (i.e., if data frame length is greater than buffer size). In such a case, the actual data length is equal to the given buffer size. Also, data length may not be written if the ATTN input is asserted, resulting in the deactivation or reactivation of an active channel. DATA LENGTH will not exceed the programmed buffer size.
MPTY	**Empty**: 1-bit, if set by the CPU, it means the buffer is empty, i.e., the buffer is ready for storing received data. The PT7A6632 resets this bit when the buffer is not empty. The PT7A6632 will keep polling this bit until it is set. The 6632 resets the bit whenever it updates the status.
CMND	**Command**: 1-bit, when set by the CPU, it means the buffer is a Command Buffer. If reset by the CPU, it is a Data Buffer.
CF/$\overline{P}$	**Complete Frame/Partial Data Buffer:** 1-bit, set by the 6632 to show that the data buffer contains the last byte of an HDLC framed data or that synchronization is wrong. It will also be set by the 6632 if the HDLC data or non-HDLC data receiving is aborted by re-synchro condition of ABORT, RRED, RSYNC or TMAX. The 6632 resets this bit when the last byte of an HDLC frame is not in this buffer and 6632 will store more data to the succeeding buffer. This bit will always be reset for non-HDLC mode or signaling mode.
ABRT FCER SHER	**Abort, Frame Check Error, Short HDLC Frame Error:** These 3 bits are used to report abnormal conditions detected by 6632. ABRT FCER SHER = 0 0 0: no errors detected, 0 0 1: short or non-integer HDLC frame error, 0 1 0: CRC error, 0 1 1: CRC error & non-integer error, 1 0 0: HDLC ABORT code received, 1 0 1: non-HDLC multiframe alignment lost, 1 1 0: elastic buffer error & RSYNC error, 1 1 1: RRED alarm.
IVBA	**Invalid Buffer Address**: 1-bit, the 6632 sets the bit if it finds an invalid Next Buffer Address, such as address of 16 zeros or in form of FFFx. In this case, the Rx channel will be in idle state and not receive more data until the channel is re-activated by the CPU.
OVER	**Overrun**: 1-bit, the 6632 sets this bit when the next empty data buffer is not available for received data before a frame is completed in HDLC data receiving, or when the next empty data buffer is not available for non-HDLC data receiving. No overrun reported for signaling channel. New data will be written in place of earlier received signaling data.

Receive Command Buffer

The Receive Command Buffer contains 8 bytes of descriptors and 2 bytes of Channel Mode & Rate Definition Data (and maybe Hyperchannel Configuring Bytes) as shown in Figure 27. The MDFS pin decides the MS byte and LS byte locations (in even and odd addresses).

Figure 27. Receive Command Buffer



- Descriptors

The first 8 bytes in the Receive Command Buffer is Descriptors that specifies Next Buffer Address, Data Length and Status respectively. See Table 12 for the definition.

Table 12. Descriptors in Receive Command Buffer

Name	Description
Next Buffer Address	16-bit address word pointing to next buffer for 6632 to access
Data Length	8-bit, decides the non-flexible-hyperchannel process or flexible hyperchannel process. Data Length = 0, 1 or 2, only normal channel process, Data Length > 2, there is hyperchannel process. In flexible hyperchannel mode, the Data Length is read to decide how many additional channels to be added to/remove from the hyperchannel, and the bytes contain the additional channel numbers are read to add/remove the corresponding channels.
MPTY	**Empty: 1-bit,** the CPU sets it to show that the buffer is empty, i.e., command data is not ready. In this case the 6632 will keep polling this bit until it is reset.The CPU resets this bit when the command data is ready. 6632 sets the bit to inform the CPU that it completes command processing in the buffer.
CMND	**Command**: 1-bit, set by the CPU to indicate the buffer is a Command Buffer.
IVBA	**Invalid Buffer Address**: 1-bit, the 6632 sets the bit if it finds an invalid Next Buffer Address, such as address of 16 zeros or in form of FFFx. In this case, the Rx channel will be deactivated until the channel is re-activated by the CPU.

- MODE Byte (Channel Mode)

The Channel Mode Byte is set up by the CPU to specify channel modes of HDLC, non-HDLC signaling, non-HDLC data, loop, non-loop, inversion or non-inversion.

The details are shown in Table 13.

Table 13. MODE Byte in Receive Command Buffer

MODE	Name	Description	
Bits 7 - 4		Not used	
Bit 3	**INV**	1	Invertion
		0	Non-invertion
Bit 2	**LOOP**	1	Loop channel
		0	Non-loop channel
Bit 1, Bit 0	**SIG,** HDLC	00	**Non-HDLC data channel mode**: used in modes 0 and 1 of DMI application. The 6632 check the availability of the allocated buffer and writes received data to the buffer. The 6632 updates the filled buffer status and asserts $\overline{\text{INTR}}$, then moves to the next data buffer. The data receiving and writing will continue until it is interrupted by an ATTN signal or no more buffer available.
		01	**HDLC data channel mode:** The channel is an HDLC channel or an LAPD message-oriented channel. The 6632 deformats the HDLC data -- 16-bit CRC-CCITT polynomial is used to calculate FCS, and ABORT, Flags and inserted zeros are recognized, no special processing for the header (address and control fields).
		10	**Non-HDLC signaling channel mode:** used in DMI or G.732 application to receive the bit-oriented signaling data without HDLC format. The received data are stored into data buffers in the way shown in Table 14. The 6632 detects the multiframe alignment and reports if any error is found.
		11	Reserved

Table 14. Receive Buffer Data Arrangement for Non-HDLC Bit-Oriented Signaling Channel

(Address)	7			(Contents)				0
i i+1	Next Buffer Address = i or j							
i+2 i+7	Remaining Descriptors							
(i+7)+1	X	1	X	X	X	B1	A1	A13
(i+7)+2	X	1	X	X	X	B2	A2	A14
(i+7)+3	X	1	X	X	X	B3	A3	A15
. .	.				.			
(i+7)+11	X	1	X	X	X	B11	A11	A23
(i+7)+12	X	1	X	X	X	B12	A12	A1
(i+7)+13	X	1	X	X	X	B13	A13	A1
(i+7)+14	X	1	X	X	X	B14	A14	A2
(i+7)+15	X	1	X	X	X	B15	A15	A3
(i+7)+16	X	1	X	X	X	B16	A16	A4
(i+7)+17	X	1	X	X	X	B17	A17	A5
. .	.				.			
(i+7)+23	X	1	X	X	X	B23	A23	A11
(i+7)+24	1	0	Ys	0	1	1	1	A12

a. T1 Mode

(Address)	7			(Contents)				0
i i+1	Next Buffer Address = i or j							
i+2 i+7	Remaining Descriptors							
(i+7)+1	D17	C17	B17	A17	D1	C1	B1	A1
(i+7)+2	D18	C18	B18	A18	D2	C2	B2	A2
(i+7)+3	D19	C19	B19	A19	D3	C3	B3	A3
. .	.				.			
(i+7)+11	D27	C27	B27	A27	D11	C11	B11	A11
(i+7)+12	D28	C28	B28	A28	D12	C12	B12	A12
(i+7)+13	D29	C29	B29	A29	D13	C13	B13	A13
(i+7)+14	C30	C30	B30	A30	D14	C14	B14	A14
(i+7)+15	D31	C31	B31	A31	D15	C15	B15	A15
(i+7)+16	1	1	Ys	1	0	0	0	0

b. CEPT PCM-30 Mode

- FILL/MASK Byte (Rate Definition)

The PT7A6632 FILL/MASK byte is used as a masking pattern on the HDLC-formatted (including FLAG, header, data, CRC, and ABORT code) or non-HDLC-formatted data in order to adapt subrates that are multiples of 8kb/s to the 64kb/s rate. The 8-bit sequence is applied to data on a bit by bit basis to remove time-fill (FILL/MASK bit = 0) bits. See an example in Figure 13 in Section “Receive Bit-Level Processor” and Table 9.

For bit-oriented signaling mode, the FILL/MASK should be set as 1111 1111, otherwise the PT7A6632 will not override any other FILL/MASK pattern.

- Flexible Hyperchannel Configuring Byte (Optional)

The byte follows the FILL/MASK byte if any. It is used to configure flexible hyperchannel. Bits 0 - 4 specify number of a channel to be grouped into or removed from a hyperchannel. Bits 6 and 7 is for hyperchannel enable and add/delete respectively. See Table 10 for details.

Data Length is used to specify flexible hyperchannel. When Data Length = 0, 1 or 2, only non-hyperchannel process. When Data Length > 2, there is hyperchannel process, while the Data Length indicates how many additional channels to be added to the hyperchannel. See Section “Flexible Hyperchannel” in Transmit Command Buffer.

Minimum Buffer Size

The size of receive data buffer must ensure normal buffer maintenance and buffer transition without losing data.

Table 15

	Receive Data Buffer	**Receive Command** Buffer
Min. Buffer Size	8 Bytes (Descriptors) + 6 Bytes (Data)	8 Bytes (Descriptors) + 2 Bytes (Command)

Device Operation

Device Initialization

The device is initialized by RESET signal. Upon reset, all the channels are set in the following states:
- the operation mode is HDLC, inversion, non-loop,
- FILL/MASK byte: 0000 0000,
- all channels are inactive,
- Flexible hyperchannels are disabled,
- no data transferred from the external memory or written to the external memory.

The PT7A6632 monitors the TMAX, RSYNC and RRED signals and correspondingly reset the Transmit channel counter and the Receive channel counter to ascertain the framing synchronization.

Channel Initialization

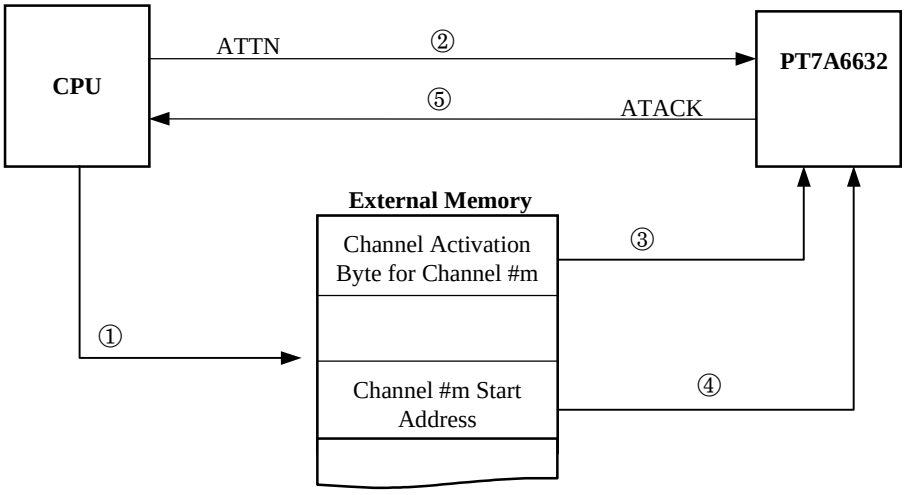
The channels are initialized for preparing data transmission and reception by CPU asserting the ATTN signal.

Before asserting the ATTN, the CPU first allocates memory in the external memory for a Command Buffer containing 8 bytes of descriptors including Next Buffer Starting Address, Data Length, Status, and 2 bytes of Mode and Fill/Mask. And a chain of linked data buffers are set up by the CPU following the command buffer, containing Next Buffer Start Address, Buffer Size, Data Length, Status and Data bytes. Then the CPU set up the Activation Memory containing channel No. to be activated and channel direction, and Channel Starting Address (pointers) in the external memory. Then the CPU sends out the ATTN signal.

The PT7A6632 receives the ATTN, starting to access the Activation Memory (asserting SYSACC) for the Channel Number and the channel start address, which will be stored internally in the PT7A6632. PT7A6632 asserts the ATACK after completion the access, CPU negates the ATTN in response to the ATACK, and PT7A6632 negates the ATACK in response to negation of ATTN. The channel initialization is completed. The process is illustrated in Figure 28.

This process can be repeated for each channel to be initialized. The PT7A6632 must make three activation memory accesses to complete the channel ATTN processing. The worst case of time delay from ATTN assertion to ATACK assertion is three T1/CEPT PCM-30 channel periods. The earliest is 1.5 channel period.

Figure 28. Channel Initialization



① CPU prepares data buffer and writes to activation byte for a channel.
② CPU asserts ATTN.
③ PT7A6632 responds to ATTN, reads channel number, Rx/Tx, Active/Inactive in channel activation byte.
④ PT7A6632 find out the corresponding channel start address and read the start address of the first buffer allocated for the channel.
⑤ PT7A6632 informs task completion by asserting ATACK.

Data Transmission and Reception Operation

In transmission, the PT7A6632 reads the first command buffer according to the channel start address, judges status of buffer, fetches the MODE and FILL/MASK information for the channel, then it reads the Next Buffer Start Address in the current buffer. It goes to the next buffer to get Data Length/Buffer Size, and data bytes to send the data out in according to mode specified and update the status if necessary. The PT7A6632 processes channel by channel in this way. See figure 29 for example.

In receiving, the PT7A6632 reads the command buffer of a channel to locates the CPU-allocated buffers for received data storage, and stores the processed data into the data buffer and write the Data Length. It updates the Status of the completed buffer if necessary. See figure 30 for example.

Figure 29. Typical Linked Buffer Transmit Sequence

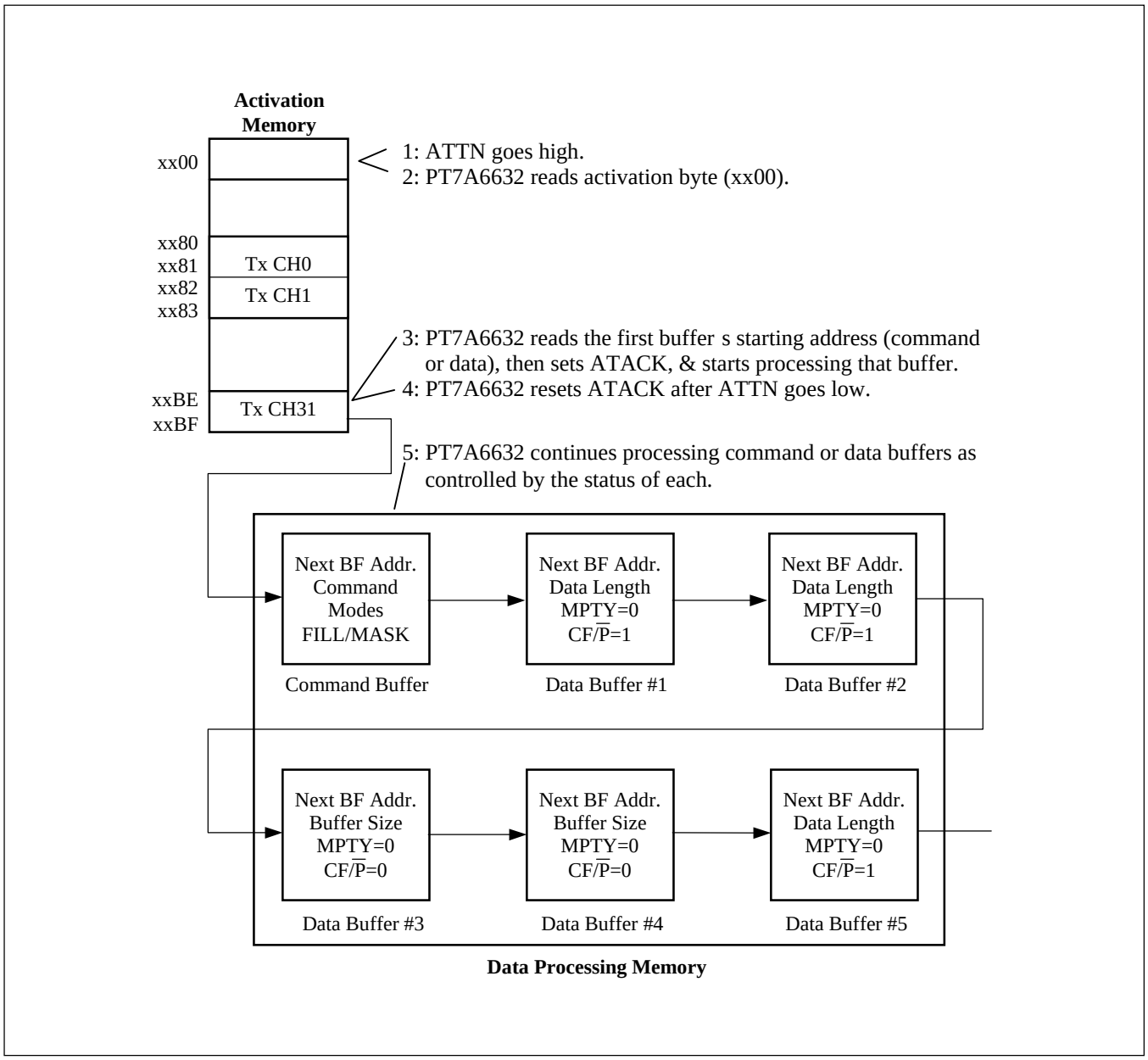
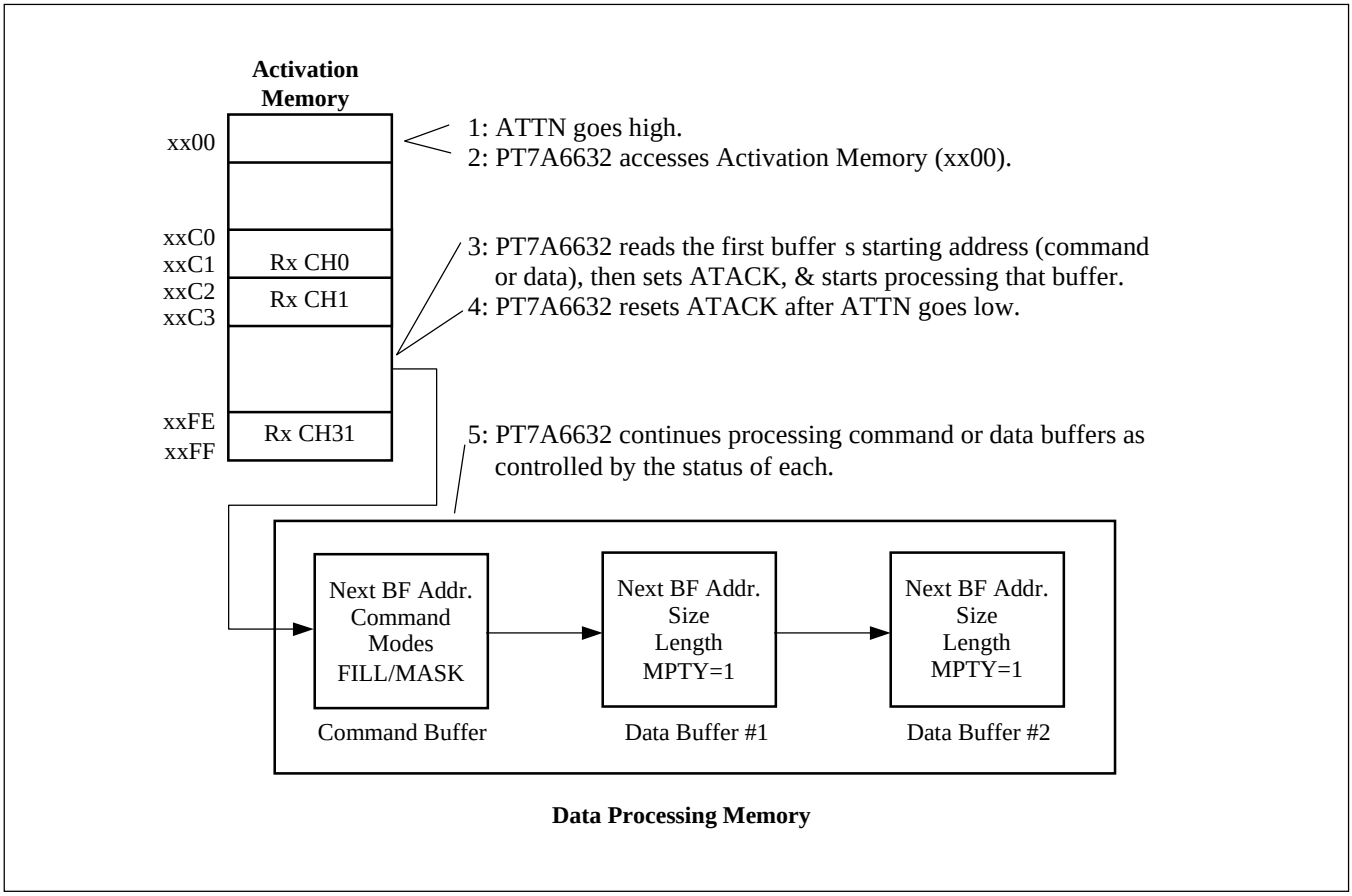


Figure 30. Typical Linked Buffer Receive Activity



Channel Period for Memory Access

The PT7A6632 accesses the external memory for buffer management and data processing.

Normally, the T1/CEPT PCM-30 data flow requires that a byte of data should be supplied for transmission and a byte of data be taken from the receiving source within a single channel period. So the PT7A6632 divides a channel period into 2 halves, the first half is Tx memory access period and the second is Rx memory access period, 4 TCLK periods for each. In the first half of channel period, the PT7A6632 reads command information, descriptors information and transmission data from the external memory for Tx channels, and in second half of channel period, it reads command information, descriptors information from external memory and write the received data to the memory for Rx channels.

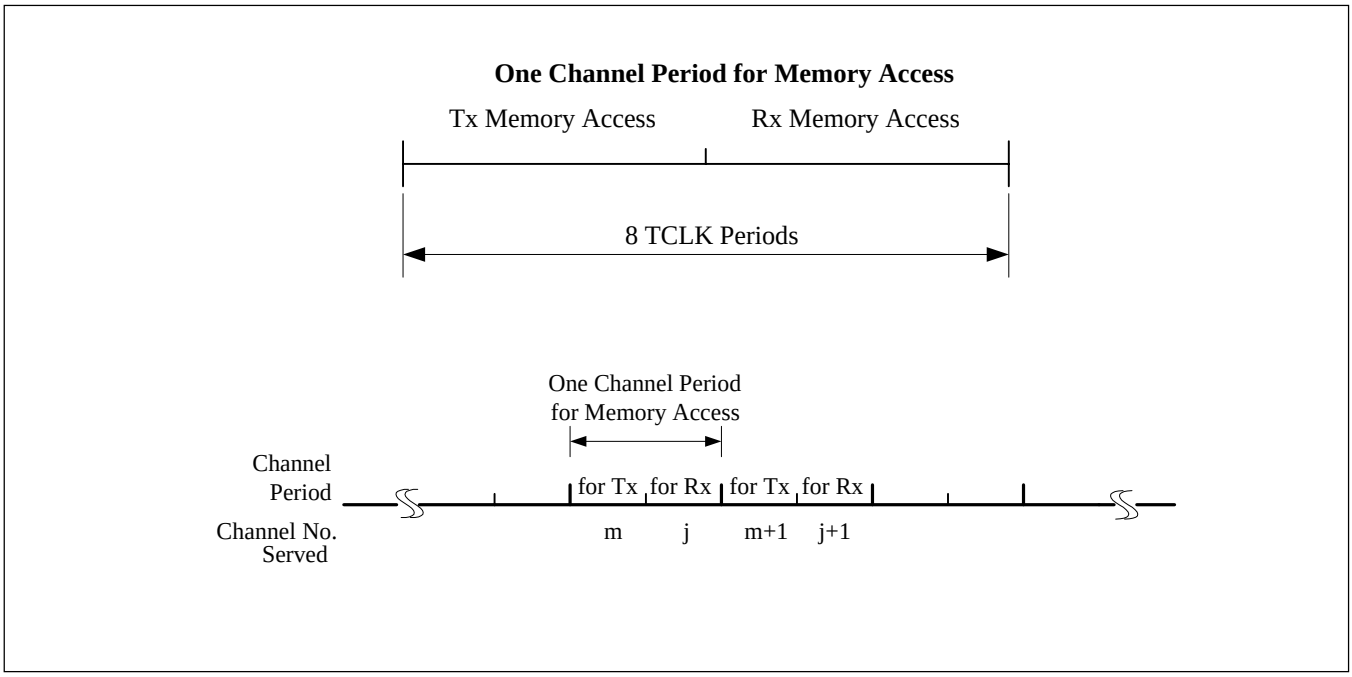
Typically, the PT7A6632 fetches a data byte from the memory during Tx channel period m for transmission of the data byte over channel m in the next appropriate Tx channel m, and the PT7A6632 takes a data byte from the receiving circuit of channel j and will store the data into the external memory in the next appropriate Rx channel period j. Then the PT7A6632 moves to process the next Tx channel (m+1) and Rx channel (j+1). See Figure 31.

In each Tx or Rx memory access period, the PT7A6632 can access external memory for data byte for once, or twice if the descriptor reading is necessary, even more, three times if an ATTN signal asserted by the CPU.

At the start of each half-channel period, the PT7A6632 first outputs the channel number CH0 - CH4, and the channel direction Rx/Tx of the current channel. After around half TCLK period, the PT7A6632 asserts DMND to inform the external memory that it will access it after 1 TCLK period from the rising edge of DMND. Then the PT7A6632 asserts the $\overline{AS}$ strobe, whose falling edge will make the address valid on the address bus. The PT7A6632 sends out $\overline{READ}$ or $\overline{WRITE}$ strobe to read data from the memory or write data into the memory during low of the $\overline{READ}$ or $\overline{WRITE}$. After finish memory access (1, 2 or 3 times access as applicable) and sets the DMND low to inform end of memory access of this half-channel period. During the process, if the ATTN is asserted and the PT7A6632 accesses the Activation Memory, it will assert SYSACC and negate it after Activation Memory access completed.

Address setup time, address hold time, data setup time and data hold time are specified such that a wide variety of off-the-shelf RAM devices may be used. The $\overline{READ}$ output from the PT7A6632 may be used as an Output Enable ($\overline{OE}$) input to the RAM devices. Since the PT7A6632 uses its SYSCLK input to generate various strobes for memory access, the access time requirements are automatically scaled depending on the T1/CEPT PCM-30 application.

Figure 31. Channel Period



Memory Address

Memory Address Extension

The output of CH0 - CH4 and Rx/$\overline{Tx}$ of the PT7A6632 can be used as upper address bits to extend the 16-bit addresses to 22-bit addresses. See an example in Figure 32. Or these six bits can be mapped by an external lookup table to another set of n bits (where n is specified by the CPU). Since the channel number and Rx/$\overline{Tx}$ are output by the PT7A6632 well in advance of the 16-bit address, address translation time is not a concern.

Activation Memory Address

The Activation Memory has 256 byte locations as shown in Figure 33. The addresses can be decided by the CPU by setting $\overline{UAEN}$ and SYSACC output of the PT7A6632. When $\overline{UAEN}$ = 0, the address output lines A8-A15 of the PT7A6632 is set low, so the address of the Activation Memory is in 00xx(H). When $\overline{UAEN}$ = 1, PT7A6632 sets its outputs of A8-A15 in high impedance and the CPU can drive the addresses A8-A15.

Figure 32. Address Extension

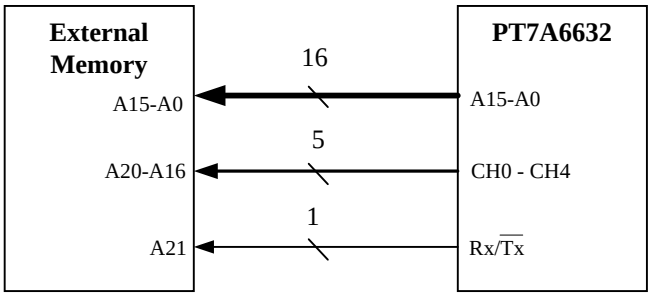
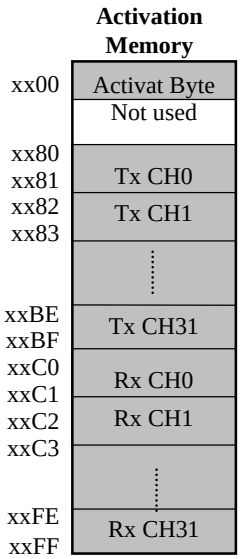


Figure 33. Activation Memory Address



(Addresses xx80, xx81 and xxB2 through xxBF are not used in T1 modes.)

(Addresses xxC0, xxC1 and xxF2 through xxFF are not used in T1 mode.)

Upper address lines xx (A8-A15):
When $\overline{UAEN}$ = 0, xx = 00.
When $\overline{UAEN}$ = 1, A8 A15 output of PT7A6632 is set in high impedance, xx are decided by the CPU.

Memory Address Restrictions

Activation Memory Address -- The PT7A6632 judges the channel start address for its invalidity immediately after it reads the Activation Memory for the address in response to the ATTN assertion. If the 16-bit address is found invalid, the channel will be deactivated. The channel start address is thought invalid by the PT7A6632 when it is all zero or in form of FFFx.

Data/Command Buffer Address -- The PT7A6632 checks next buffer address in each buffer. If found a next buffer address is invalid, the PT7A6632 will set the channel inactive and set the IVBA bit of the current buffer. The channel can be reactivated only when CPU asserts the ATTN signal.

The 16-bit next buffer address is thought invalid by the PT7A6632 if it is all zero or in form of FFFx, namely, the address is valid when it is within 0001 to FFEF.

The PT7A6632 locates a descriptor byte or a data byte by adding offset to a next buffer address read from last buffer. The maximum address in a buffer is the address of the last byte. As for 16-bit address lines, the addresses are restricted in the range of 2^{16} - 1 (65,535), the last byte address in a buffer should meet the following condition:

Last byte address in a buffer = buffer start address + 7 (decimal) of descriptor bytes + 12-bit data length or buffer size <= 65,535.

If the last byte address exceeds the restriction, the PT7A6632 will access memory locations not intended for the channel. All the external memory addresses should be within one 64k byte bank.

Interrupt Indication

At the rising edge of $\overline{\text{INTR}}$, channel No. and status contents can be shifted into the external FIFO. The $\overline{\text{INTR}}$ is asserted by the PT7A6632 when PT7A6632 updates the status of a buffer. After update, the PT7A6632 negates the $\overline{\text{INTR}}$ and at its rising edge the channel No. and status are guaranteed to be valid on the bus so that external FIFO can take the information, and the actual address of the status byte is also be placed on the bus. The PT7A6632 removes the interruption channel No. and buffer status without waiting for acknowledge from the CPU. See Figure 34.

The CPU can take the actual status byte address and it can relocate the completed buffers within the 64k byte bank and also cross-check against its own list of linked buffer addresses. If all the buffer start addresses are divisible exactly by 8, they can be derived from the STATUS byte addresses by setting the three LSB addresses to zero.

Figure 34. Interrupt Indication

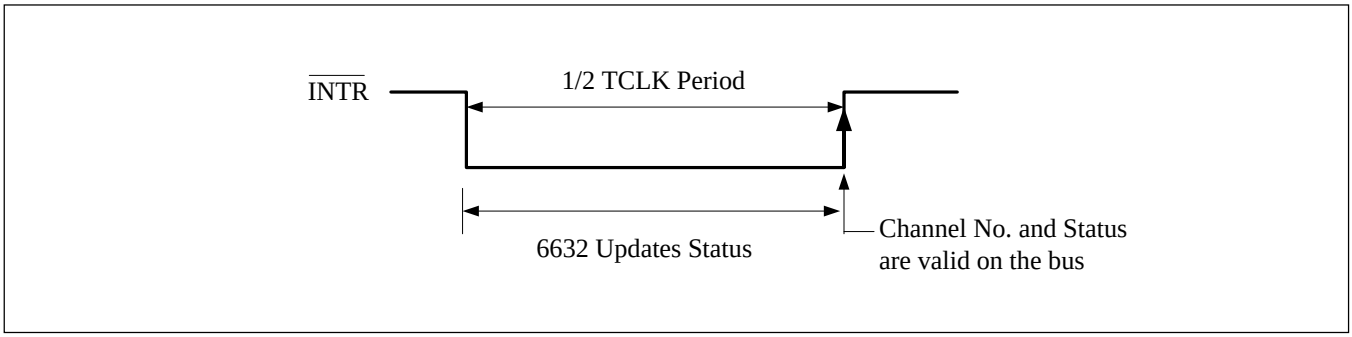
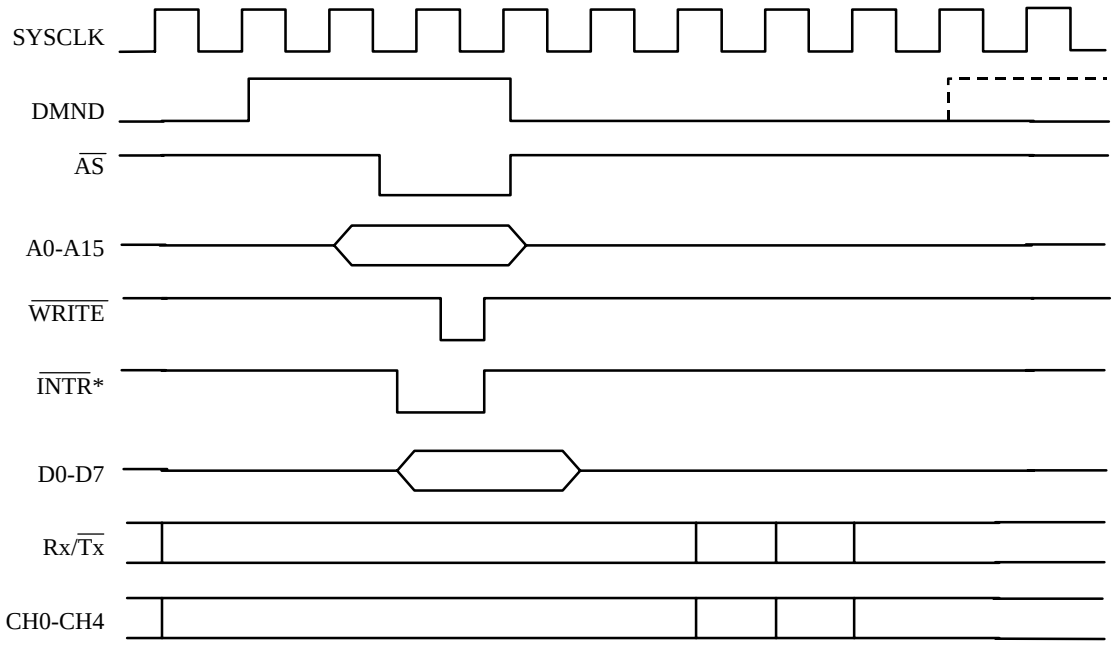
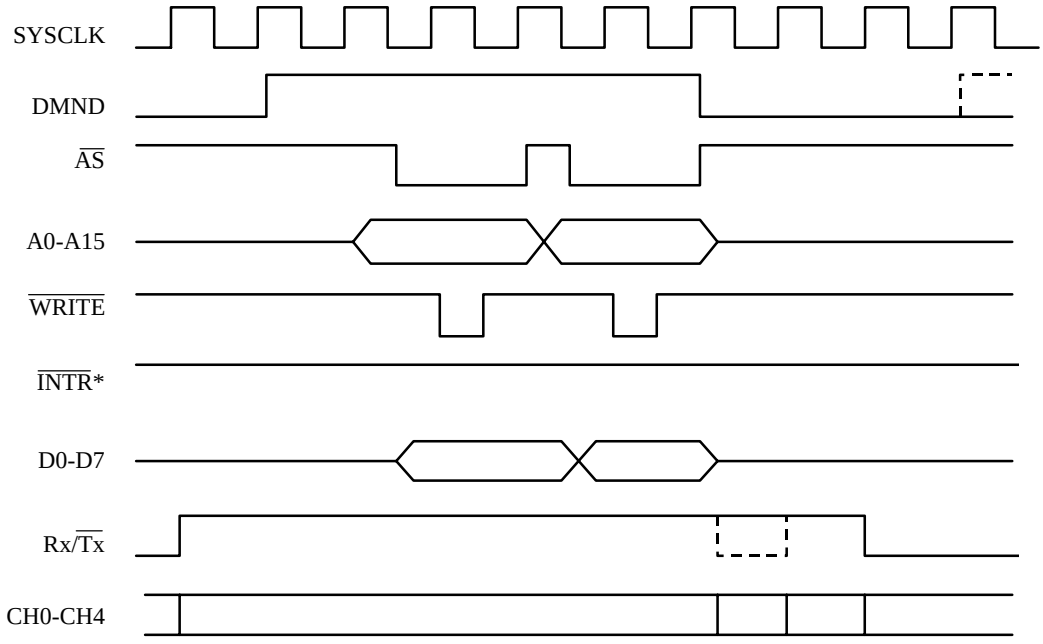


Figure 35. PT7A6632 External Memory Example Interface Waveforms - Single Write Memory Access



* Activated by status write only.

Figure 36. PT7A6632 External Memory Example Interface Waveforms - Double Write Memory Access



* Activated by status write only.

Figure 37. PT7A6632 External Memory Example Interface Waveforms - Single Read Memory Access

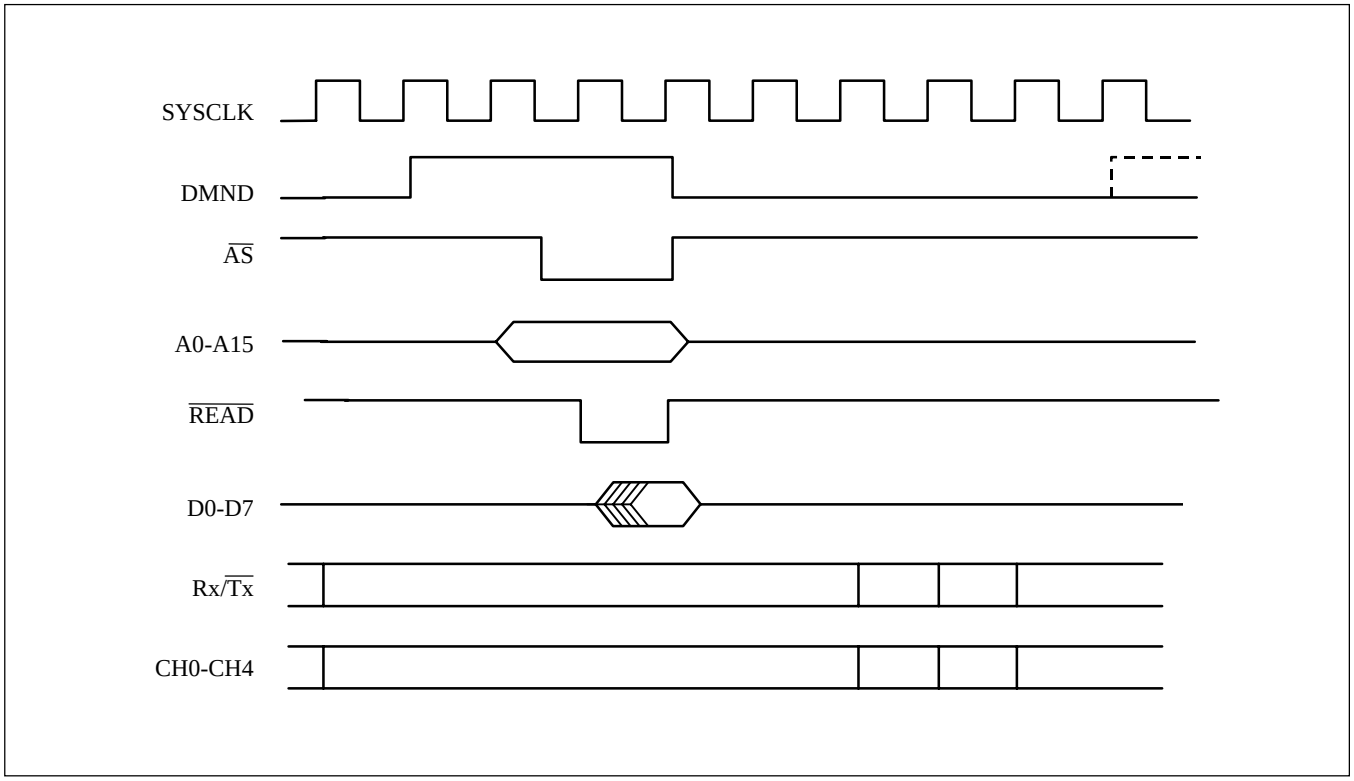
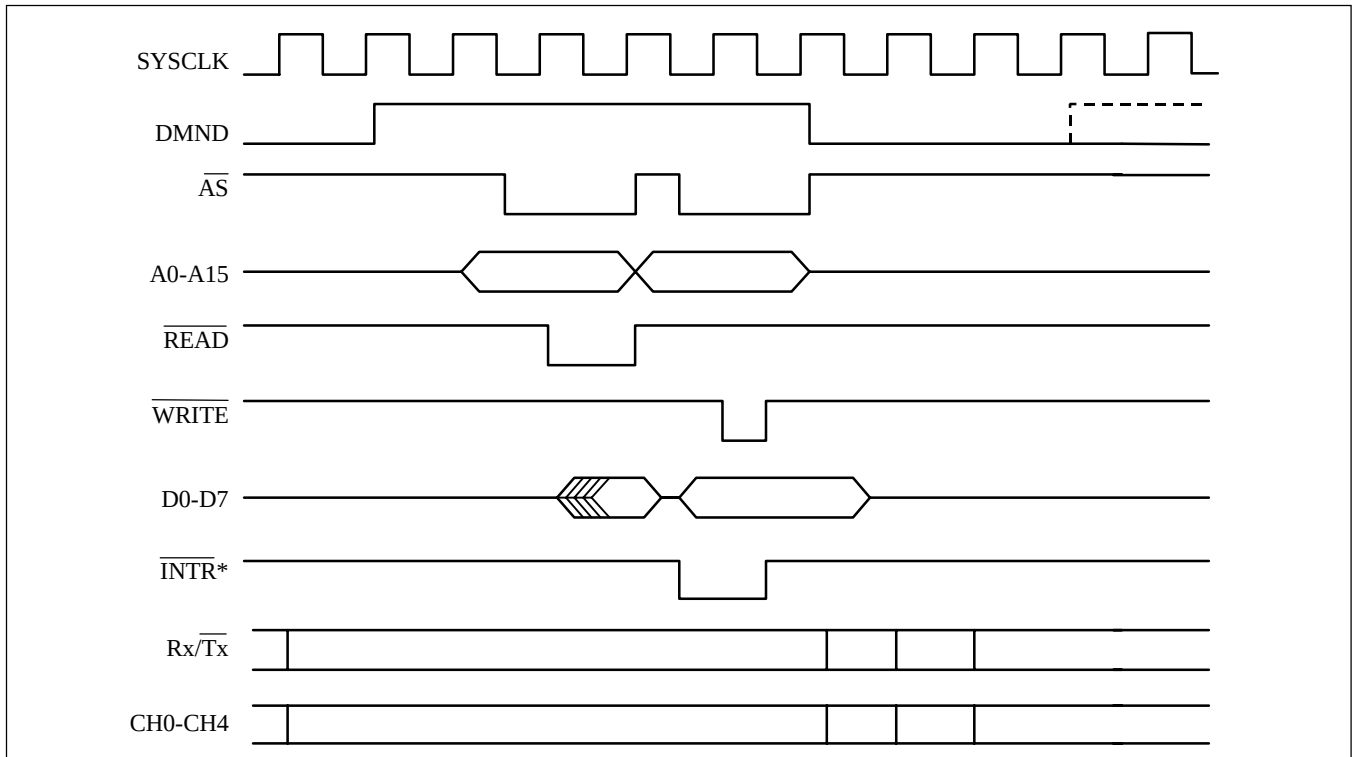


Figure 38. PT7A6632 External Memory Example Interface Waveforms - Read Write Double Memory Access



* Activated by status write only.

Figure 39. PT7A6632 External Memory Example Interface Waveforms - Write Read Double Memory Access

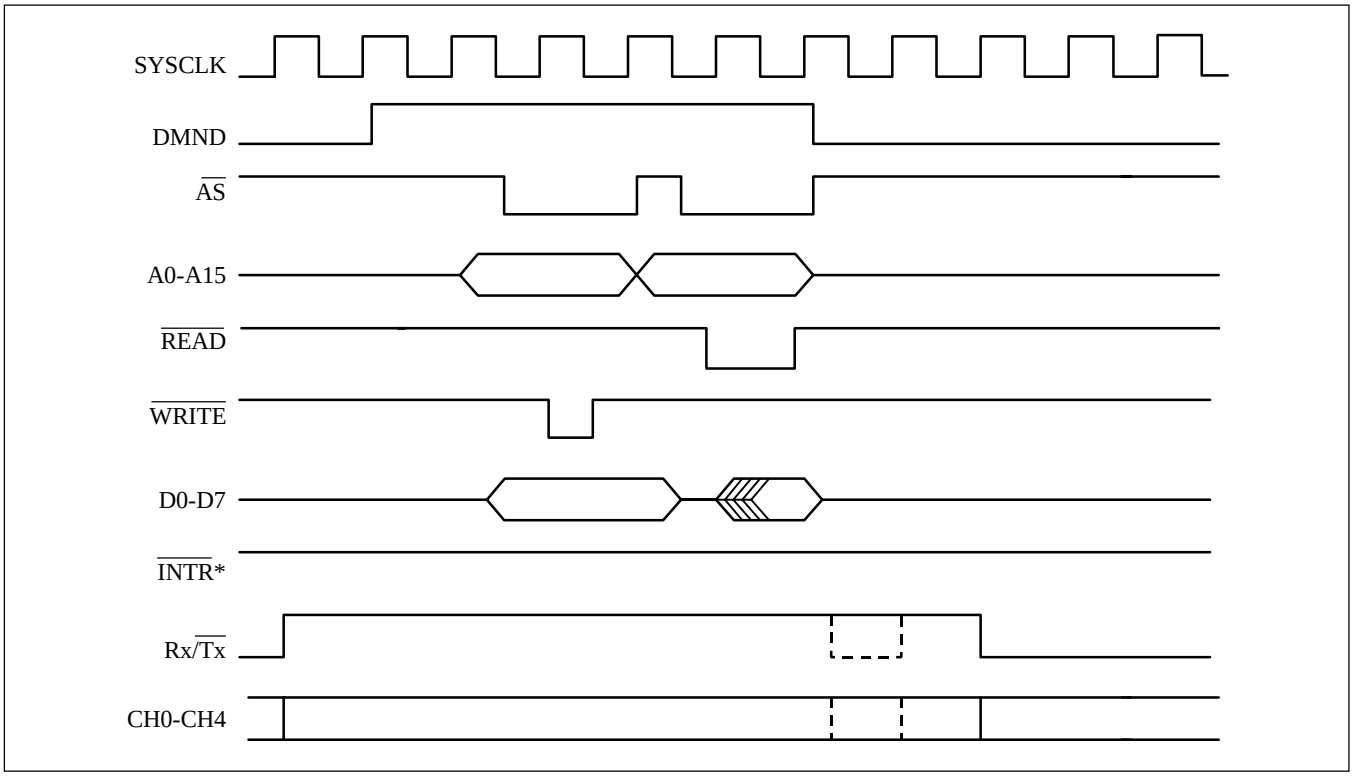


Figure 40. PT7A6632 External Memory Example Interface Waveforms - Single Activation Read Memory Access

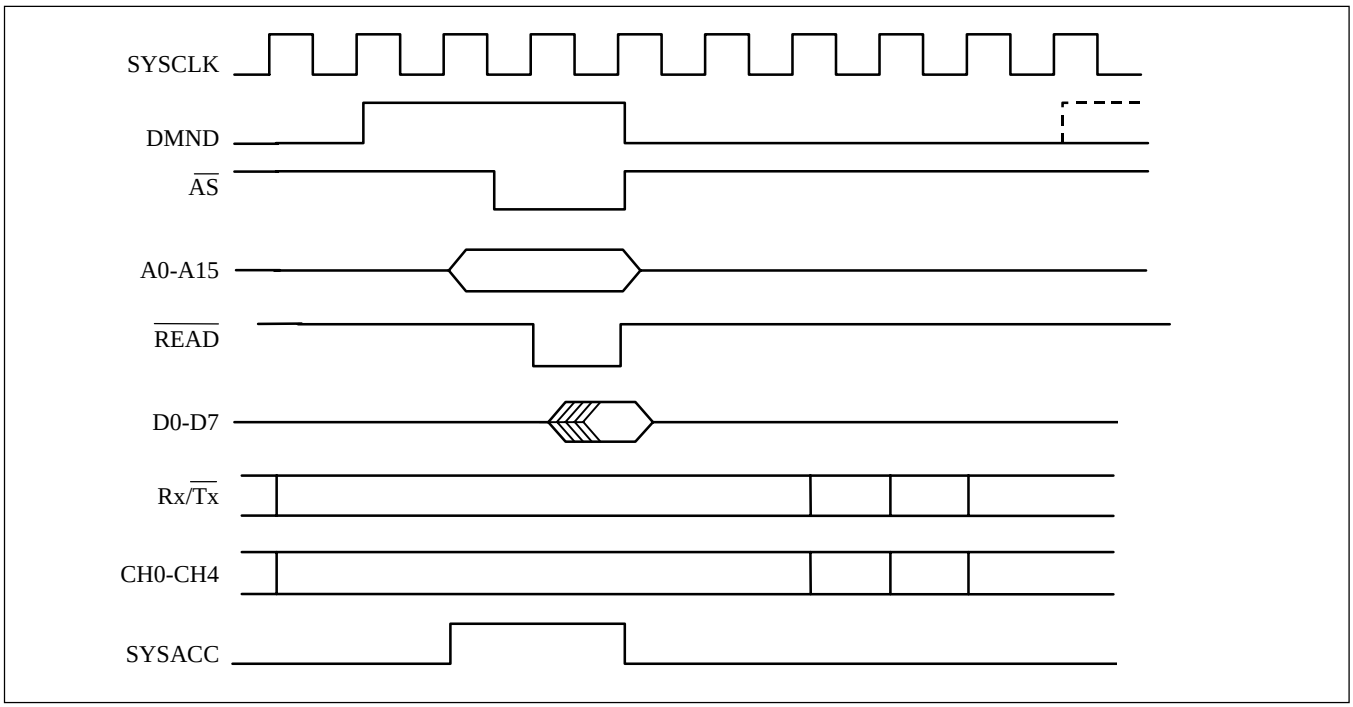


Figure 41. PT7A6632 External Memory Example Interface Waveforms - Single Write Memory Access Plus a Single Activation Read Access

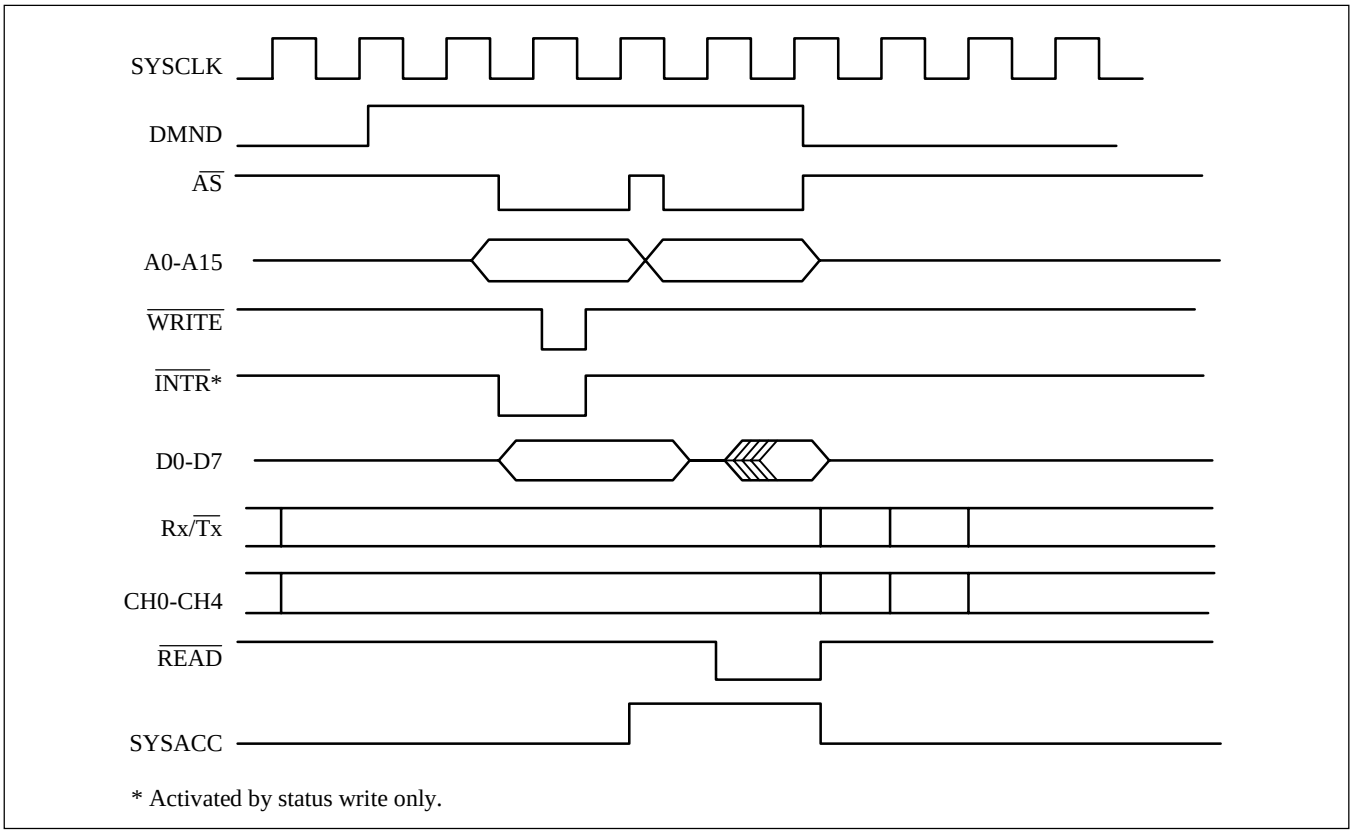


Figure 42. PT7A6632 External Memory Example Interface Waveforms - Single Write Memory Access Plus a Double Activation Read Access

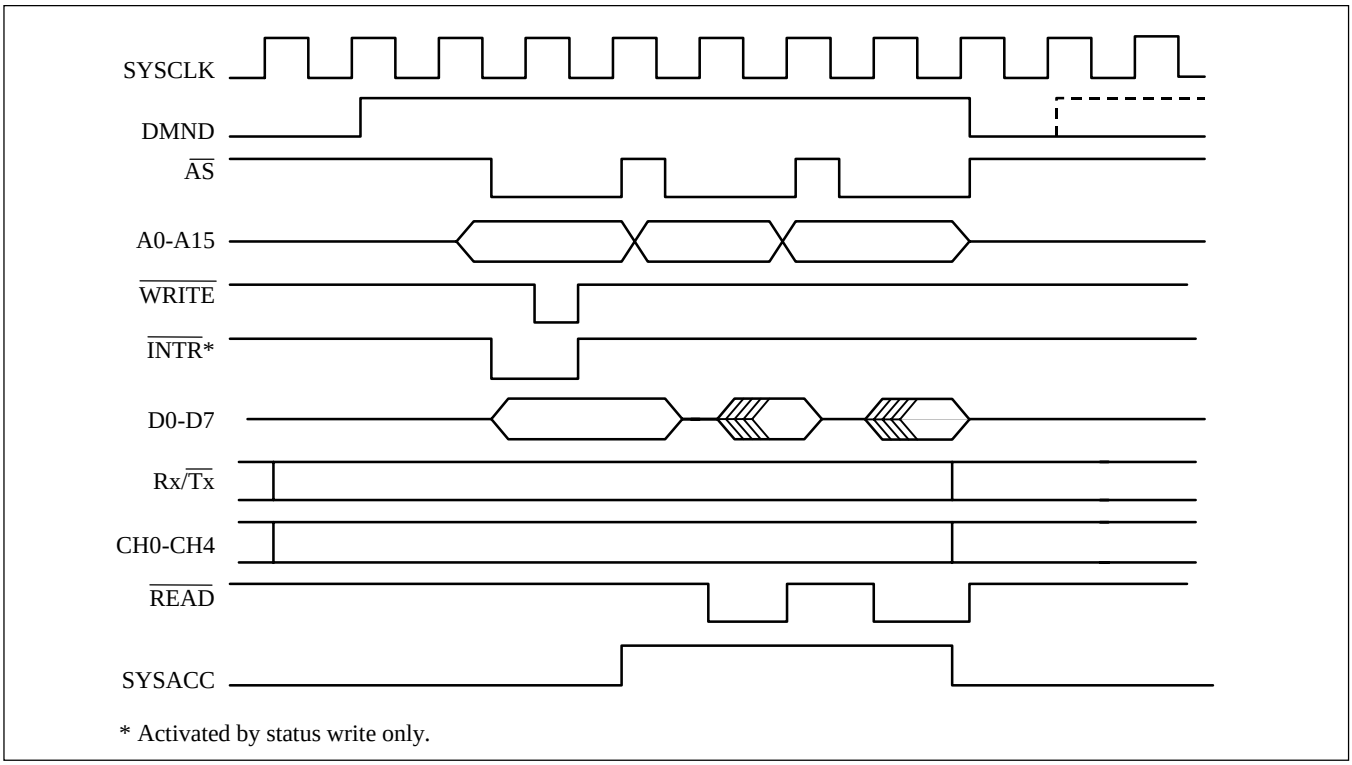
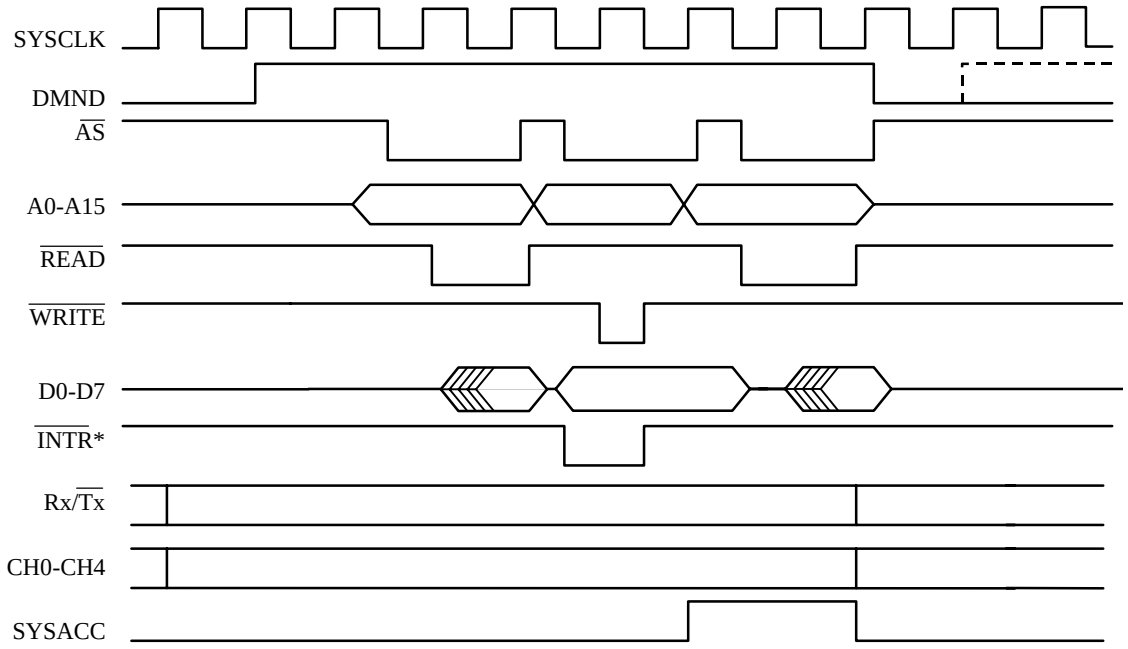


Figure 43. PT7A6632 External Memory Example Interface Waveforms - Write/Read Double Memory Access Plus a Single Activation Read Access



* Activated by status write only.

Detailed Specifications

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V_{CC} Only)	-0.3 to 7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3 to 7.0V
DC Input Voltage	-0.3 to 7.0V
DC Output Current	120mA
Power Dissipation	2W

Note:
Operation at levels greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Operation Condition tables is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Table 16. Recommended Operating Conditions

Sym	Description	Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage	Over Recommended Operating Conditions	4.5	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C

Note:
Typical figures are at 25°C and are for design aid only; not production tested.

DC Electrical, Power Supply and Capacitance Characteristics

Table 17. DC Electrical, Power Supply and Capacitance Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	V_{CC} = 5V, all clock sources are connected to corresponding pins		4	12	mA
V_{IH}	Input HIGH Voltage	500mV noise margin	2.4			V
V_{IL}	Input LOW Voltage	500mV noise margin			0.8	V
V_{OL}	Output LOW Voltage	I_{OL} = 10mA*		0.5	1	V
V_{OH}	Output HIGH Voltage (CMOS)	I_{OH} = 10mA*	3.5	4.5		V
I_{OL}	Output LOW Current	V_{OL} = 0.5V	4	12		mA
I_{OH}	Output HIGH Current	V_{OH} = 4.5V	4	10		mA
C_{IN}	Input Pin Capacitance				10	pF
C_{OUT}	Output Pin Capacitance				10	pF

Note:
Typical figures are at 25°C and are for design aid only; not production tested.
* I_{OL} and I_{OH} are obsolute values.

AC Characteristics

(Note: All output AC timing measurements are referenced to the 0.4V for low level and 2.4V for high level, and all input AC timing measurements are referenced to the 0.8V for low level and 2.0V for high level.)

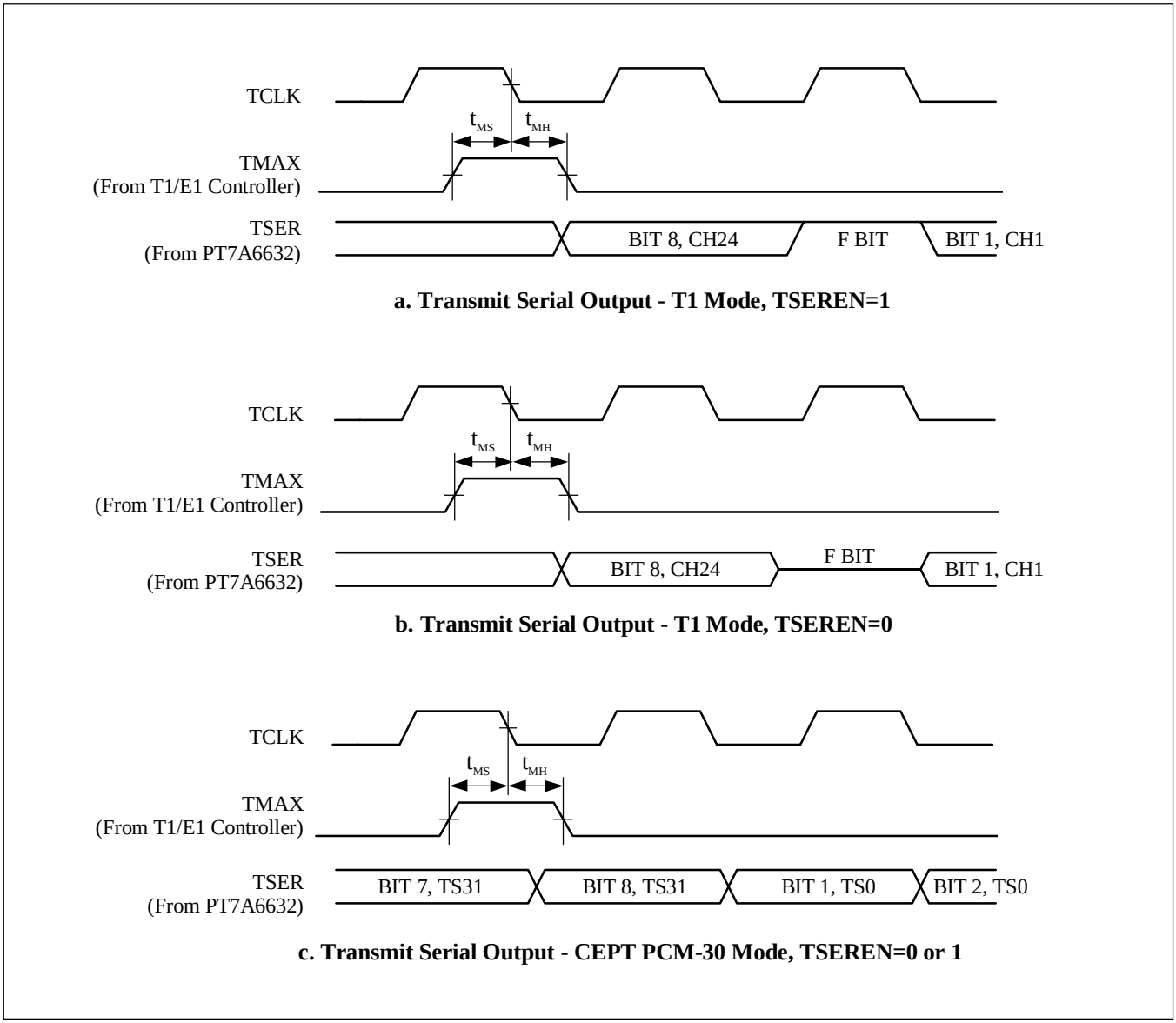
Serial Interface

- Transmit Frame Synchronization Timing

Table 18. Transmit Frame Synchronization Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{MS}	TMAX Setup Time		50			ns
t_{MH}	TMAX Hold Time		50			ns

Figure 44. Diagram of Transmit Frame Synchronization Timing (SIS = 1)

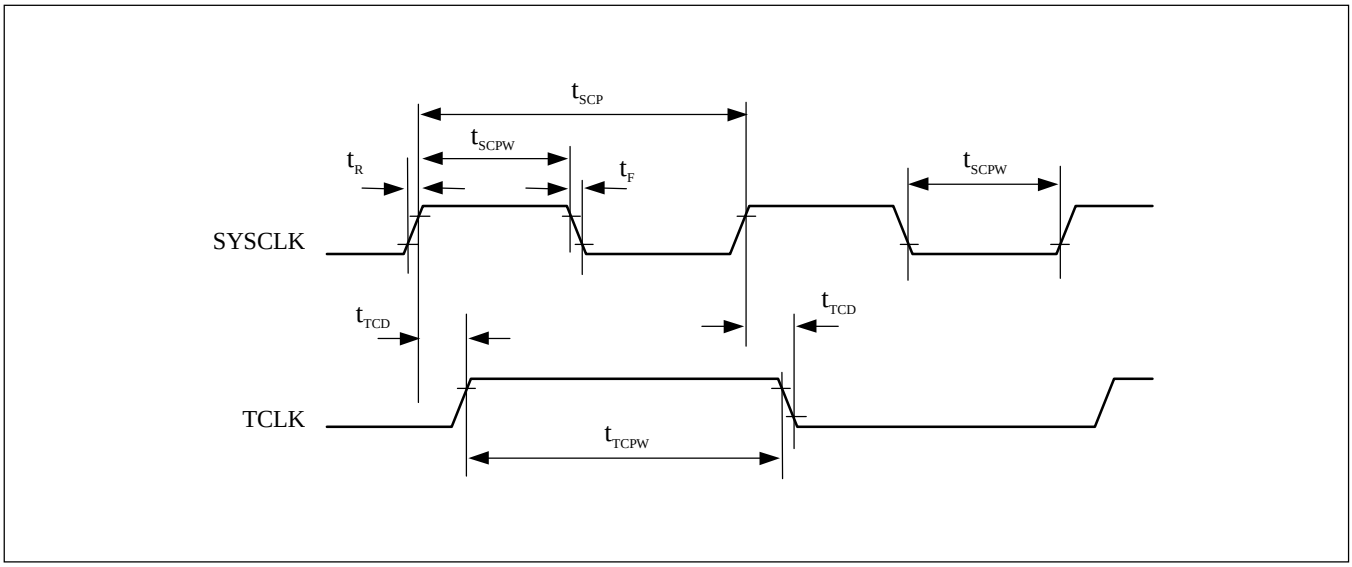


- Clock Timing

Table 19. Clock Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{TCD}	TCLK Delay		0		50	ns
t_{SCPW}	SYSCLK Pulse Width		110	122		ns
t_{TCPW}	TCLK Pulse Width		200	244		ns
t_{SCP}	SYSCLK Period		240	244	1000	ns
t_R/t_F	Rise Time/Fall Time (SYSCLK)				5	ns

Figure 45. Clock Timing



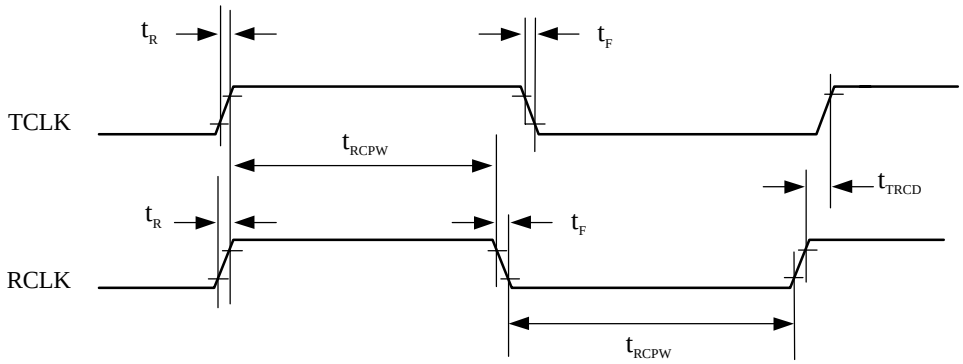
• TCLK - RCLK Timing

Table 20. TCLK - RCLK Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RCPW}	RCLK Pulse Width		200	244		ns
t_{TRCD}	TCLK, RCLK Difference				*	ns
t_R/t_F	Rise Time/Fall Time (RCLK, TCLK)				10	ns

* RCLK is to be centered around TCLK. The summation of RCLK and TCLK periodic differences over any duration of time must never exceed 14 TCLK periods.

Figure 46. TCLK - RCLK Timing

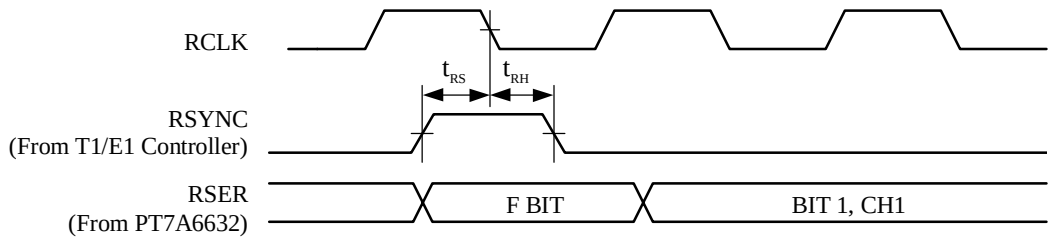


• PT7A6632 Receive Frame Synchronization Timing

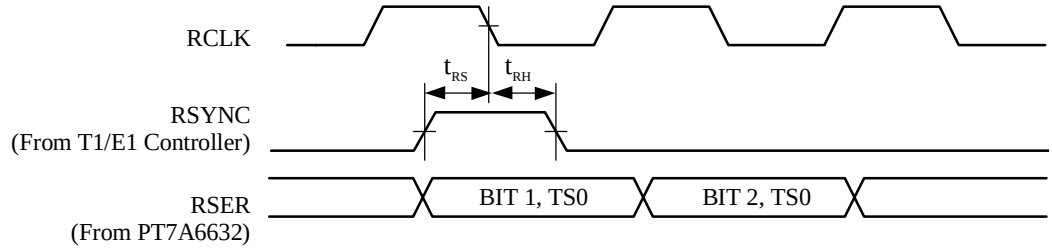
Table 29. Receive Frame Synchronization Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RS}	RSYNC Setup Time		50			ns
t_{RH}	RSYNC Hold Time		50			ns

Figure 47. Diagram of Receive Frame Synchronization Timing (SIS=1)



a. Receive Serial Output - T1 Mode



b. Receive Serial Output - CEPT PCM-30 Mode

External Memory Interface

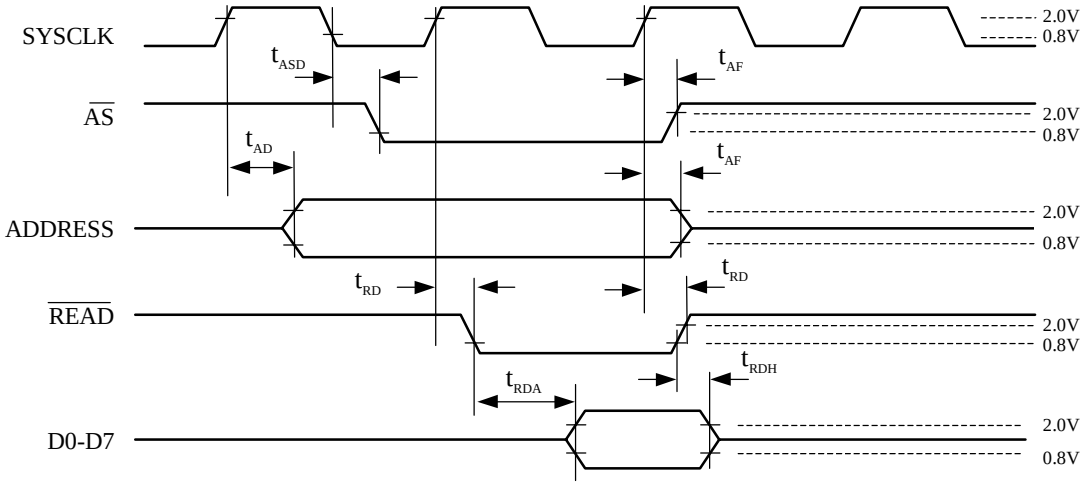
- Read Cycle Timing

Table 22. Read Cycle Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{ASD}	Address Strobe Delay		10		75	ns
t_{AD}	Address Delay		10		78	ns
t_{AF}	Address Float Delay		10		75	ns
t_{RD}	Read Enable Delay		10		78	ns
t_{RDA}	Read Data Access Time				*	ns
t_{RDH}	Read Data Hold Time		0		**	ns

* Read data access time for shared memory = t_{SCP} -125ns.
** Data drive to data bus float = t_{SCPW} - 65ns.

Figure 48. Read Cycle Timing



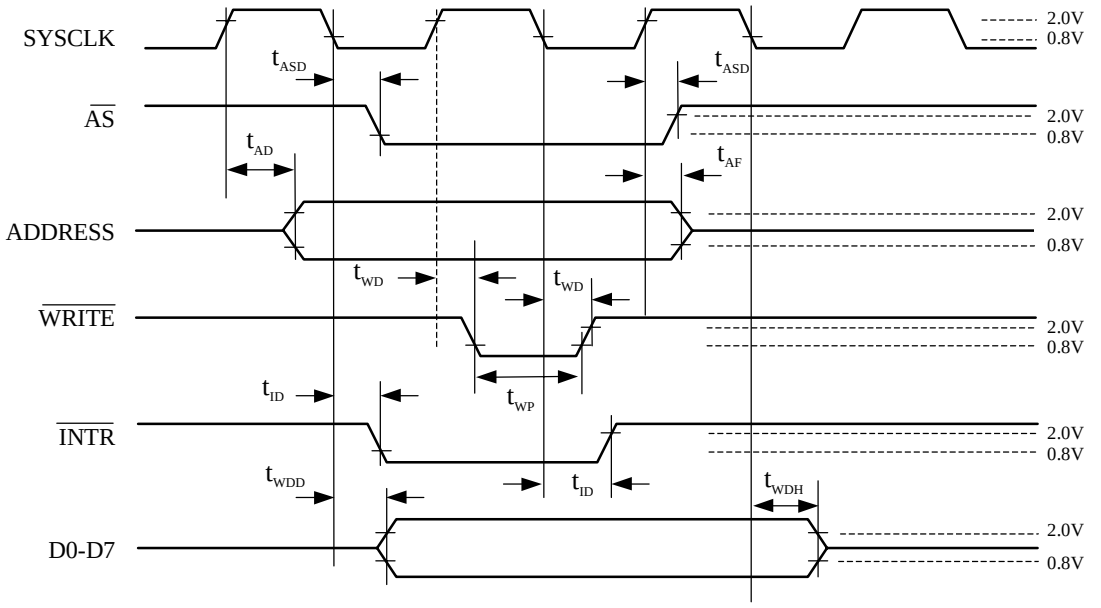
• Write Cycle Timing

Table 23. Write Cycle Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{ASD}	Address Strobe Delay		10		78	ns
t_{AD}	Address Delay		10		100	ns
t_{AF}	Address Float Delay		10		90	ns
t_{WD}	Write Delay		10		75	ns
t_{WP}	Write Pulse Width		80	117		ns
t_{ID}	Interrupt Delay		10			ns
t_{WDD}	Write Data Delay		10		120	ns
t_{WDH}	Write Data Hold Time*		10		90	ns

* Data drive to data bus float time

Figure 49. Write Cycle Timing

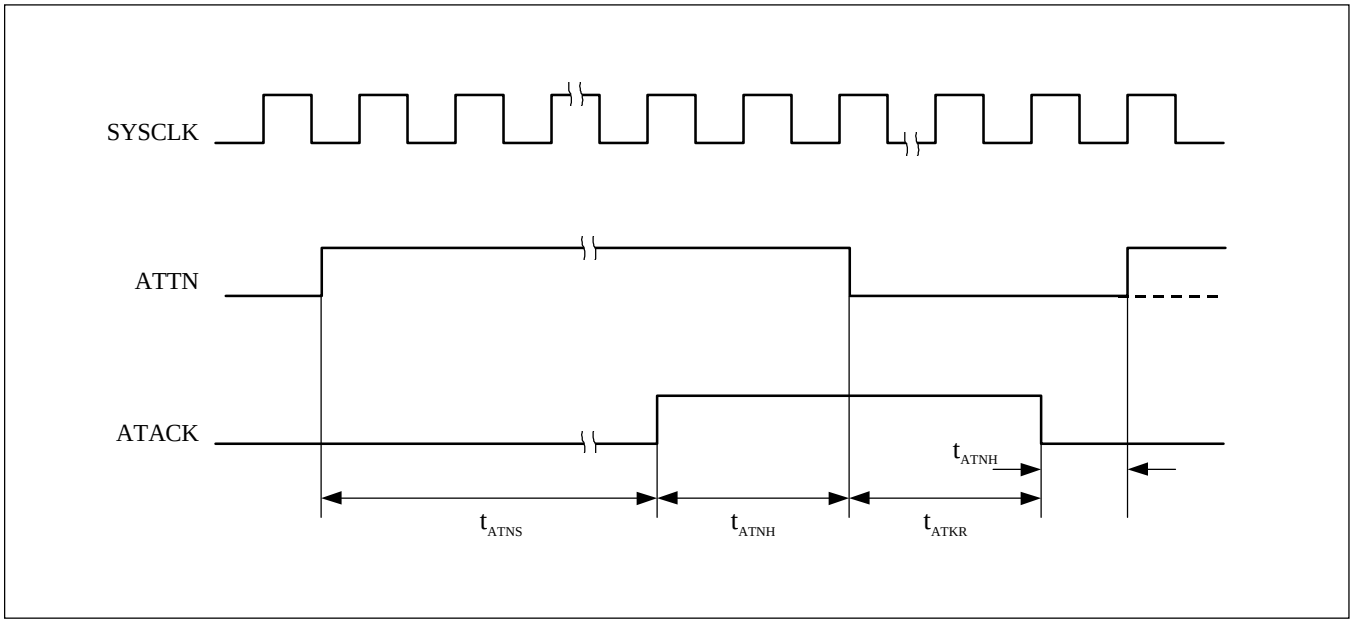


Channel Activation/Deactivation

Table 24. Channel Activation/Deactivation Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{ATNS}	ATTN to ATACK Response Time		20		48	SYSCLKs
t_{ATNH}	ATTN Hold Time		0			ns
t_{ATKR}	ATACK Reset Delay		2		4	SYSCLKs

Figure 50. Channel Activation/DeactivationTiming



Input Characteristics

Table 25. Input Characteristics

Signal Name	Reference Signal	Effective Edge	Setup (Min.)	Hold (Min.)	Units
ATTN	SYSCLK	Rising	50	50	ns
RESET	TCLK	Rising	60	60	ns
D0-D7	SYSCLK	Rising	50	0	ns
TMAX (SIS = 1)	TCLK	Falling	50	50	ns
TMAX (SIS = 0)	TCLK	Rising	50	50	ns
RSER (SIS = 1)	RCLK	Falling	50	50	ns
RSER (SIS = 0)	RCLK	Rising	50	50	ns
RRED (SIS = 1)	RCLK	Falling	50	50	ns
RRED (SIS = 0)	RCLK	Rising	50	50	ns
RSYNC (SIS =1)	RCLK	Falling	50	50	ns
RSYNC (SIS = 0)	RCLK	Rising	50	50	ns

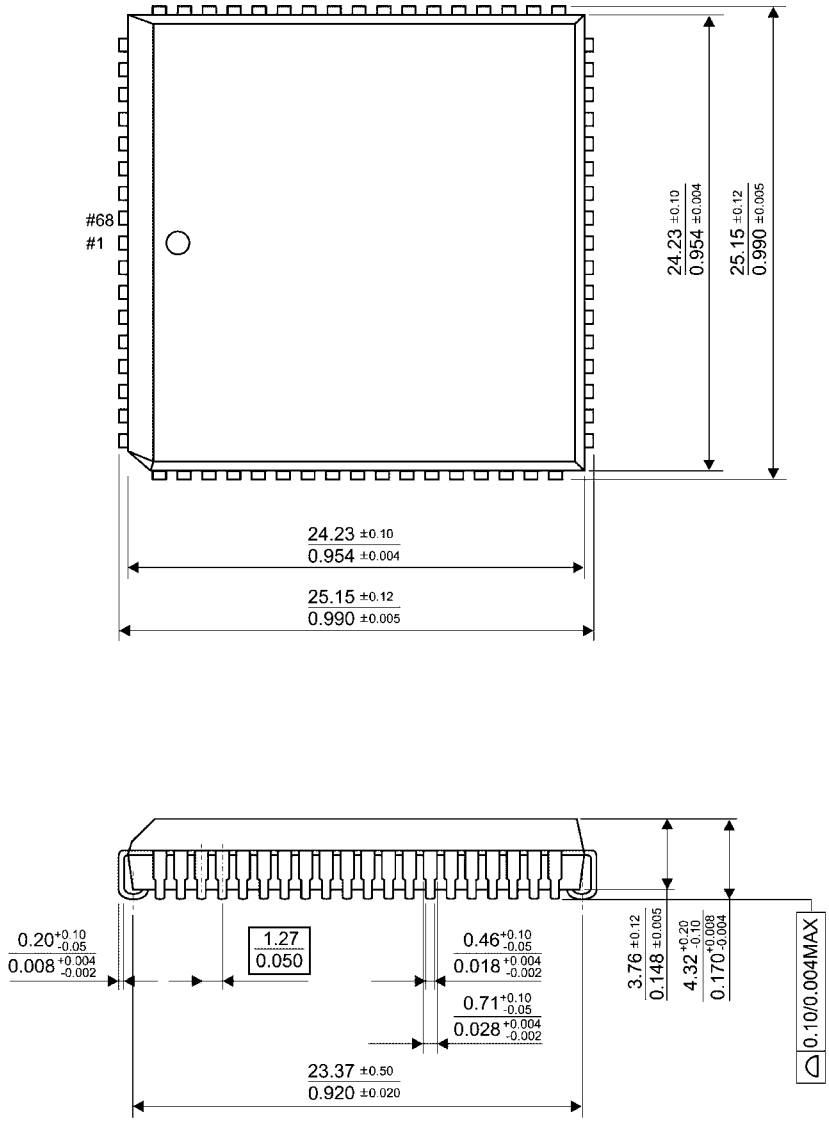
Output Characteristics

Table 26. Output Characteristics

Signal Name	Reference Signal	Effective Edge	Delay (Max.)	Hold (Min.)	Units
DMND	SYSCLK	Rising	90	10	ns
$\overline{AS}$	SYSCLK	Rising/Falling	78	10	ns
A0-A15	SYSCLK	Rising	100	10	ns
SYSACC	SYSCLK	Rising	70	10	ns
$\overline{READ}$	SYSCLK	Rising	78	10	ns
$\overline{WRITE}$	SYSCLK	Rising/Falling	120	10	ns
D0-D7	SYSCLK	Falling	120	10	ns
$\overline{INTR}$	SYSCLK	Falling	120	10	ns
CH0-CH4	SYSCLK	Rising	70	10	ns
Rx/$\overline{Tx}$	SYSCLK	Rising	70	10	ns
ATACK	SYSCLK	Rising	75	10	ns
TSER	TCLK	Falling	65	10	ns

Mechanical Specifications

Figure 51. 68-Pin PLCC



Dimensions in Millimeters/inches

Ordering Information

Table 27. Ordering Information

Part Number	Package
PT7A6632J	68-Pin PLCC

Notes

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