PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83026I-01

LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

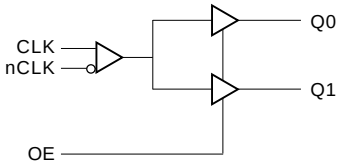
GENERAL DESCRIPTION

The ICS83026I-01 is a low skew, 1-to-2 Differential-to-LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The differential input can accept most differential signal types (LVPECL, LVDS, LVHSTL, HCSL and SSTL) and translate to two single-ended LVCMOS outputs. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

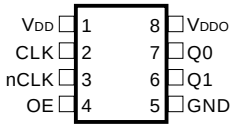
FEATURES

- 2 LVCMOS / LVTTL outputs
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 350MHz (typical)
- Output skew: 10ps (typical)
- Part-to-part skew: 1ns (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V core, 3.3V, 2.5V or 1.8V output operating supply
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS83026I-01
8-Lead SOIC
3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Positive supply pin.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	$V_{DD}/2$	Inverting differential clock input. $V_{DD}/2$ default when left floating.
4	OE	Input	Pullup	Output enable. Selects pin to tri-state outputs. LVCMOS / LVTTL interface levels.
5	GND	Power		Power supply ground.
6	Q1	Output		Clock output. LVCMOS / LVTTL interface levels.
7	Q0	Output		Clock output. LVCMOS / LVTTL interface levels.
8	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V			17	pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V			16	pF
		V_{DD} = 3.465V, V_{DDO} = 1.95V			15	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance	V_{DD}, V_{DDO} = 3.3V		7		Ω
		V_{DD} = 3.3V, V_{DDO} = 2.5V		8		Ω
		V_{DD} = 3.3V, V_{DDO} = 1.8V		10		Ω

TABLE 3. CONTROL FUNCTION TABLE

Input	Outputs
OE	**Q0, Q1**
0	HiZ
1	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.71V TO 3.465V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Positive Supply Current			8		mA
I_{DDO}	Output Supply Current			3		mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.375V TO 3.465V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE		-0.3		0.8	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V	2.6			V
			V_{DDO} = 2.5V	1.8			V
			V_{DDO} = 1.8V	1.15			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low					TBD	µA
I_{OZH}	Output Tristate Current High					TBD	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information section, "Output Load Test Circuit" diagrams.

TABLE 3C. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.71V TO 1.89V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE		$0.65V_{DD}$		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE		-0.3		$0.35V_{DD}$	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 1.95V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 1.95V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -100µA	V_{DDO} - 0.2			V
			I_{OH} = -2mA	V_{DDO} - 0.45			V
V_{OL}	Output Low Voltage		I_{OL} = 100µA			0.2	V
			I_{OL} = 2mA			0.45	V
I_{OZL}	Output Tristate Current Low					TBD	µA
I_{OZH}	Output Tristate Current High					TBD	µA

TABLE 3D. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.71V TO 3.465V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{DD} = 3.465V			150	µA
		CLK	V_{IN} = V_{DD} = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
		CLK	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4A. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay; NOTE 1	*f* ≤ 350MHz		1.9		ns
*t*sk(o)	Output Skew; NOTE 2, 4			10		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				1.0	ns
t_R	Output Rise Time	20% to 80%		350		ps
t_F	Output Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay; NOTE 1	*f* ≤ 350MHz		2.1		ns
*t*sk(o)	Output Skew; NOTE 2, 4			10		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				1.0	ns
t_R	Output Rise Time	20% to 80%		400		ps
t_F	Output Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

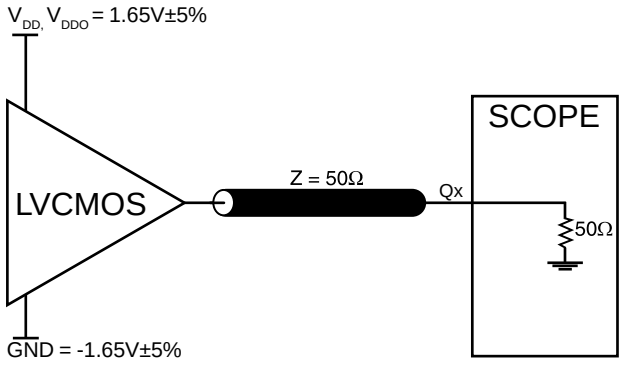
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.71V TO 1.89V, T_A = -40°C TO 85°C

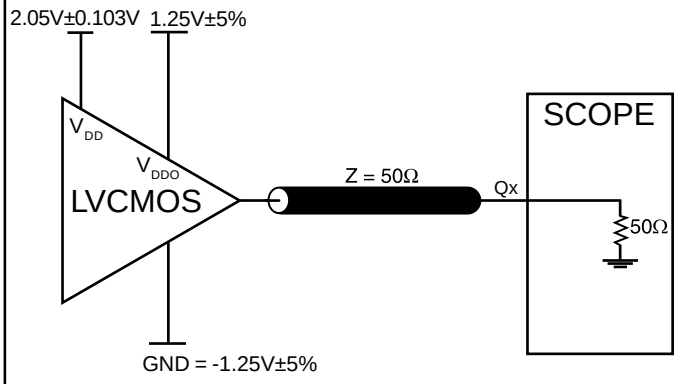
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay; NOTE 1	*f* ≤ 350MHz		2.5		ns
*t*sk(o)	Output Skew; NOTE 2, 4			10		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				1.0	ns
t_R	Output Rise Time	20% to 80%		450		ps
t_F	Output Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

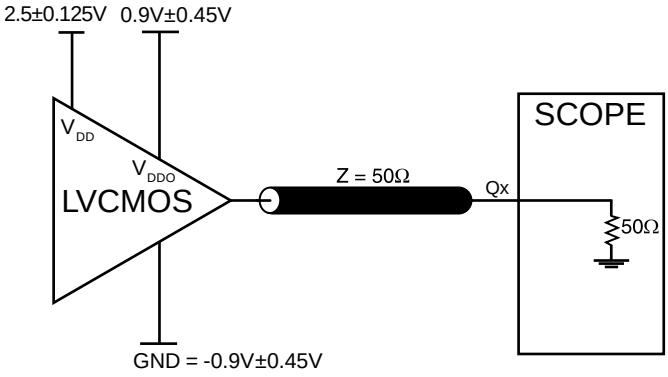
PARAMETER MEASUREMENT INFORMATION



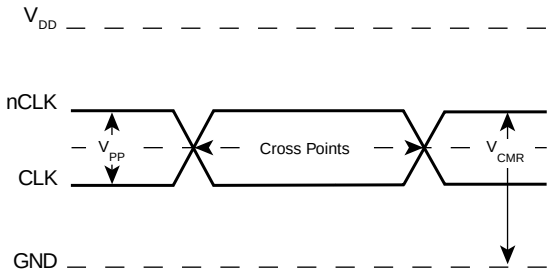
3.3V OUTPUT LOAD AC TEST CIRCUIT



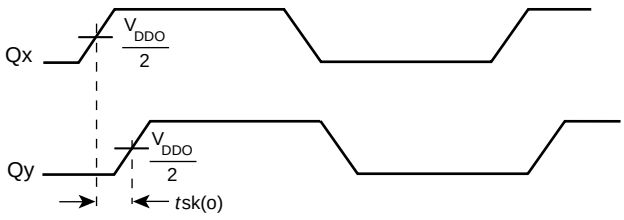
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



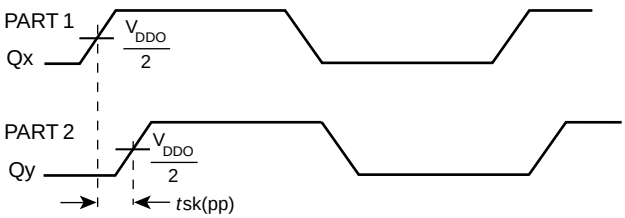
3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT



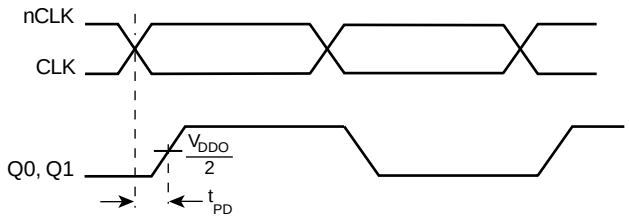
DIFFERENTIAL INPUT LEVEL



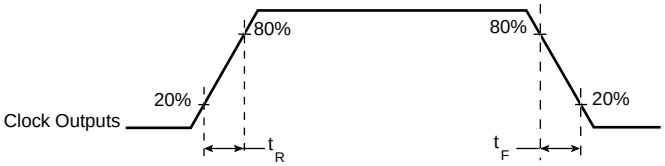
OUTPUT SKEW



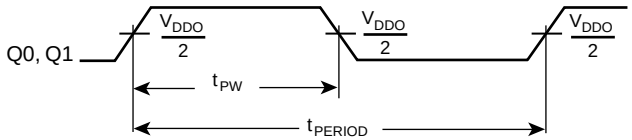
PART-TO-PART SKEW



PROPAGATION DELAY

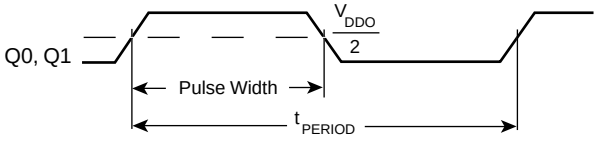


OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

t_{PW} & t_{PERIOD}



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc & t_{PERIOD}

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83026I-0I is: 260

PACKAGE OUTLINE - SUFFIX M

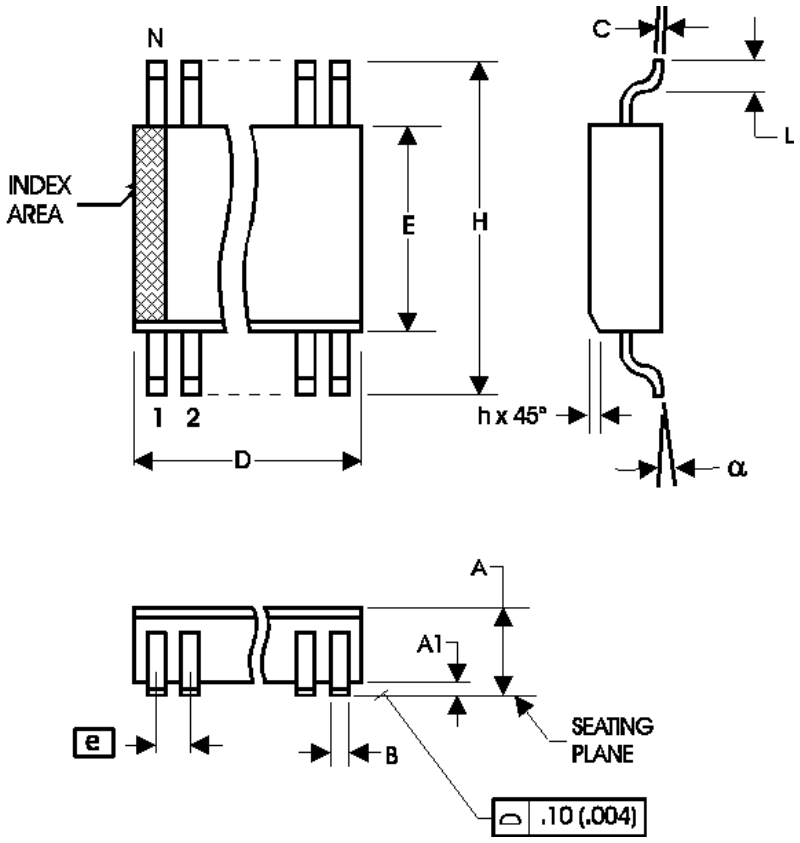


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83026BMI-01	026BI01	8 lead SOIC	96 per tube	-40°C to 85°C
ICS83026BMI-01T	026BI01	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C