



## ULTRA MICROPOWER RAIL-TO-RAIL CMOS OPERATIONAL AMPLIFIER

### GENERAL DESCRIPTION

The ALD1706 is a monolithic CMOS ultra micropower high slew-rate, high performance operational amplifier intended for a broad range of analog applications using  $\pm 1V$  to  $\pm 6V$  dual power supply systems, as well as +2V to +12V battery operated systems. All device characteristics are specified for +5V single supply or  $\pm 2.5V$  dual supply systems. Supply current is  $40\mu A$  maximum at 5V supply voltage. It is manufactured with Advanced Linear Devices' enhanced AC MOS silicon gate CMOS process.

The ALD1706 is designed to offer high performance for a wide range of applications requiring very low power dissipation. It offers the popular industry standard single operational amplifier pin configuration.

The ALD1706 has been developed specifically for the +5V single battery or  $\pm 1V$  to  $\pm 6V$  dual battery user. Several important characteristics of the device make application easier to implement at those voltages. First, the operational amplifier can operate with rail to rail input and output voltages. This means the signal input voltage and output voltage can be close to or equal to the positive and negative supply voltages. This feature allows numerous analog serial stages and flexibility in input signal bias levels. Secondly, the device was designed to accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Thirdly, the output stage can typically drive up to 25pF capacitive and 20K $\Omega$  resistive loads. These features, combined with extremely low input currents, high open loop voltage gain of 100V/mV, useful bandwidth of 400KHz, a slew rate of 0.17V/ $\mu s$ , low offset voltage and temperature drift, make the ALD1706 a versatile, micropower operational amplifier.

The ALD1706, designed and fabricated with silicon gate CMOS technology, offers 0.1pA typical input bias current. On chip offset voltage trimming allows the device to be used without nulling in most applications.

### FEATURES

- 20 $\mu A$  supply current
- All parameters specified for +5V single supply or  $\pm 2.5V$  dual supply systems
- Rail to rail input and output voltage ranges
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- 0.1pA typical (30pA max.)
- Ideal for high source impedance applications
- Dual power supply  $\pm 1.0V$  to  $\pm 6.0V$  operation
- Single power supply +2V to +12V operation
- High voltage gain -- typically 100V/mV @  $\pm 2.5V$  (100dB)
- Drive as low as a 20K $\Omega$  load
- Output short circuit protected
- Unity gain bandwidth of 0.4MHz
- Slew rate of 0.17V/ $\mu s$

### APPLICATIONS

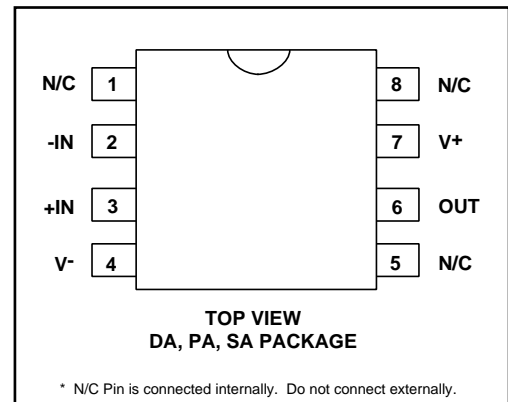
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter

### ORDERING INFORMATION

Operating Temperature Range		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package
ALD1706A DA ALD1706B DA ALD1706 DA	ALD1706A SA ALD1706B SA ALD1706 SA	ALD1706A PA ALD1706B PA ALD1706 PA ALD1706G PA

\* Contact factory for industrial temperature range

### PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_+$	_____	13.2V
Differential input voltage range	_____	-0.3V to $V_+ + 0.3V$
Power dissipation	_____	600 mW
Operating temperature range	PA, SA package _____	0°C to +70°C
	DA package _____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

## OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$   $V_S = \pm 2.5V$  unless otherwise specified

Parameter	Symbol	1706A			1706B			1706			1706G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Supply Voltage	$V_S$	$\pm 1.0$		$\pm 6.0$	$\pm 1.0$		$\pm 6.0$	$\pm 1.0$		$\pm 6.0$	$\pm 1.0$		$\pm 6.0$	V	Dual Supply Single Supply
	$V_+$	2.0		12.0	2.0		12.0	2.0		12.0	2.0		12.0	V	
Input Offset Voltage	$V_{OS}$			0.9			2.0			4.5			10.0	mV	$R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
				1.7			2.8			5.3			11.0	mV	
Input Offset Current	$I_{OS}$		0.1	25		0.1	25		0.1	25		0.1	30	pA	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
				240			240			240			450	pA	
Input Bias Current	$I_B$		0.1	30		0.1	30		0.1	30		0.1	50	pA	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
				300			300			300			600	pA	
Input Voltage Range	$V_{IR}$	-0.3		5.3	-0.3		5.3	-0.3		5.3	-0.3		5.3	V	$V_+ = +5V$ $V_S = \pm 2.5V$
		-2.8		2.8	-2.8		2.8	-2.8		2.8	-2.8		2.8	V	
Input Resistance	$R_{IN}$		$10^{12}$			$10^{12}$			$10^{12}$			$10^{12}$		$\Omega$	
Input Offset Voltage Drift	$TCV_{OS}$		7			7			7			10		$\mu\text{V}/^\circ\text{C}$	$R_S \leq 100K\Omega$
Power Supply Rejection Ratio	PSRR	70	80		65	80		65	80		60	80		dB	$R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		70	80		65	80		65	80		60	80		dB	
Common Mode Rejection Ratio	CMRR	70	83		65	83		65	83		60	83		dB	$R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		70	83		65	83		65	83		60	83		dB	
Large Signal Voltage Gain	$A_V$	32	100		32	100		32	100		20	80		V/ mV	$R_L = 1M\Omega$ $R_L = 1M\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		20			20			20			10			V/ mV	
Output Voltage Range	$V_{O\ low}$		0.001	0.01		0.001	0.01		0.001	0.01		0.001	0.01	V	$R_L = 1M\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
	$V_{O\ high}$	4.99	4.999		4.99	4.999		4.99	4.999		4.99	4.999		V	
	$V_{O\ low}$		-2.40	-2.30		-2.40	-2.30		-2.40	-2.30		-2.40	-2.30	V	
	$V_{O\ high}$	2.30	2.40		2.30	2.40		2.30	2.40		2.30	2.40		V	
Output Short Circuit Current	$I_{SC}$		200			200			200			200		$\mu\text{A}$	
Supply Current	$I_S$		20	40		20	40		20	40		20	50	$\mu\text{A}$	$V_{IN} = 0V$ No Load
Power Dissipation	$P_D$			200			200			200			250	$\mu\text{W}$	$V_S = \pm 2.5V$

**OPERATING ELECTRICAL CHARACTERISTICS (cont'd)**
**T<sub>A</sub> = 25°C V<sub>S</sub> = ±2.5V unless otherwise specified**

Parameter	Symbol	1706A			1706B			1706			1706G			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Capacitance	C <sub>IN</sub>		1			1			1			1		pF	
Bandwidth	B <sub>W</sub>		400			400			400			400		KHz	
Slew Rate	S <sub>R</sub>		0.17			0.17			0.17			0.17		V/μs	A <sub>V</sub> = +1 R <sub>L</sub> = 1MΩ
Rise time	t <sub>r</sub>		1.0			1.0			1.0			1.0		μs	R <sub>L</sub> = 1MΩ
Overshoot Factor			20			20			20			20		%	R <sub>L</sub> = 1MΩ C <sub>L</sub> = 25pF
Settling Time	t <sub>s</sub>		10.0			10.0			10.0			10.0		μs	0.1% A <sub>V</sub> = -1 R <sub>L</sub> = 1MΩ C <sub>L</sub> = 25pF

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±1.0V unless otherwise specified**

Parameter	Symbol	1706A			1706B			1706			1706G			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		70			70			70			70		dB	R <sub>S</sub> ≤ 1MΩ
Common Mode Rejection Ratio	CMRR		70			70			70			70		dB	R <sub>S</sub> ≤ 1MΩ
Large Signal Voltage Gain	A <sub>V</sub>		50			50			50			50		V/ mV	R <sub>L</sub> = 1MΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	0.9	-0.95 0.95	-0.9	0.9	-0.95 0.95	-0.9	0.9	-0.95 0.95	-0.9	0.9	-0.95 0.95	-0.9	V V	R <sub>L</sub> = 1MΩ
Bandwidth	B <sub>W</sub>		0.3			0.3			0.3			0.3		MHz	
Slew Rate	S <sub>R</sub>		0.17			0.17			0.17			0.17		V/μs	A <sub>V</sub> = +1 C <sub>L</sub> = 25pF

**V<sub>S</sub> = ±2.5V -55°C ≤ T<sub>A</sub> ≤ +125°C unless otherwise specified**

Parameter	Symbol	1706B DA			1706 DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V <sub>OS</sub>			3.0			6.5	mV	R <sub>S</sub> ≤ 100KΩ
Input Offset Current	I <sub>OS</sub>			8.0			8.0	nA	
Input Bias Current	I <sub>B</sub>			10.0			10.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		dB	R <sub>S</sub> ≤ 1MΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		dB	R <sub>S</sub> ≤ 1MΩ
Large Signal Voltage Gain	A <sub>V</sub>	15	50		15	50		V/ mV	R <sub>L</sub> = 1MΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	2.30	-2.40 2.40	-2.30	2.30	-2.40 2.40	-2.30	V V	R <sub>L</sub> = 1MΩ

## Design & Operating Notes:

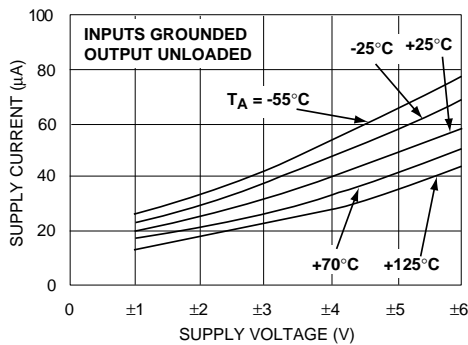
1. The ALD1706 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1706 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency.
2. The ALD1706 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V below the positive supply voltage. Since offset voltage trimming on the ALD1706 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions above this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that

the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than  $10^{12}\Omega$  would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

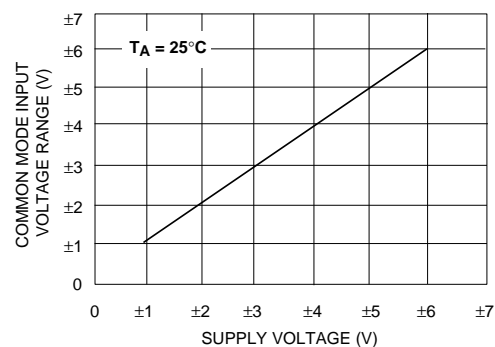
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
5. The ALD1706 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.
6. The ALD1706, with its micropower operation, offers numerous benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats less than  $0.1^{\circ}\text{C}$  above ambient temperature under most operating conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

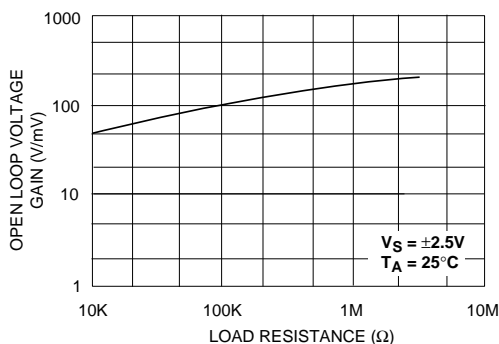
**SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



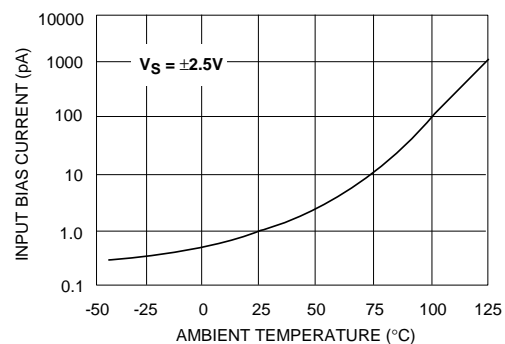
**COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE**

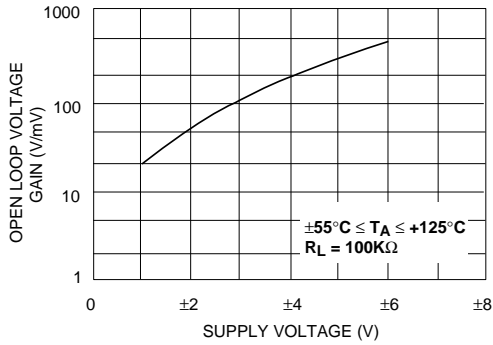


**INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE**

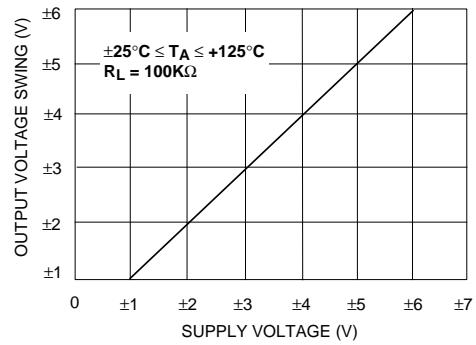


# TYPICAL PERFORMANCE CHARACTERISTICS

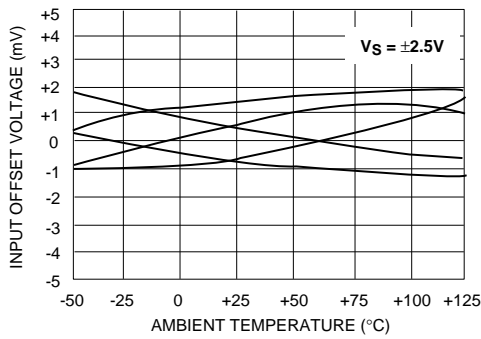
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE**



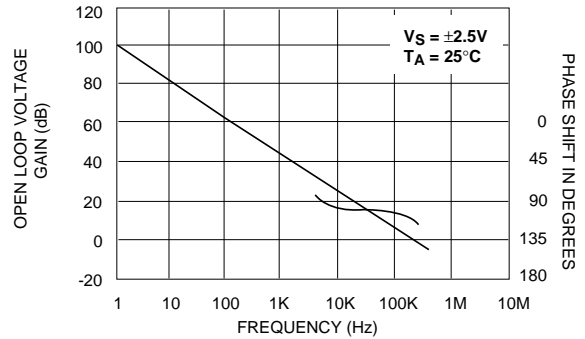
**OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE**



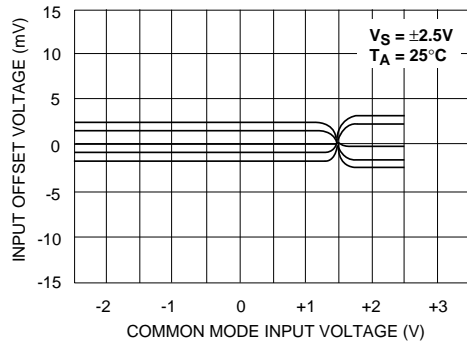
**INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS**



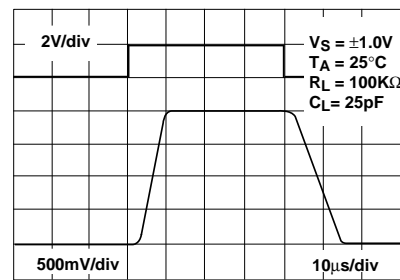
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY**



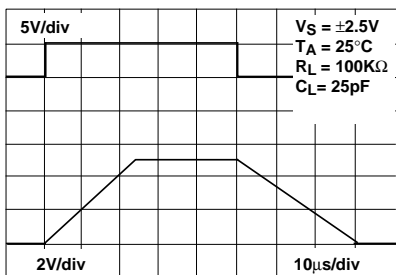
**INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE**



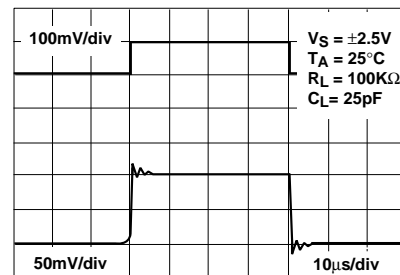
**LARGE - SIGNAL TRANSIENT RESPONSE**



**LARGE - SIGNAL TRANSIENT RESPONSE**

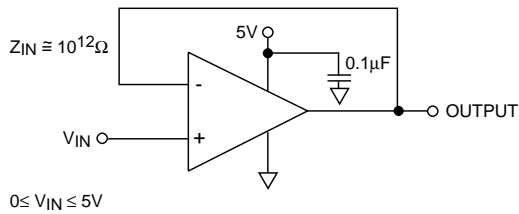


**SMALL - SIGNAL TRANSIENT RESPONSE**



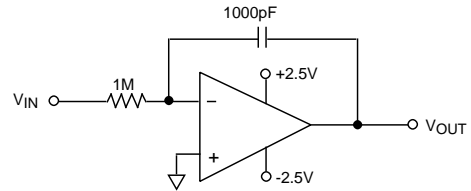
## TYPICAL APPLICATIONS

### RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER

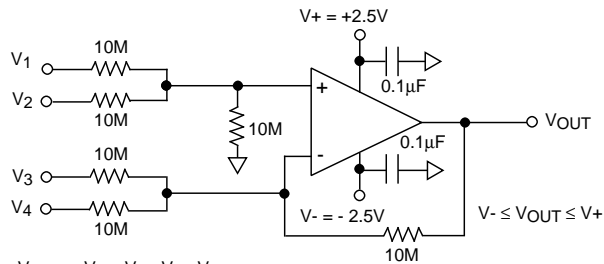


\* See Rail to Rail Waveform

### CHARGE INTEGRATOR



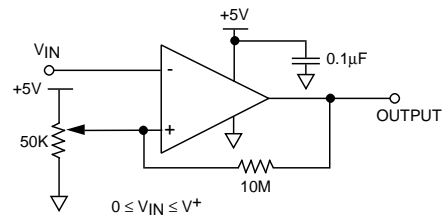
### HIGH INPUT IMPEDANCE RAIL-TO-RAIL PRECISION DC SUMMING AMPLIFIER



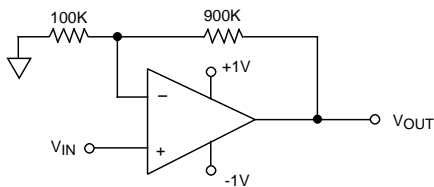
$$V_{OUT} = V_1 + V_2 - V_3 - V_4$$

$R_{IN} = 10M\Omega$  Accuracy limited by resistor tolerances and input offset voltage

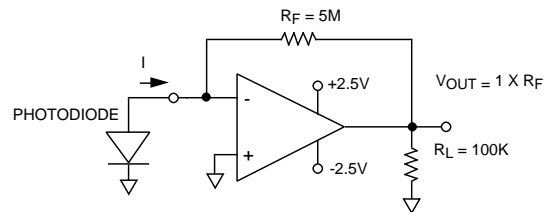
### RAIL-TO-RAIL VOLTAGE COMPARATOR



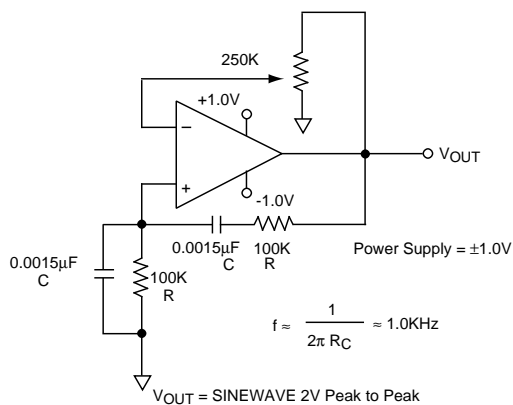
### HIGH IMPEDANCE NON-INVERTING AMPLIFIER



### PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



### WIEN BRIDGE OSCILLATOR



### MICROPOWER BUFFERED VARIABLE VOLTAGE SOURCE

