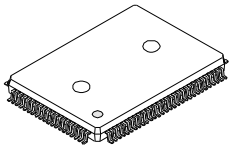
OLED DRIVER IC

DESCRIPTION

The SC16806 is an 80-line OLED row driver used with column driver SC16805 to drive dot-matrix OLED panels. It supports a bi-directional cascade interface, sleep mode control function as well as 80 output amplifiers. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.



QFP-100-14x20-0.65

FEATURES

* CMOS technology
* 80 output current sinkers
* High speed line rate
* Low power consumption
* Maximum operating voltage:18V
* Bi-directional cascade interface
* Sleep mode control

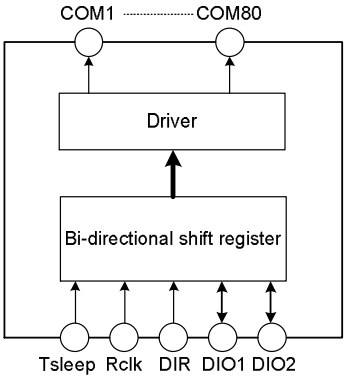
ORDERING INFORMATION

Device	Package
SC16806	QFP-100-14X20-0.65

APPLICATIONS

* OLED display panel.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (unless otherwise stated, T_{amb}=25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	AV_{DD}	-0.3~18	V
	V_{DD}	-0.3~5.5	V
I/O Pin Voltage	V_X	-0.3~V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30~+85	°C
Storage Temperature	T_{stg}	-55~+125	°C

DC ELECTRICAL CHARACTERISTICS (unless otherwise stated, T_{amb}=25°C, V_{DD}=5V, AV_{DD} =18V)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Driver Power Supply	AV_{DD}		5.0	-	18	V
Operating Voltage	V_{DD}		2.0	-	5.5	V
Operating Current	I_{CC}	V_{DD}=5V, Rclk=1MHz No output load	-	-	1	mA
Standby Current	I_{SB}	Tsleep=0V	-	-	1	μA
High Level Input Voltage	V_{IH}		0.8V_{DD}	-	5	V
Low Level Input Voltage	V_{IL}		0	-	0.2V_{DD}	V
Low Level Common Sink Current	I_{ROW}	V_{ROW}=0.5V	30	-	-	mA
High Level Input Leakage Current	I_{IH}	V_{DD}=5V, V_O=0V,Tsleep=0V, V_{IN}=5V	-	-	2	μA
Low Level Input Leakage Current	I_{IL}	V_{DD}=5V, V_O=0V,Tsleep=0V, V_{IN}=0V	-	-	2	μA

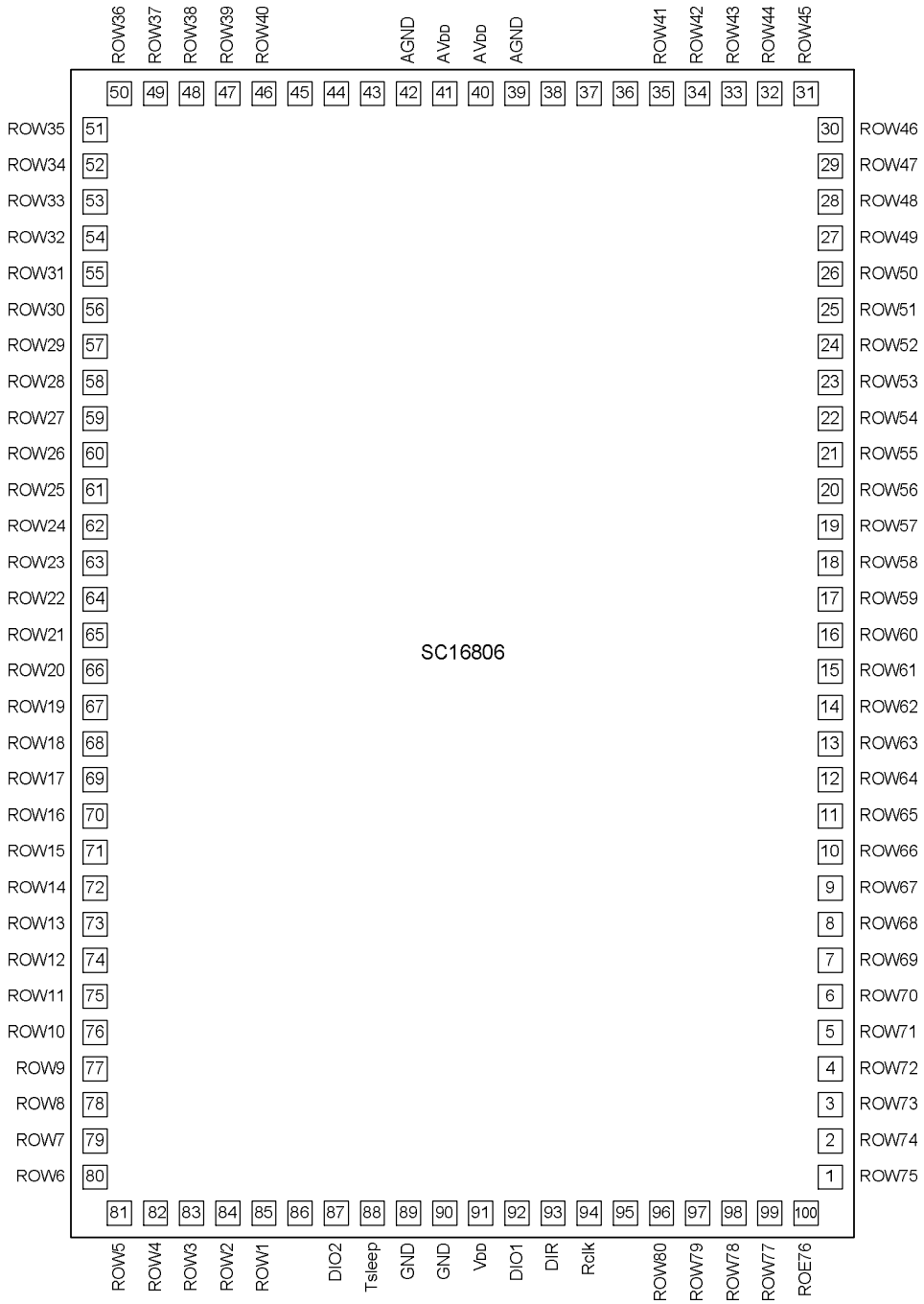
AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, T_{amb}=25°C, V_{DD}=5V, AV_{DD} =18V)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Rclk Cycle	t_C		20	-	-	μs
Rclk High Level Pulse Duration	t_{WH}		1000	-	-	ns
Rclk Low Level Pulse Duration	t_{WL}		1000	-	-	ns
Data Setup Time	t_{SU}		50	-	-	ns
Data Hold Time	t_{HD}		50	-	-	ns
Rclk Rising Edge To DIO Delay Time	t_{YD}		-	-	100	ns
Rclk Falling Edge To ROW Delay Time*	t_{YR}		-	-	120	ns

Note:*=The value of t_{YR} depends on the value of the load.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin no.	Pin name	Description
85~46 35~96	ROW1~ROW40 ROW41~ROW80	OLED driving output pin.
40~41	AVDD	OLED operation power supply: +5V~+18V
39, 42	AGND	Analogy ground, connected to GND
89, 90	GND	Ground pin.
92	DIO1	Input enable signal: When DIR=0, DIO1 set up input, and DIO2 is output. When DIR=1, DIO1 set up output, and DIO2 is input.
87	DIO2	
94	Rclk	Input for shift clock
93	DIR	Input for data flow direction select
88	Tsleep	Sleep mode control pin, when Tsleep=0, the circuit enter sleep mode
91	VDD	Power supply for internal logic: 2.0~5.5V
86, 95, 36~38, 43~45	NC	No connection

FUNCTION DESCRIPTION

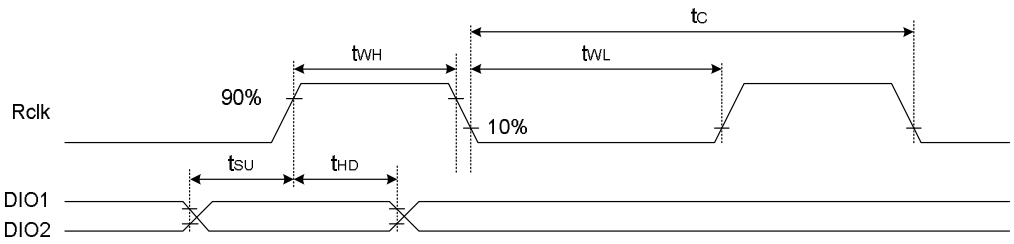
Bi- directional shift register

This bi-directional shift register is used to transfer common data. The direction of the shift is selected by the DIR input. The output of this shift register is used to transfer the common data to the next stage of cascaded ROW driver.

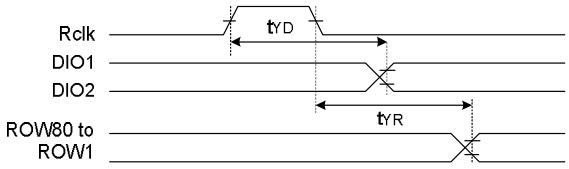
Output amplifier

The output amplifier output the OLED driver sink current.

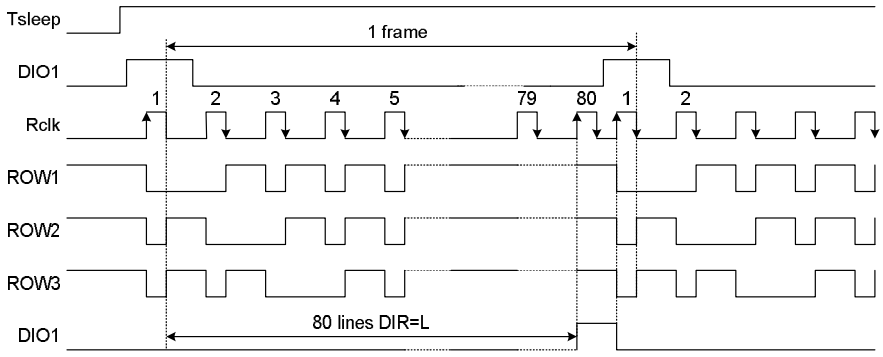
INPUT TIMING CHARACTERISTICS



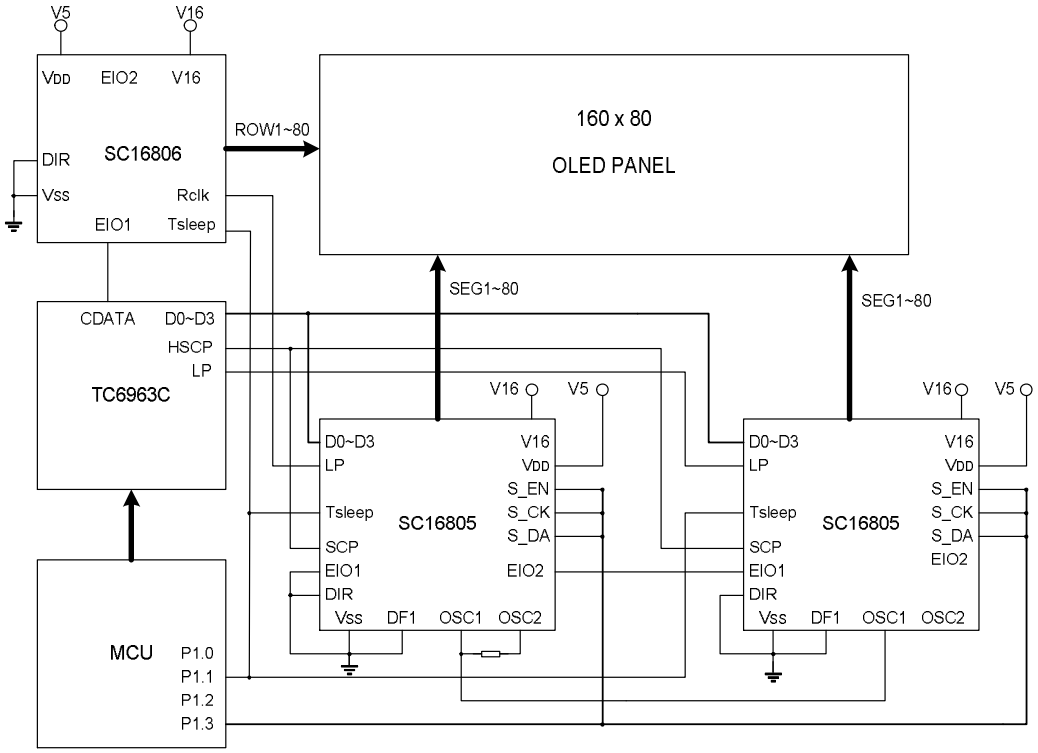
OUTPUT TIMING CHARACTERISTICS



TIMING DIAGRAM

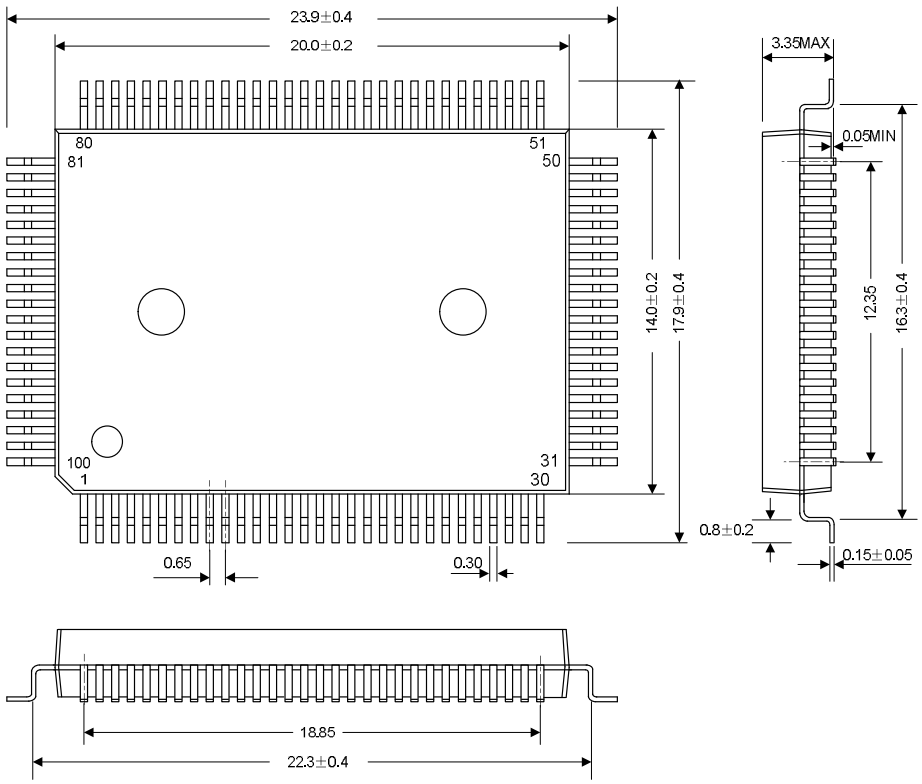


TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

QFP-100-14×20-0.65 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.