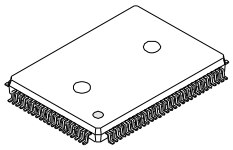
OLED DRIVER IC

DESCRIPTION

The SC16805 is an 80-output OLED column driver utilizing low power CMOS technology specially designed for driving large capacity dot –matrix OLED panels. It includes four primary blocks, namely: 80-bit data register address selector, 80-bit data register, 80-bit data latch, 80-bit output current amplifier and a reference current generator. In order to obtain suitable brightness and minimize the drift between drivers, the constant current is adjustable.



QFP-100-14x20-0.65

FEATURES

* CMOS technology
* Low power consumption
* 80 output channels
* Output current: 200μA (max.)
* Serial or 4-bits parallel data interface with controller
* Shift clock frequency: 10MHz (max.)
* A function for cascading more than one device
* Operating voltage: 18V (max.)
* Bi- directional data transfer through the device
* External brightness adjustment with serial interface.
* Sleep mode control

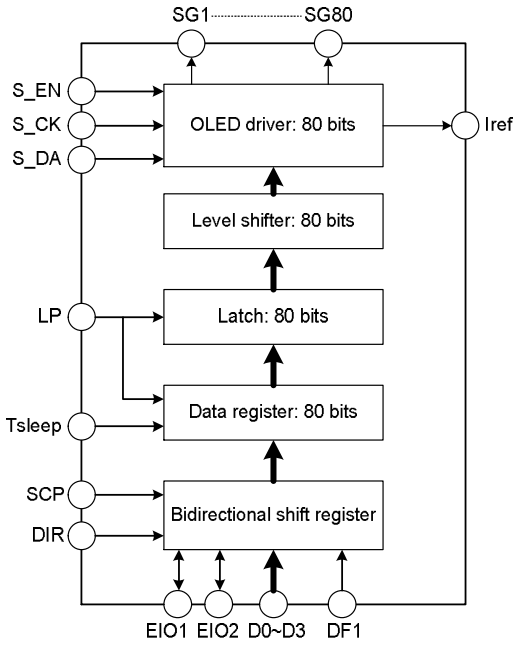
ORDERING INFORMATION

Device	Package
SC16805	QFP-100-14X20-0.65

APPLICATIONS

* OLED display panel.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (unless otherwise specified, T_{amb}=25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	AV_{DD}	-0.3~18	V
	V_{DD}	-0.3~5.5	V
I/O Pin Voltage	V_X	-0.3~V_{DD}+0.3	V
Operating Temperature	Topr	-30~+85	°C
Storage Temperature	Tstg	-55~+125	°C

DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_{amb}=25°C, V_{DD}=5V, AV_{DD} =18V)

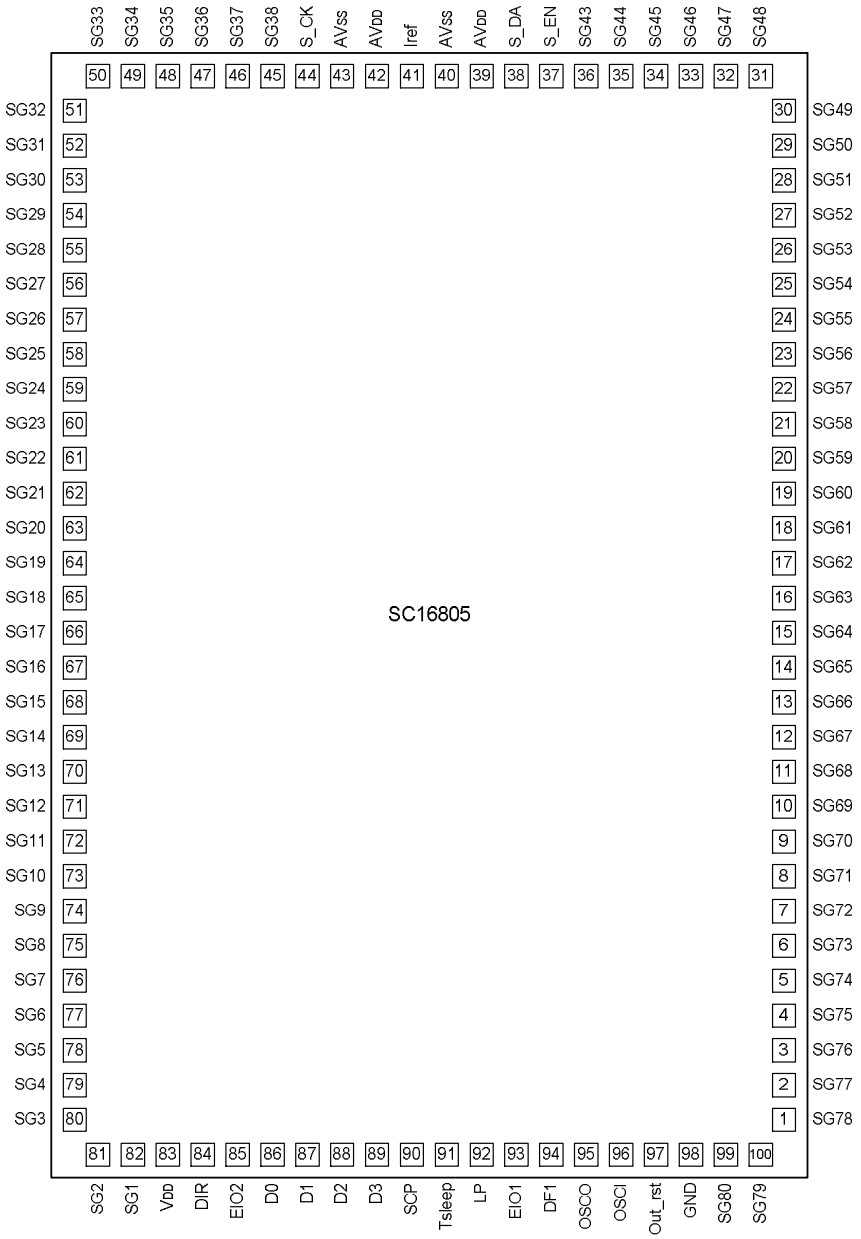
Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Driver Power Supply	AV_{DD}		5.0	-	18	V
Operating Voltage	V_{DD}		2.0	5.0	5.5	V
Operating Current	I_{CC}	V_{DD}=5V, SCP=1MHz No output load	-	-	1	mA
Standby Current	I_{SB}	Tsleep=0V	-	-	1	μA
High Level Input Voltage	V_{IH}		0.8V_{DD}	-	5.0	V
Low Level Input Voltage	V_{IL}		0	-	0.2V_{DD}	V
High level segment output current	I_{SEGOH}	V_{SEGOH}=10V	-30	-	-200	μA
High Level Segment Output Current Tolerance	I_{TOL1}*	I_{SEGOH}=-200uA	-	-	±5	%
High Level Segment Output Current Tolerance	I_{TOL2}*	I_{SEGOH}=-150uA	-	-	±1	%
High Level Input Leakage Current	I_{IH}	V_{DD}=5V, V_O=0V, V_{IN}=5V, Tsleep=0V	-	-	2	μA
Low Level Input Leakage Current	I_{IL}	V_{DD}=5V, V_O=0V, V_{IN}=0V, Tsleep=0V	-	-	2	μA
Oscillation Resistor	Rosc	t_{WH3}=5us	-	120	-	KΩ

AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_{amb}=25°C, V_{DD}=5V, AV_{DD} =18V)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
LP Pulse Width	t_{W1}		140	-	-	ns
LP Negative To SCP Rising Edge	t_{LPX}		70	-	-	ns
SCP Cycle	t_C		140	-	-	ns
SCP High Level Pulse Duration	t_{WH2}		50	-	-	ns
SCP Low Level Pulse Duration	t_{WL}		50	-	-	ns
SCP To LP Rising Time	t_{XLP}		20	-	-	ns
Data Setup Time	t_{SU1}		50	-	-	ns
Data Hold Time	t_{HD}		50	-	-	ns
EIO Setup Time	t_{SU2}		50	-	-	ns
EIO Reset time	t_{CE}		-	-	120	ns
Out_rst To SEG Rising Time(see note1)	t_{CS}		-	-	200	ns
EIO Output Delay Time	t_{XE}		-	-	55	ns

Note: 1.t_{CS} value depends on the value of the load.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin no.	Pin name	Description
82~45 36~99	SE1 ~ SG38 SG43 ~ SG80	OLED segment driver (column) output pin The output varies at the falling edge of LP.
39, 42	AVDD	Logic operation power supply AVDD: +5V~ +18V
41	Iref	Reference current output pin
97	Out_rst	Row synchronization clock output pin.
93 85	EIO1 EIO2	Enable input/output pin When DIR=0, EIO1 set up input, and EIO2 is output; When DIR=1, EIO1 set up output, and EIO2 is input.
86~89	D0 ~ D3	Display data input pins When DF1=0, data are input D0, and D1~D3 are connected to Vss. When DF2=1, data are inputted into D0~D3 pins.
83,	V_{DD}	Logic power supply V_{DD}: 2.0V~ 5.5V
84	DIR	Input for data flow direction select.
	V_{SS}	The digit ground.
43， 40	AV_{SS}	The analogy ground, connected with VSS.
94	DF1	Input for selection data format
91	Tsleep	The sleep mode control pin, when Tsleep=0, the circuit enter sleep mode.
92	LP	This pin is used to input the latch pulse signals of the display data
90	SCP	Input for frame signal
37	S_EN	Lightness dimming enable signal
44	S_CK	Lightness dimming clock
38	S_DA	Lightness dimming data
95	OSCO	Oscillator output pin
96	OSCI	Oscillator input pin

FUNCTION DESCRIPTION

Bidirectional shift register

The output of this shift register is used to store the data bus signals in the data register. The direction of the shift is selected by the DIR input. As the enable signal is in a disabled state, the internal clock signal and data bus are fixed at "L", thereby, placing the chip in power saving mode. When multiple segment drivers are used, the EIO terminals of the various drivers connected in series and the EIO terminal of the first driver is connected to VSS. The enable control circuit automatically senses when 80 bits of data have been received. It sends the enable signal, thus eliminating the need for an external control signal from the control unit.

Data register

This register converts the data bus signal from serial to parallel mode via the output of the bidirectional shift register. Consequently, the relationship between the serial display data and segment output is independent of the shift clock input number.

Latch

The latch circuit receivers the contents of the data register when triggered by the falling edge of the LP, and output them to the OLED driver.

Level shifter

The level shifter is a level interface circuit used to convert the V_{DD} control unit signals to V16 driver signal level.

OLED driver

The OLED driver outputs the OLED driver current.

Display data and driver output pins relationship

4-bit parallel mode

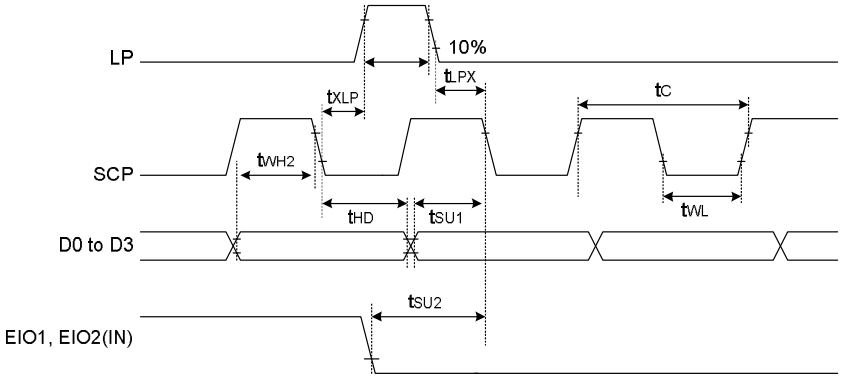
DF1	DIR	EIO1	EIO2	Data Input	Clock						
					1st	2nd	3rd	.....	30th	31st	32nd
V_{DD}	V_{DD}	Output	Input	D0	SG77	SG73	SG69	.....	SG9	SG5	SG1
				D1	SG78	SG74	SG70	.....	SG10	SG6	SG2
				D2	SG79	SG75	SG71	.....	SG11	SG7	SG3
				D3	SG80	SG76	SG72	.....	SG12	SG8	SG4
	V_{SS}	Input	Output	D0	SG4	SG8	SG12	.....	SG72	SG76	SG80
				D1	SG3	SG7	SG11	.....	SG71	SG75	SG79
				D2	SG2	SG6	SG10	.....	SG70	SG74	SG78
				D3	SG1	SG5	SG9	.....	SG69	SG73	SG77

1-bit serial mode

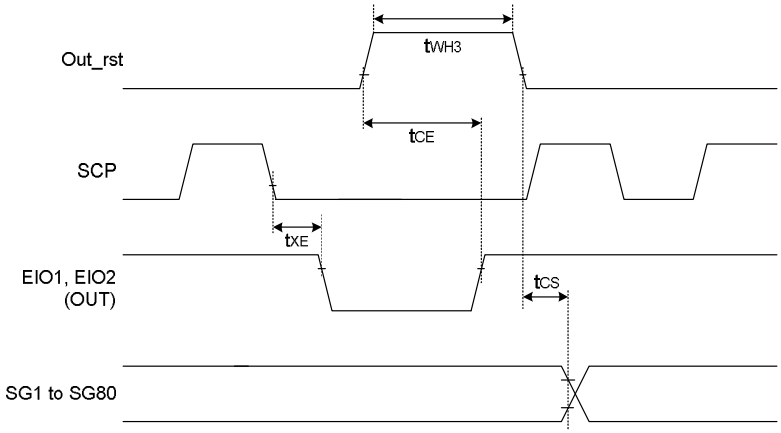
DF1	DIR	EIO1	EIO2	Data Input	Output						
					SG80	SG79	SG78	.....	SG3	SG2	SG1
V_{DD}	V_{SS}	Input	Output	D0	L3	L2	L1	.....	F2	F1	F0
	V_{DD}	Output	Input	D0	F0	F1	F2	.....	L1	L2	L3

Note: DF1 pin must be connected to either V_{DD} or V_{SS}, DF1 cannot be floating.

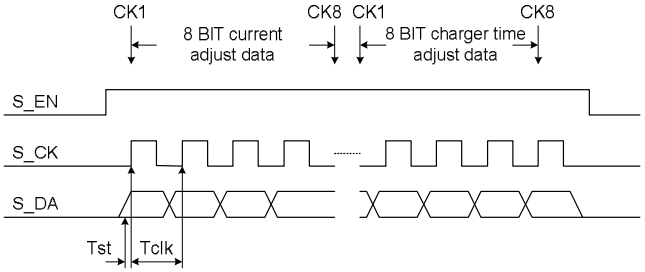
INPUT TIMING CHARACTERISTICS



OUTPUT TIMING CHARACTERISTICS



TIMING DIAGRAM

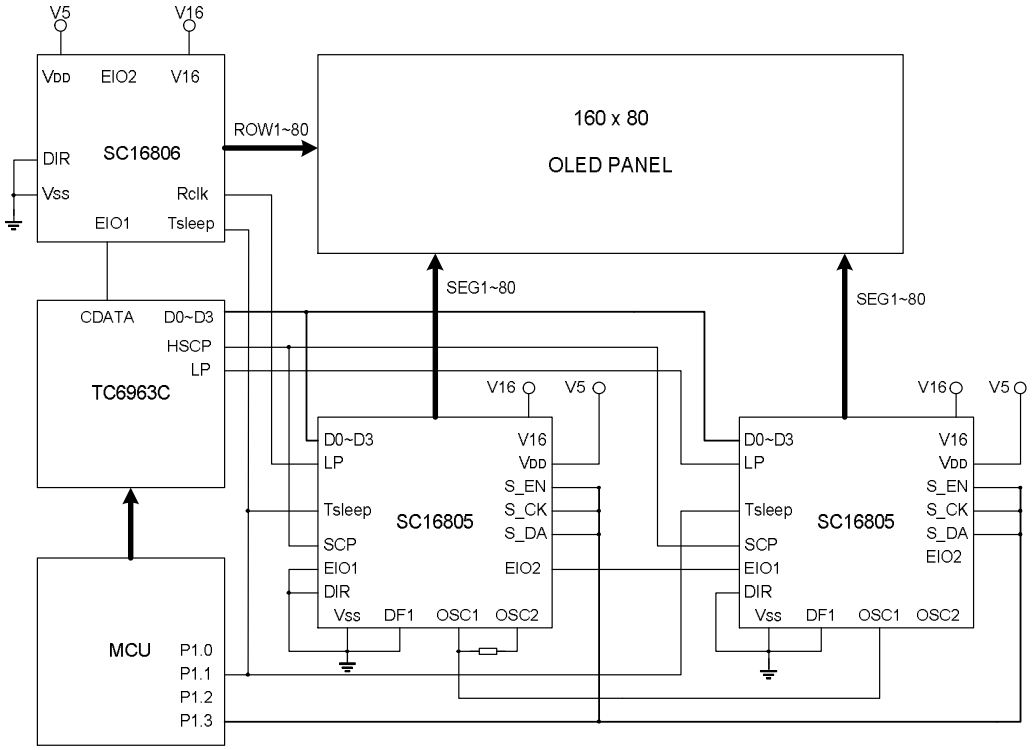


Note: 1: First transmit the least bit.

2: At 00H, there are the minimum current, and the charger time is minimum. And changed with the increasing data, but not in linearity.

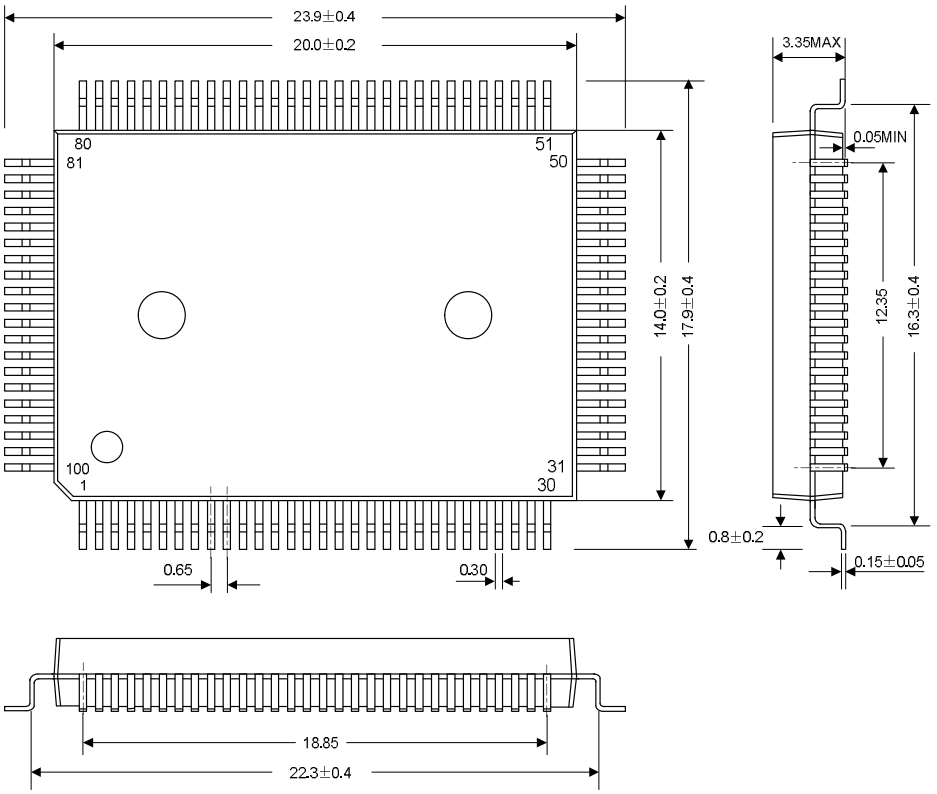
3: Tst, Tclk is only for reference, Tst is above 10ns, and Tclk is smaller than 1μs.

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

QFP-100-14×20-0.65 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.
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