GENERAL DESCRIPTION

The XR16C850[1] (850) is a Universal Asynchronous Receiver and Transmitter (UART). This device supports Intel and PC mode data bus interface and is software compatible to industry standard 16C450, 16C550, ST16C580 and ST16C650A UARTs.

The 850 has 128 bytes of TX and RX FIFOs and is capable of operating up to a serial data rate of 2 Mbps. The internal registers include the 16C550 register set plus Exar's enhanced registers for additional features to support today's highly demanding data communication needs. The enhanced features include automatic hardware and software flow control, selectable TX and RX trigger levels, and wireless infrared (IrDA) encoder/decoder.

The XR16C850 is available in the 44 pin PLCC and 48 pin TQFP packages. They both provide the standard Intel Bus mode and PC ISA bus (PC) mode. The Intel Bus mode is compatible with the ST16C450 and ST16C550 while the PC mode allows connection to the PC ISA bus.

NOTE: *1 Covered by U.S. patent #5,649,122 and #5,949,787.*

FEATURES

Added feature in devices with top mark date code of "F2 YYWW" and newer:

- 5 volt tolerant inputs
- 0 ns address hold time (T_{AH})

- 2.97 to 5.5 volt operation
- Pin to pin compatible to ST16C550, ST16C580, ST16C650A and TL16C750
- 128-byte Transmit and Receive FIFOs
- Transmit/Receive FIFO Counters
- Programmable TX/RX FIFO Trigger Levels
- Automatic Hardware/Software Flow Control
- Auto RS-485 half duplex direction support
- Programmable Xon/Xoff characters
- Infrared (IrDA) TX and RX Encoder/Decoder
- Sleep Mode (100 uA stand-by)

APPLICATIONS

- Battery Operated Electronics
- Internet Appliances
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort
- Wireless Infrared Data Communications Systems

FIGURE 1. BLOCK DIAGRAM

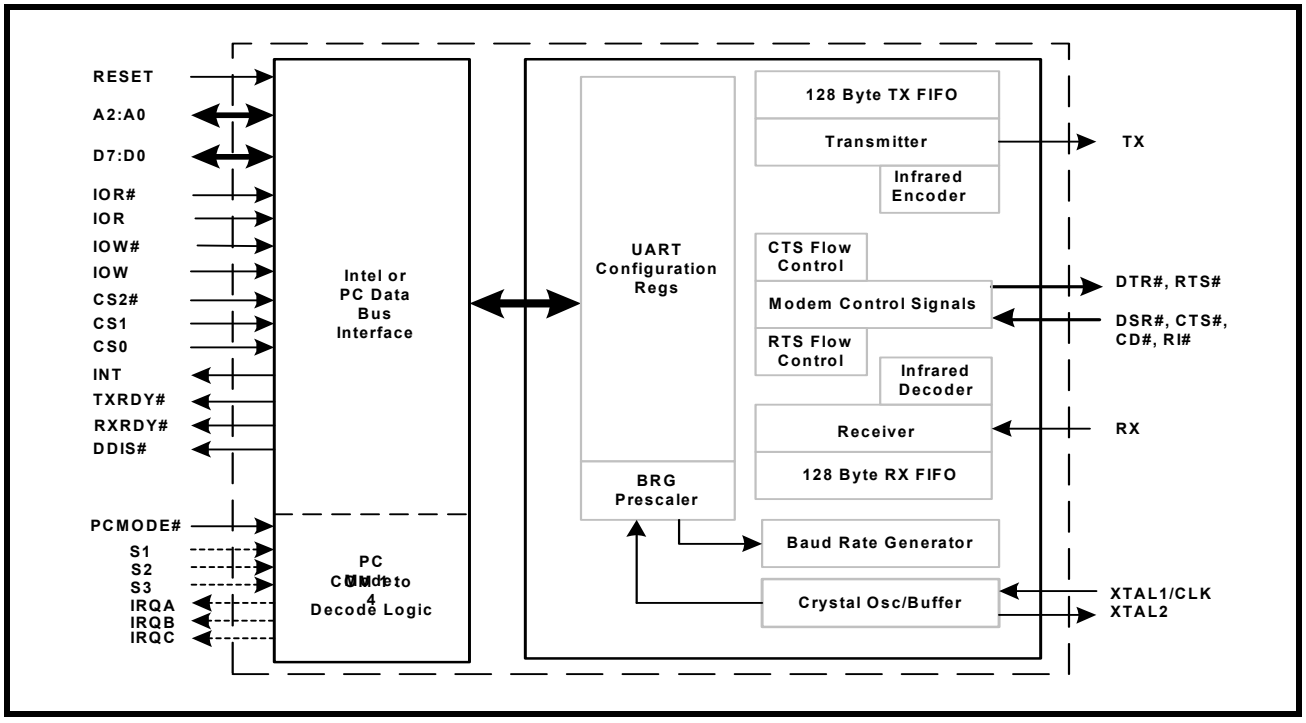
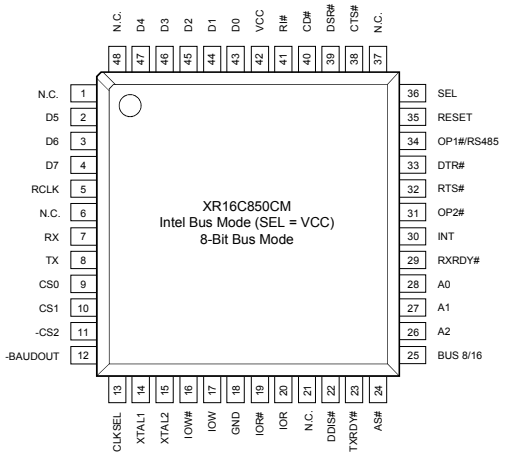
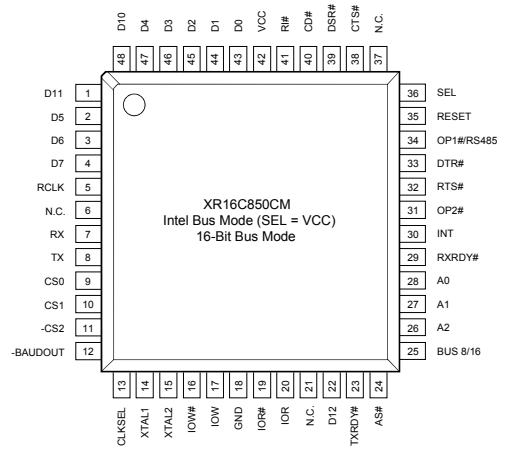
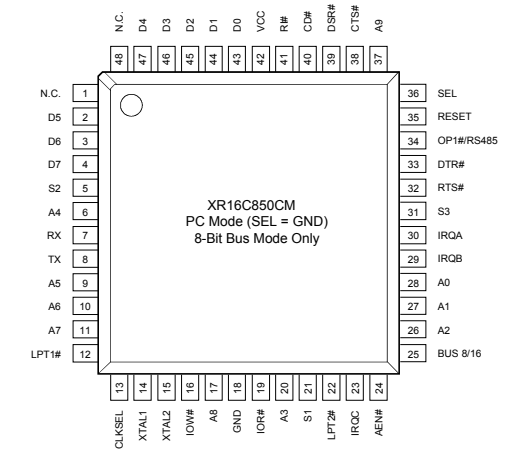


FIGURE 2. PINOUTS IN INTEL BUS MODE AND PC MODE, TQFP AND PLCC PACKAGES

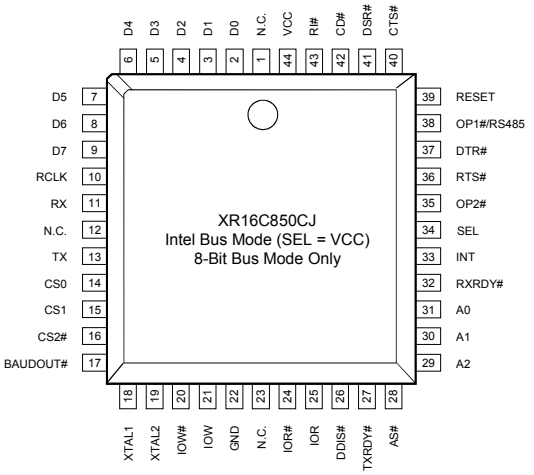
48-TQFP PACKAGE

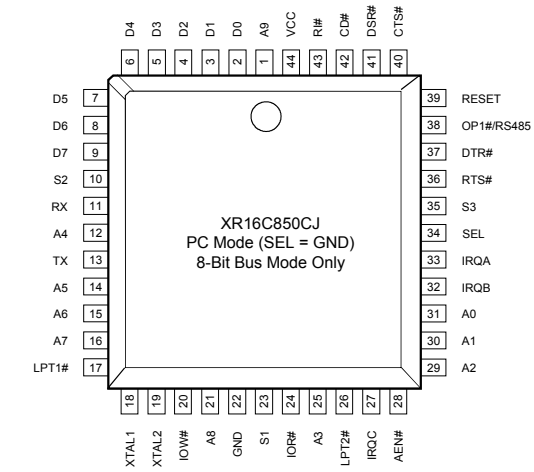






44-PLCC PACKAGE





ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16C850CJ	44-Lead PLCC	0°C to +70°C	Active
XR16C850CM	48-Lead TQFP	0°C to +70°C	Active
XR16C850IJ	44-Lead PLCC	-40°C to +85°C	Active
XR16C850IM	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

NOTE: Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
INTEL BUS MODE INTERFACE. THE SEL PIN IS CONNECTED TO VCC.				
A2 A1 A0	29 30 31	26 27 28	I	Address data lines [2:0]. A2:A0 selects internal UART's configuration registers.
D0 D1 D2 D3 D4 D5 D6 D7	2 3 4 5 6 7 8 9	43 44 45 46 47 2 3 4	I/O	Data bus lines [7:0] (bidirectional).
IOR#	24	19	I	Input/Output Read (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], places it on the data bus to allow the host processor to read it on the leading edge. Either an active IOR# or IOR is required to transfer data from 850 to CPU during a read operation. If not used, connect this pin to VCC. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
IOR	25	20	I	Input/Output Read (active high). Same as IOR# but active high. Either an active IOR# or IOR is required to transfer data from 850 to CPU during a read operation. If not used, connect this pin to GND. During PC Mode, this pin becomes A3. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
IOW#	20	16	I	Input/Output Write (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Either an active IOW# or IOW is required to transfer data from 850 to the Intel type CPU during a write operation. If not used, connect this pin to VCC. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
IOW	21	17	I	Input/Output Write (active high). The rising edge instigates the internal write cycle and the falling edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Either an active IOW# or IOW is required to transfer data from 850 to the Intel type CPU during a write operation. During PC Mode, this pin becomes A8. If not used, connect this pin to GND. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
CS0	14	9	I	Chip Select 0 input (active high). This input selects the XR16C850 device. If CS1 or CS2# is used as the chip select then this pin must be connected to VCC. During PC Mode, this pin becomes A5. Caution: SEE"FACTORY TEST MODE" ON PAGE 7.
CS1	15	10	I	Chip Select 1 input (active high). This input selects the XR16C850 device. If CS0 or CS2# is used as the chip select then this pin must be connected to VCC. During PC Mode, this pin becomes A6. Caution: SEE"FACTORY TEST MODE" ON PAGE 7.
CS2#	16	11	I	Chip Select 2 input (active low). This input selects the XR16C850 device. If CS0 or CS1 is used as the chip select then this pin must be connected to GND. During PC Mode, this pin becomes A7. Caution: SEE"FACTORY TEST MODE" ON PAGE 7.
INT	33	30	O	Interrupt Output. This output becomes active whenever the transmitter, receiver, line and/or modem status register has an active condition and is enabled by IER. See interrupt section for more details. During PC mode, this pin becomes IRQA.
RXRDY#	32	29	O	Receive Ready (active low). A logic 0 indicates receive data ready status, i.e. the RHR is full or the FIFO has one or more RX characters available for unloading. For details, see **Table 2**. During PC Mode, this pin becomes IRQB.
TXRDY#	27	23	O	Transmit Ready (active low). Buffer ready status is indicated by a logic 0, i.e. at least one location is empty and available in the FIFO or THR. For details, see **Table 2**. During PC Mode, this pin becomes IRQC.
AS#	28	24	I	Address Strobe input (active low). In the Intel bus mode, the leading-edge transition of AS# latches the chip selects (CS0, CS1, CS2#) and the address lines A0, A1 and A2. This input is used when the address lines are not stable for the duration of a read or write operation. In devices with top mark date code of "F2 YYWW" and newer, the address bus is latched even if this input is not used. These devices feature a '0 ns' address hold time. See "AC Electrical Characteristics" . If not required, this input can be permanently tied to GND. During PC Mode, this pin becomes AEN#.
D10 D11 D12	- - -	48 1 22	O	High order data bus. When BUS8/16 is selected as 16 bit data bus mode (BUS8/16 is grounded), RX data errors (break, parity, framing) can be read via these pins. D10 = Parity, D11 = Framing, and D12 = Break. When BUS8/16 is selected as 8 bit data bus mode (BUS8/16 is at VCC), D10 and D11 are inactive and D12 becomes DDIS#. During PC Mode, D10 and D11 are inactive and D12 becomes LPT2#.
BUS8/16	-	25	I	8 or 16 Bit Bus select. For normal 8 bit operation, this pin should be connected to VCC or left open. To select 16 bit bus mode, this pin should be connected to GND. When 16 bit bus mode is enabled, DDIS# becomes D12. 16 bit bus mode is not available for PC Mode. Only RX data error will be provided during this operation. This pin has an internal pull-up resistor.
CLKSEL	-	13	I	Clock Select. The div-by-1 or div-by-4 pre-scaleable clock is selected by this pin. The div-by-1 clock is selected when CLKSEL is connected to VCC or the div-by-4 is selected when CLKSEL is connected to GND. MCR bit-7 can override the state of this pin following reset or initialization (see MCR bit-7). This pin is not available on 40 and 44 pin packages which provide MCR bit-7 selection only. This pin has an internal pull-up resistor.
RCLK	10	5	I	This input is used as external 16X clock input to the receiver section. If not used, connect the -BAUDOUT pin to this input externally. During PC Mode, this pin becomes S2.

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
BAUD-OUT#	17	12	O	Baud Rate Generator Output (active low). This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to BAUDOUT# when the receiver is operating at the same data rate. When the PC mode is selected, the baud rate generator clock output is internally connected to the RCLK input. This pin then functions as the printer port decode logic output (LPT1#), see Table 3.
DDIS#	26	22	O	Drive Disable Output. This pin goes to a logic 0 whenever the host CPU is reading data from the 850. It can control the direction of a data bus transceiver between the CPU and 850 or other logic functions. If 16 bit bus mode is selected, this pin becomes D12. During PC Mode, this pin becomes LPT2#.
OP2#	35	31	O	Output Port 2. General purpose output. During PC Mode, this pin becomes S3.
PC MODE INTERFACE SIGNALS. CONNECT SEL PIN TO GND TO SELECT PC MODE.				
A3	25	20	I	Address-3 Select Bit. This pin is used as the 4th address line to decode the COM1-4 and LPT ports. See Table 1 for details. During Intel Bus Mode, this pin becomes IOR.
A4	12	6	I	Address-4 Select Bit. This pin is used as the 5th address line to decode the COM1-4 and LPT ports. This pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40-Pin PDIP package which operates in the Intel Bus Mode Only. See Table 1 for details. During Intel Bus Mode, this pin is inactive.
A5 A6 A7 A8	14 15 16 21	9 10 11 17	I	Address-5 thru Address-8 Select Bit. These pins are used as the 6th thru 9th address lines to decode the COM1-4 and LPT ports. See Table 1 for details. During Intel Bus Mode, A5 becomes CS0, A6 becomes CS1, A7 becomes CS2#, and A8 becomes IOW.
A9	1	37	I	Address-9 Select Bit. This pin is used as the 10th address line to decode the COM1-4 and LPT ports. This pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40-Pin PDIP package which operates in the Intel Bus Mode Only. See Table 1 for details. During Intel Bus Mode, this pin is inactive.
AEN#	28	24	I	Address Enable input (active low). When AEN# transitions to logic 0, it decodes and validates COM 1-4 ports address per S1, S2 and S3 inputs. During Intel Bus Mode, this pin becomes AS#.
S1 S2 S3	23 10 35	21 5 31	I	Select 1 to 3. These are the standard PC COM 1-4 ports and IRQ selection inputs. See Table 1 and Table 3 for details. The S1 pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40 pin PDIP packages which operates in the Intel Bus Mode Only. During Intel Bus Mode, S1 is inactive, S2 becomes RCLK, and S3 becomes OP2#.
IRQA IRQB IRQC	33 32 27	30 29 23	O	Interrupt Request A, B and C Outputs (active high, three-state). These are the interrupt outputs associated with COM 1-4 to be connected to the host data bus. See interrupt section for details. The Interrupt Requests A, B or C functions as IRQx to the PC bus. IRQx is enabled by setting MCR bit-3 to logic 1 and the desired interrupt(s) in the interrupt enable register (IER). During Intel Bus Mode, IRQA becomes INT, IRQB becomes RXRDY#, and IRQC becomes TXRDY#.
LPT1#	17	12	O	Line Printer Port-1 Decode Logic Output (active low). This pin functions as the PC standard LPT-1 printer port address decode logic output, see Table 1. The baud rate generator clock output, BAUDOUT#, is internally connected to the RCLK input in the PC mode. During Intel Bus Mode, LPT1# becomes BAUDOUT#.

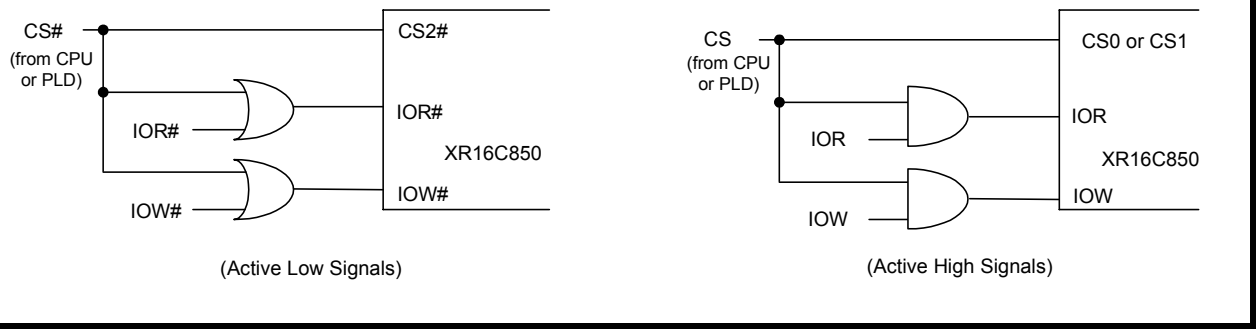
NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
LPT2#	26	22	O	Line Printer Port-2 Decode Logic Output (active low) - This pin functions as the PC standard LPT-2 printer port address decode logic output, see **Table 1**. During Intel Bus Mode, LPT2# becomes DDIS#/D12.
MODEM OR SERIAL I/O INTERFACE				
TX	13	8	O	Transmit Data or wireless infrared transmit data. This output is active low in normal standard serial interface operation (RS-232, RS-422 or RS-485) and active high in the infrared mode. Infrared mode can be enabled by connecting pin ENIR to VCC or through software selection after power up.
RX	11	7	I	Receive Data or wireless infrared receive data. Normal received data input idles at logic 1 condition and logic 0 in the infrared mode. The wireless infrared pulses are applied to the decoder. This input must be connected to its idle logic state in either normal, logic 1, or infrared mode, logic 0, else the receiver may report “receive break” and/or “error” condition(s).
RTS#	36	32	O	Request to Send or general purpose output (active low). This port may be used for automatic hardware flow control, see EFR bit-6, MCR bit-1, FCTR bits 0-1 and IER bit-6. RTS# output must be asserted before auto RTS flow control can start. If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, leave it unconnected.
CTS#	40	38	I	Clear to Send or general purpose input (active low). If used for automatic hardware flow control, data transmission will be stopped when this pin is de-asserted and will resume when this pin is asserted again. See EFR bit-7, MCR bit-2 and IER bit-7. If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
DTR#	37	33	O	Data Terminal Ready or general purpose output (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, leave it unconnected.
DSR#	41	39	I	Data Set Ready input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
CD#	42	40	I	Carrier Detect input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
RI#	43	41	I	Ring Indicator input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
ANCILLARY SIGNALS				
XTAL1	18	14	I	Crystal or external clock input. See **Figure 7** for typical oscillator connections. Caution: this input is not 5V tolerant.
XTAL2	19	15	O	Crystal or buffered clock output. See **Figure 7** for typical oscillator connections.
SEL	34	36	I	PC Mode Select (active low). When this input is at logic 0, it enables the on-board chip select decode function according to PC ISA bus COM[4:1] and IRQ[4,3] port definitions. See **Table 3** for details. This pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40 pin PDIP packages which operate in the Intel Bus Mode only.

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
OP1#/ RS485	38	34	O	Output Port 1 (General purpose output) or RS-485 Direction Control Signal. RS-485 direction control can be selected when FCTR Bit-3 is set to “1”. During data transmit cycle, RS485 pin is low. An inverter is usually required before connecting to RS-485 Transceiver.
RESET	39	35	I	Reset Input (active high). When it is asserted, the UART configuration registers are reset to default values, see **Table 15**.
VCC	44	42	Pwr	Power supply input. All inputs are 5V tolerant except for XTAL1 for devices with top mark date code of "F2 YYWW" and newer. Devices with top mark date code of "EC YYWW" and older do not have 5V tolerant inputs.
GND	22	18	Pwr	Power supply common ground.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

Factory Test Mode

For devices with top mark date code of "EC YYWW" and older devices, please note that if IOR# (or IOR) and IOW# (or IOW) are both asserted simultaneously, the 850 will enter a Factory Test Mode. The most noticeable Factory Test Mode symptom is the continuous transmission of the same character on the TX pin. This usually happens during power-up or when another device in the design requires both signals to be asserted simultaneously (like an SDRAM). A solution to this would be to OR (AND if using active-high signals) the chip selects with the read and write signals to the XR16C850 as shown below:



For devices with top mark date code of "F2 YYWW" and higher devices, the solution for the Factory Test Mode given in the figure above has been incorporated into the UART. It will only enter Factory Test Mode when all three signals (chip select, read and write) are asserted simultaneously.

1.0 PRODUCT DESCRIPTION

The XR16C850 (850) provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The XR16C850 represents such an integration with greatly enhanced features. The 850 is fabricated using an advanced CMOS process.

Enhanced Features

The 850 is an upward solution that provides 128 bytes of transmit and receive FIFO memory, instead of 32 bytes provided in the 16C650A, 16 bytes in the 16C550, or none in the 16C450. The 850 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 850 by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 128 byte FIFO in the 850, the data buffer will not require unloading/loading for 12.2 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO trigger level interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 850 provides a RS-485 half-duplex direction control signal, pin OP1#/RS485 to select the external transceiver direction. It automatically changes the state of the output pin for receive state after the last stop-bit of the last character has been shifted out of the TX shift register. Afterward, upon loading a TX data byte, it changes state of the output pin back for transmit state. The RS-485 direction control pin is not activated after reset. To activate the direction control function, the user has to set EFR Bit-4, and FCTR Bit-3 to “1”. This pin (OP1#/RS485) is high for receive state, low for transmit state.

Data Bus Interface

Two data bus interfaces are available to the user. The PC mode allows direct interconnect to the PC ISA bus while the Intel Bus Mode operates similar to the standard CPU interface available on the 16C450/550/650A. When the PC mode is selected, the external logic circuitry required for PC COM port address decode and chip select is eliminated. These functions are provided internally in the 850.

Data Rate

The 850 is capable of operation up to 1.5 Mbps with a 24 MHz crystal or external clock input with a 16X sampling clock. However, it is possible to operate up to 2.25 Mbps with a 36 MHz external clock for devices with top mark date code of "F2 YYWW" and newer, and up to 2 Mbps with a 33 MHz external clock for devices with top mark date code of "EC YYWW" and older. With a crystal of 14.7456 MHz and through a software option, the user can select data rates up to 921.6 Kbps.

The rich feature set of the 850 is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. In addition, there is a PC Mode that has two additional three state interrupt lines and one selectable open source interrupt output. The open source interrupt scheme allows multiple interrupts to be combined in a “WIRE-OR” operation, thus reducing the number of interrupt lines in larger systems. Following a power on reset or an external reset, the 850 is software compatible with previous generation of UARTs, 16C450 and 16C550 and 16C650A.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Host Data Bus Interface

The host interface is 8 data bits wide with 3 address lines and control signals to execute bus read and write transactions. The 850 supports 2 types of host interfaces: Intel and PC mode. The Intel bus interface is selected by connecting SEL to logic 1. When the SEL pin is set to a logic 1, the 850 interface is the same as industry standard 16C550. The Intel bus interconnections are shown in **Figure 3**. The special PC mode is selected when SEL is connected to logic 0. The PC mode interconnections are shown in **Figure 4**.

FIGURE 3. XR16C850 INTEL BUS INTERCONNECTIONS

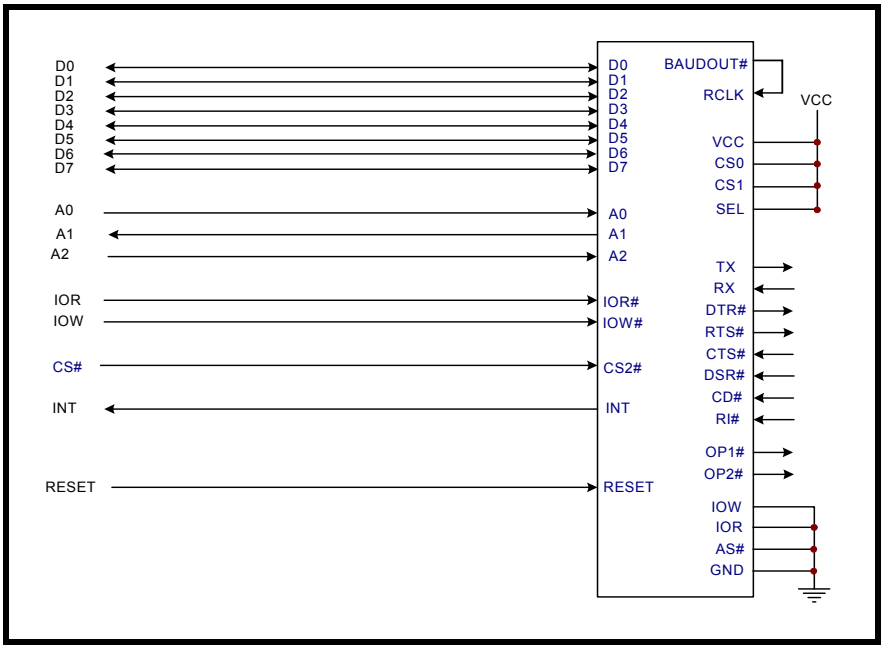
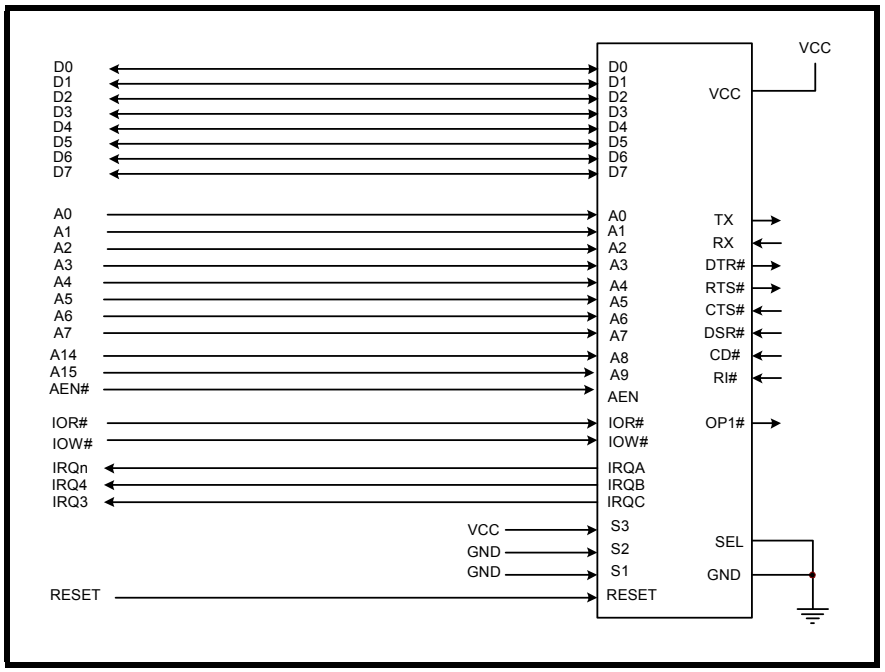


FIGURE 4. XR16C850 PC MODE INTERCONNECTIONS



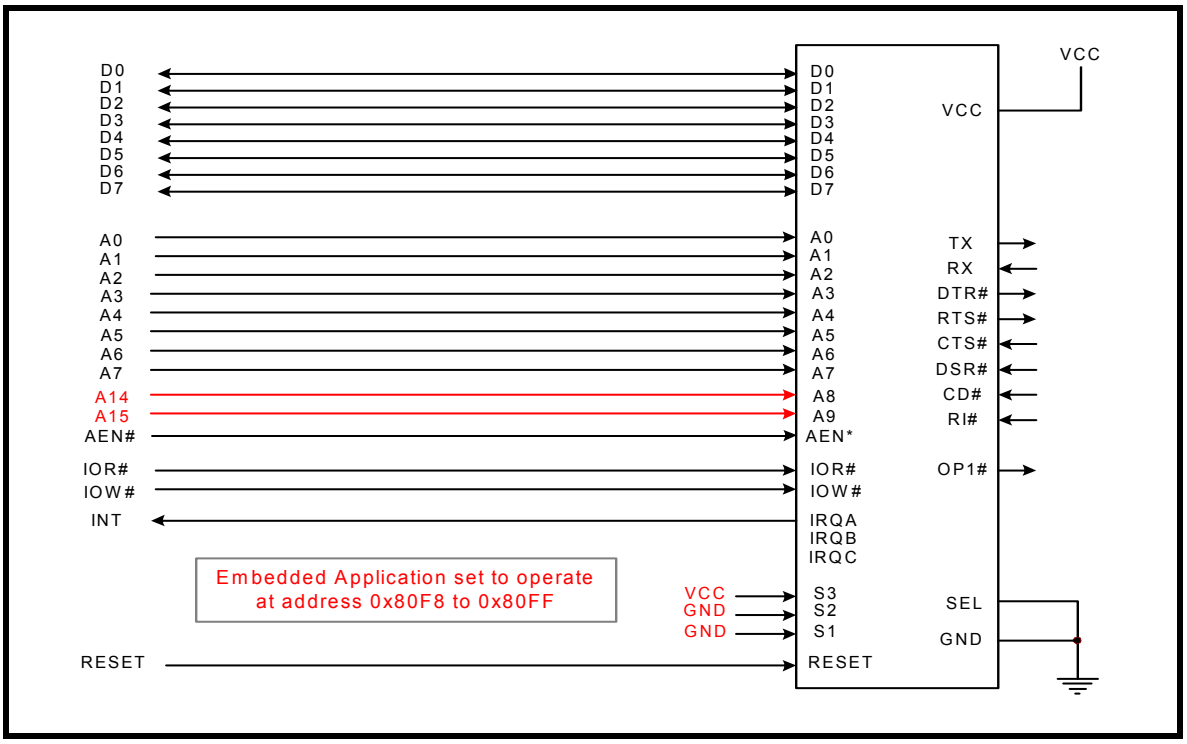
2.2 PC MODE

The PC mode interface includes an on-chip address decoder and interrupt selection function for the standard PC COM 1-4 ports addresses. The selection is made through three input signals: S1, S2 and S3. The selection summary is shown in **Table 1**. Although the on-chip address decoder was designed for PC applications ranging from 0x278 to 0x3FF, it can fit into an embedded applications by offsetting the address lines to the 850. An example is shown in **Figure 5** where the UART is operating from 0x80F8 to 0x80FF address space. Operating in the PC mode eliminates external address decode components.

TABLE 1: PC MODE INTERFACE ON-CHIP ADDRESS DECODER AND INTERRUPT SELECTION.

SEL# INPUT	S3, S2, S1 INPUTS	A3-A9 ADDRESS LINES TO ON-CHIP DECODER	COM/LPT PORT SELECTION	IRQ OUTPUT SELECTION
0	0 0 0	0x3F8 - 0x3FF	COM-1	IRQB (for PC's IRQ4)
0	0 0 1	0x2F8 - 0x2FF	COM-2	IRQC (for PC's IRQ3)
0	0 1 0	0x3E8 - 0x3EF	COM-3	IRQB (for PC's IRQ4)
0	0 0 0	0x3F8 - 0x3FF	COM-4	IRQB (for PC's IRQ4)
0	1 0 0	0x2F8 - 0x2FF	COM-1	IRQA (for PC's IRQn
0	1 0 1	0x3E8 - 0x3EF	COM-2	IRQA (for PC's IRQn)
0	1 1 0	0x2E8 - 0x2EF	COM-3	IRQA (for PC's IRQn)
0	1 1 1	0x3F8 - 0x3FF	COM-4	IRQA (for PC's IRQn)
0	X X X	0x278 - 0x27F	LPT-2	N/A
0	X X X	0x378 - 0x37F	LPT-1	N/A

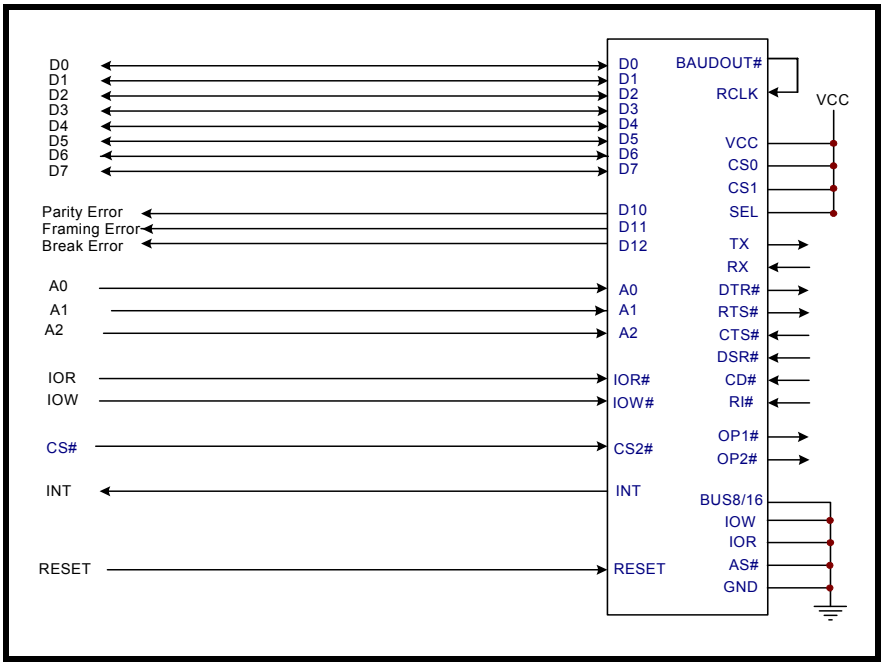
FIGURE 5. PC MODE INTERFACE IN AN EMBEDDED APPLICATION.



2.3 16-Bit Bus Interface

The 16-bit bus interface is only available on the 48 pin package. The 16-bit bus mode is enabled when the BUS8/16 pin is connected to GND. In this mode, the RX data errors can be read via the higher order data bus pins D10-D12. See Figure 6.

FIGURE 6. XR16C850 16-BIT BUS INTERFACE



2.4 5-Volt Tolerant Inputs

For devices that have top mark date code "F2 YYWW" and newer, the 850 can accept a voltage of up to 5.5V on any of its inputs (except XTAL1) when operating from 2.97V to 5.5V. XTAL1 is not 5 volt tolerant. Devices that have top mark date code "EC YYWW" and older do not have 5V tolerant inputs.

2.5 Device Reset

The RESET input resets the internal registers and the serial interface outputsto their default state (see Table 15). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.6 Device Identification and Revision

The XR16C850 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x10 for the XR16C850 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.7 Internal Registers

The 850 has a set of enhanced registers for controlling, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scractchpad register (SPR).

Beyond the general 16C550 features and capabilities, the 850 offers enhanced feature registers (EMSR, TRG, FC, FCTR, EFR, Xon/Xoff 1, Xon/Xoff 2) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, automatic RS-485 half-duplex direction output enable/disable, FIFO trigger level control, and FIFO level counters. All the register functions are discussed in full detail later in **"Section 3.0, UART INTERNAL REGISTERS" on page 25**.

2.8 DMA Mode

The DMA Mode (a legacy term) in this document does not mean "Direct Memory Access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 850 activates the interrupt output pin for each data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 850 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY# A/B	0 = 1 byte. 1 = no data.	0 = at least 1 byte in FIFO 1 = FIFO empty.	1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties.
TXRDY# A/B	0 = THR empty. 1 = byte in THR.	0 = FIFO empty. 1 = at least 1 byte in FIFO.	0 = FIFO has at least 1 empty location. 1 = FIFO is full.

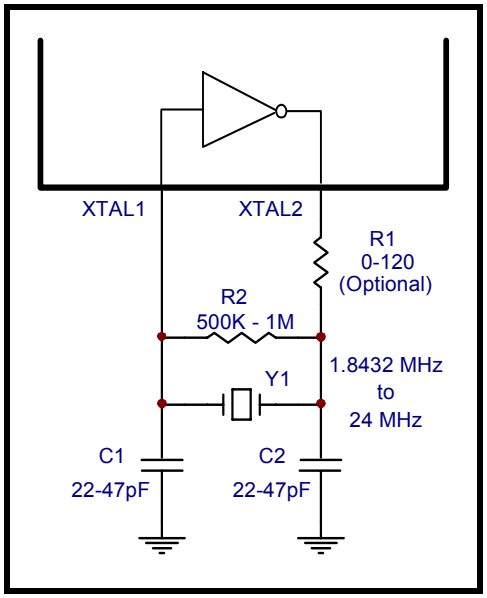
2.9 Interrupts

The output function of interrupt outputs change according to the operating bus type. During the Intel Bus Mode, the INT output will always be active high and MCR bit-3 will have no effect on the INT output pin. In the PC Mode, the IRQ outputs are in three-state mode unless MCR bit-3 and S3 are both a logic 1. **Table 3** summarizes its behavior in Intel and PC mode of operation.

TABLE 3: INTERRUPT OUTPUT FUNCTIONS

BUS MODE	MCR BIT-3	S3 (PC MODE ONLY)	INTERRUPT OUTPUT (INT OR IRQ)
Intel	X	X	Active High
PC	0	0	Three-State
	0	1	Three-State
	1	0	Three-State
	1	1	Active High

FIGURE 7. TYPICAL OSCILLATOR CONNECTIONS



2.10 Crystal Oscillator or External Clock

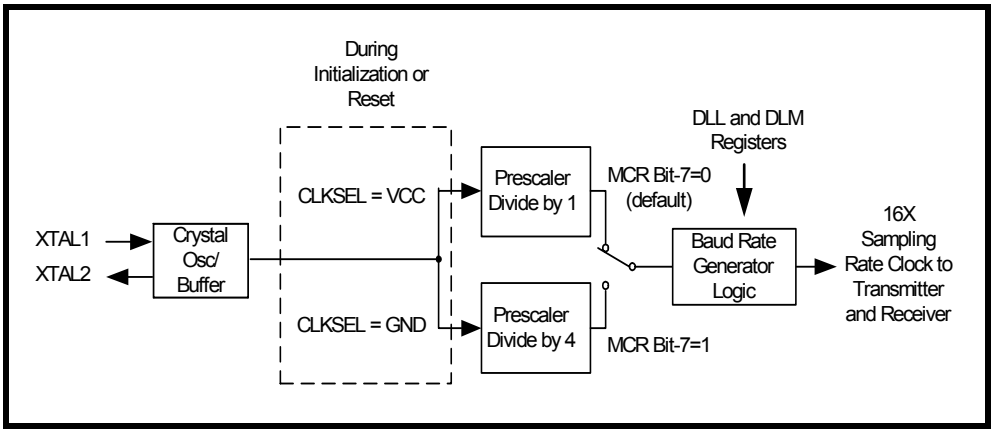
The 850 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see **"Section 2.11, Programmable Baud Rate Generator" on page 14**. To use the same clock for the receiver as used with the transmiter of the UART in the Intel bus mode, the BAUDCLK pin must be connected to the RCLK pin external to the UART.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 7**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typically, the oscillator connections are shown in **Figure 7**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.11 Programmable Baud Rate Generator

The UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up or a reset. Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 8. BAUD RATE GENERATOR



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. **Table 4** shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 4: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.12 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 128 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

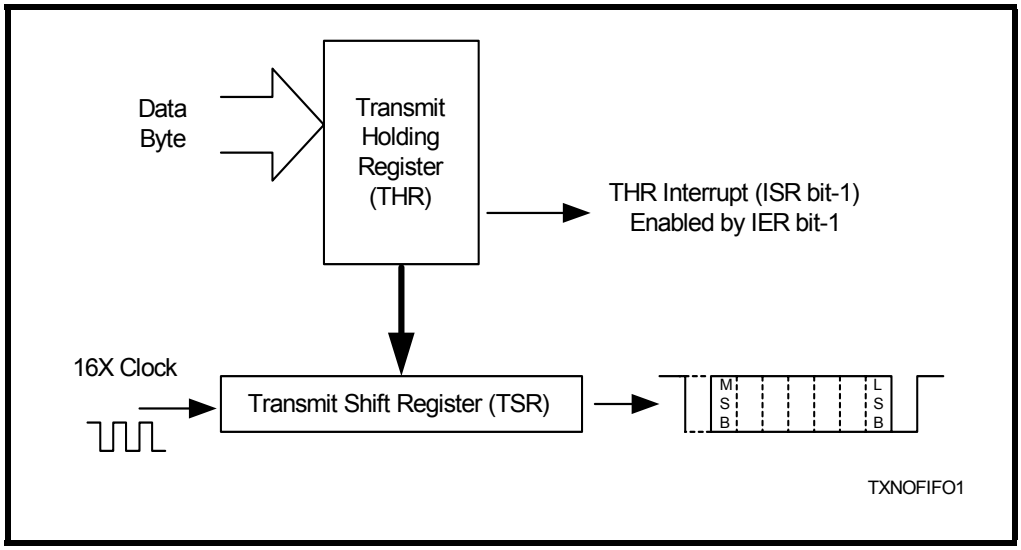
2.12.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 128 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.12.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

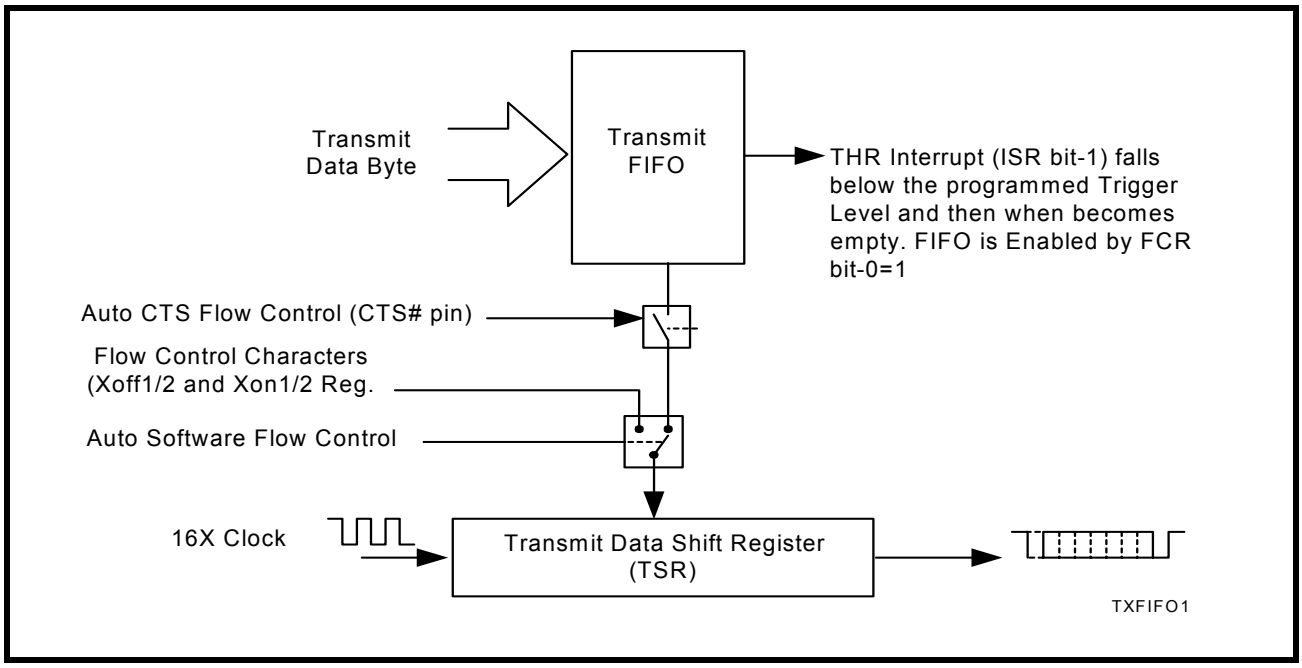
FIGURE 9. TRANSMITTER OPERATION IN NON-FIFO MODE



2.12.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 128 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 10. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.13 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 128 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.13.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 128 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 11. RECEIVER OPERATION IN NON-FIFO MODE

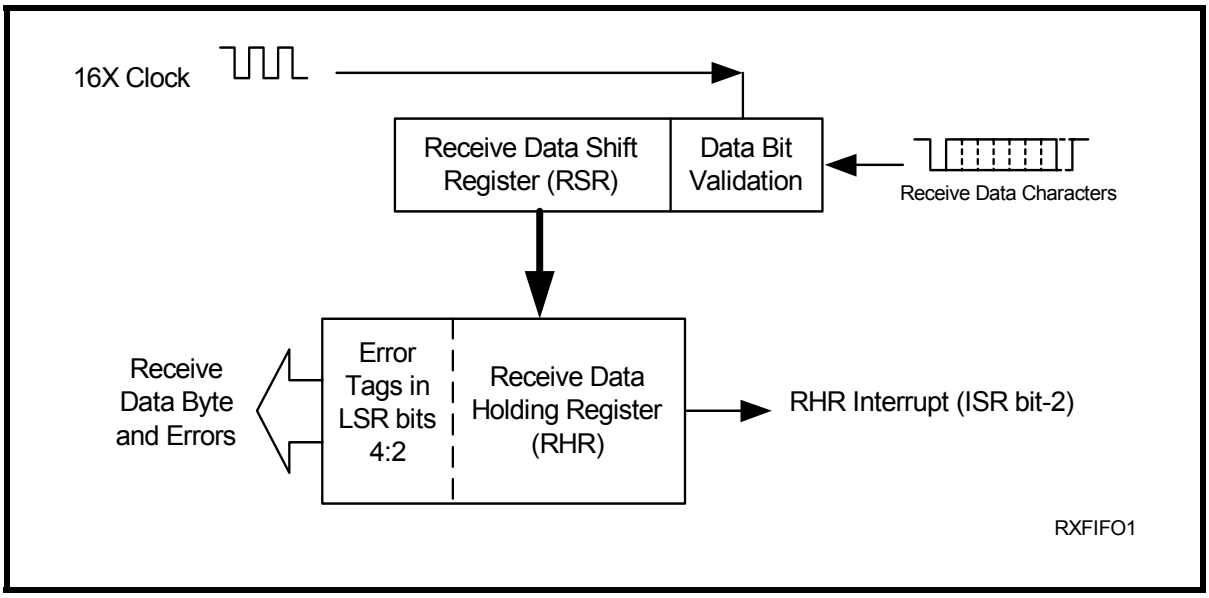
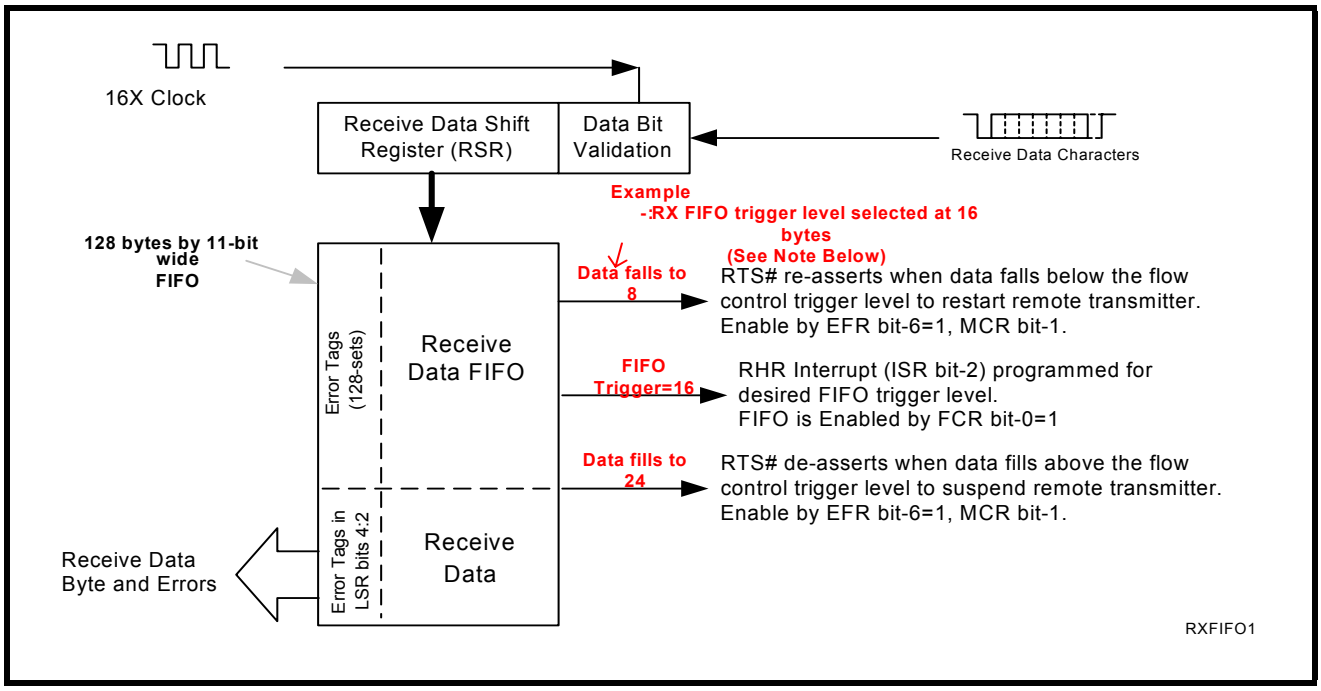


FIGURE 12. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for* **Figure 12** *(Table 10).*

2.14 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 13**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).
- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.15 Auto RTS Hysteresis

The 850 has a new feature that provides flow control trigger hysteresis while it maintains compatibility to 16C650A and 16C550. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the upper limit of the hysteresis level. The RTS# pin will return to a logic 0 after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the 850 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted to a logic 0 (RTS On). For complete details, see **Table 5**.

TABLE 5: AUTO RTS HYSTERESIS

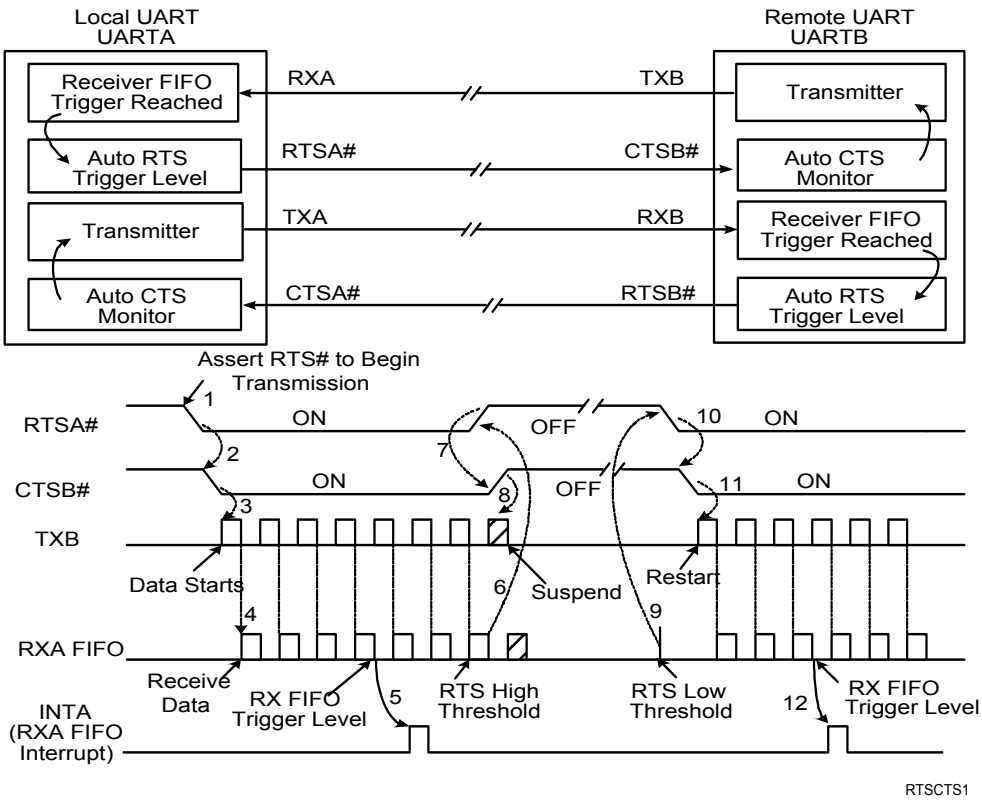
TRIGGER TABLE SELECTED (SEE TABLE 10)	FCTR BIT-1	FCTR BIT-0	TRIGGER LEVEL (CHARACTERS)	RTS HYSTERESIS (CHARACTERS)	INT PIN ACTIVATION	RTS# DE-ASSERTED (CHARACTERS)	RTS# ASSERTED (CHARACTERS)
Trigger Table-A	0	0	1	-	1	4	0
	0	0	4	-	4	8	1
	0	0	8	-	8	14	4
	0	0	14	-	14	14	8
Trigger Table-B	0	0	8	-	8	16	0
	0	0	16	-	16	24	8
	0	0	24	-	24	28	16
	0	0	28	-	28	28	24
Trigger Table-C	0	0	8	-	8	16	0
	0	0	16	-	16	56	8
	0	0	56	-	56	60	16
	0	0	60	-	60	60	56
Trigger Table-D (Programmable)	0	1	N	±4	N	N + 4	N - 4
	1	0	N	±6	N	N + 6	N - 6
	1	1	N	±8	N	N + 8	N - 8

2.16 Auto CTS (Hardware) Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 13**):

- Enable auto CTS flow control using EFR bit-7.
- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

FIGURE 13. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.17 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 14), the 850 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 850 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 850 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 850 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 14) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 850 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 850 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 850 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 850 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS Hysteresis value in **Table 5**. **Table 6** below explains this when Trigger Table-B (See **Table 10**) is selected.

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

2.18 Special Character Detect

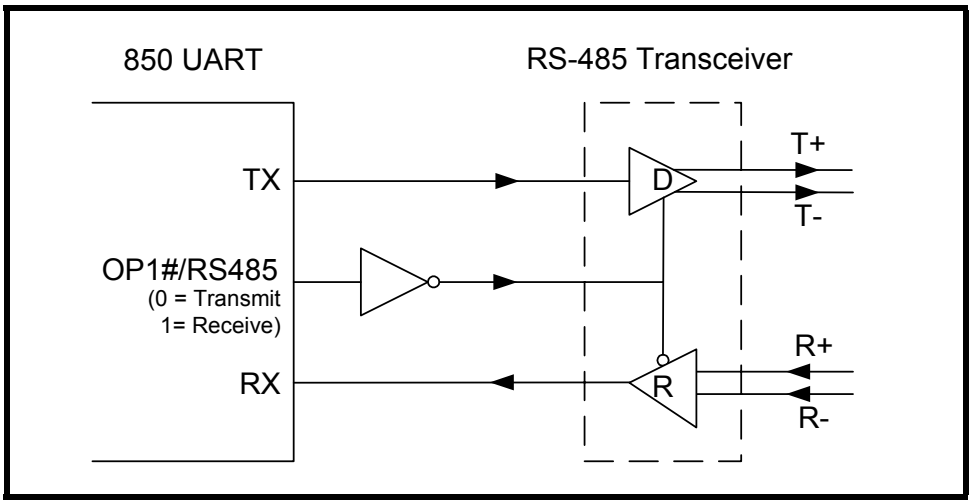
A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 850 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.19 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by MCR bit-2. It de-asserts OP1#/RS485 output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts OP1# output prior to sending the data. See **Figure 14**.

FIGURE 14. AUTO RS-485 HALF-DUPLEX CONTROL



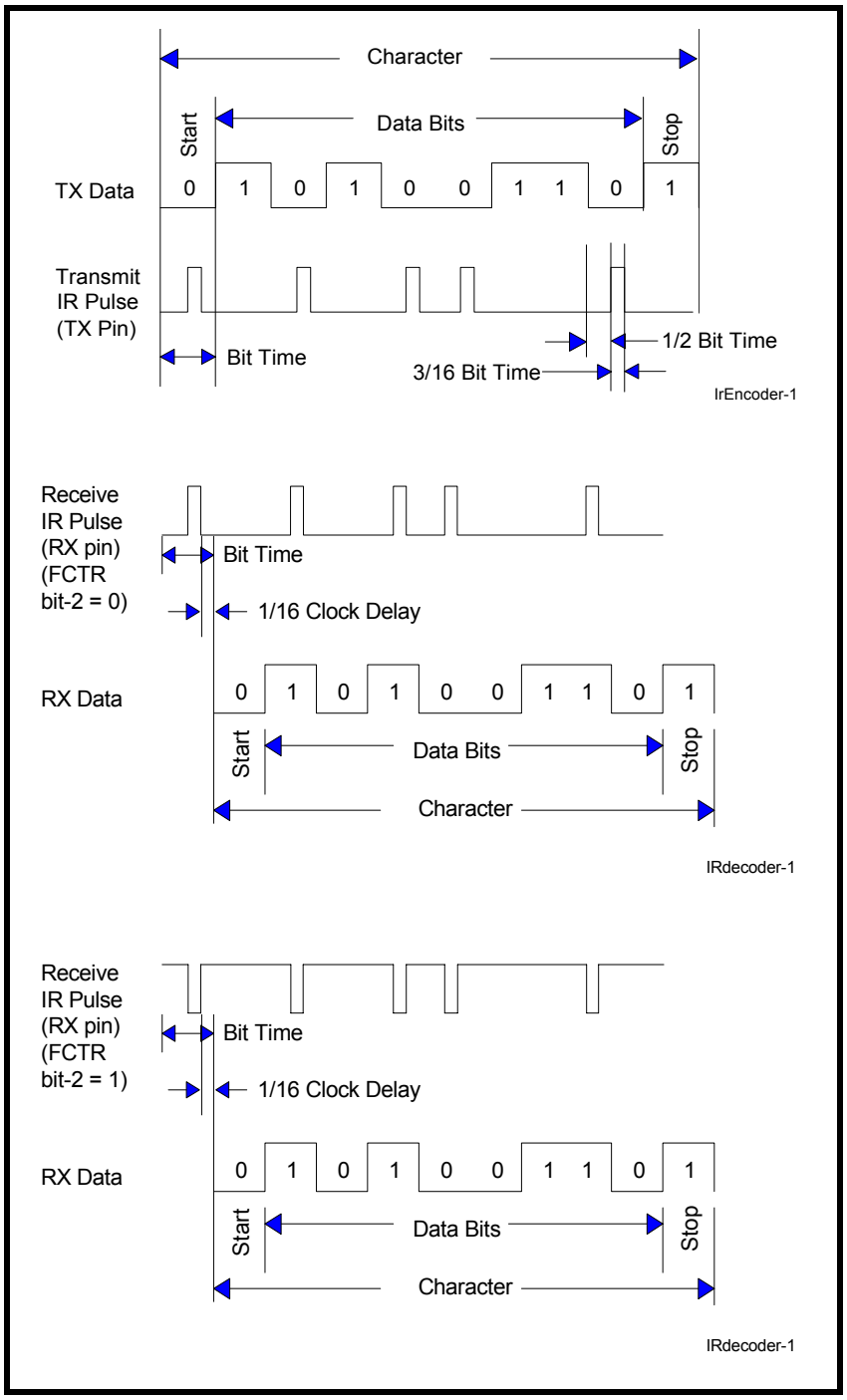
2.20 Infrared Mode

The 850 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 15**.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 15**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream. However, this is not true with some infrared modules on the market which indicate a logic 0 by a light pulse. So the 850 has a provision to invert the input polarity to accomodate this. In this case, the user can enable FCTR bit-2 to invert the incoming infrared RX signal.

FIGURE 15. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.21 Sleep Mode with Auto Wake-Up

The 850 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 850 to enter sleep mode:

- no interrupts pending for the 850 (ISR bit-0 = 1)
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin is idling at a logic 1

The 850 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 850 resumes normal operation by any of the following:

- a receive data start bit transition (logic 1 to 0)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 850 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 850 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The 850 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

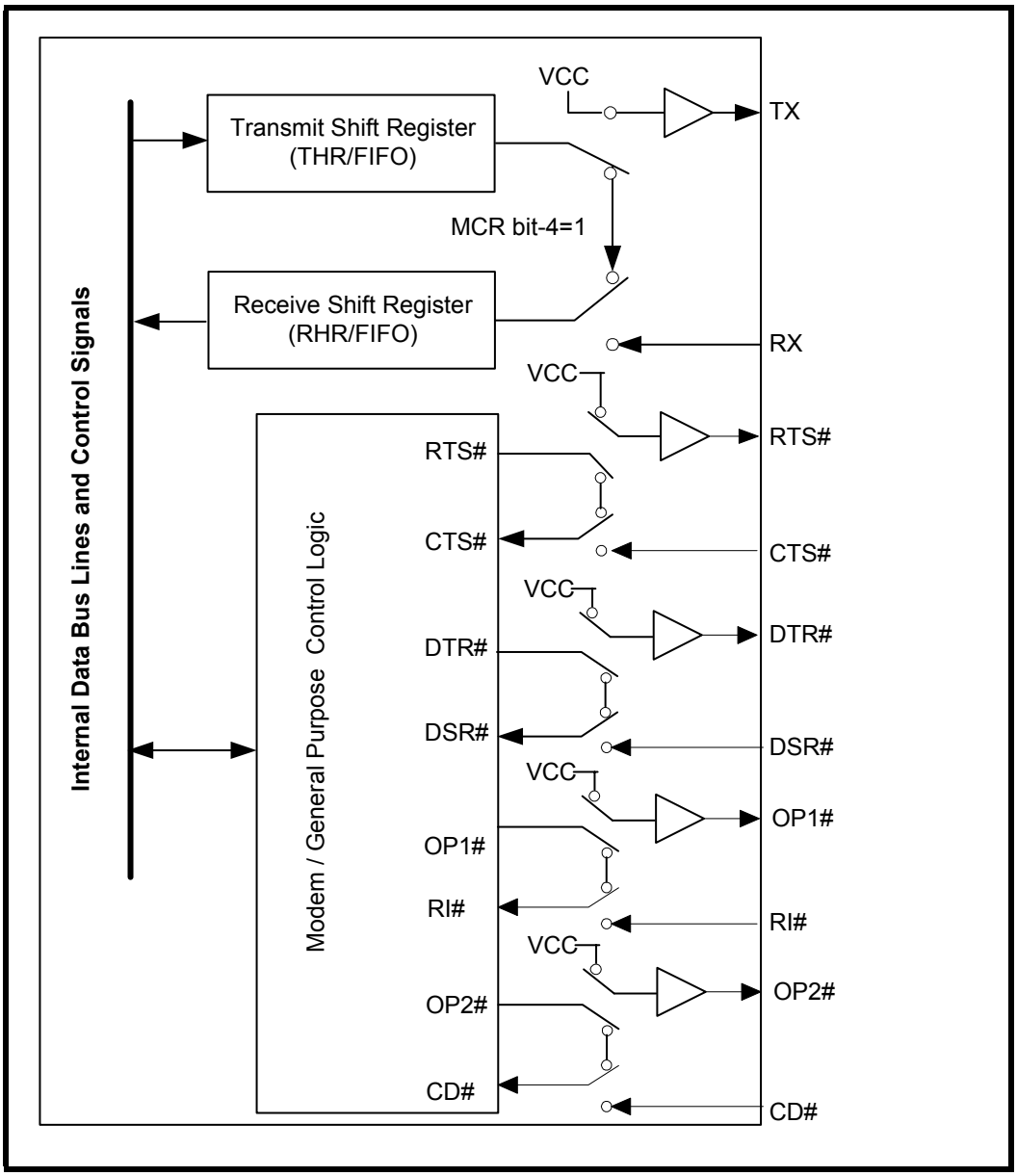
If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, and modem input lines remain steady when the 850 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 42. If the input lines are floating or are toggling while the 850 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX input is idling at logic 1 or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on the RX input.

2.22 Internal Loopback

The 850 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 16 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 16. INTERNAL LOOPBACK



3.0 UART INTERNAL REGISTERS

The 850 has a set of configuration registers selected by address lines A0, A1 and A2. The 16C550 compatible registers can be accessed when LCR[7] = 0 and the baud rate generator divisor registers can be accessed when LCR[7] = 1 and LCR ≠ 0xBF. The enhanced registers are accessible only when LCR = 0xBF. The complete register set is shown on Table 7 and Table 8.

TABLE 7: XR16C850 UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Div Latch High Byte	Read/Write	
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR[7] = 0, FCTR[6] = 0
1 1 1	FLVL - TX/RX FIFO Level Counter Register	Read-only	LCR[7] = 0, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	
ENHANCED REGISTERS			
0 0 0	TRG - TX/RX FIFO Trigger Level Reg FC - TX/RX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Reg	Read/Write	
0 1 0	EFR - Enhanced Function Reg	Read/Write	
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

.

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS# Int. Enable	0/ RTS# Int. Enable	0/ Xoff Int.. Enable	0/ Sleep Mode Enable	Modem Status Int. Enable	RX Line Status- Int. Enable	TX Empty Int. Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7] = 0
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres- caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	OP2#/ INT Output Enable	OP1#/ Auto RS485 Output	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over- run Error	RX Data Ready	LCR[7] = 0
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 0 FCTR[6]=0
1 1 1	EMSR	WR	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	RX/TX FIFO Count	RX/TX FIFO Count	LCR[7] = 0 FCTR[6]=1
1 1 1	FLVL	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR ≠ 0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	1	0	0	0	0	
Enhanced Registers											
0 0 0	TRG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX Mode	SCPAD Swap	Trig Table Bit-1	Trig Table Bit-0	Auto RS485 Direction Control	RX IR Input Inv.	Auto RTS Hyst Bit-1	Auto RTS Hyst Bit-0	
0 1 0	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5]	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 16.

4.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 15.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16C850 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated. Reading ISR will clear this interrupt. It is not necessary to disable this interrupt by setting IER bit-1 = 0. The UART will automatically issue this interrupt again when more data is loaded into the FIFO and the FIFO level drops below the trigger level and/or it becomes empty.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from low to high.

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, **Table 9**, shows the data values (bits 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto RS-485 control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS# is when its transmitter toggles the input pin (from low to high) during auto CTS flow control enabled by EFR bit-7.
- RTS# is when its receiver toggles the output pin (from low to high) during auto RTS flow control enabled by EFR bit-6.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register (but flags and tags not cleared until character(s) that generated the interrupt(s) has been emptied or cleared from FIFO).
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR until empty.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared by a read to ISR or when Xon character(s) is received.
- Special character interrupt is cleared by a read to ISR or after the next character is received.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.

TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[5:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See **Table 9**). See **"Section 4.4.1, Interrupt Generation:" on page 29** and **"Section 4.4.2, Interrupt Clearing:" on page 29** for details.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Transmit FIFO Trigger Select

(logic 0 = default, TX trigger level = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. **Table 10** below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

The FCTR Bits 5-4 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. **Table 10** shows the complete selections.

TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-5	FCTR BIT-4	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table-A	0	0			0	0		1 (default)	16C550, 16C2550, 16C2552, 16C554, 16C580
			0	0			1 (default)		
			0	1			4		
			1	0			8		
			1	1			14		
Table-B	0	1			0	0		16	16C650A
					0	1		8	
					1	0		24	
					1	1		30	
			0	0			8		
			0	1			16		
			1	0			24		
			1	1			28		
Table-C	1	0			0	0		8	16C654
					0	1		16	
					1	0		32	
					1	1		56	
			0	0			8		
			0	1			16		
			1	0			56		
			1	1			60		
Table-D	1	1	X	X	X	X	Programmable via TRG register. FCTR[7] = 0.	Programmable via TRG register. FCTR[7] = 1.	16L2752, 16L2750, 16C2852, 16C854, 16C864

4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See **Table 11** for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR[5] = logic 0, parity is not forced (default).
- LCR[5] = logic 1 and LCR[4] = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR[5] = logic 1 and LCR[4] = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 11: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: OP1# Output/Auto RS485 Control

OP1# is a general purpose output. If Auto RS-485 mode is enabled, this works as the half-duplex direction control output. See FCTR[3] for more details.

- Logic 0 = OP1# output is at logic 1.
- Logic 1 = OP1# output is at logic 0.

MCR[3]: OP2# or IRQn Enable during PC Mode

OP2# is a general purpose output available during the Intel bus interface mode of operation. In the PC bus mode, this bit enables the IRQn operation. See PC Mode section and IRQn pin description. The OP2# output is not available in the PC Mode.

During Intel Bus Mode Operation:

- Logic 0 = Sets OP2# output to a logic 1 (default).
- Logic 1 = Sets OP2# output to a logic 0.

During PC Mode Operation:

See Table 3 for more details.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and **Figure 16**.

MCR[5]: Xon-Any Enable

- Logic 0 = Disable Xon-Any function (for 16C550 compatibility, default).
- Logic 1 = Enable Xon-Any function. In this mode, any RX character received will resume transmit operation. The RX character will be loaded into the RX FIFO , unless the RX character is an Xon or Xoff character and the 850 is programmed to use the Xon/Xoff flow control.

MCR[6]: Infrared Encoder/Decoder Enable

- Logic 0 = Enable the standard modem receive and transmit input/output interface (default).
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. While in this mode, the infrared TX output will be a logic 0 during idle data conditions.

MCR[7]: Clock Prescaler Select

This bit overrides the CLKSEL pin selection available on the 48 and 52 pin packages. See Figure 8.

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one fourth.

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is set to a logic 1, an LSR interrupt will be generated immediately when any character in the RX FIFO has an error (parity, framing, overrun, break).

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Error Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error. If IER bit-2 is set, an interrupt will be generated immediately.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Error Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, “mark” or logic 1.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A logic 1 on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a logic 0 will resume data transmission. Normally MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

DSR# (active high, logical 1). Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

RI# (active high, logical 1). Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

CD# (active high, logical 1). Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.10 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.11 Enhanced Mode Select Register (EMSR)

This register replaces SPR (during a Write) and is accessible only when FCTR[6] = 1.

EMSR[1:0]: Receive/Transmit FIFO Count (Write-Only)

When Scratchpad Swap (FCTR[6]) is asserted, EMSR bits 1-0 controls what mode the FIFO Level Counter is operating in.

TABLE 12: SCRATCHPAD SWAP SELECTION

FCTR[6]	EMSR[1]	EMSR[0]	Scratchpad is
0	X	X	Scratchpad
1	0	0	RX FIFO Counter Mode
1	0	1	TX FIFO Counter Mode
1	1	0	RX FIFO Counter Mode
1	1	1	Alternate RX/TX FIFO Counter Mode

During Alternate RX/TX FIFO Counter Mode, the first value read after EMSR bits 1-0 have been asserted will always be the RX FIFO Counter. The second value read will correspond with the TX FIFO Counter. The next value will be the RX FIFO Counter again, then the TX FIFO Counter and so on and so forth.

EMSR[7:2]: Reserved

4.12 FIFO Level Register (FLVL) - Read-Only

The FIFO Level Register replaces the Scratchpad Register (during a Read) when FCTR[6] = 1. Note that this is not identical to the FIFO Data Count Register which can be accessed when LCR = 0xBF.

FLVL[7:0]: FIFO Level Register

This register provides the FIFO counter level for the RX FIFO or the TX FIFO or both depending on EMSR[1:0]. See Table 12 for details.

4.13 Baud Rate Generator Registers (DLL and DLM) - Read/Write

The concatenation of the contents of DLM and DLL gives the 16-bit divisor value which is used to calculate the baud rate:

- Baud Rate = (Clock Frequency / 16) / Divisor

See MCR bit-7 and the baud rate table also.

4.14 Device Identification Register (DVID) - Read Only

This register contains the device ID (0x10 for XR16C850). Prior to reading this register, DLL and DLM should be set to 0x00.

4.15 Device Revision Register (DREV) - Read Only

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00.

4.16 Trigger Level / FIFO Data Count Register (TRG) - Write-Only

User Programmable Transmit/Receive Trigger Level Register.

TRG[7:0]: Trigger Level Register

These bits are used to program desired trigger levels when trigger Table-D is selected. FCTR bit-7 selects between programming the RX Trigger Level (a logic 0) and the TX Trigger Level (a logic 1).

4.17 FIFO Data Count Register (FC) - Read-Only

This register is accessible when LCR = 0xBF. Note that this register is not identical to the FIFO Level Register which is located in the general register set when FCTR bit-6 = 1.

FC[7:0]: FIFO Data Count Register

Transmit/Receive FIFO Count. Number of characters in Transmit (FCTR[7] = 1) or Receive FIFO (FCTR[7] = 0) can be read via this register.

4.18 Feature Control Register (FCTR) - Read/Write

This register controls the XR16C2850 new functions that are not available in ST16C550 or ST16C650A.

FCTR[1:0]: Auto RTS Hysteresis

User selectable RTS# hysteresis levels for hardware flow control application. After reset, these bits are set to "0" to select the next trigger level for hardware flow control. See Table 5 for more details.

FCTR[2]: IrDa RX Inversion

- Logic 0 = Select RX input as encoded IrDa data (Idle state will be logic 0).
- Logic 1 = Select RX input as inverted encoded IrDa data (Idle state will be logic 1).

FCTR[3]: Auto RS-485 Direction Control

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register becomes empty and transmit shift register is shifting data out.
- Logic 1 = Enable Auto RS485 Direction Control function. The direction control signal, RS485 pin, changes its output logic state from low to high one bit time after the last stop bit of the last character is shifted out. Also, the Transmit interrupt generation is delayed until the transmitter shift register becomes empty. The RS485 output pin will automatically return to a logic low when a data byte is loaded into the TX FIFO.

FCTR[5:4]: Transmit/Receive Trigger Table Select

See Table 10 for more details.

TABLE 13: TRIGGER TABLE SELECT

FCTR BIT-5	FCTR BIT-4	TABLE
0	0	Table-A (TX/RX)
0	1	Table-B (TX/RX)
1	0	Table-C (TX/RX)
1	1	Table-D (TX/RX)

FCTR[6]: Scratchpad Swap

- Logic 0 = Scratch Pad register is selected as general read and write register. ST16C550 compatible mode.
- Logic 1 = FIFO Count register (Read-Only), Enhanced Mode Select Register (Write-Only). Number of characters in transmit or receive FIFO can be read via scratch pad register when this bit is set. Enhanced Mode Select Register is selected when it is written into.

FCTR[7]: Programmable Trigger Register Select

- Logic 0 = Registers TRG and FC selected for RX.
- Logic 1 = Registers TRG and FC selected for TX.

4.19 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see **Table 14**). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Single character and dual sequential characters software flow control is supported. Combinations of software flow control can be selected by programming these bits.

TABLE 14: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3 CONT-3	EFR BIT-2 CONT-2	EFR BIT-1 CONT-1	EFR BIT-0 CONT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit of the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]= '10') then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]= '01') then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt, if enabled via IER bit-5.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts to a logic 1 at the next upper trigger level or hysteresis level. RTS# will return to a logic 0 when FIFO data falls below the next lower trigger level. The RTS# output must be asserted (logic 0) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled (default).
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled (default).
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts to logic 1. Data transmission resumes when CTS# returns to a logic 0.

4.20 Software Flow Control Registers (XOFF1, XOFF2, XON1, XON2) - Read/Write

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see Table 6.

TABLE 15: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0xXX
DLM	Bits 7-0 = 0xXX
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
EMSR	Bits 7-0 = 0x00
FLVL	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
FC	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX	Logic 1
OP1#	Logic 1 (Intel Bus Mode)
OP2#	Logic 1
RTS#	Logic 1
DTR#	Logic 1
RXRDY#	Logic 1 (Intel Bus Mode) Three-State Condition (PC Mode)
TXRDY#	Logic 0 (Intel Bus Mode) Three-State Condition (PC Mode)
INT	Logic 0 (Intel Bus Mode) Three-State Condition (PC Mode)

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	GND-0.3 V to 7 V
Operating Temperature	-40^{O} to +85^{O}C
Storage Temperature	-65^{O} to +150^{O}C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA *(MARGIN OF ERROR: ± 15%)*

Thermal Resistance (48-TQFP)	theta-ja =59^{O}C/W, theta-jc = 16^{O}C/W
Thermal Resistance (44-PLCC)	theta-ja = 50^{O}C/W, theta-jc = 21^{O}C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC = 2.97V TO 5.5V

SYMBOL	PARAMETER	LIMITS 3.3V		LIMITS 5.0V		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{ILCK}	Clock Input Low Level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock Input High Level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage (top mark date code of "EC YYWW" and older)	2.0	VCC	2.2	VCC	V	
V_{IH}	Input High Voltage (top mark date code of "F2 YYWW and newer)	2.0	5.5	2.2	5.5	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 6 mA
V_{OL}	Output Low Voltage		0.4			V	I_{OL} = 4 mA
V_{OH}	Output High Voltage			2.4		V	I_{OH} = -6 mA
V_{OH}	Output High Voltage	2.0				V	I_{OH} = -1 mA
I_{IL}	Input Low Leakage Current		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		2.7		4	mA	
I_{SLEEP}	Sleep Current		30		50	uA	See Test 1

Test 1: The following inputs should remain steady at VCC or GND state to minimize sleep current: A0-A2, D0-D7, IOR#, IOW#, CS# and modem inputs. Also, RX input must idle at logic 1 state while in sleep mode. In mixed voltage environments, where the voltage at any of the inputs of the 651 is lower than its VCC supply voltage, the sleep current will be higher than the maximum values given here.

AC ELECTRICAL CHARACTERISTICS

TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3V		LIMITS 5.0V		UNIT
		MIN	MAX	MIN	MAX	
CLK	Clock Pulse Duration	45		30		ns
OSC	Crystal Frequency (top mark date code "EC YYWW" and older)		8		24	MHz
OSC	Crystal Frequency (top mark date code "F2 YYWW" and newer)		16		24	MHz
OSC	External Clock Frequency (top mark date code "EC YYWW" and older)		22		33	MHz
OSC	External Clock Frequency (top mark date code "F2 YYWW" and newer)		22		36	MHz
TAS	Address Setup Time (AS# tied to GND)	5		0		ns
TAH	Address Hold Time (AS# tied to GND) (top mark date code of "EC YYWW" and older)	10		5		ns
TAH	Address Hold Time (AS# tied to GND) (top mark date code of "F2 YYWW" and newer)	0		0		ns
TCS	Chip Select Width	75		50		ns
TRD	IOR# Strobe Width	75		50		ns
TDY	Read/Write Cycle Delay	75		50		ns
TRDV	Data Access Time		35		25	ns
TDD	Data Disable Time	0	25	0	15	ns
TWR	IOW# Strobe Width	75		50		ns
TDS1	Data Setup Time (AS# tied to GND)	20		15		ns
TDH1	Data Hold Time (AS# tied to GND)	5		5		ns
T_{ASW}	Address Strobe Width	75		50		ns
T_{AS1}	Address Setup Time (AS# used)	5		5		ns
T_{AH1}	Address Hold Time (AS# used)	10		5		ns
T_{AS2}	Address Setup Time (AS# used)	5		5		ns
T_{AH2}	Address Hold Time (AS# used)	10		5		ns
T_{CS1}	Delay from Chip Select to AS#	5		5		ns
T_{CSH}	Delay from AS# to Chip Select	10		5		ns
T_{CS2}	Delay from AS# to Chip Select	5		5		ns
T_{RD1}	Delay from AS# to Read	10		5		ns

AC ELECTRICAL CHARACTERISTICS

TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.97V TO 5.5V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 3.3V		LIMITS 5.0V		UNIT
		MIN	MAX	MIN	MAX	
T_{RD2}	Delay from Chip Select to IOR#	10		5		ns
T_{DIS}	Delay from IOR# to DDIS#	20		10		ns
T_{WR1}	Delay from AS# to IOW#	10		5		ns
T_{DS2}	Data Setup Time (AS# used)	20		15		ns
T_{DH2}	Data Hold Time (AS# used)	5		5		ns
T_{AS3}	Address Setup Time (PC Mode)	10		5		ns
T_{RD3}	Delay from AEN# to IOR#	10		5		ns
T_{RD4}	Delay from IOR# to AEN#	10		5		ns
T_{WR2}	Delay from AEN# to IOW#	10		5		ns
T_{WR3}	Delay from IOW# to AEN#	5		5		ns
T_{DS3}	Data Setup Time (PC Mode)	20		15		ns
T_{DH3}	Data Hold Time (PC Mode)	5		5		ns
TWDO	Delay From IOW# To Output		75		50	ns
TMOD	Delay To Set Interrupt From MODEM Input		75		50	ns
TRSI	Delay To Reset Interrupt From IOR#		75		50	ns
TSSI	Delay From Stop To Set Interrupt		1		1	Bclk
TRRI	Delay From IOR# To Reset Interrupt		75		50	ns
TSI	Delay From Stop To Interrupt		75		50	ns
TINT	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
TWRI	Delay From IOW# To Reset Interrupt		75		50	ns
TSSR	Delay From Stop To Set RXRDY#		1		1	Bclk
TRR	Delay From IOR# To Reset RXRDY#		75		50	ns
TWT	Delay From IOW# To Set TXRDY#		75		50	ns
TSRT	Delay From Center of Start To Reset TXRDY#		8		8	Bclk
TRST	Reset Pulse Width	40		40		ns
N	Baud Rate Divisor	1	2^{16}-1	1	2^{16}-1	-
Bclk	Baud Clock	16X				Hz

FIGURE 17. CLOCK TIMING

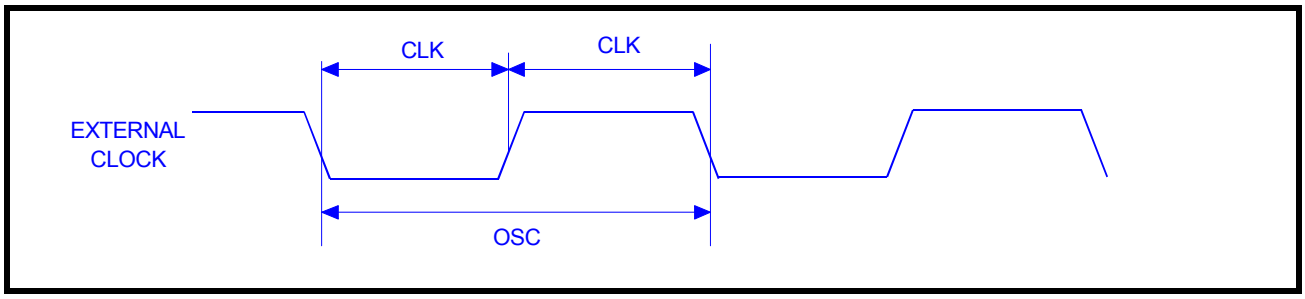


FIGURE 18. MODEM INPUT/OUTPUT TIMING

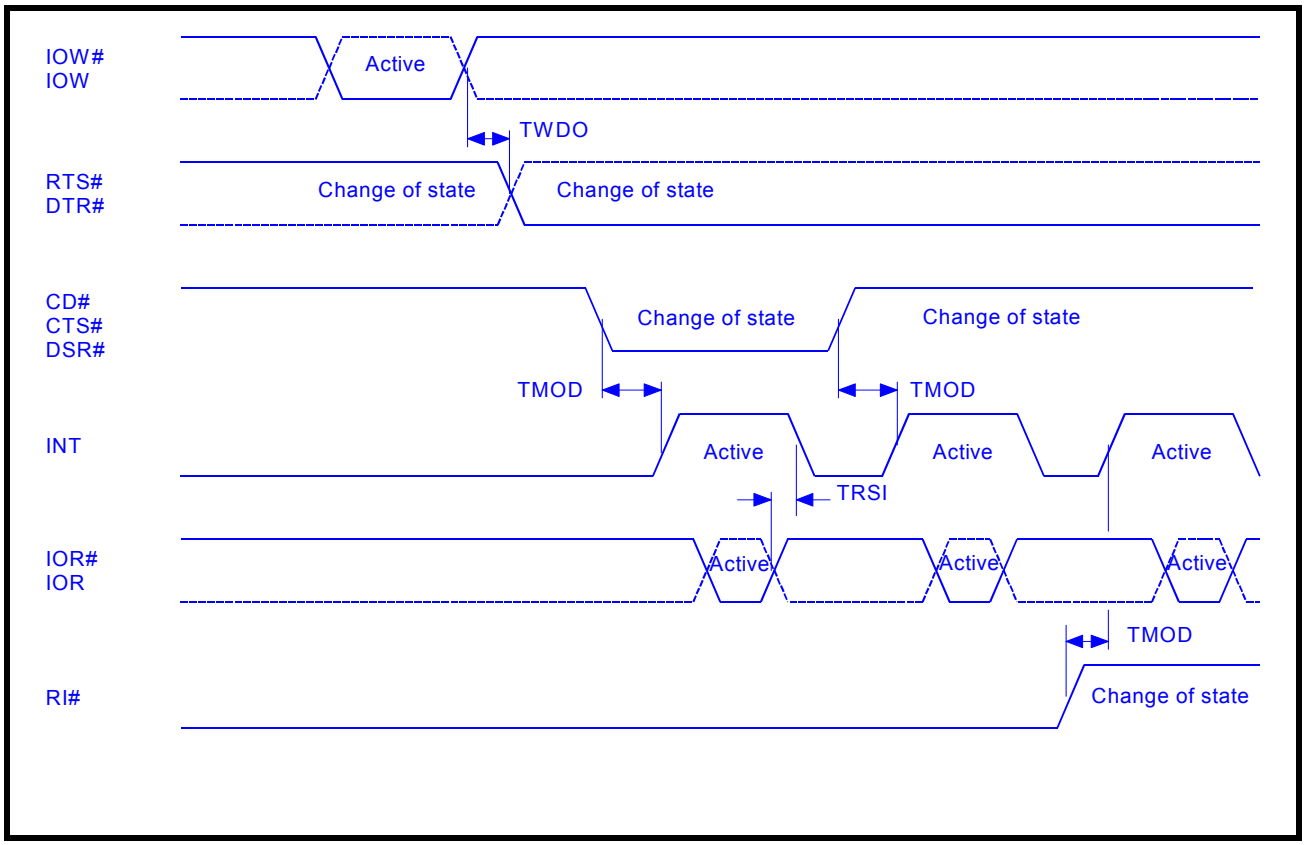
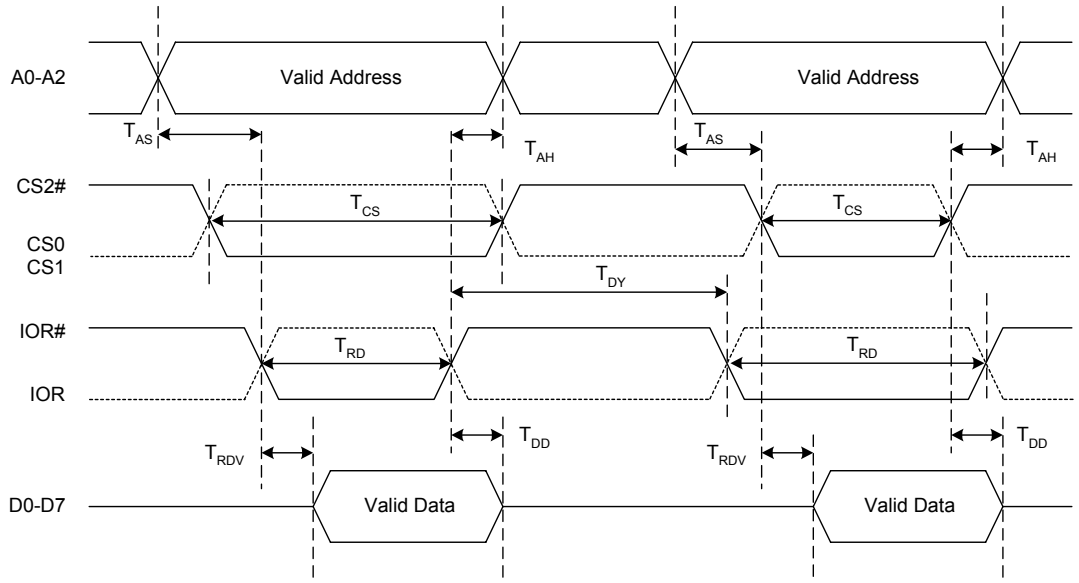
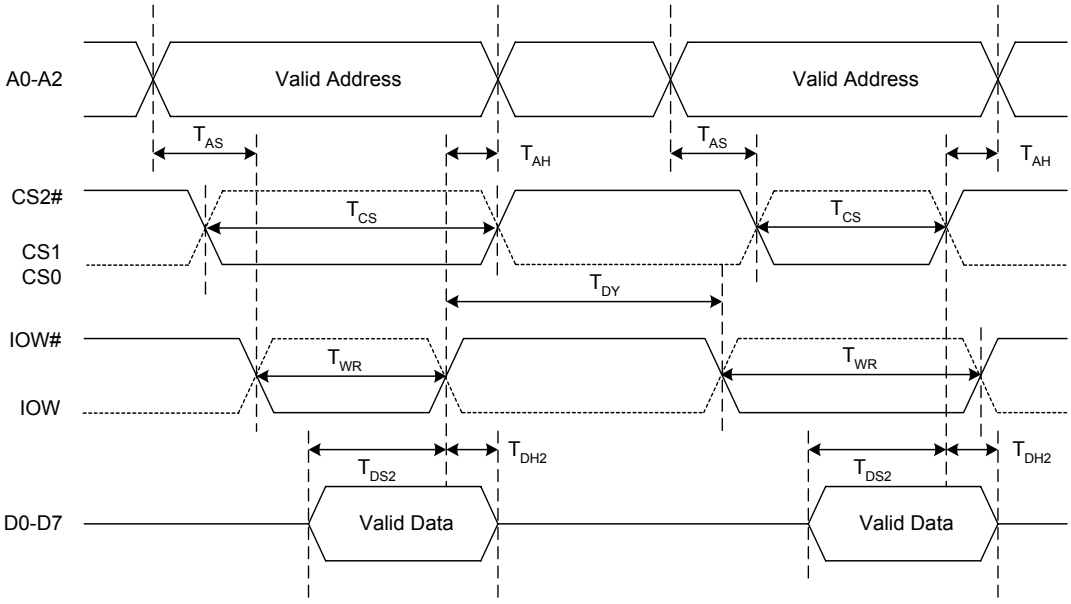


FIGURE 19. DATA BUS READ TIMING IN INTEL BUS MODE WITH AS# TIED TO GND



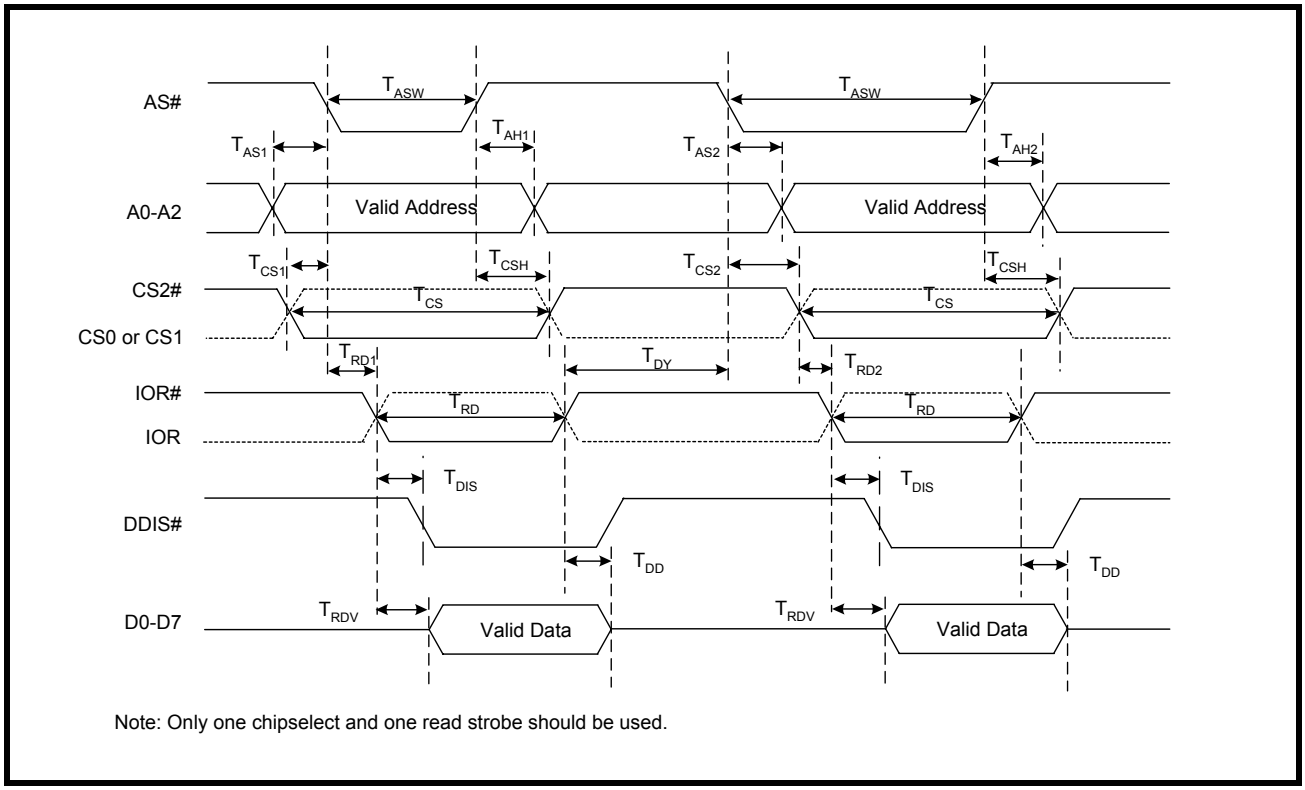
Note: Only one chipselect and one read strobe should be used.

FIGURE 20. DATA BUS WRITE TIMING IN INTEL BUS MODE WITH AS# TIED TO GND



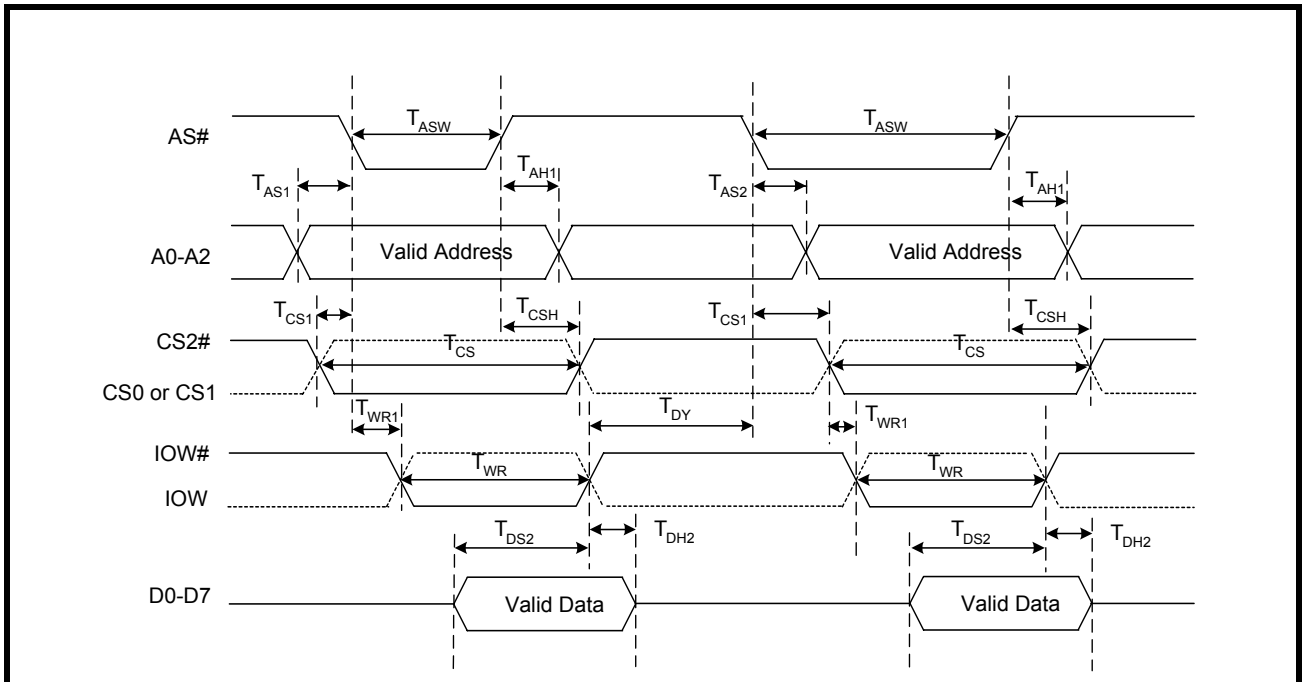
Note: Only one chipselect and one write strobe should be used.

FIGURE 21. DATA BUS READ TIMING IN INTEL BUS MODE USING AS#



Note: Only one chipselect and one read strobe should be used.

FIGURE 22. DATA BUS WRITE TIMING IN INTEL BUS MODE USING AS#



Note: Only one chipselect and one write strobe should be used.

FIGURE 23. DATA BUS READ TIMING IN PC MODE

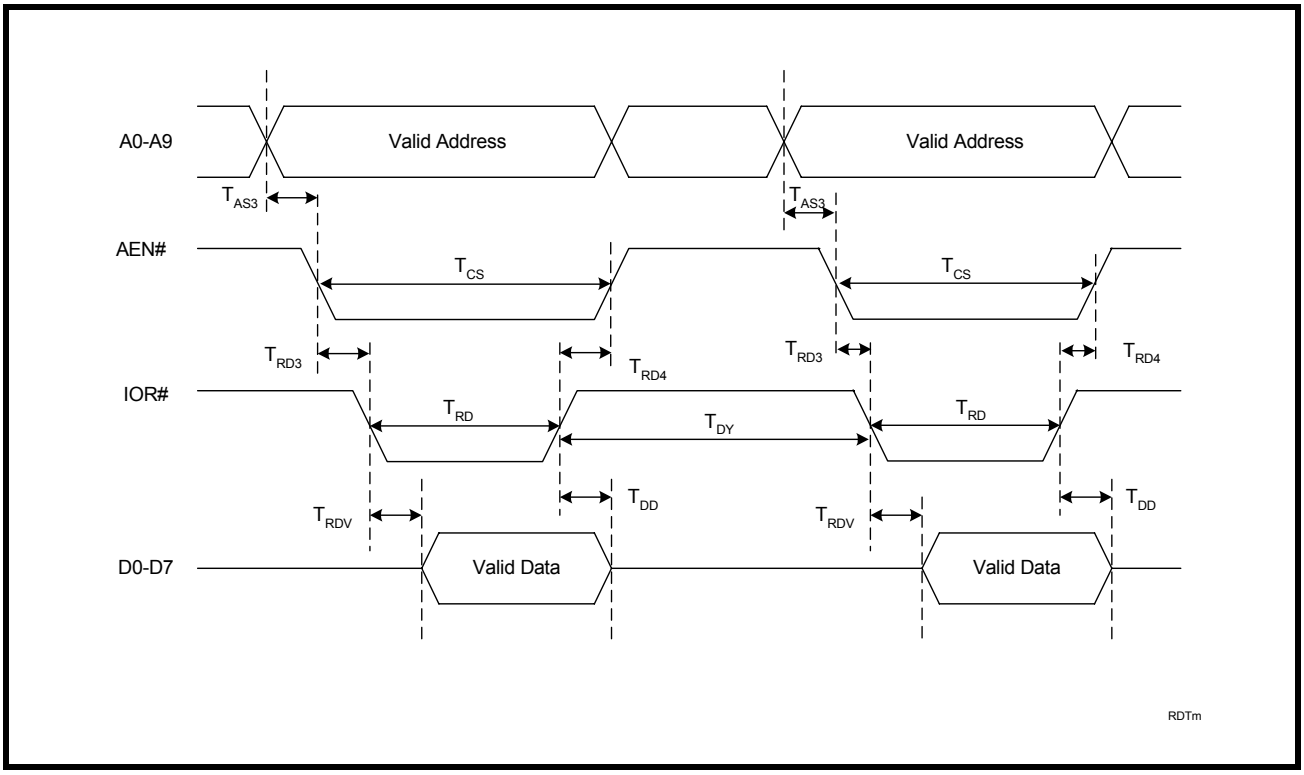


FIGURE 24. DATA BUS WRITE TIMING IN PC MODE

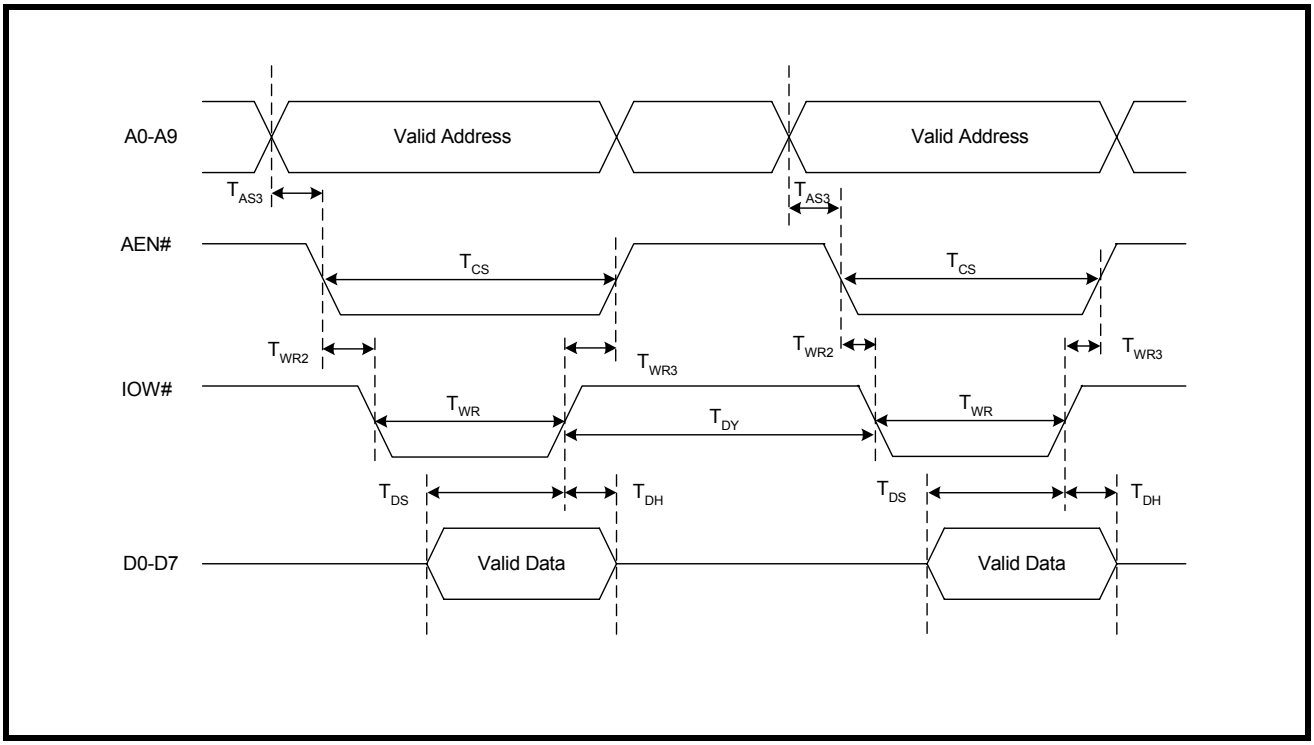


FIGURE 25. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE]

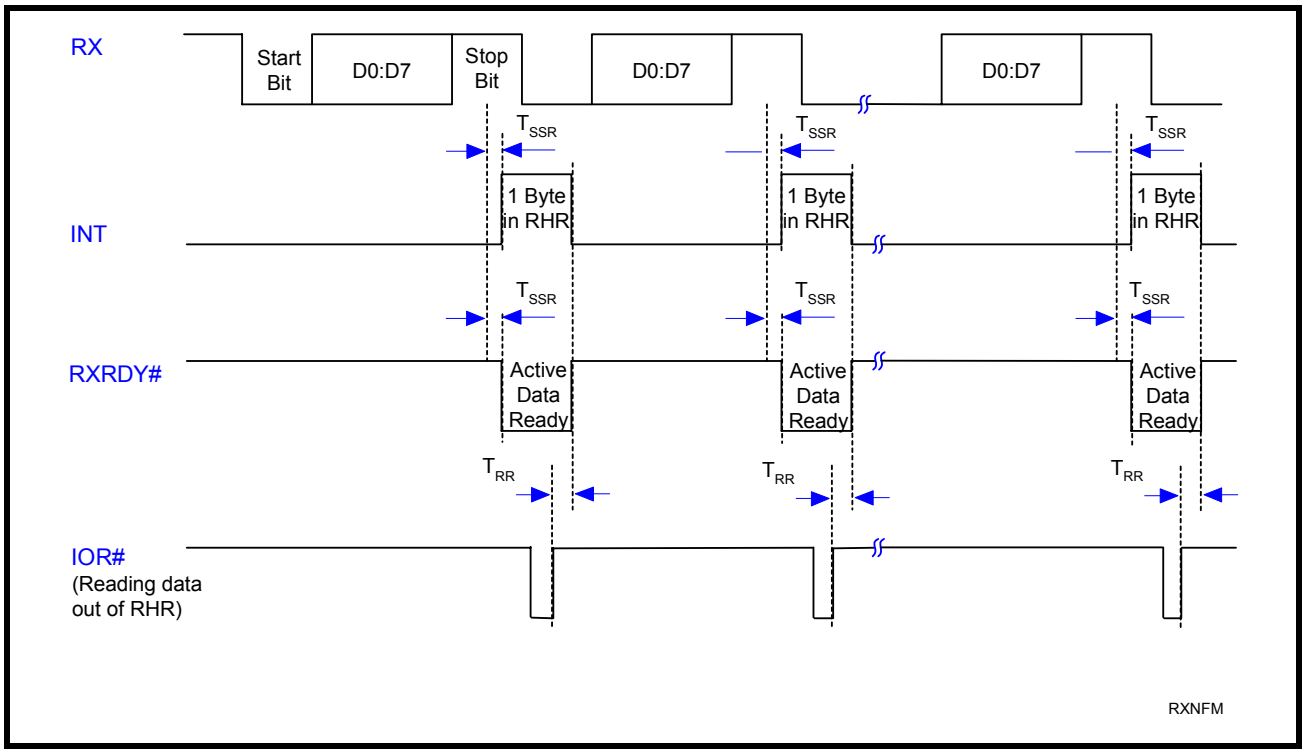


FIGURE 26. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE]

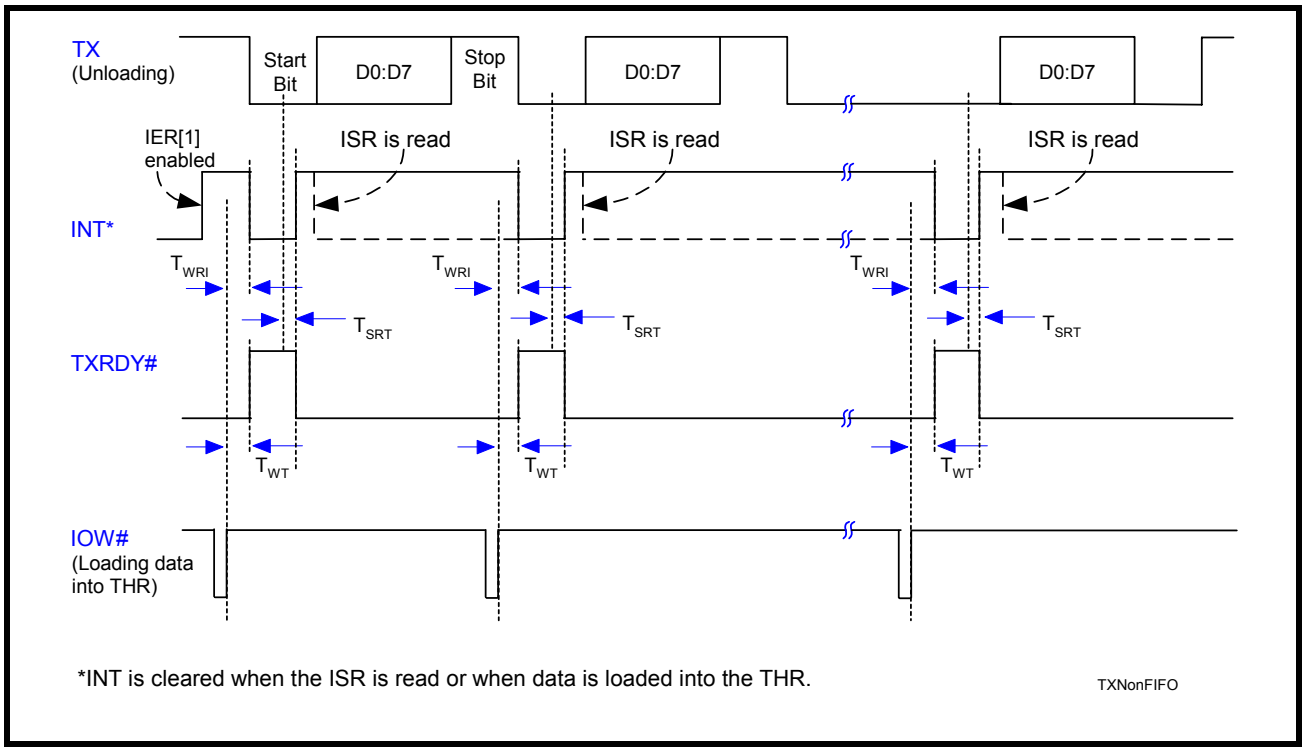


FIGURE 27. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED]

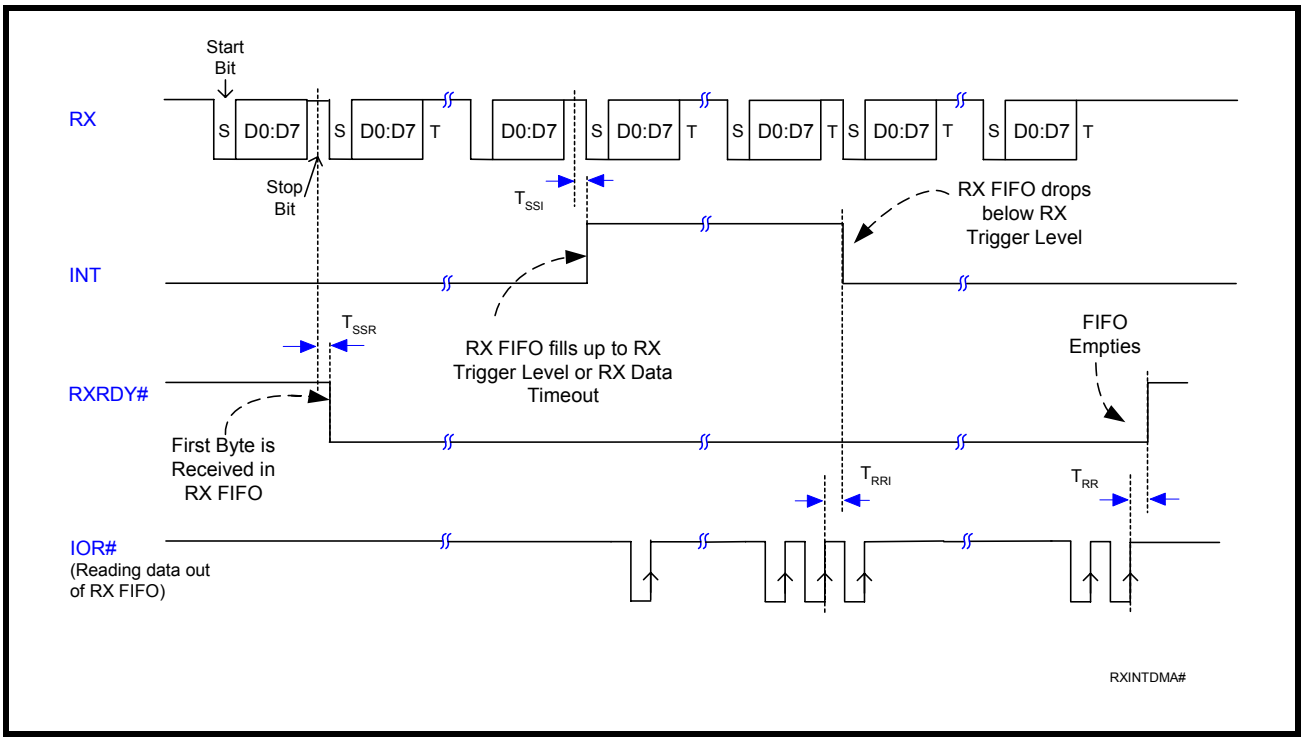


FIGURE 28. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED]

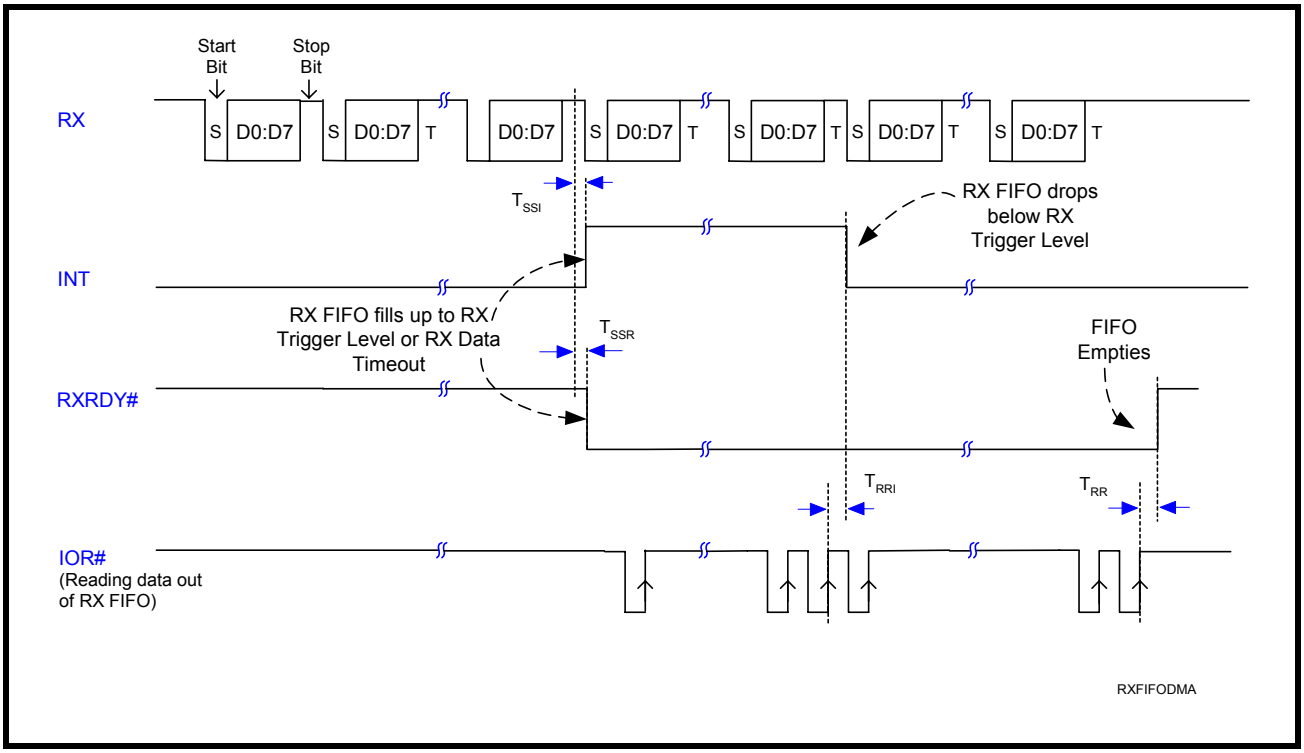


FIGURE 29. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED]

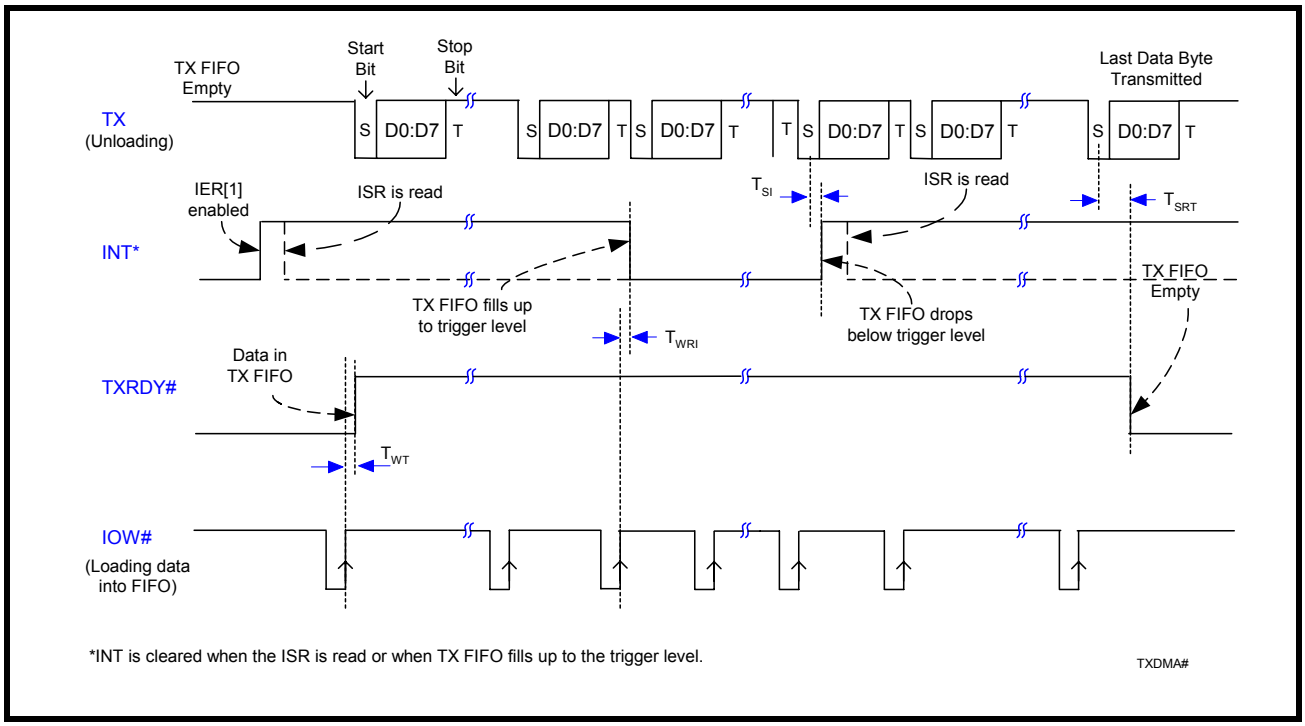
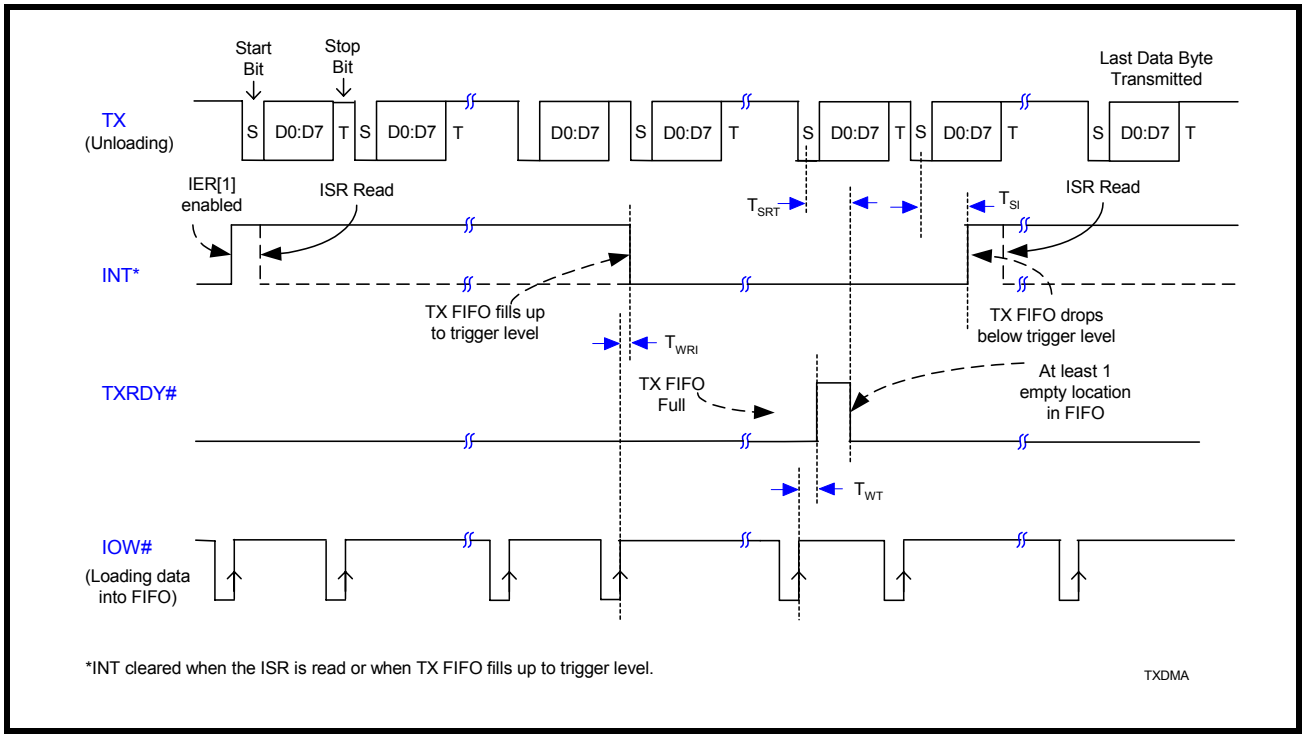
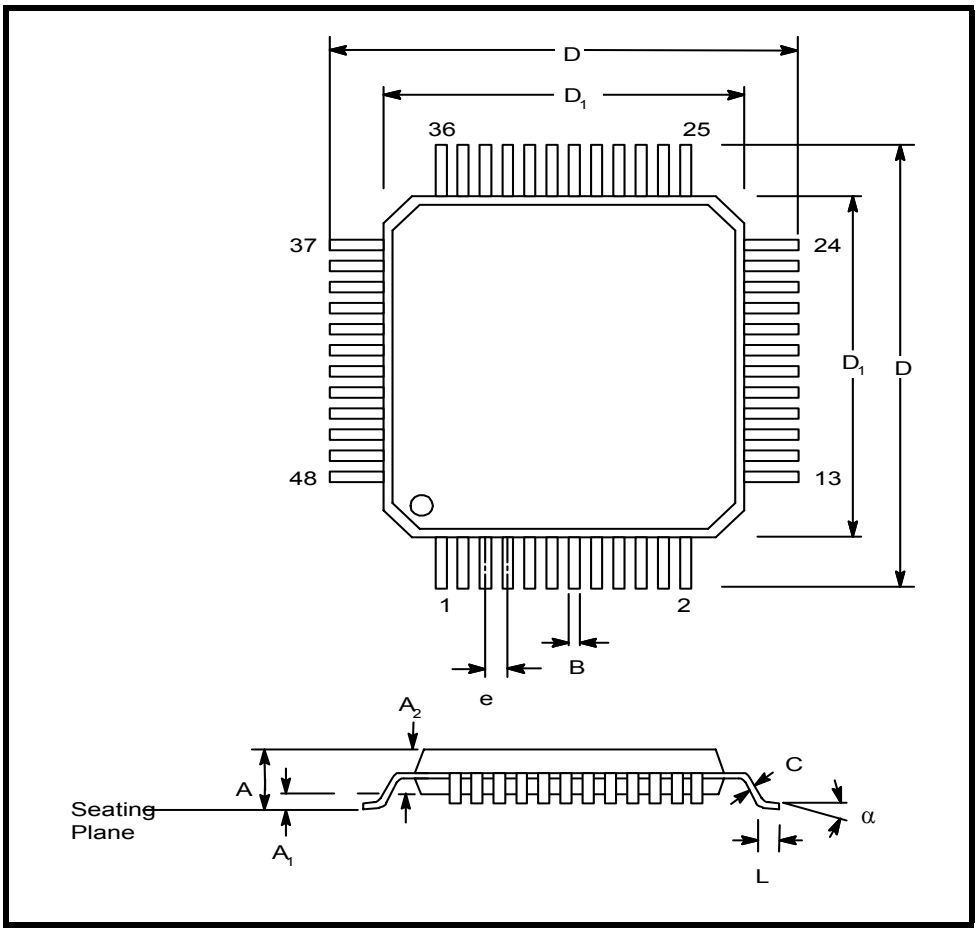


FIGURE 30. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED]



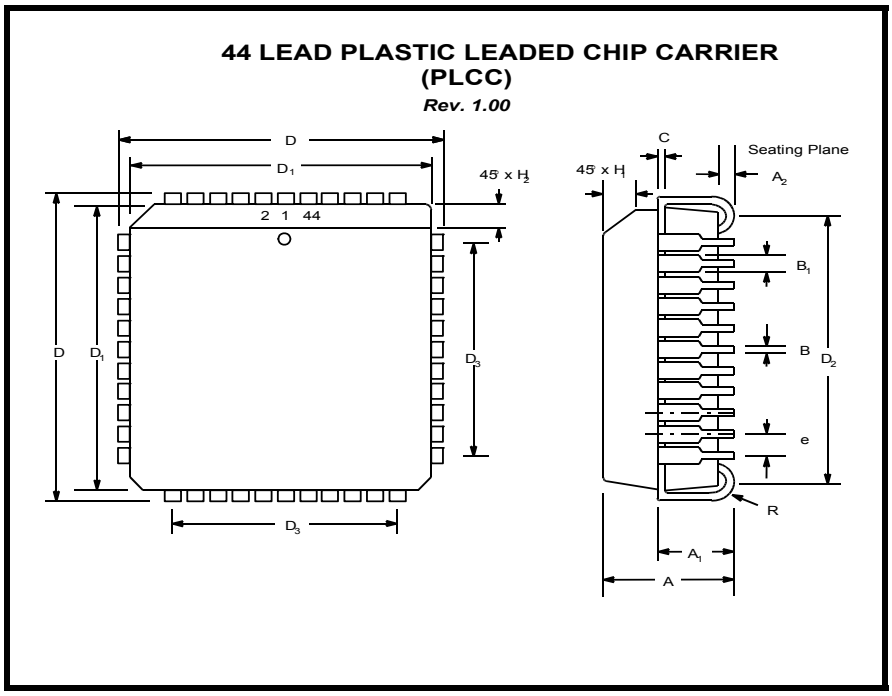
***PACKAGE DIMENSIONS (48 PIN TQFP - 7 X 7 X 1** mm)*



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A1	0.002	0.006	0.05	0.15
A2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

PACKAGE DIMENSIONS (44 PIN PLCC)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

REVISION HISTORY

DATE	REVISION	DESCRIPTION
February 2000	Rev 1.0.0	Initial datasheet.
April 2002	Rev 2.0.0	Changed to standard style format. Internal Registers are described in the order they are listed in the Internal Register Table. Clarified timing diagrams. Corrected Auto RTS Hysteresis table. Renamed Rclk (Receive Clock) to Bclk (Baud Clock) and timing symbols. Added T_{AH}, T_{CS} and OSC.
January 2003	Rev 2.1.0	Changed to single column format. Added Factory Test Mode description and workaround.
May 2003	Rev 2.1.1	Corrected patent number on first page.
June 2003	Rev 2.2.0	Added and Updated Device Status in Ordering Information: 40-pin PDIP and 52-pin QFP are discontinued.
March 2004	Rev 2.3.0	Devices with top mark date code of "F2 YYWW" and newer have 5V tolerant inputs (except for XTAL1) and have 0 ns address hold time (T_{AH}). Factory test mode entry (SEE"FACTORY TEST MODE" ON PAGE 7.) was improved and DREV register was updated to 0x06. In addition, the packages are now in Green Molding Compound.
August 2005	Rev 2.3.1	Removed discontinued packages (40-pin PDIP and 52-pin QFP) from Ordering Information.

TABLE OF CONTENTS