78Q8392L/A03
Low Power Ethernet Coaxial Transceiver

November 2008

DESCRIPTION

The 78Q8392L/A03 Ethernet Transceiver is a replacement for the SSI/TDK/Teridian 78Q8392L/A02 coax line transmitter/receiver. Only a single resistor value change is required for upgrading an existing 78Q8392L/A02 design to the 78Q8392L/A03.

The device includes analog transmit and receive buffers, a 10 MHz on-board oscillator, timing logic for jabber and heartbeat functions, output drivers and bandgap reference, in addition to a current reference and collision detector.

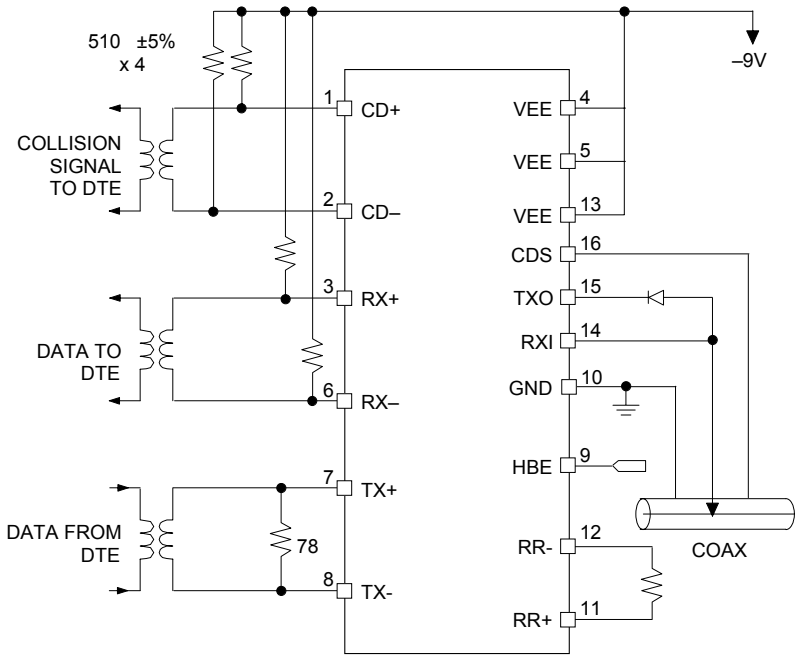
This transceiver provides the interface between the single-ended coaxial cable signals and the Manchester-encoded differential logic signals. Primary functional blocks include the receiver, transmitter, collision detection and jabber timer. This IC may be used in either internal or external MAU environments.

The 78Q8392L/A03 is available in lead-free 16-pin plastic and 28-pin PLCC packages.

FEATURES

- **Very low power consumption**
- **Compliant with Ethernet II, IEEE 802.3 10Base5 and 10Base2**
- **Integrates all transceiver functions except signal and power isolation**
- **Innovative design minimizes external component count and power consumption**
- **Jabber timer function integrated on chip**
- **Externally selectable CED heartbeat allows operation with IEEE 802.3 compatible repeaters**
- **Squelch circuitry at all inputs rejects noise**
- **Power-on reset and test modes**
- **Advanced BiCMOS process**

CONNECT DIAGRAM



FUNCTIONAL DESCRIPTION

The 78Q8392L/A03 incorporates six basic functions of the Ethernet Transceiver, including receiving, transmitting, collision signaling, collision detection, jabber timing, and the heartbeat function. Refer to Figure 1 for a general system block diagram.

RECEIVER FUNCTIONS

The receiver senses signals through the RXI input, which minimizes reflections on the transmission media using a low capacitance, high resistance input buffer amplifier. The CDS ground input attaches directly to the input buffer from the coaxial shield to eliminate ground loop noise.

In addition to the input buffer, the receiver data path consists of an equalizer, data slicer, receiver squelch circuitry, and an output line driver.

The equalizer improves the cable-induced jitter; the data slicer restores equalized received signals to fast transition signals with binary levels to drive the receiver line driver; and the receiver line driver drives the AUI cable through an isolation transformer that connects to the AUI interface.

Noise on the transmission media is rejected by the receiver squelch circuitry, which determines valid data via three criteria: Average DC level, pulse width and transition period. The DC voltage level is detected and compared to a set level in the receiver comparator circuit. The pulse width must be greater than 20 ns to pass the narrow pulse filter; the transition timer outputs a true level on the RX Data Valid line provided the time between transitions is less than about 200 ns. As long as a valid RXI signal is detected, the output line driver remains enabled. The transition timer disables the line driver when there are no further transitions on the data medium, and the RX+, RX- pins go to a zero differential voltage state (Figure 3).

TRANSMITTER FUNCTIONS

The transmitter data path consists of a transmit input buffer, pulse-shaping filter, transmit squelch circuitry and transmit output line driver. The self-biasing transmit input buffer receives data through an isolation transformer and translates the AUI differential analog signal to a square pulse suitable for driving the pulse shaping filter.

The filter outputs a correctly shaped and band limited signal to the transmit output driver, which drives the transmission medium through a high impedance current source. When the transmitter is off, the capacitance of the transmit driver is isolated from the transmission media by an external diode with a low capacitance node. The shield of the transmission media serves as the ground return for the transmitter function.

A transmit squelch circuit, which consists of a pulse threshold detector, a pulse width detector, and a pulse duration timer, is used to suppress noise, as well as crosstalk on the AUI cable. The squelch circuitry disables the transmit driver if the signal at TX+ or TX- is smaller than the pulse threshold. Pulse noise is rejected by a pulse width detector that passes only pulses with durations greater than 20 ns. The pulse duration timer disables the transmit driver if no pulses are received for two-bit periods following valid pulses. At the end of a transmission, the pulse duration timer disables the transmitter and triggers the blanking timer, used to block “dribble” bits.

COLLISION DETECTION

A collision occurs when two or more transmitters simultaneously transmit on the transmission media. A collision is detected by comparing the average DC level of the transmission media to a collision threshold. The received signal at RXI is buffered and sent through a low pass filter, then compared in the collision threshold circuit. If the average DC level exceeds a collision threshold, a 10 MHz signal is output on the CD± pins.

COLLISION SIGNALING

When collision signaling is enabled (HBE pin is high and the average DC level on RXI exceeds the collision threshold V_{CD}), a 10 MHz signal is sent from the CD± pins through an isolation transformer to the DTE. When the function is disabled, this output goes to a zero differential state. The 10 MHz signal output from the CD± pins indicates a collision on the transmission media, a heartbeat function, or that the transmitter is in jabber mode.

JABBER FUNCTION

When valid data on the TX± pins is detected, the jabber timer is started. If there is valid data for more than 20 ms, a latch is set which disables the transmitter output and enables the 10 MHz output on the CD± pins. The latch is reset within 0.5 seconds after the valid data is removed from the transmitter input (TX±). This action resets the jabber timer and disables the 10 MHz signal on the CD± pins. The TX± inputs must remain inactive during the 0.5 second reset period.

HEARTBEAT FUNCTION

The 10 MHz CD outputs are enabled for about 1 µs at approximately 1.1 µs after the end of each transmission. The heartbeat signal tells the DTE that the circuit is functioning. This is implemented by starting the heartbeat timer when the valid data signal indicates the end of a transmission. This function is disabled when HBE pin is tied to VEE.

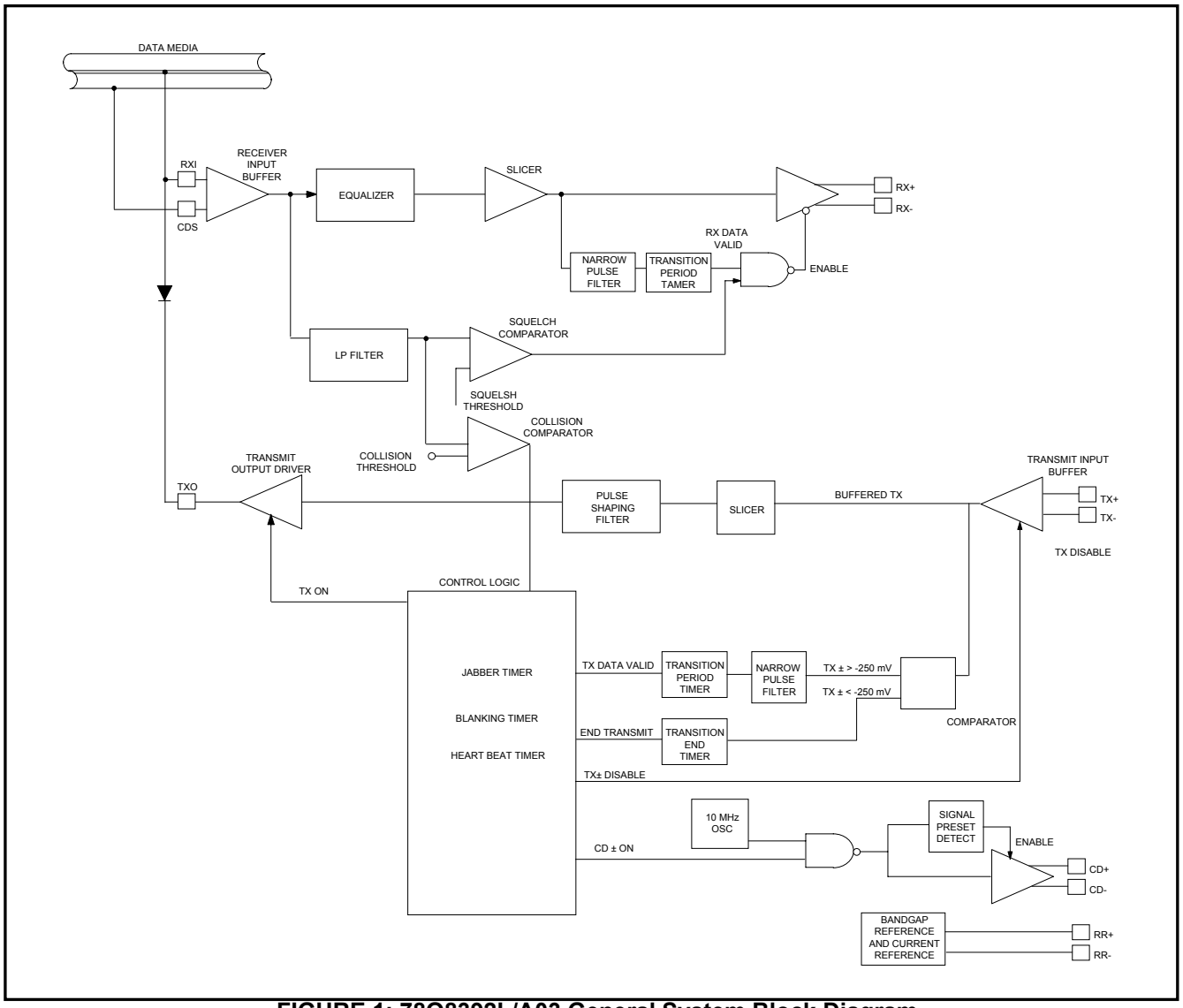


FIGURE 1: 78Q8392L/A03 General System Block Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
CD+*/CD-	O	Collision Output. Balanced differential line driver outputs from the collision detect circuitry. The 10 MHz signal from the internal oscillator is transferred to these outputs in the event of collision, excessive transmission (jabber), or during CD Heartbeat condition. These outputs are open emitters; pulldown resistors to VEE are required. When operating into a 78Ω transmission line, these resistors should be 510Ω. In Cheapernet applications, where the 78Ω drop cable is not used, higher resistor values (up to 1.5k) may be used to save power.
RX+*/RX-	O	Receive Output. Balanced differential line driver outputs from the Receiver. These outputs also require 510Ω pulldown resistors.
TX+*/TX-	I	Transmit Input. Balanced differential line receiver inputs to the Transmitter. The common mode voltage for these inputs is determined internally and must not be externally established. Signals meeting Transmitter squelch requirements are waveshaped and output at TXO.
HBE	I	Heartbeat Enable. This input enables CD Heartbeat when grounded or left opened, disables it when connected to VEE.
RR+/RR-	I	External Resistor. A fixed 976Ω 1% resistor connected between these pins establishes internal operating currents. Note: The previous generation 78Q8392L/A02 used a 1kΩ 1% resistor
RXI	I	Receive Input. Connects directly to the coaxial cable. Signals meeting Receiver squelch requirements are equalized for inter-symbol distortion, amplified, and output at RX+ and RX- pins.
TXO	O	Transmit Output. Connects via an isolation diode to the coaxial cable.
CDS	I	Collision Detect Sense. Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to avoid ground drops from altering the receive mode collision threshold.
GND	S	Positive Supply Pin.
VEE	S	Negative Supply Pins. These pins should be connected to a large metal frame area on the PC board to handle heat dissipation, and bypassed to the GND pin with a 0.1μF capacitor as close to the package as possible.

*IEEE names for CD± = CI±, RX± = DI±, TX± = DO±

Notes: Pin type: I-input; O-output; S-power supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operations should be limited to those conditions specified under recommended operating characteristics.

PARAMETER	RATING
Supply Voltage	-10V
Input Voltage	0 to VEE
Storage Temperature	-65 to 150°C
Soldering (Reflow or Dip)	235°C for 10 sec
Package power dissipation	1.0 watts @ 25°C

DC OPERATING CHARACTERISTICS

0°C ≤ T (ambient) ≤ +70°C, VEE = -9V ± 5%

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
I_{EE1}	Supply current out of V_{EE} pin - non-transmitting			6	8	mA
I_{EE2}	Supply current out of V_{EE} pin - transmitting			50	65	mA
I_{RXI}	Receive input bias current (RXI)	See Note 3	-2		+25	µA
I_{TDC}	Transmit output dc current level (TXO)	See Note 4	37	41	45	mA
I_{TAC}	Transmit output ac current level (TXO)	See Notes 4 & 5	±28		I_{TDC}	mA
V_{CD}	Collision threshold (Receive mode)	See Note 9	-1.58	-1.52	-1.404	V
V_{OD}	Differential output voltage (RX±, CD±)	See Notes 3 & 7	±550		±1200	mV
V_{OC}	Common mode output voltage (RX±, CD±)	See Note 3, 6 & 7	-3.0	-2.5	-2.0	V
V_{OB}	Differential output voltage imbalance (RX±, CD±)	See Notes 3, 7 & 8			±40	mV
V_{TS}	Transmitter squelch threshold (TX±)		-340	-260	-200	mV
C_X	Input capacitance (RXI)			1.2		pF
R_{RXI}	Shunt resistance – non-transmitting (RXI)	See Note 3	100	150		kΩ
R_{TXO}	Shunt resistance – transmitting (TXO)	See Note 4	200			kΩ

DC OPERATING CHARACTERISTICS (continued)

NOTES

1. Currents into device pins are positive, currents out of device pins are negative. If not specified, voltages are referenced to ground.
2. All typical are for VEE = -9V, Ta = 25°C.
3. -8.55V > VEE > -9.45V.
4. The voltage on TXO is -4V < V(TXO) < 0.0V.
5. The AC current measurement is referenced to the DC current level.
6. Operating or idle state.
7. Test load as shown in Figure 2.
8. Device measurement taken in idle state.
9. This threshold can be determined by monitoring the CD± output with a DC level in RXI.

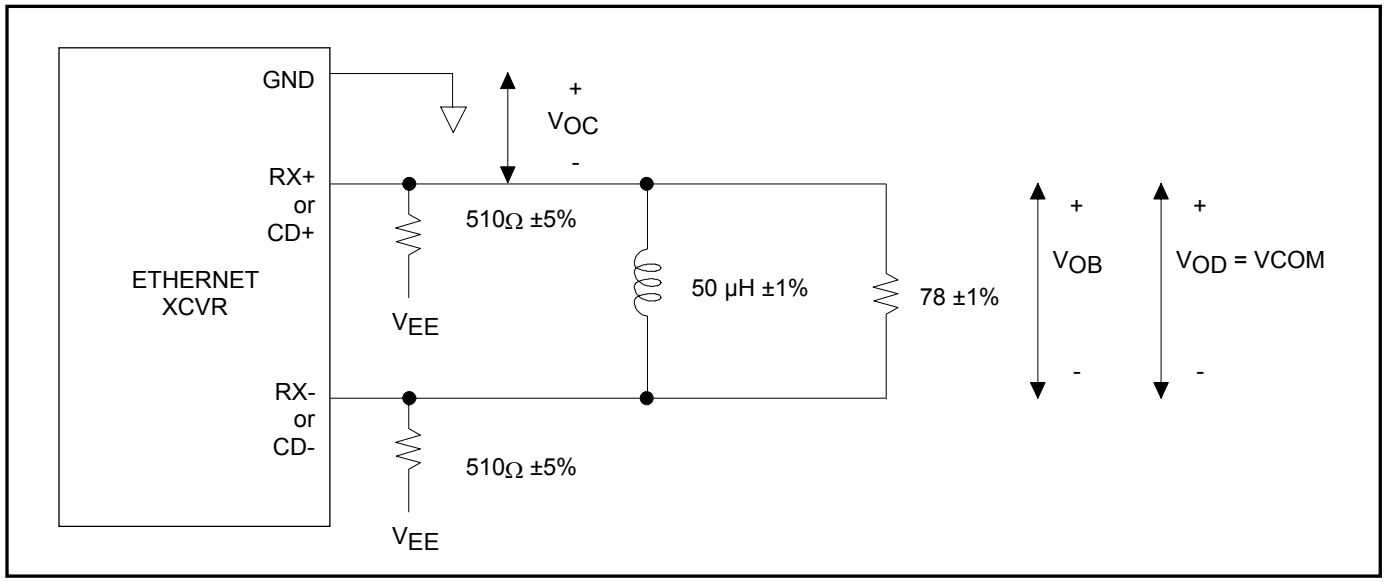


FIGURE 2: Test Load for CD± or RX±

AC OPERATING CHARACTERISTICS

0°C < T(ambient) < +70°C, VEE = 9V ± 5%

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
t_{RON}	Receiver startup delay (RXI to RX±)			400	500	ns
t_{Rd}	Receiver propagation delay (RXI to RX±)			10	50	ns
t_{Rr}	Differential outputs rise time (RX± , CD±)			4	5	ns
t_{Rf}	Differential outputs fall time (RX± , CD±)			4	5	ns
t_{RJ}	Receiver & cable total jitter			2	4	ns
t_{TST}	Transmitter startup delay (TX± to TXO)			100	200	ns
t_{Td}	Transmitter propagation delay (TX± to TXO)			35	50	ns
t_{Tr}	Transmitter rise time – 10% to 90% (TXO)		20	25	30	ns
t_{Tf}	Transmitter fall time- 90% to 10% (TXO)		20	25	30	ns
t_{TM}	t_{Tr} and t_{Tf} mismatch			0.5	2	ns
t_{TON}	Transmit turn-on pulse width at V_{TS} (TX±)		8	20	30	ns
t_{TOFF}	Transmit turn-off pulse width at V_{TS} (TX±)		140	160	180	ns
t_{CON}	Collision turn-on delay			700	900	ns
t_{COFF}	Collision turn-off delay				2000	ns
f_{CD}	Collision frequency (CD±)		8.5	10	11.5	MHz
t_{CP}	Collision pulse width (CD±)		40		60	ns
t_{HON}	CD Heartbeat delay (TX± to CD±)		0.6	1.0	1.6	µs
t_{HW}	CD Heartbeat duration (CD±)		0.6	1.0	1.5	µs
t_{JA}	Jabber activation delay (TX± to TXO off and CD±)		20		60	ms
t_{JR}	Jabber reset unjab time (TX± to TXO and CD±)		250	500	650	ms
t_{RO}	Receive Off Pulse Width (RX+ to RX-)		200			ns

ELECTRICAL SPECIFICATIONS (continued)

TRANSMIT SPECIFICATIONS

The first bit transmitted from TXO may have data and phase violations. The second through last bit reproduce the TX± signal with less than or equal to the specified jitter.

There is no logical signal inversion between TX± and TXO output. A low level from TX+ to TX- results in more current flowing from the coaxial cable into the TXO pin.

At the end of transmission, when the transmitter changes from the enabled state to the idle state, no spurious pulses are generated, i.e., the transition on TXO proceeds monotonically to zero current.

RECEIVE SPECIFICATIONS

The first bit sent from RX± may have data and phase violations. The second through last bit reproduce the received signal with less than or equal to the specified jitter.

There is no logical signal inversion between the RXI input and the RX± output. A high level at RXI produces a positive differential voltage from RX+ to RX-.

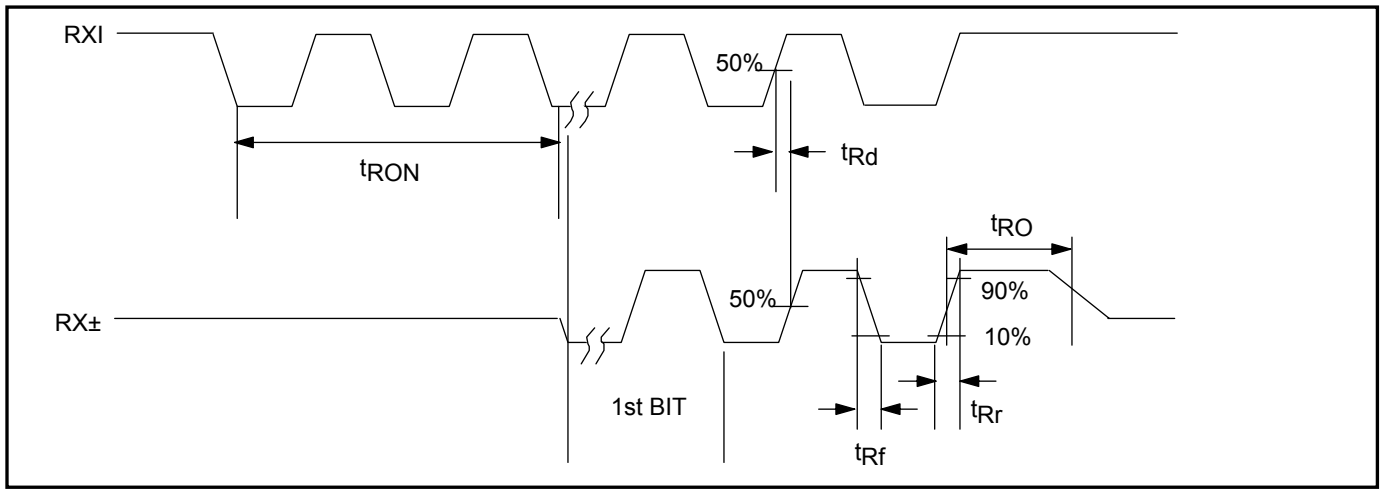


FIGURE 3: Receiver Timing

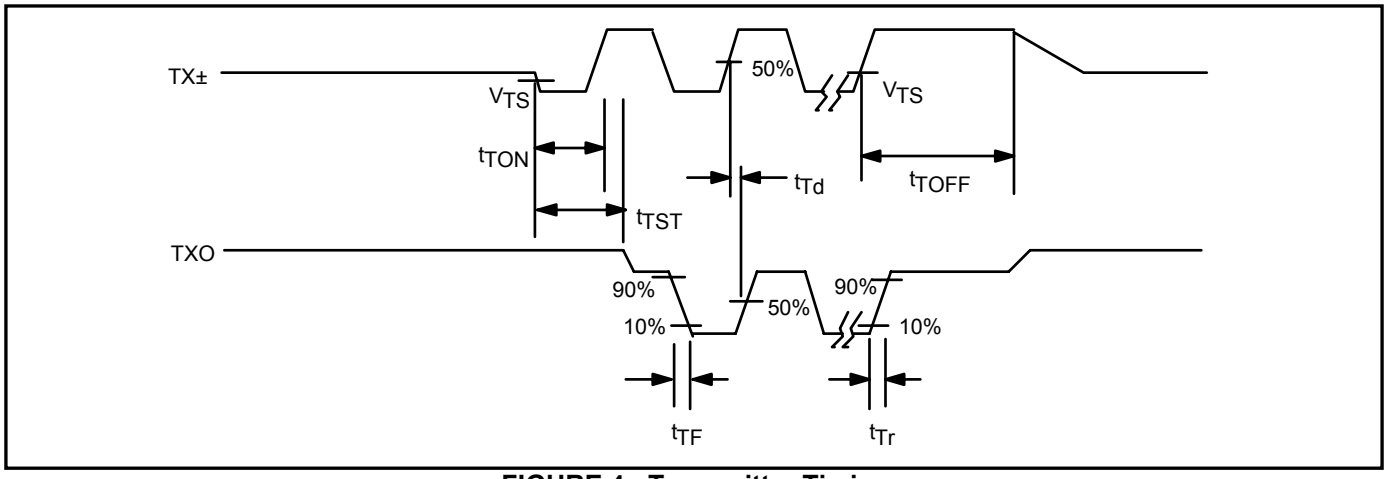


FIGURE 4: Transmitter Timing

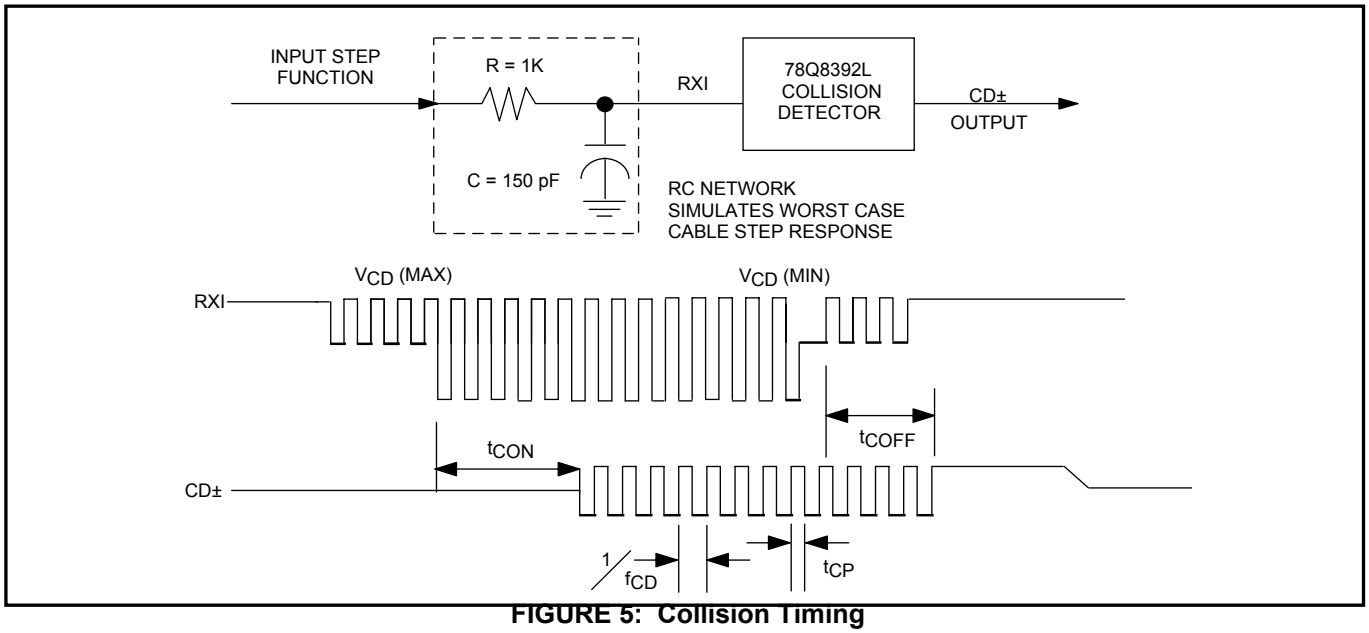


FIGURE 5: Collision Timing

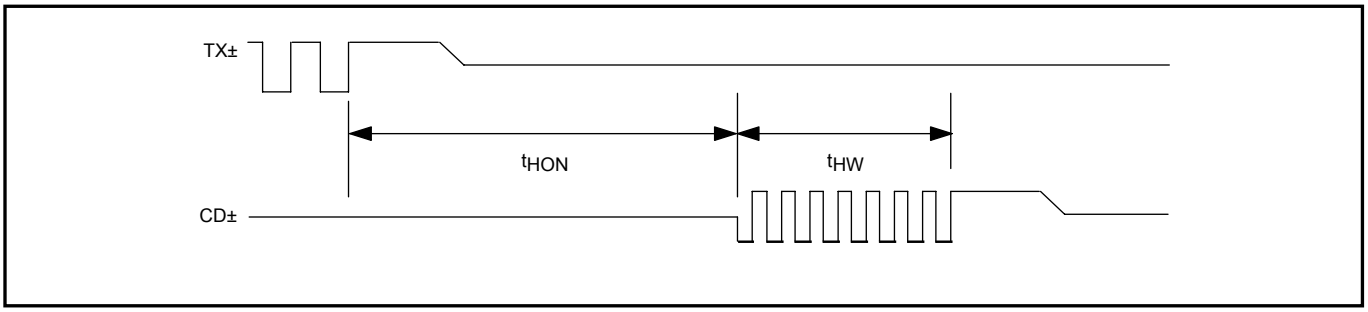


FIGURE 6: Heartbeat Timing

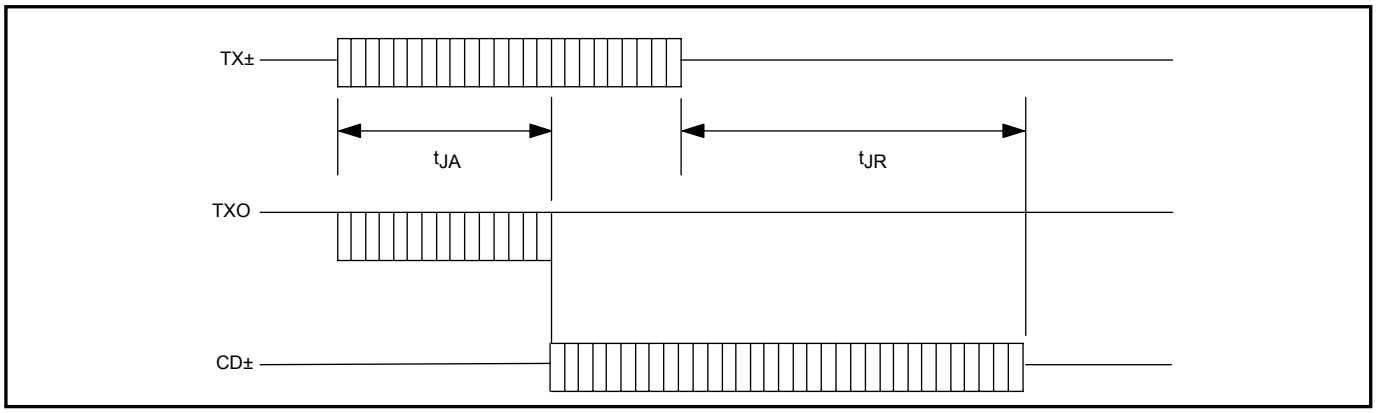


FIGURE 7: Jabber Timing

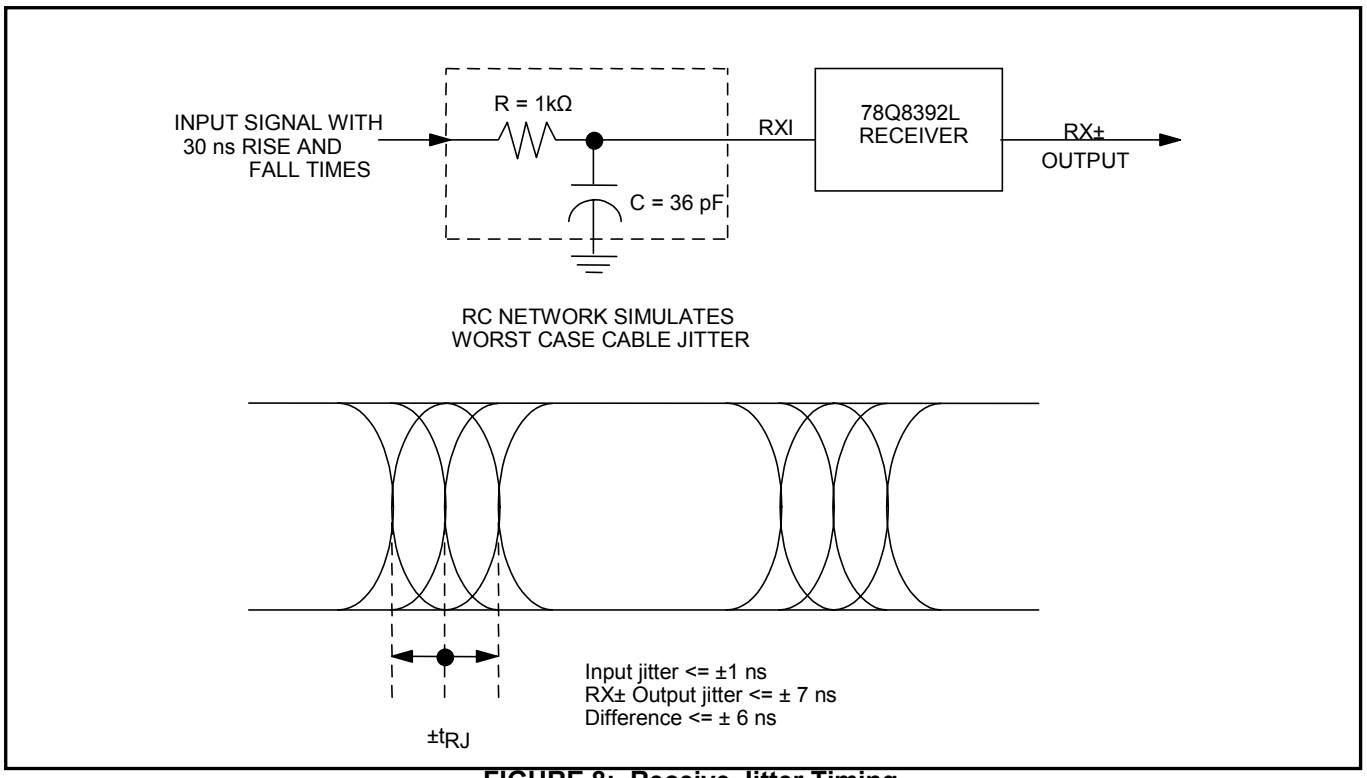


FIGURE 8: Receive Jitter Timing

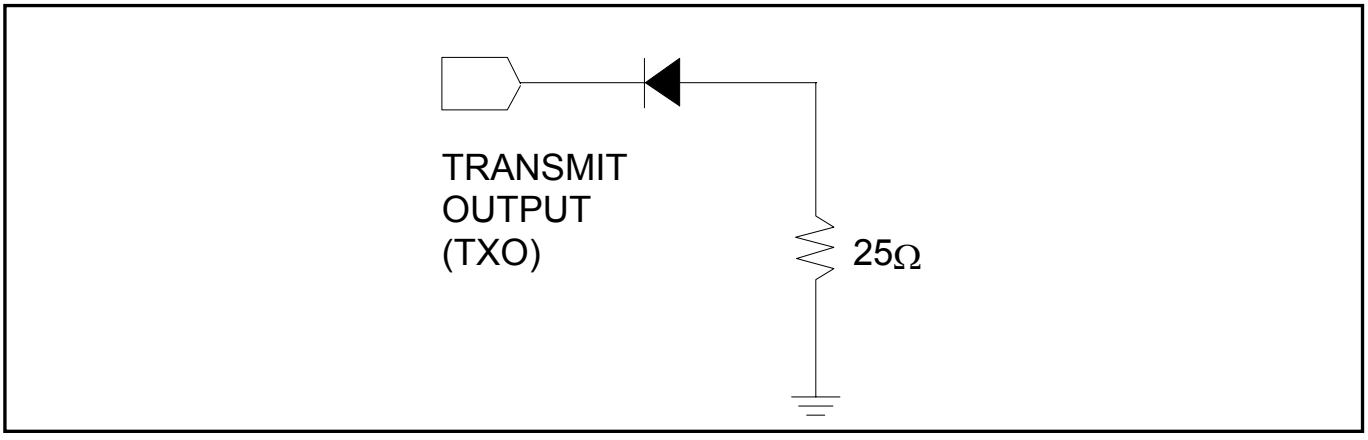


FIGURE 9: Test Loads TXO

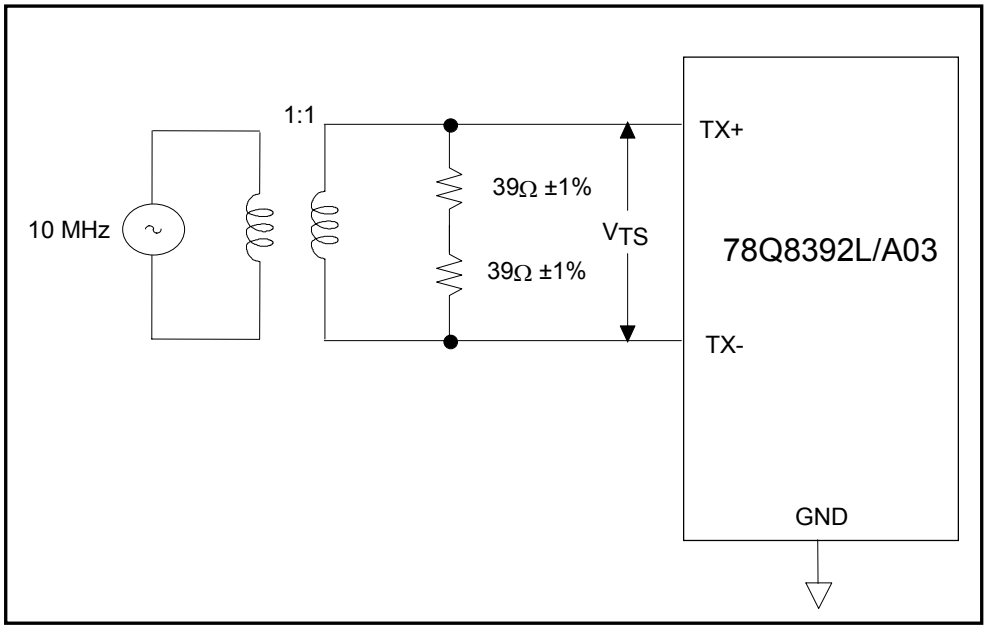
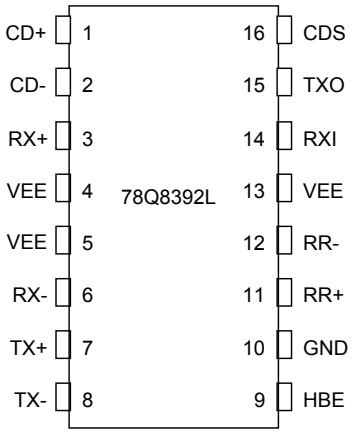


FIGURE 10: Test Circuit for TX± Input

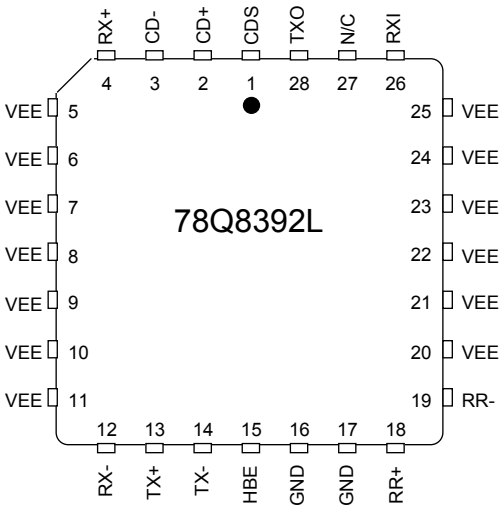
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



16-Pin DIP

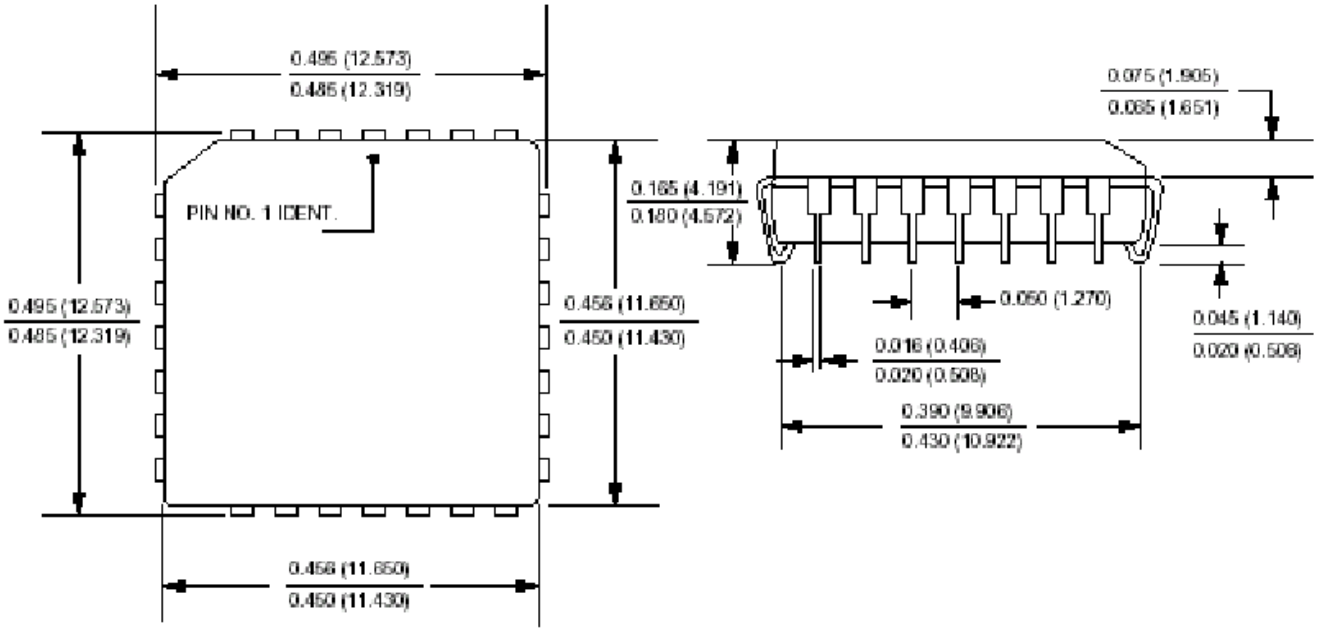


28-Pin PLCC

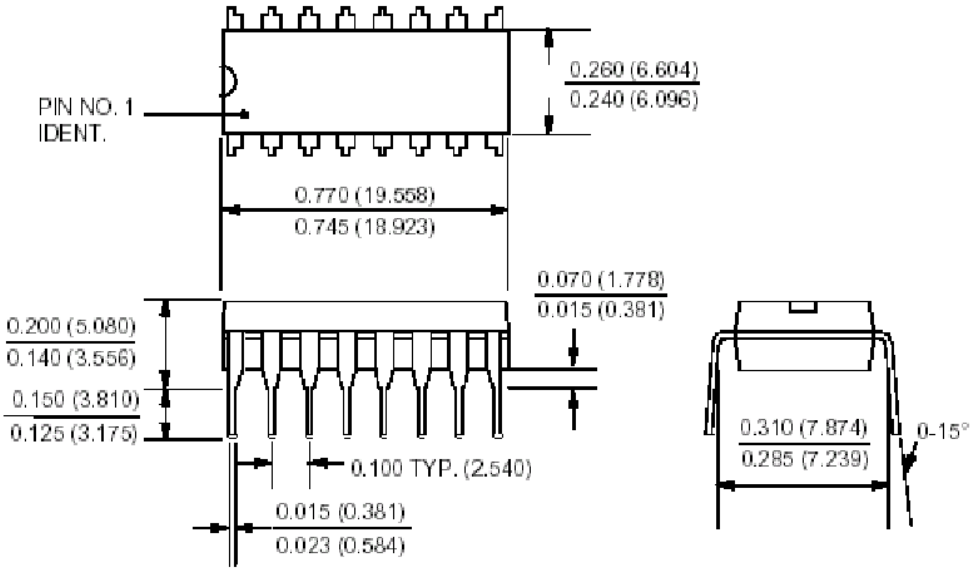
Θ_{JA} = 45°C/W for the 28_pin PLCC package

MECHANICAL DRAWING (inch / mm)

28-Pin PLCC



16-Pin DIP



ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
78Q8392L/A03 16-Pin Plastic DIP (lead free)	78Q8392LA03-CP/F	78Q8392L-CP SP(Date Code)P3F (Lot Number)
78Q8392L/A03 28-Pin Plastic PLCC (lead free)	78Q8392LA03-28CH/F	78Q8392L-28CH SP(Date Code)P3F (Lot Number)

REVISION HISTORY

Rev. #	Date	Comments
1.1	December 2005	Final Data Sheet release
1.2	January 2006	Corrected package marking error (from C to P)
1.3	November, 2008	Added package dimensions

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