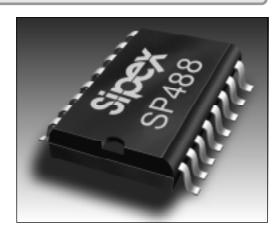


## SP488A and SP489A

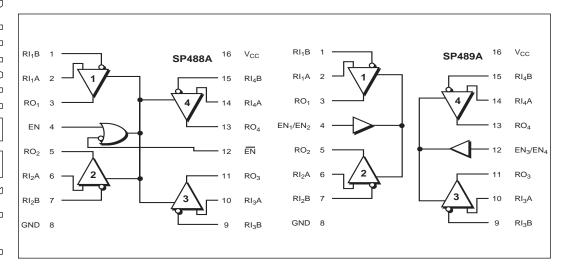
# High Speed Quad RS-485/RS-422 Line Receivers

- High Speed Versions of **Sipex's** SP488 & SP489
- 30Mbps Transmission Rates
- Quad Differential Line Receivers
- RS-485 or RS-422 Applications
- Tri-state Output Control
- 30ns Typical Receiver Propagation Delays
- -7V to +12V Common Mode Input Range
- 1mA Supply Current
- Single +5V Supply Operation
- Pin Compatible with SN75173, SN75175, LTC488 and LTC489



#### **DESCRIPTION...**

The **SP488A** and **SP489A** are high speed quad differential line receivers capable of meeting the RS-485 and RS-422 protocols while running at five times the normal transmission rates. The **SP488A** and **SP489A** are enhanced versions of **Sipex's** SP488 and SP489 quad RS-485/RS-422 line receivers. The **SP488A** features a common receiver enable control; the **SP489A** provides independent receiver enable controls for each pair of receivers. Both feature tri–state outputs and wide common–mode input range. The receivers have a fail–safe feature which forces a logic "1" output when receiver inputs are left floating. Both are available in 16–pin plastic DIP and SOIC packages.



SP488A/489ADS/07

SP488A/489A High Speed Quad RS-485/RS-422 Line Receivers

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#### **ABSOLUTE MAXIMUM RATINGS**

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V <sub>CC</sub>	+7V
Input Voltages	
Logic	–0.5V to (V <sub>cc</sub> +0.5V)
Receiver	±14V
Receiver Output Voltage	0.5V to (V <sub>cc</sub> +0.5V)
Input Currents	
Logic	±25mA
Storage Temperature	65°C to +150°C
Power Dissipation	
Plastic DIP	375mW
(derate 7mW/°C above +70°C)	
Small Outline	375mW
(derate 7mW/°C above +70°C)	
Lead Temperature (soldering, 10 sec)	300°C



ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

#### **SPECIFICATIONS**

 $V_{CC} = 5V\pm5\%$ ; typicals at 25°C;  $T_{MIN} \le T_A \le T_{MAX}$  unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS Digital Inputs Voltage					EN, EN, EN,/EN <sub>2</sub> , EN <sub>3</sub> /EN <sub>4</sub>
V <sub>L</sub> V <sub>H</sub> Input Current	2.0		0.8 ±2	Volts Volts μΑ	$0V \le V_{IN} \le V_{CC}$
RECEIVER INPUTS Input Resistance Differential Input Threshold Input Current (A, B)	12 -0.2		+0.2 +1.0 -0.8	kOhm Volts mA mA	$ -7V \le V_{CM} \le 12V \\ -7V \le V_{CM} \le 12V \\ V_{CC} = 0V \text{ or } 5.25V; \ I_{IN2} \\ V_{IN} = +12V \\ V_{IN} = -7V $
Maximum Data Rate	30		-0.0	Mbps	$V_{IN} = -7 V$
RECEIVER OUTPUTS Output Voltage VOH VOL High Impedance Output Curr	3.5 ent		0.4 <u>+</u> 1	V V μΑ	$\begin{split} I_{_{\mathrm{O}}} &= -4 \text{mA}; \ V_{_{\mathrm{ID}}} = +0.2 \text{V} \\ I_{_{\mathrm{O}}} &= +4 \text{mA}; \ V_{_{\mathrm{ID}}} = -0.2 \text{V} \\ \text{EN} &= \emptyset, \ \overline{\text{EN}} = V_{_{\mathrm{CC}}}, \ \text{EN}_{_{\mathrm{I}}} \text{EN}_{_{2}} = \emptyset, \\ \text{EN}_{_{\mathrm{J}}} \text{EN}_{_{4}} = \emptyset, \ 0.4 \text{V} \leq V_{_{\mathrm{O}}} \leq 2.4 \text{V} \end{split}$
POWER REQUIREMENTS Supply Voltage Supply Current	4.75	TBD	5.25	Volts	mA No load
ENVIRONMENTAL AND ME	CHANICA	AL			
Operating Temperature  -C  -E  Storage Temperature  Package P T		pin Plastio 6–pin SO		ပံ ပဲ	

#### **AC PARAMETERS**

 $V_{CC} = 5V\pm5\%$ ; typicals at 25°C; 0°C  $\leq T_A \leq +70$ °C unless otherwise noted.

MIN.	TYP.	MAX.	UNIT	CONDITIONS
				C <sub>1</sub> = 15pF; <i>Figure 1, 3</i>
	TBD		ns	
	TBD		ns	
skd)	TBD		ns	
1				10% to 90%
	1		ns	
	TBD		ns	
				90% to 10%
	IBD		ns	
	TBD		ns	$C_L = 15pF$ ; Figures 2 and 4
				(S2 closed)
	TBD		ns	CL = 15pF; Figures 2 and 4
				(S1 closed)
	TBD		ns	CL = 15pF; Figures 2 and 4
				(S1 closed)
	TBD		ns	CL = 15pF; Figures 2 and 4
				(S2 closed)
	MIN.	TBD TBD TBD TBD TBD TBD TBD TBD TBD	TBD	TBD ns ns TBD ns

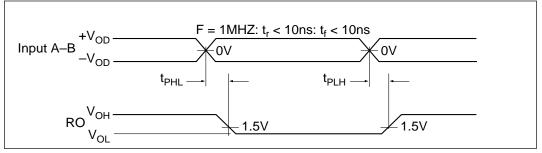


Figure 1. Receiver Propagation Delays

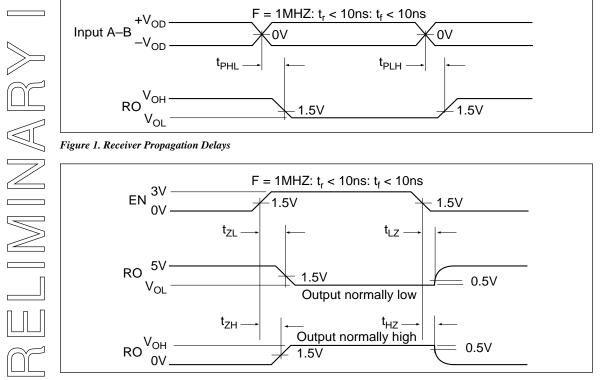
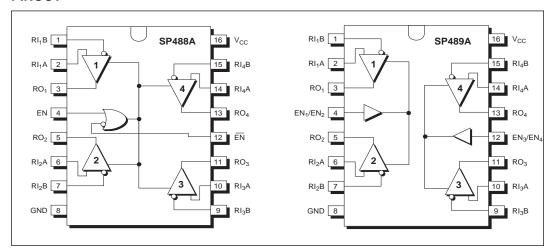


Figure 2. Receiver Enable/Disable Timing

### **PINOUT**



#### **SP488A PINOUT**

Pin 1 — RI<sub>1</sub>B — Receiver 1 input B.

Pin 2 — RI<sub>1</sub>A \_ Receiver 1 input A.

Pin 3 —  $RO_1$  — Receiver 1 Output — If Receiver 1 output is enabled, if  $RI_1A > RI_1B$  by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if  $RI_1A < RI_1B$  by 200mV, Receiver 1 output is low.

Pin 4 — EN — Receiver Output Enable. Please refer to **SP488A** *Truth Table* (1).

Pin 5 —  $RO_2$  — Receiver 2 Output — If Receiver 2 output is enabled, if  $RI_2A > RI_2B$  by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if  $RI_2A < RI_2B$  by 200mV, Receiver 2 output is low.

Pin 6 — RI<sub>2</sub>A — Receiver 2 input A.

Pin 7 — RI<sub>2</sub>B — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

Pin 9 — RI<sub>3</sub>B — Receiver 3 input B.

Pin 10 — RI<sub>3</sub>A — Receiver 3 input A.

Pin 11 —  $RO_3$  — Receiver 3 Output — If Receiver 3 output is enabled, if  $RI_3A > RI_3B$  by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if  $RI_3A < RI_3B$  by 200mV, Receiver 3 output is low.

Pin 12—EN—Receiver Output Enable. Please refer to **SP488A** Truth Table (1).

Pin 13 —  $RO_4$  — Receiver 4 Output — If Receiver 4 output is enabled, if  $RI_4A > RI_4B$  by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if  $RI_4A < RI_4B$  by 200mV, Receiver 4 output is low.

Pin 14 — RI<sub>4</sub>A — Receiver 4 input A.

Pin 15 — RI<sub>4</sub>B — Receiver 4 input B.

Pin 16 — Supply Voltage  $V_{CC}$  —  $4.75V \le V_{CC} \le 5.25V$ .

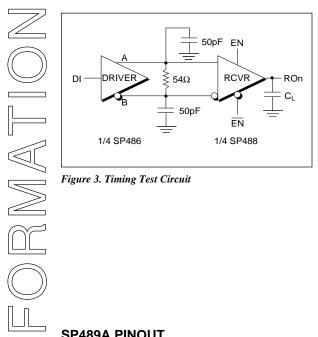


Figure 3. Timing Test Circuit

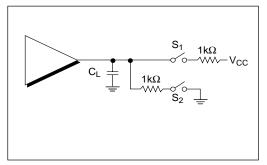


Figure 4. Enable/Disable Timing Test Circuit

#### **SP489A PINOUT**

Pin 1 — RI<sub>1</sub>B — Receiver 1 input B.

Pin 2 — RI<sub>1</sub>A — Receiver 1 input A.

Pin 3 — RO<sub>1</sub> — Receiver 1 Output — If Receiver 1 output is enabled, if  $RI_{1A} > RI_{1}B$  by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if RI<sub>1</sub>A < RI<sub>1</sub>B by 200mV, Receiver 1 output is low.

Pin 4 — EN1/EN2 — Receiver 1 and 2 Output Enable. Please refer to **SP489A** *Truth Table* (2).

Pin 5 — RO<sub>2</sub> — Receiver 2 Output — If Receiver 2 output is enabled, if RI<sub>2</sub>A > RI<sub>2</sub>B by 200 mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if RI<sub>2</sub>A < RI<sub>2</sub>B by 200mV, Receiver 2 output is low.

Pin 6 — RI<sub>2</sub>A — Receiver 2 input A.

Pin 7 — RI<sub>2</sub>B — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

Pin 9 — RI<sub>3</sub>B — Receiver 3 input B.

Pin 10 — RI<sub>3</sub>A — Receiver 3 input A.

Pin 11 — RO<sub>3</sub> — Receiver 3 Output — If Receiver 3 output is enabled, if  $RI_2A > RI_2B$  by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if RI<sub>2</sub>A < RI<sub>2</sub>B by 200mV, Receiver 3 output is low.

Pin 12 — EN3/EN4 — Receiver 3 and 4 Output Enable. Please refer to **SP489A** Truth Table (2).

Pin 13 — RO<sub>4</sub> — Receiver 4 Output — If Receiver 4 output is enabled, if  $RI_AA > RI_AB$  by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if RI<sub>4</sub>A < RI<sub>4</sub>B by 200mV, Receiver 4 output is low.

Pin 14 — RI<sub>4</sub>A — Receiver 4 input A.

Pin 15 — RI<sub>4</sub>B — Receiver 4 input B.

Pin 16 — Supply Voltage  $V_{CC}$  — 4.75 $V \le V_{CC} \le$ 5.25V.

DIFFERENTIAL	ENA	OUTPUT	
A – B	EN	EN	RO
V <sub>ID</sub> ≥ 0.2V	H X	X L	H
-0.2V < V <sub>ID</sub> < +0.2V	H X	X L	X X
V <sub>ID</sub> ≤ 0.2V	H X	X L	L L
Х	L	Н	Hi–Z

T.11.	7	CD 400 A	T 41.	T-11.
Table	•	SP488A	Iruth	Table

DIFFERENTIAL	ENABLES	OUTPUT
A – B	EN <sub>1</sub> /EN <sub>2</sub> or EN <sub>3</sub> /EN <sub>4</sub>	RO
V <sub>ID</sub> ≥ 0.2V	Н	н
-0.2V < V <sub>ID</sub> < +0.2V	Н	х
V <sub>ID</sub> ≤ 0.2V	Н	L
X	L	Hi–Z

Table 2. SP489A Truth Table

#### FEATURES...

The **SP488A** and **SP489A** are low–power quad differential line receivers meeting RS-485 and RS-422 serial protocol. The **SP488A** and **SP489A** feature **Sipex's** BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-485 and RS-422 serial protocols over 10Mbps under load in harsh environments. In fact, the **SP488A** and **SP489A** can transmit signals up to 30Mbps.

The RS-485 standard is ideal for multi-drop applications and for long-distance communication. RS-485 allows up to 32 drivers and 32 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-485 transceivers are equipped with a wide (-7V to +12V) common mode range to accommodate ground potential differences. Because RS-485 is a differential interface, data is virtually immune to noise in the transmission line.

Normally an RS-485 driver will produce no less than 1.5V before cable attenuation. After cable loss, the signal may degrade and have an amplitude of less than 1.0V. The receiver input sensitivity of the **SP488A** and **SP489A** allows the devices to receive signals as low as 200mV.

The **SP488A** features active high and active low common receiver enable controls; the **SP489A** provides independent, active high receiver enable controls for each pair of receivers. Both feature tri-state outputs and a -7V to +12V common-mode input range permitting a ±7V ground difference between devices on the communications bus. The **SP488A/489A** are equipped with a fail-safe feature which forces a logic high at the receiver output when the input is left floating. Both are available in 16-pin plastic DIP and SOIC packages.

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ORDERING INFORMATION						
Quad RS485 Receivers:						
Model	Enable/Disable	Temperature Range	Package			
SP488ACP	Common; active Low and Active Hig	gh 0°C to +70°C	16-pin Plastic DIP			
SP488ACT	Common; active Low and Active High	h 0°C to +70°C	16-pin SOIC			
SP488AEP	Common; active Low and Active High	h40°C to +85°C	16-pin Plastic DIP			
SP488AET	Common; active Low and Active Hig	gh –40°C to +85°C	16-pin SOIC			
SP489ACP	One per driver pair; active High	0°C to +70°C	16-pin Plastic DIP			
SP489ACT	One per driver pair; active High	0°C to +70°C	16-pin SOIC			
SP489AEP	One per driver pair; active High	40°C to +85°C	16-pin Plastic DIP			
SP489AET	One per driver pair; active High	–40°C to +85°C	16-pin SOIC			

Please consult the factory for pricing and availability on a Tape-On-Reel option.



SIGNAL PROCESSING EXCELLENCE

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SP488A/489ADS/07

SP488A/489A High Speed Quad RS-485/RS-422 Line Receivers

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