AK4320

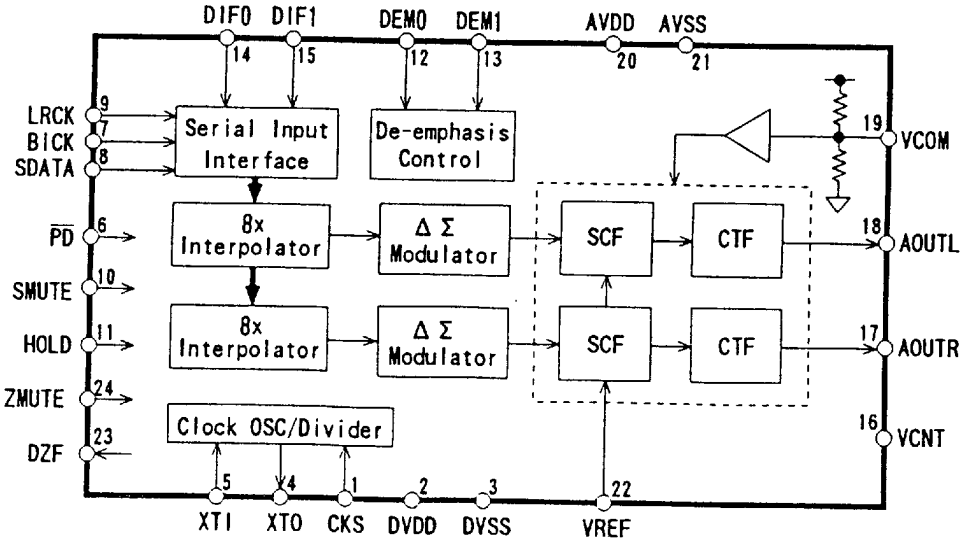
High Performance 20Bit Δ Σ DAC

General Description

The AK4320 is a high performance 1bit stereo DAC for digital audio systems and includes 20bit digital filter. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4320, the analog outputs are filtered in the analog domain by a combination of switched-capacitor filter(SCF) and continuous-time filter(CTF). Therefore, any external filters are not required. As the loss of accuracy from clock jitter is improved by using SCF techniques, the AK4320 is ideal for digital broadcating application, DBS, CATV and digital recording application, DAT, MD, DCC etc. The master clock can be either 256fs or 384fs, supporting various audio environment.

Features

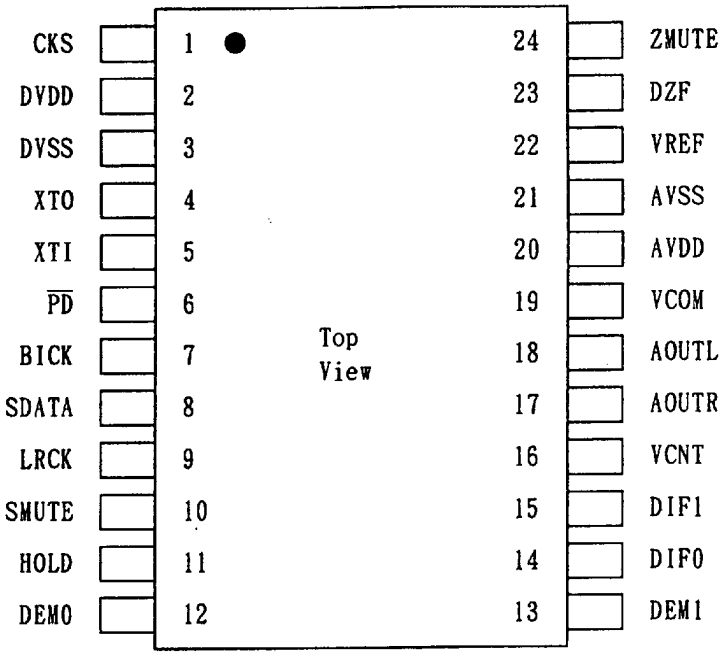
- ☐ High Performance Stereo 1bit DAC
- ☐ On chip Perfect filtering
  - 20Bit 8 times FIR Interpolator
  - 2nd order SCF
  - 2nd order CTF
  - Total Response: ± 0.1dB at 20kHz
- ☐ On chip Buffer with Single End Output
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ Soft Mute with Hold
- ☐ High Tolerance to Clock Jitter
- ☐ Dynamic Range: 100dB
- ☐ S/N: 110dB
- ☐ Low Out-of-Band Noise
- ☐ Power Supply: 5V ± 10%
- ☐ Small Package: 24pin SSOP



■ Ordering Guide

AK4320-VM	-10～+70℃	24pin SSOP(0.65mm pitch)
AKD4320	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	CKS	I	Master Clock Select Pin (Pull-down pin) "L": XTI=256fs, "H": XTI=384fs
2	DVDD	-	Digital Power Supply Pin, +5V
3	DVSS	-	Digital Ground Pin
4	XTO	O	Crystal Oscillator Output Pin When an external clock is input, this pin should be left floating.
5	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external CMOS clock can be input on XTI.
6	$\overline{PD}$	I	Power-Down Pin When at "L", the AK4320 is in power-down mode and is held in reset. The AK4320 should always be reset upon power-up.
7	BICK	I	Serial Data Clock Pin 64fs clock is recommended to be input on this pin.
8	SDATA	I	Serial Data Input Pin 2's complement MSB-first data is input on this pin.
9	LRCK	I	L/R Clock Pin This input determines which channel is currently being input on SDATA pin. "H": Lch, "L": Rch
10	SMUTE	I	Soft Mute Pin (Pull-down pin) When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
11	HOLD	I	Soft Mute Hold Pin (Pull-down pin)
12 13	DEM0 DEM1	I	De-emphasis Mode Pins This function corresponds to 3 types of sampling rate.
14 15	DIF0 DIF1	I I	Digital Input Format Pins (Pull-down pins) These two pins select one of four formats for the incoming data. When "H", these pins should be tied to AVDD.
16	VCNT	O	Voltage Control Pin
17	AOUTR	O	Rch Analog Output Pin
18	AOUTL	O	Lch Analog Output Pin
19	VCOM	O	Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 47uF electrolytic cap.(★)
20	AVDD	-	Analog Supply, +5V
21	AVSS	-	Analog Ground Pin
22	VREF	I	Voltage Reference Input Pin The differential Voltage between this pin and AVSS set the analog output range. Normally connected to AVSS with a 0.1uF ceramic capacitor.
23	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".
24	ZMUTE	I	ZERO Mute Enable Pin (Pull-down pin) When this pin is "H", analog outputs are muted by zero detection. This pin should be fixed at "H" or "L" level.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog (AVDD pin)	AVDD	-0.3	6.0	V
Digital (DVDD pin)	DVDD	-0.3	AVDD+0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Input Voltage	VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature	Ta	-10	70	℃
Storage Temperature	Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog (AVDD pin)	AVDD	4.5	5.0	5.5	V
(Note 2) Digital (DVDD pin)	DVDD	4.5	5.0	AVDD	V
Voltage Reference (Note 3)	VREF	2.5	-	AVDD	V

Notes: 2. AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. (★)

3. Analog output voltage scales with the voltage of VREF.
AOUT(typ. @0dB)=2.8Vpp*VREF/5。

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=5.0V; VREF=AVDD; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 20bit Input Data; Measurement Bandwidth=10Hz～20kHz; $R_L \geqq 5k\Omega$; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				20	Bits
Dynamic Characteristics (Note 4)					
THD+N (0dB Output)	(Note 5)	-78	-84		dB
(★) (-3dB Output)		-84	-88		dB
(-10dB Output)		-	-87		dB
Dynamic Range (-60dB Output)	(Note 6)	96	100		dB
S/N	(Note 7)	96	100		dB
S/N at Muting (ZMUTE="H")	(Note 7)	104	110		dB
Interchannel Isolation(1kHz)		100	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.1	0.2	dB
Gain Drift	(Note 8)		20	-	ppm/℃
DC Accuracy					
Output Voltage	(Note 9)	2.66	2.8	2.94	Vpp
Load Resistance		5			kΩ
Power Supplies					
Power Supply Current					
Normal Operation ($\overline{PD}$="H")					
AVDD			14.5	22	mA
DVDD			5.5	8	mA
Power-Down-Mode ($\overline{PD}$="L")					
AVDD+DVDD	(Note =)		10	50	uA
Power Dissipation (AVDD+DVDD)					
Normal Operation			100	150	mW
Power-Down-Mode	(Note =)		50	250	uW
Power Supply Rejection	(Note 11)		50		dB

Notes:4. Measured by AD725C(SHIBASOKU). Averaging mode.(★)
5. Inverse of S/(N+D).
6. A-weighted. 98dB(typ) at 16bit input data.
7. A-weighted. Digital input all zeros.
8. The voltage on VREF pin is held +5V externally.(★)
9. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF pin. AOUT(typ.@0dB)=2.8Vpp*VREF/5.
10. Power Dissipation in the power-down mode is applied with no external clocks (XTI, BICK, LRCK held "H" or "L").
11. PSR is applied to AVDD, DVDD with 1kHz, 600mVpp. VREF pin is held +5V.

FILTER CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=5.0V±10%; fs=44.1kHz; DEM0="1", DEM1="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ±0.06dB (Note 12)	PB	0		20.0	kHz
-6.0dB		-	22.05	-	kHz
Stopband (Note 12)	SB	24.1			kHz
Passband Ripple	PR			±0.06	dB
Stopband Attenuation	SA	43			dB
Group Delay (Note 13)	GD	-	14.7	-	1/fs
Digital Filter + Analog Filter					
Frequency Response 0~20.0kHz		-	±0.1	-	dB

Note: 12. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.06dB), SB=0.546*fs.

13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=5.0V±10%)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (ZMUTE pin)	VIH	90%DVDD	-	-	V
(All pins except ZMUTE pin)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage (ZMUTE pin)	VIL	-	-	10%DVDD	V
(All pins except ZMUTE pin)	VIL	-	-	30%DVDD	V
Input Voltage at AC coupilng (XTI pin)	VAC	1	-	-	Vpp
High-Level Output Voltage Iout=-20uA	VOH	DVDD-0.1	-	-	V
Low-Level Output Voltage Iout=20uA	VOL	-	-	0.1	V
Input Leakage Current (Note 14)	Iin	-	-	±10	uA

Note: 14. DIF0, DIF1, ZMUTE, SMUTE, HOLD, CKS pins have internal pull-down devices, nominally 90kΩ.

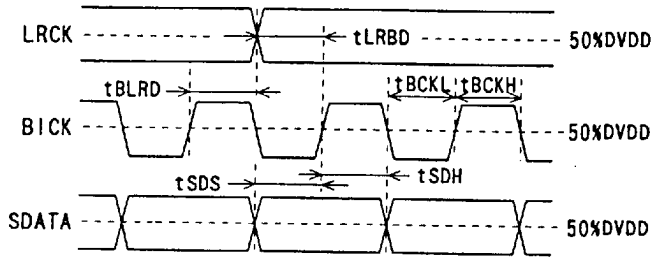
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=5.0V ± 10%; C_L = 20pF)

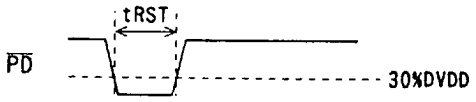
Parameter		Symbol	min	typ	max	Unit
Control Clock Frequency						
Crystal Resonator	256fs:	fCLK	7.10	11.2896	13.9	MHz
	384fs:	fCLK	10.70	16.9344	20.7	MHz
External Clock	256fs:	fCLK	4.096	11.2896	13.9	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	6.144	16.9344	20.7	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
LRCK Frequency	(Note 15)	fs	16	44.1	54	kHz
Serial Interface Timing	(Note 16)					
BICK Period		tBCK	290			ns
BICK Pulse Width Low		tBCKL	100			ns
Pulse Width High		tBCKH	100			ns
BICK rising to LRCK edge	(Note 17)	tBLRD	40			ns
LRCK Edge to BICK rising	(Note 17)	tLRBD	40			ns
SDATA Hold Time		tSDH	40			ns
SDATA Setup Time		tSDS	40			ns
Reset Timing						
$\overline{PD}$ Pulse Width	(Note 18)	tRST	100			ns

Notes: 15. If the duty of LRCK changes lager than ±1/8 from 50%, the AK4320 is reset by the internal phase circuit automatically.
16. Refer to the operating overview section "Serial Data Interface".
17. SCLK rising edge must not occur at the same time as L/$\overline{R}$ edge.
18. The AK4320 can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

■ Timing Diagram



Data Input Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4320 are XTI(256fs/384fs), LRCK(fs), BICK(64fs). The master clock (XTI) should be synchronized with LRCK but the phase is free of care. The XTI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of XTI is determined by the sampling rate(LRCK), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an XTI frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3) (Figure 1).

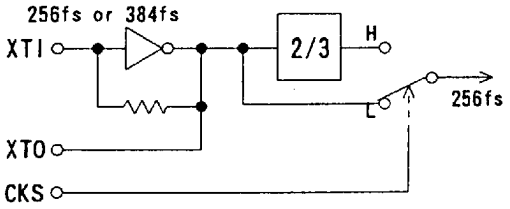


Figure 1. Internal Clock Circuit

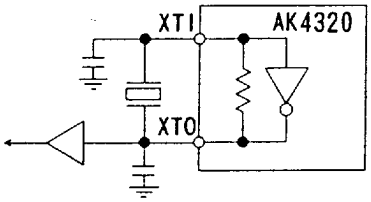


Figure 2. Crystal resonator connection

The master clock can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. Not only CMOS clock but sine wave signal with 1Vp-p can be input to the XTI pin by AC coupling. Table 1 illustrates standard audio word rates and corresponding frequencies used in the DAC.

LRCK (fs) (kHz)	CKS	XTI (MHz)
32.0	L	8.1920
	H	12.2880
44.1	L	11.2896
	H	16.9344
48.0	L	12.2880
	H	18.4320

Table 1. Examples of System Clock

As the AK4320 includes the phase detect circuit for LRCK, the AK4320 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not needed except only upon power-up. (Please refer to the "System Reset" section.)

All external clocks(XTI, BICK, LRCK) should always be present whenever the AK4320 is in normal operation mode($\overline{PD}$="H"). If these clocks are not provided, the AK4320 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4320 should be in the power-down mode($\overline{PD}$="L").

■ Serial Data Interface

Data is input to the AK4320 via three serial input pins(SDATA, BICK, LRCK). The AK4320 supports four serial data formats which can be selected via DIF0 and DIF1 pins(Table 2). Format 0 is compatible with existing 16-bit DACs and digital filters. Format 1 is an 20-bit version of format 0. Format 2 is similar to AKM ADCs (AK5339/69/40/45/89/90) and many DSP serial ports. Format 3 is compatible with the I²S serial data protocol. Format 2 and 3 support 20-bit input, 18-bit input followed by two zeros or 16-bit followed by four zeros. In all serial input modes, the serial data is MSB-first and 2's complement format.

DIF1	DIF0	Mode	Fig
0	0	0: LSB Justified, 16bit	3
0	1	1: LSB Justified, 20bit	3
1	0	2: MSB Justified, 16-20bit	4
1	1	3: I²S Compatible	5

Table 2. Digital Input Formats

*The use of 64fs clock is recommeded as BICK. (★)
*Mode 0 should be used if BICK is 32fs.

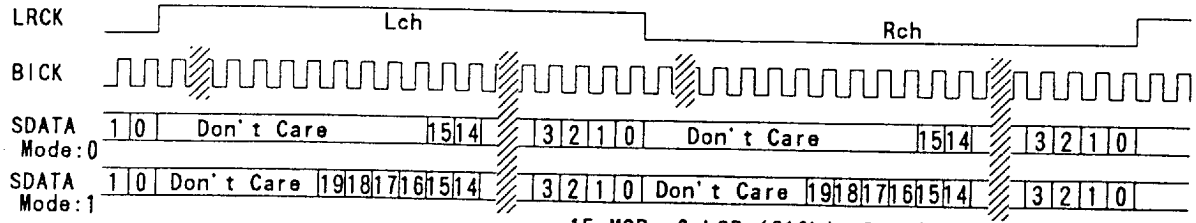


Figure 3. Digital Input Formats 0 & 1

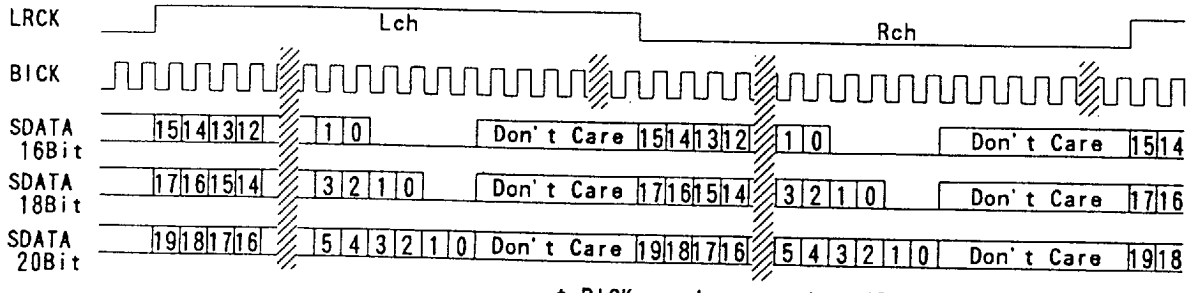


Figure 4. Digital Input Format 2

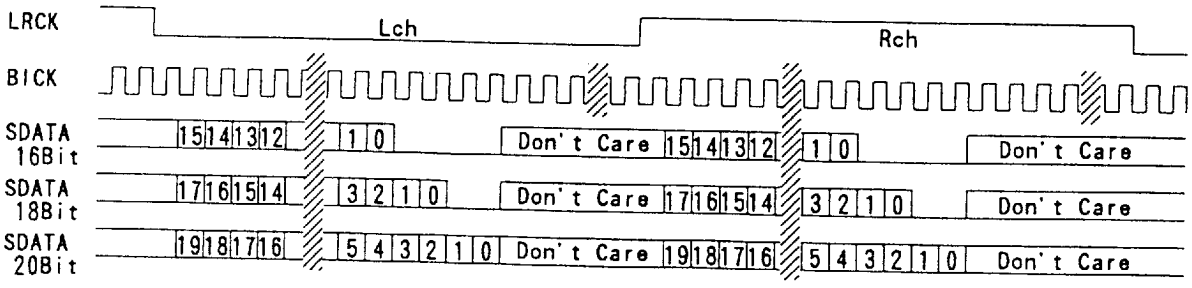


Figure 5. Digital Input Format 3

■ De-emphasis filter

The AK4320 includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three sampling frequencies(32kHz, 44.1kHz, 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 1. De-emphasis filter control

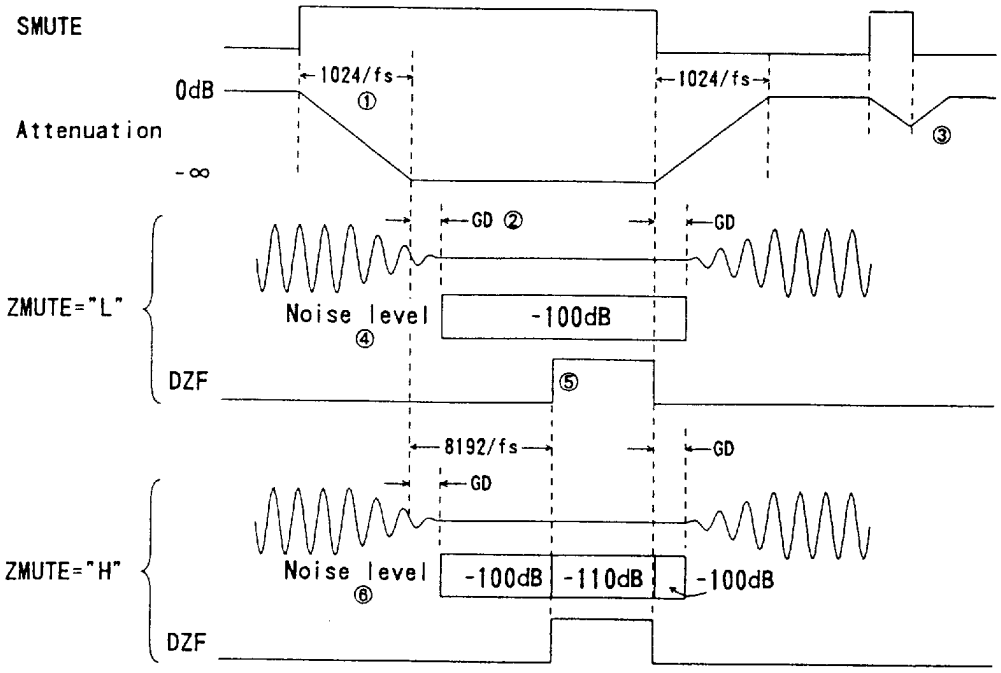
■ Zero detection & Zero mute operation

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H". Analog outputs condition at zero detection depends on the setting of ZMUTE pin. If ZMUTE is "H", analog outputs are muted at analog domain by zero detection. When ZMUTE is "L", Analog outputs aren't muted by zero detection. When muting by ZMUTE, the noise level on analog outputs is reduced up to the system noise level and the S/N is improved.

When ZMUTE is "H", the muting speed of analog outputs can be controlled by a capacitor on VCNT pin. For example, when VCNT pin connected to DVSS with a 0.01uF ceramic capacitor, it takes 20ms to mute the analog outputs.

■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. If ZMUTE is set "H" at the same time, analog outputs are muted by zero detection. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission. The soft mute function has also a hold mode. This mode can hold the attenuation level at soft mute. Please refer to Figure 7 about the operation.



Notes:

①The output signal is attenuated by -∞ during 1024 LRCK cycles(1024/fs).

②Analog output corresponding to digital input have the group delay(GD).

③If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

④As analog outputs aren't muted at ZMUTE "L", the noise level on analog outputs is -100dB.

⑤When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

⑥As analog outputs are muted at ZMUTE "H", the noise level on analog outputs is about -110dB.

Figure 6. Soft mute and zero detection (at HOLD="L")

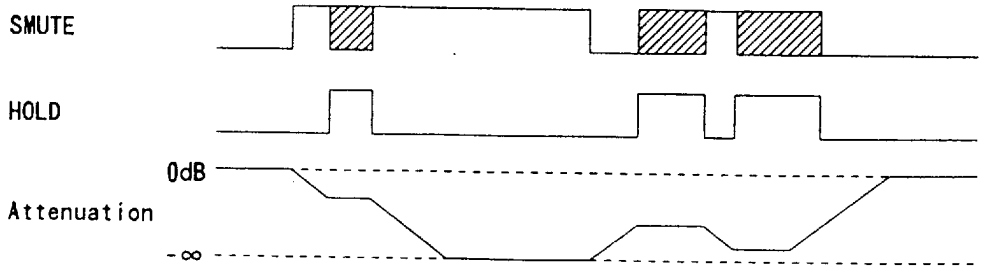
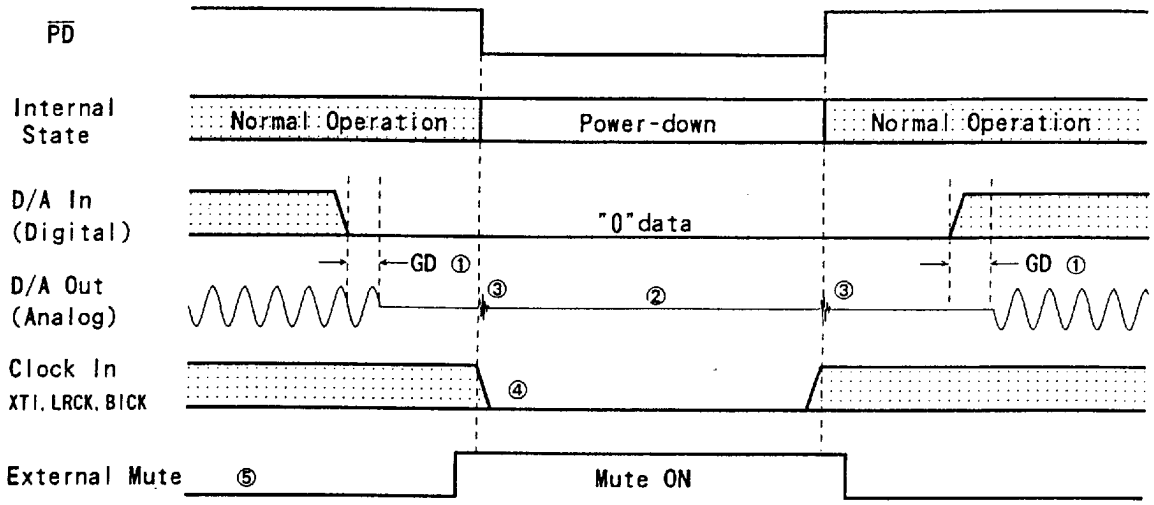


Figure 7. Soft mute with HOLD control

■ Power-Down

The AK4320 are placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 8 shows an example of the system timing at the power-down and power-up.



Notes:

①Analog output corresponding to digital input have the group delay(GD).

②Analog outputs are floating(Hi-Z) at the power-down mode. The output noise level is about -110dB.

③Click noise about -50dB occurs at the edges("↑ ↓") of $\overline{PD}$ signal. This noise is output even if ZMUTE is "H" and "0" data is input.(★)

④When the external clocks(XTI, BICK, LRCK) are stopped, the AK4320 should be in the power-down mode.

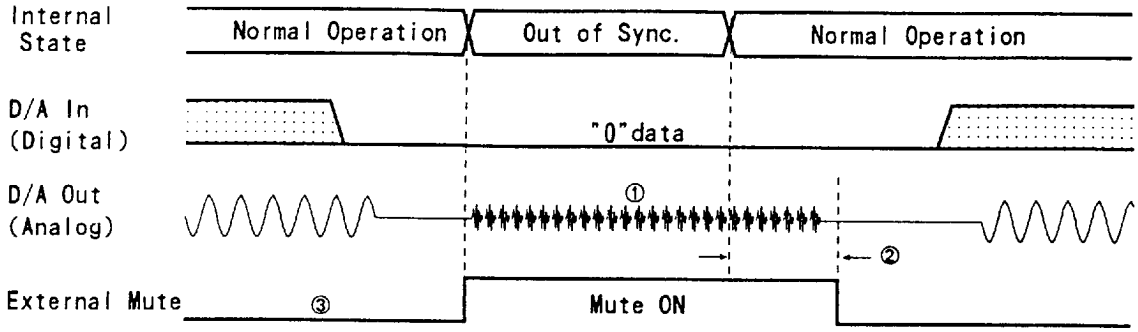
⑤Please mute the analog output externally if the click noise(③) influences system application. The timing example is shown in this figure.

Figure 8. Power-down/up sequence example

■ System Reset

The AK4320 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking by LRCK "↑" upon exiting reset.

If the phase difference between LRCK and internal control signals is larger than +1/16～-1/16 of word period(1/fs), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK. Since RAM address shifts during this synchronization, correct data would not be output until 14 sampled data are input. Refer to Figure 9.



When cycle ratio between LRCK and XTI can be not kept 1:256(1:384 at 384fs) by changing LRCK frequency etc., internal reset by out-of-synchronization may occur. Some noise occurs at resetting and after returning to normal operation. This noise also occurs evenif "0" data is being input to the AK4320.

①Click noise is output continuously when out-of-synchronization occurs continuously.
②Some noise occurs until 14*LRCK cycles after LRCK returns to normal condition.
③Please mute the analog output externally if there is possibility of out of synchronization in the application. The timing example is shown in this figure.

Figure 9. Out-of-synchronization timing example

SYSTEM DESIGN

Figure 10 shows the system connection diagram. An evaluation board[AKD4320] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

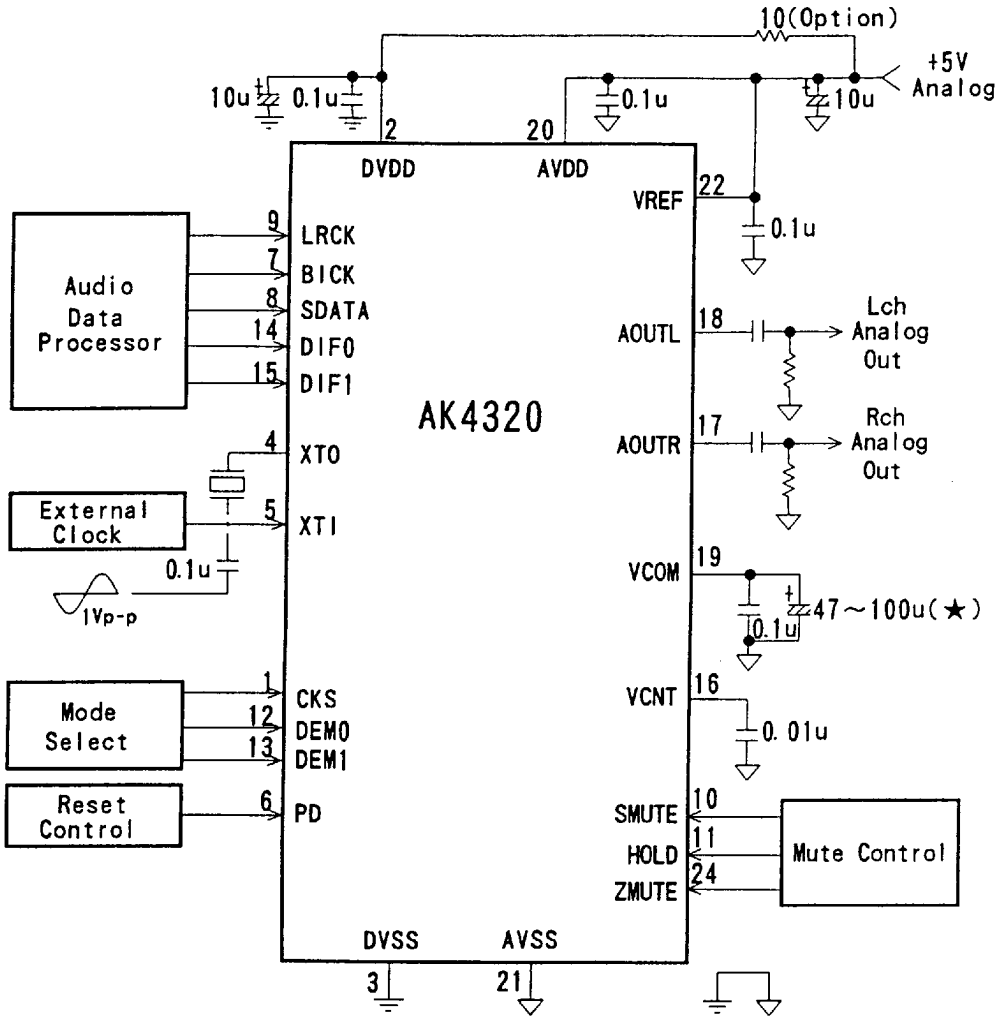


Figure 10. Typical Connection Diagram(★)

Notes:

- LRCK=fs, BICK≧64fs, XTI=256fs at CKS="L", XTI=384fs at CKS="H".
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency as possible, with the low value ceramic capacitor being the nearest.

2. Voltage reference

The differential Voltage between VREF and AVSS set the analog output range. VREF pin is normally connected to AVDD with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor around 47uF in parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4320.

3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.8Vpp(1Vrms). AC coupling capacitors of larger than 1uF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit). The output signal is inverted by using the circuit in figure 11.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV. Figure 11 shows the example of external op-amp circuit with 6dB gain.

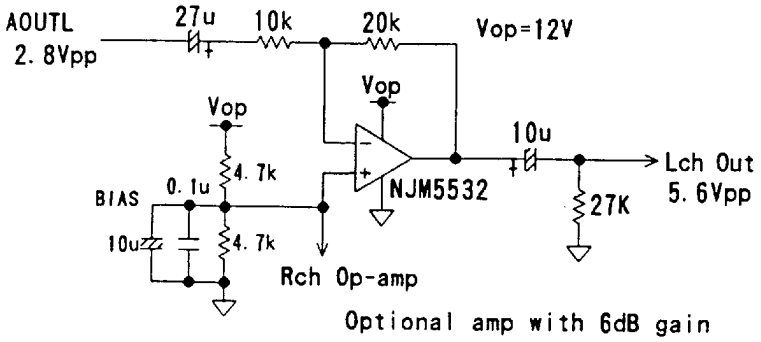
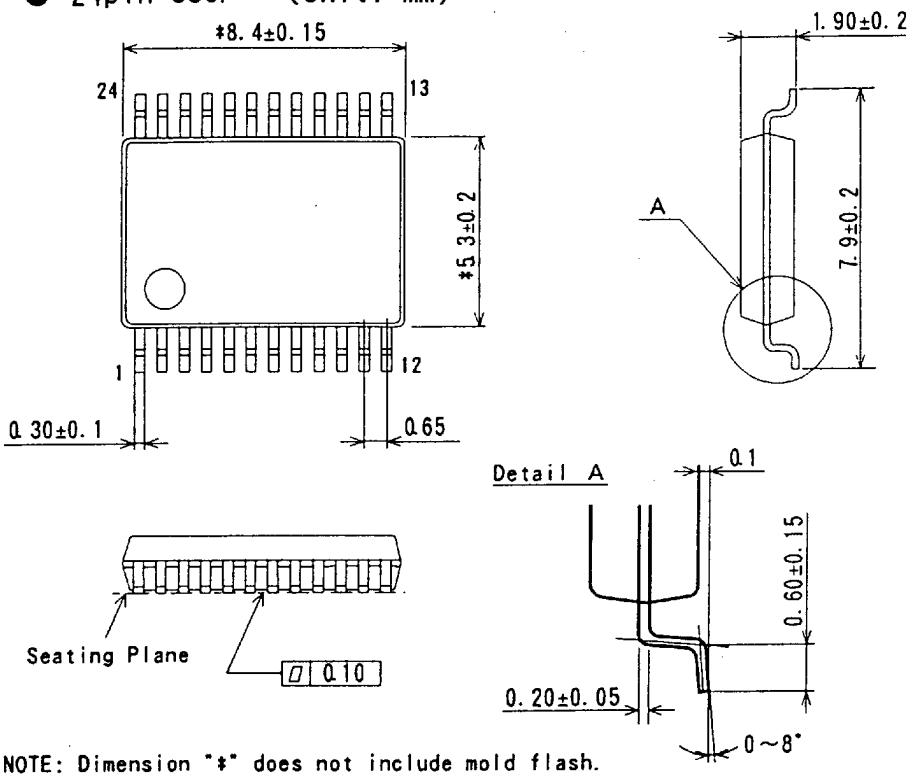


Figure 11. External analog circuit example(gain=6dB)

PACKAGE

● 24pin SSOP (Unit: mm)

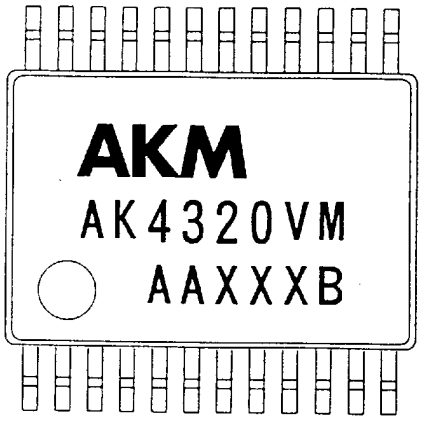


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound :	Epoxy
Lead frame material :	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXB

AA : Lot# (alphabet)

XXXB : Date Code (X : numbers, B : alphabet)