AsahiKASEI
ASAHI KASEI EMD

AK4372

DAC with built-in PLL & HP-AMP

GENERAL DESCRIPTION

The AK4372 is a 24-bit DAC with an integrated PLL and headphone amplifier. The PLL input frequency is synchronized to typical mobile phone clock frequencies. The AK4372 features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features "pop-noise free" power-on/off, a mute control, and it delivers 40mW of power into 16Ω. The AK4372 is packaged in a 24-pin CSP (2.5mm×2.5mm) package, ideal for portable applications.

FEATURE

- ☐ Multi-bit ΔΣ DAC
- ☐ Sampling Rate
  - 8kHz ~ 48kHz
- ☐ On chip perfect filtering 8 times FIR interpolator
  - Passband: 20kHz
  - Passband Ripple: ±0.02dB
  - Stopband Attenuation: 54dB
- ☐ Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz
- ☐ System Clock
  - PLL Mode (MCKI): 27MHz, 26MHz, 19.8MHz, 19.68MHz, 19.2MHz, 15.36MHz, 14.4MHz, 13MHz, 12MHz and 11.2896MHz
  - PLL Mode (BICK or LRCK): 64fs, 32fs or fs
  - EXT Mode: 256fs/384fs/512fs/768fs/1024fs
  - Input Level: AC Couple Input Available
- ☐ Audio I/F Format: MSB First, 2's Complement
  - I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified
  - Master/Slave Mode
- ☐ Digital Mixing: LR, LL, RR, (L+R)/2
- ☐ Bass Boost Function
- ☐ Digital ATT
- ☐ Analog Mixing Circuit: 3 Inputs (Single-ended or Full-differential)
- ☐ Stereo Lineout
  - S/N: 90dB@3.3V
  - Output Volume: +6 to –24dB (or 0 to –30dB), 2dB step
- ☐ Headphone Amplifier
  - Output Power: 40mW x 2ch @16Ω, 3.3V
  - S/N: 92dB@3.3V
  - Pop Noise Free at Power-ON/OFF and Mute
  - Output Volume: 0 ~ –63dB & +12/+6/0 dB Gain
    1.5dB step (0 ~ –30dB), 3dB step (–30 ~ –63dB)
- ☐ μP Interface: 3-wire/I^2C
- ☐ Power Supply: 1.6V ~ 3.6V
- ☐ Power Supply Current: 3.8mA @1.8V (6.8mW, DAC+HP, No output)
- ☐ AK4372ECB: Ta= –30 ~ 85°C
  AK4372VCB: Ta= –40 ~ 85°C
- ☐ Small Package: 24pin CSP (2.5mm x 2.5mm, 0.4mm pitch)
- ☐ Register Compatible with AK4368

■ Block Diagram

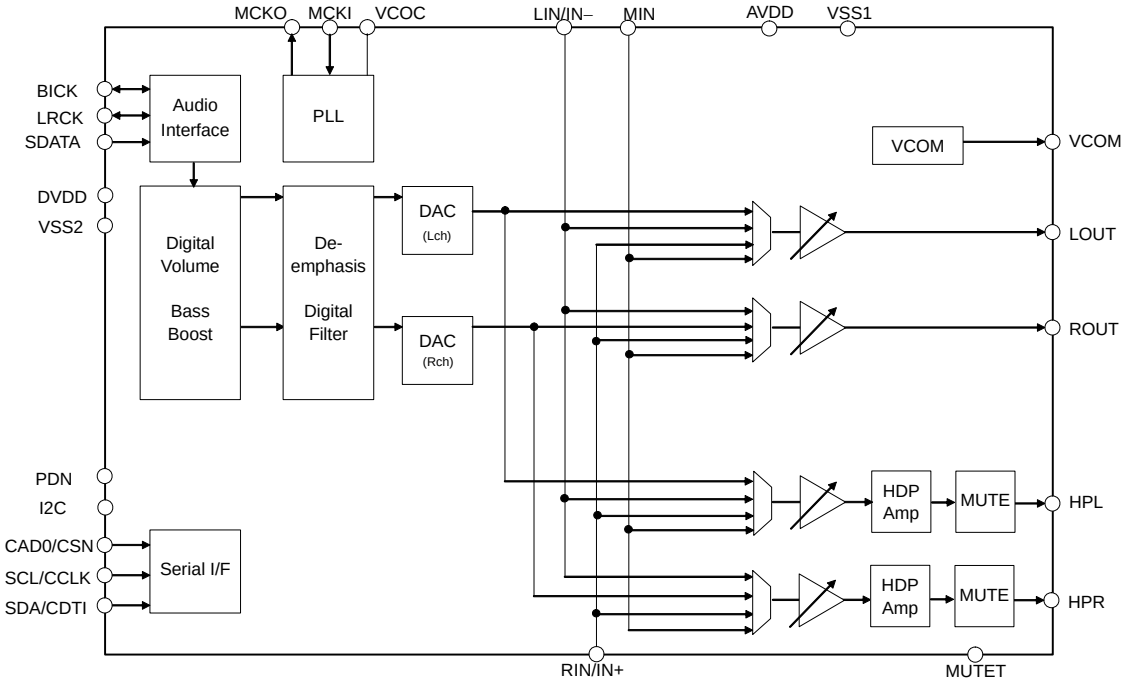
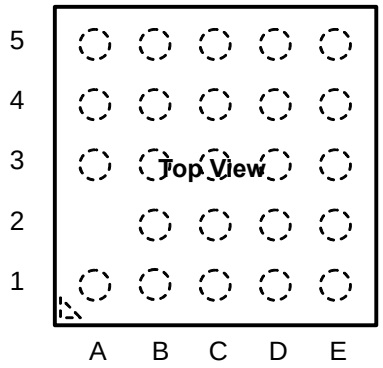


Figure 1. Block Diagram

■ Ordering Guide

AK4372ECB	–30 ~ +85°C	24pin CSP (0.4mm pitch)	Black Type
AK4372VCB	–40 ~ +85°C	24pin CSP (0.4mm pitch)	Black Type
AKD4372	Evaluation board for AK4372		

■ Pin Layout



5	VSS2	CCLK	CSN	PDN	MUTET
4	VCOC	MCKO	CDTI	LOUT	ROUT
3	MCKI	LRCK	DVDD	I2C	VCOM
2		BICK	LIN	HPR	AVDD
1	SDATA	RIN	MIN	HPL	VSS1
	A	B	C	D	E

Top View

■ Comparison with AK4370/71

1 Function

Function	AK4370	AK4371	AK4372
Analog Mixing	2-Stereo Single-ended Input or Full-differential Input	3-Stereo Single-ended Input or Full-differential Input	1-Stereo + 1-Mono Single-ended Input or Full-differential Input
PLL	No	Yes	Yes
Internal VREF	No	Yes	No
Hands-free Amp	No	Yes	No
Ta	–30 ~ +85°C	–30 ~ +85°C	AK4372ECB: –30 ~ +85°C AK4372VCB: –40 ~ +85°C
Package	24 pin QFN (4mm x 4mm, 0.5mm pitch)	32 pin QFN (4mm x 4mm, 0.4mm pitch)	24 pin CSP (2.5mm x 2.5mm, 0.4mm pitch)

2 Register (difference from AK4370/71)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	~~PMVREF~~	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	Clock Control	PLL4	0	M/S	MCKAC	BF	PS0	PS1	MCKO
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
07H	Headphone Out Select 0	HPG1	HPG0	MINHR	MINHL	RINHR	LINHL	DARHR	DALHL
08H	Lineout Select 0	0	LOG	MINR	MINL	RINR	LINL	DARR	DALL
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
0AH	Reserved	0	0	0	0	0	0	0	0
0BH	Reserved	0	0	0	0	0	0	0	0
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Headphone Out Select 1	~~RIN3HR~~	~~RIN3HL~~	~~LIN3HR~~	~~LIN3HL~~	~~RIN2HR~~	~~RIN2HL~~	LINHR	RINHL
0EH	Headphone ATT	0	HPZ	HMUTE	ATTH4	ATTH3	ATTH2	ATTH1	ATTH0
0FH	Lineout Select 1	~~RIN3R~~	~~RIN3L~~	~~LIN3R~~	~~LIN3L~~	~~RIN2R~~	~~RIN2L~~	LINR	RINL
10H	Mono Mixing	0	0	~~L3M~~	~~L3HM~~	~~L2M~~	~~L2HM~~	LM	LHM
11H	Differential Select	0	0	0	0	0	~~LDIFM~~	LDIFH	LDIF
12H	Reserved	~~RIN3M~~	~~LIN3M~~	~~RIN2M~~	~~LIN2M~~	~~RIN1M~~	~~LIN1M~~	~~DARM~~	~~DALM~~
13H	Reserved	0	~~PMMO~~	~~MOG~~	~~MMUTE~~	~~ATTM3~~	~~ATTM2~~	~~ATTM1~~	~~ATTM0~~

These bits are changed from the AK4370/71.
These bits are deleted in the AK4372.
These bits are deleted in the AK4370.

PIN/FUNCTION

No.	Pin Name	I/O	Function
A1	SDATA	I	Audio Serial Data Input Pin
B2	BICK	I/O	Audio Serial Data Clock Pin
B3	LRCK	I/O	Input / Output Channel Clock Pin
A3	MCKI	I	External Master Clock Input Pin
C3	DVDD	-	Digital Power Supply Pin, 1.6 ~ 3.6V
A4	VCOC	O	Output for Loop Filter of PLL Circuit This pin must be connected to VSS2 with one resistor and one capacitor in series.
A5	VSS2	-	Ground 2 Pin. Connected to VSS1.
B4	MCKO	O	Master Clock Output Pin
C4	SDA	I/O	Control Data Input/Output Pin (I2C mode : I2C pin = "H")
	CDTI	I	Control Data Input Pin (3-wire serial mode : I2C pin = "L")
B5	SCL	I	Control Data Clock Pin (I2C mode : I2C pin = "H")
	CCLK	I	Control Data Clock Pin (3-wire serial mode : I2C pin = "L")
C5	CAD0	I	Chip Address 0 Select Pin (I2C mode : I2C pin = "H")
	CSN	I	Chip Select Pin (3-wire serial mode : I2C pin = "L")
D5	PDN	I	Power-down & Reset When "L", the AK4372 is in power-down mode and is held in reset. The AK4372 must be reset once upon power-up.
D3	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
E5	MUTET	O	Mute Time Constant Control pin Connected to the VSS1 pin with a capacitor for mute time constant.
D4	LOUT	O	Lch Stereo Line Output Pin
E4	ROUT	O	Rch Stereo Line Output Pin
E3	VCOM	O	Common Voltage Output Pin Normally connected to the VSS1 pin with a 2.2μF electrolytic capacitor.
E2	AVDD	-	Analog & PLL Power Supply Pin, 1.6 ~ 3.6V
E1	VSS1	-	Ground 1 Pin
D2	HPR	O	Rch Headphone Amp Output
D1	HPL	O	Lch Headphone Amp Output
C1	MIN	I	Mono Analog Input Pin
B1	RIN	I	Rch Analog Input Pin (LDIF bit ="0" : Single-ended Input)
	IN+	I	Positive Line Input Pin (LDIF bit ="1" : Full-differential Input)
C2	LIN	I	Rch Analog Input Pin (LDIF bit ="0" : Single-ended Input)
	IN−	I	Negative Line Input Pin (LDIF bit ="1" : Full-differential Input)

Note 1. All digital input pins (I2C, SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN) must not be left floating. The MCKI pin can be left floating only when the PDN pin = "L".

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT, ROUT, MUTET, HPR, HPL, MIN, RIN/IN+, LIN/IN–	These pins must be open.
Digital	MCKI	This pin must be connected to VSS2.
	MCKO	This pin must be open.

ABSOLUTE MAXIMUM RATING

(VSS1 = VSS2 =0V; Note 2, Note 3)

Parameter			Symbol	min	max	Units
Power Supplies	Analog		AVDD	–0.3	4.6	V
	Digital		DVDD	–0.3	4.6	V
Input Current (any pins except for supplies)			IIN	-	±10	mA
Analog Input Voltage (Note 4)			VINA	–0.3	(AVDD+0.3) or 4.6	V
Digital Input Voltage (Note 5)			VIND	–0.3	(DVDD+0.3) or 4.6	V
Ambient Temperature		AK4372ECB	Ta	–30	85	°C
		AK4372VCB	Ta	–40	85	°C
Storage Temperature			Tstg	–65	150	°C

Note 2. All voltages with respect to ground.

Note 3. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 4. LIN/IN−, RIN/IN+ and MIN pins. Max is smaller value between (AVDD+0.3)V and 4.6V.

Note 5. SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN and I2C pins. Max is smaller value between (DVDD+0.3)V and 4.6V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1 = VSS2 =0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	1.6	2.4	3.6	V
(Note 6)	Digital (Note 7)	DVDD	1.6	2.4	(AVDD+0.2) or 3.6	V

Note 1. All voltages with respect to ground.

Note 6. When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. When the AK4372 is powered-down, DVDD should be powered-down at the same time or later than AVDD.

Note 7. Max is smaller value between (AVDD+0.2)V and 3.6V.

* AKEMD assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=2.4V, VSS1=VSS2=0V; fs=44.1kHz; EXT mode; BOOST OFF; Slave Mode; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; Headphone-Amp: Load impedance is a serial connection with R_L =16Ω and C_L=220μF. (Refer to Figure 50; unless otherwise specified)

Parameter			min	typ	max	Units
DAC Resolution			-	-	24	bit
Headphone-Amp: (HPL/HPR pins) (Note 8)						
Analog Output Characteristics						
THD+N	–3dBFS Output, 2.4V, Po=10mW@16Ω		-	–50	–40	dB
	0dBFS Output, 3.3V, Po=40mW@16Ω		-	–20	-	dB
D-Range	–60dBFS Output, A-weighted, 2.4V		82	90	-	dB
	–60dBFS Output, A-weighted, 3.3V		-	92	-	dB
S/N	A-weighted, 2.4V		82	90	-	dB
	A-weighted, 3.3V		-	92	-	dB
Interchannel Isolation			60	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.3	0.8	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 9)			16	-	-	Ω
Load Capacitance			-	-	300	pF
Output Voltage	–3dBFS Output (Note 10)		1.04	1.16	1.28	Vpp
	0dBFS Output, 3.3V, Po=40mW@16Ω		-	0.8	-	Vrms
Output Volume: (HPL/HPR pins)						
Step Size (HPG1-0 bits = "00")	0 ~ –30dB		0.1	1.5	2.9	dB
	–30 ~ –63dB		0.1	3	5.9	dB
Gain Control Range (HPG1-0 bits = "00")	Max (ATT4-0 bits = 00H)		-	0	-	dB
	Min (ATT4-0 bits = 1FH)		-	–63	-	dB
Stereo Line Output: (LOUT/ROUT pins, R_L=10kΩ) (Note 11)						
Analog Output Characteristics:						
THD+N (0dBFS Output)			-	–60	–50	dB
S/N	A-weighted, 2.4V		80	87	-	dB
	A-weighted, 3.3V		-	90	-	dB
DC Accuracy						
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 9)			10	-	-	kΩ
Load Capacitance			-	-	25	pF
Output Voltage (0dBFS Output) (Note 12)			1.32	1.47	1.61	Vpp
Output Volume: (LOUT/ROUT pins)						
Step Size			1	2	3	dB
Gain Control Range (LOG1-0 bit = "0")	Max (ATTS3-0 bits = FH)		-	0	-	dB
	Min (ATTS3-0 bits = 0H)		-	–30	-	dB

Note 8. DALHL=DARHR bits = "1", LINHL=RINHL=MINHL=LINHR=RINHR=MINHR bits = "0".
Note 9. AC load.
Note 10. Output voltage is proportional to AVDD voltage. Vout = 0.48 x AVDD(typ)@–3dBFS.
Note 11. DALL=DARR bits = "1", LINL=RINL=MINL=LINR=RINR=MINR bits = "0"
Note 12. Output voltage is proportional to AVDD voltage. Vout = 0.61 x AVDD(typ)@0dBFS.

Parameter	min	typ	max	Units
LINEIN: (LIN/RIN/MIN pins)				
Analog Input Characteristics				
Input Resistance (See Figure 25, Figure 26, Figure 27)				
LIN pin				
LINHL=LINHR=LINL=LINR= bits = "1"	14	25	-	kΩ
LINHL bit = "1", LINHR=LINL=LINR bits = "0"	-	100	-	kΩ
LINHR bit = "1", LINHL=LINL=LINR bits = "0"	-	100	-	kΩ
LINL bit = "1", LINHL=LINHR=LINR bits = "0"	-	100	-	kΩ
LINR bit = "1", LINHL=LINHR=LINL bits = "0"	-	100	-	kΩ
RIN pin				
RINHL=RINHR=RINL=RINR bits = "1"	14	25	-	kΩ
RINHL bit = "1", RINHR=RINL=RINR bits = "0"	-	100	-	kΩ
RINHR bit = "1", RINHL=RINL=RINR bits = "0"	-	100	-	kΩ
RINL bit = "1", RINHL=RINHR=RINR bits = "0"	-	100	-	kΩ
RINR bit = "1", RINHL=RINHR=RINL bits = "0"	-	100	-	kΩ
MIN pin				
MINHL=MINHR=MINL=MINR bits = "1"	14	25	-	kΩ
MINHL bit = "1", MINHR=MINL=MINR bits = "0"	-	100	-	kΩ
MINHR bit = "1", MINHL=MINL=MINR bits = "0"	-	100	-	kΩ
MINL bit = "1", MINHL=MINHR=MINR bits = "0"	-	100	-	kΩ
MINR bit = "1", MINHL=MINHR=MINL bits = "0"	-	100	-	kΩ
Gain				
LIN/RIN/MIN → LOUT/ROUT	–1	0	+1	dB
LIN/RIN/MIN → HPL/HPR	–0.05	+0.95	+1.95	dB
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H") (Note 13)				
AVDD+DVDD	-	5.0	8.0	mA
Power-Down Mode (PDN pin = "L") (Note 14)	-	1	100	μA

Note 13. PMDAC=PMHPL=PMHPR=PMLO bits = "1", MUTEN bit = "1", MCKO bit = "0", HP-Amp no output.
PMDAC=PMHPL=PMHPR= "1", PMLO bit= "0", AVDD+DVDD=4.0mA (typ) @2.4V, 3.8mA (typ) @1.8V.
Note 14. All digital input pins are fixed to VSS2.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD = DVDD=1.6 ~ 3.6V; fs=44.1kHz; De-emphasis = OFF)

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 15)							
Passband (Note 16)		–0.05dB	PB	0	-	20.0	kHz
		–6.0dB		-	22.05	-	kHz
Stopband (Note 16)			SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay (Note 17)			GD	-	22	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter: (Note 15, Note 18)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
Analog Filter: (Note 19)							
Frequency Response	0 ~ 20.0kHz		FR	-	±1.0	-	dB
BOOST Filter: (Note 18, Note 20)							
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 15. BOOST OFF (BST1-0 bit = "00")
Note 16. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535fs(@–0.05dB). SB=0.546fs(@–54dB).
Note 17. This time is from setting the 24-bit data of both channels from the input register to the output of analog signal.
Note 18. DAC → HPL, HPR, LOUT, ROUT
Note 19. LIN/MIN → HPL/LOUT, RIN/MIN → HPR/ROUT
Note 20. These frequency responses scale with fs. If high-level signal is input, the output clips at low frequency.

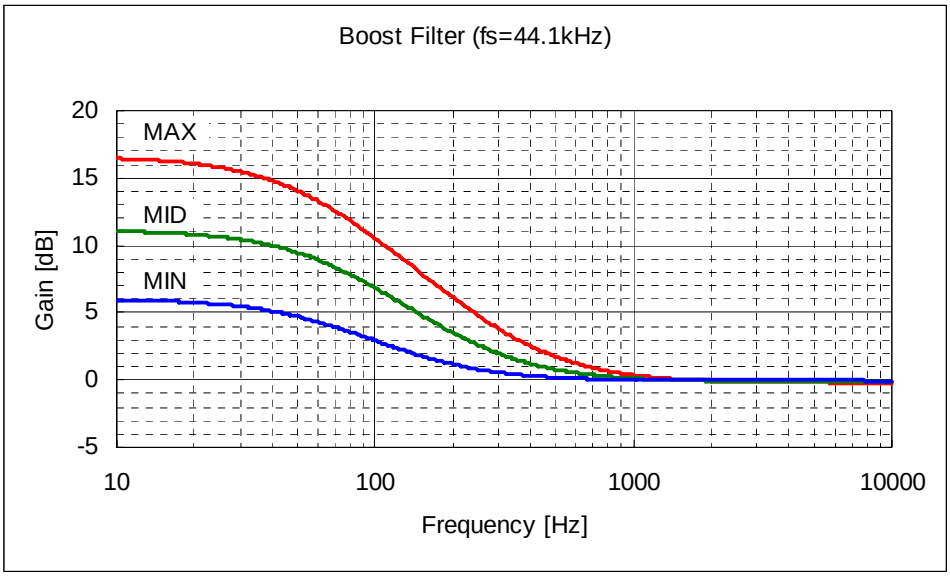


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; AVDD = DVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 21)		VAC	0.4	-	-	Vpp
High-Level Output Voltage (Iout=–200μA)		VOH	DVDD–0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout=200μA)		VOL	-	-	0.2	V
(SDA pin, 2.0V≤DVDD≤3.6V: Iout=3mA)		VOL	-	-	0.4	V
(SDA pin, 1.6V≤DVDD<2.0V: Iout=3mA)		VOL	-	-	20%DVDD	V
Input Leakage Current		Iin	-	-	±10	μA

Note 21. The MCKI pin is connected to a capacitor. (Figure 50)

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD = DVDD=1.6 ~ 3.6V; C_L = 20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Master Clock Input Timing					
Frequency (PLL mode)	fCLK	11.2896	-	27	MHz
(EXT mode)	fCLK	2.048	-	24.576	MHz
Pulse Width Low (Note 22)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High (Note 22)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width (Note 23)	tACW	18.5	-	-	ns
LRCK Timing					
Frequency	fs	8	44.1	48	kHz
Duty Cycle: Slave Mode	Duty	45	-	55	%
Master Mode	Duty	-	50	-	%
MCKO Output Timing (PLL mode)					
Frequency	fCLKO	0.256	-	12.288	MHz
Duty Cycle (Except fs=32kHz, PS1-0= "00")	dMCK	40	-	60	%
(fs=32kHz, PS1-0= "00")	dMCK	-	33	-	%
Serial Interface Timing (Note 24)					
Slave Mode (M/S bit = "0"):					
BICK Period (Note 25)					
(Except PLL Mode, PLL4-0 bit = "01110", "01111")	tBCK	312.5 or 1/(64fs)	-	1/(32fs)	ns
(PLL Mode, PLL4-0 bits = "01110")	tBCK	-	1/(32fs)	-	ns
(PLL Mode, PLL4-0 bits = "01111")	tBCK	-	1/(64fs)	-	ns
BICK Pulse Width Low					
(Except PLL Mode, PLL4-0 bit = "01110", "01111")	tBCKL	100	-	-	ns
(PLL Mode, PLL4-0 bit = "01110", "01111")	tBCKL	0.4 x tBCK	-	-	ns
BICK Pulse Width High					
(Except PLL Mode, PLL4-0 bit = "01110", "01111")	tBCKH	100	-	-	ns
(PLL Mode, PLL4-0 bit = "01110", "01111")	tBCKH	0.4 x tBCK	-	-	ns
LRCK Edge to BICK "↑" (Note 26)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 26)	tBLR	50	-	-	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Master Mode (M/S bit = "1"):					
BICK Frequency (BF bit = "1")	fBCK	-	64fs	-	Hz
(BF bit = "0")	fBCK	-	32fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–50	-	50	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 27)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 27)	tCSH	50	-	-	ns

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 28)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 29)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 30)	tPD	150	-	-	ns

Note 22. Except AC coupling.
Note 23. Pulse width to ground level when the MCKI pin is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3.)
Note 24. Refer to "Serial Data Interface".
Note 25. Min is longer value between 312.5ns or 1/(64fs) except for PLL Mode, PLL4-0 bits = "01110", "01111".
Note 26. BICK rising edge must not occur at the same time as LRCK edge.
Note 27. CCLK rising edge must not occur at the same time as CSN edge.
Note 28. I^2C is a registered trademark of Philips Semiconductors.
Note 29. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 30. When power-up, the AK4372 can be reset by bringing PDN pin = "H" from "L".

■ Timing Diagram

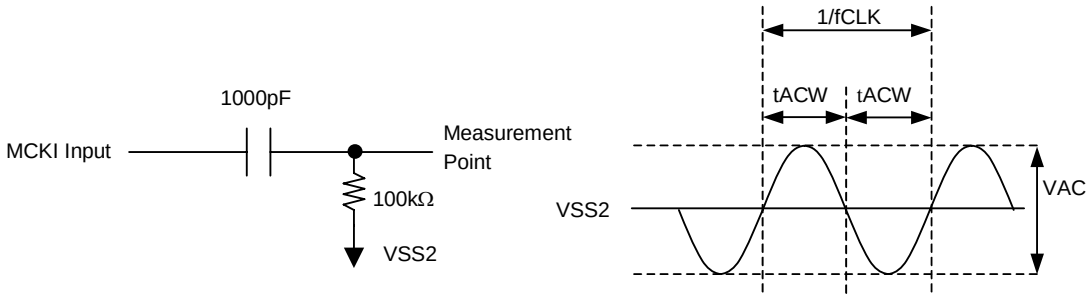


Figure 3. MCKI AC Coupling Timing

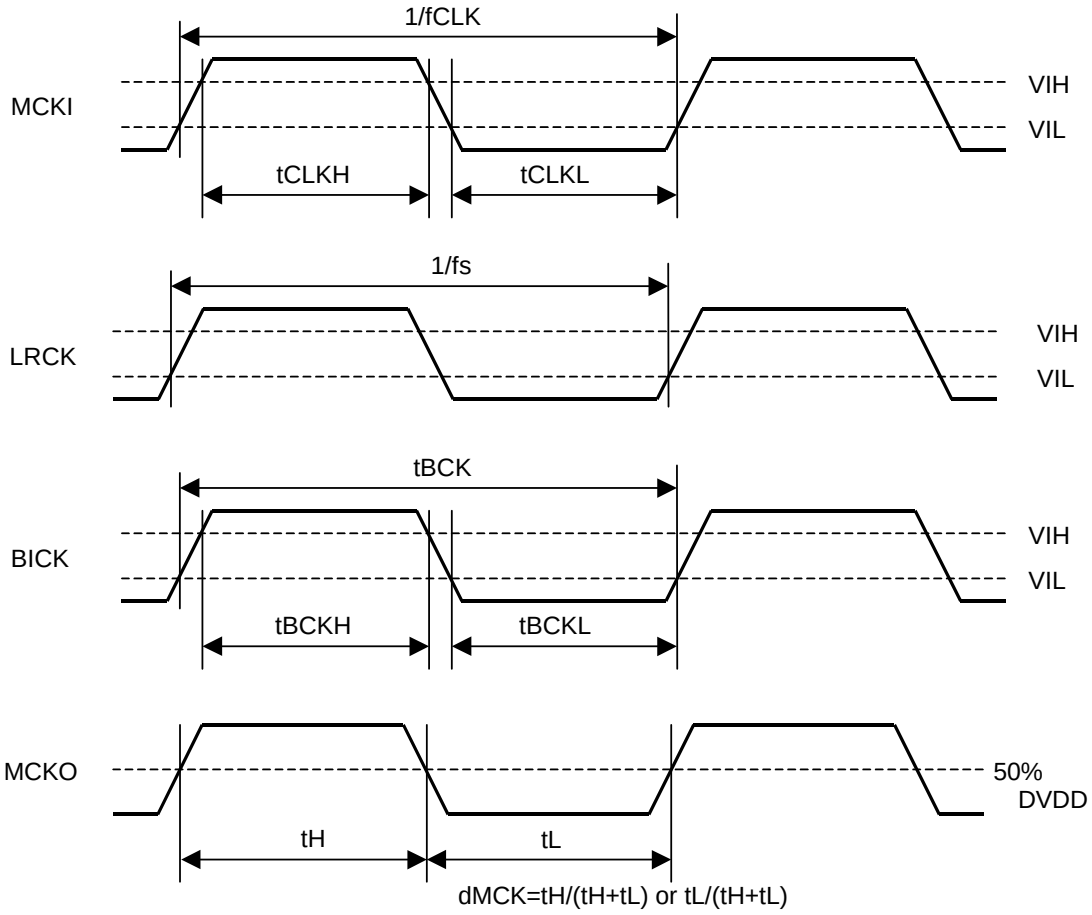


Figure 4. Clock Timing

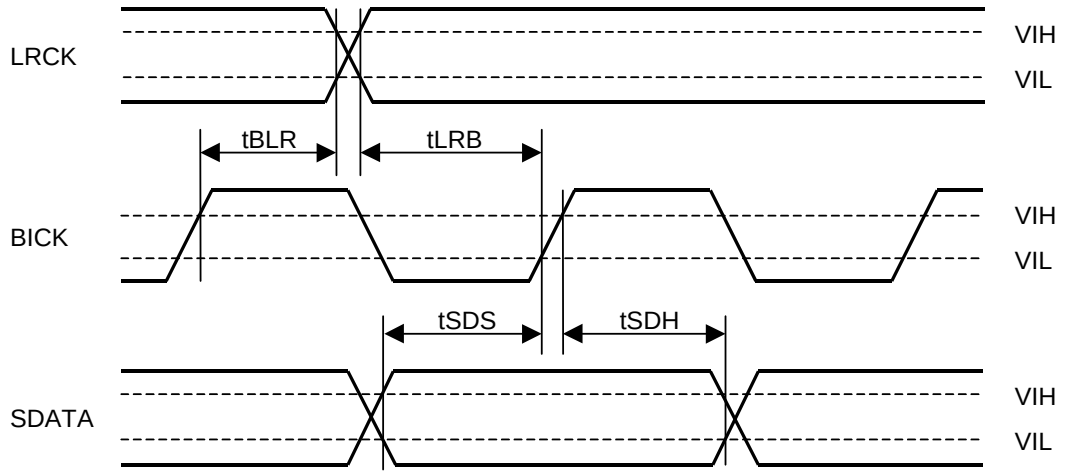


Figure 5. Serial Interface Timing (Slave Mode)

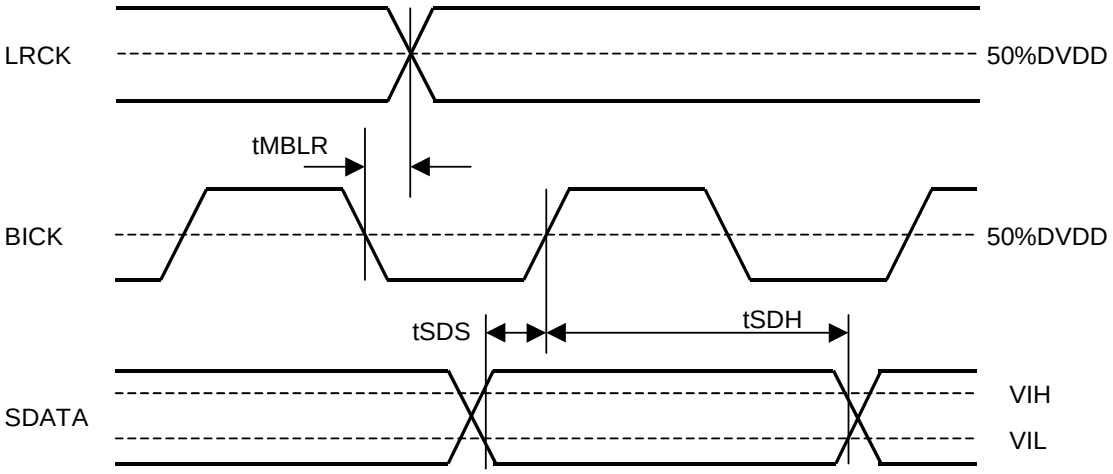


Figure 6. Serial Interface Timing (Master mode)

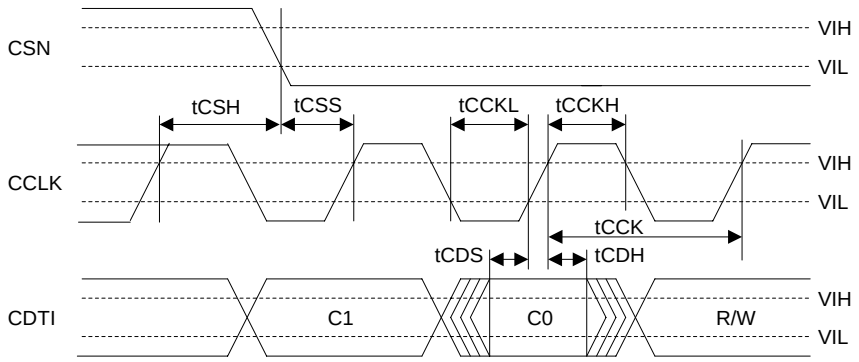


Figure 7. WRITE Command Input Timing

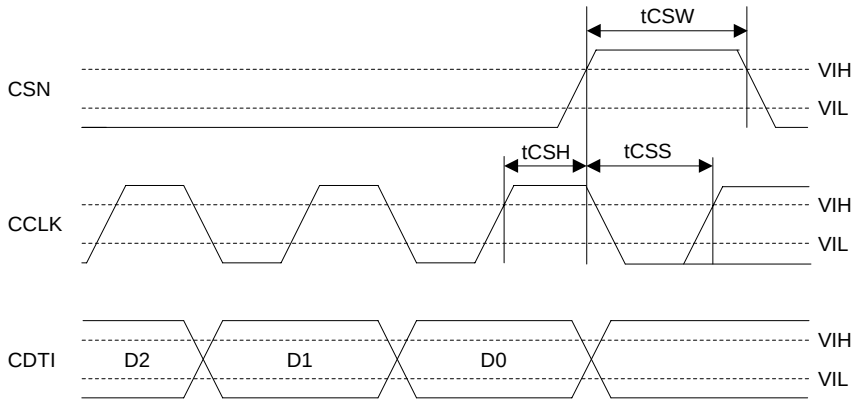


Figure 8. WRITE Data Input Timing

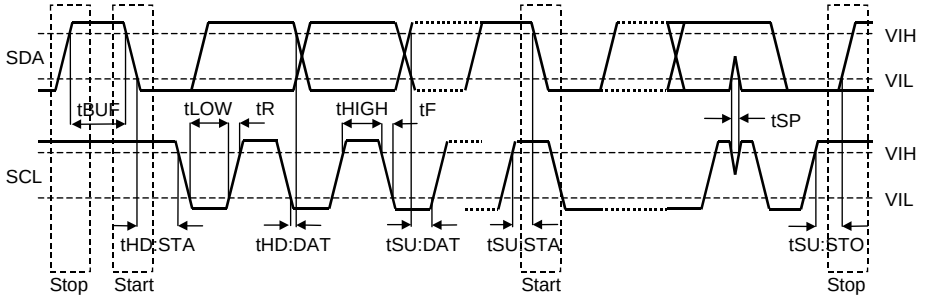


Figure 9. I^{2}C Bus Mode Timing

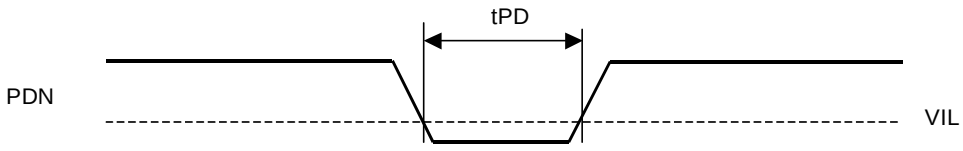


Figure 10. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

There are the following six clock modes to interface with external devices (Table 1 and Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	See Table 4	Figure 11
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 12
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	1	0	See Table 4	Figure 13
PLL Slave Mode 3 (PLL Reference Clock: LRCK pin)	1	0	See Table 4	Figure 14
EXT Master Mode	0	1	x	Figure 15
EXT Slave Mode	0	0	x	Figure 16

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL4-0 bits	Output (Selected by BF bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL4-0 bits	Input (32fs ~ 64fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	0	L	GND	Input (Selected by PLL4-0 bits)	Input (1fs)
PLL Slave Mode 3 (PLL Reference Clock: LRCK pin)	0	L	GND	Input (32fs ~ 64fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS3-0 bits	Output (Selected by BF bit)	Output (1fs)
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (32fs ~ 64fs)	Input (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4372 is power-down mode (PDN pin = "L") and exits reset state, the AK4372 is slave mode. After exiting reset state, the AK4372 changes to master mode by setting M/S bit = "1".

When the AK4372 is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4372 should be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode (PMPLL bit = "1")

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL4-0 and FS3-0 bits (Table 4, Table 5, Table 6). The PLL lock time is shown in Table 4, whenever the AK4372 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL4	PLL3	PLL2	PLL1	PLL0	Reference Clock		fs (Note 31)	R,C at VCOC		PLL Lock Time (typ)	
									R[Ω]	C[F]		
0	0	0	0	0	0	MCKI	11.2896MHz	Type 1	10k	22n	20ms	(default)
1	0	0	0	0	1	MCKI	14.4MHz	Type 1	10k	22n	20ms	
2	0	0	0	1	0	MCKI	12MHz	Type 1	10k	47n	20ms	
3	0	0	0	1	1	MCKI	19.2MHz	Type 1	10k	22n	20ms	
4	0	0	1	0	0	MCKI	15.36MHz	Type 1	10k	22n	20ms	
5	0	0	1	0	1	MCKI	13MHz	Type 1	15k	330n	100ms	
6	0	0	1	1	0	MCKI	19.68MHz	Type 1	10k	47n	20ms	
7	0	0	1	1	1	MCKI	19.8MHz	Type 1	10k	47n	20ms	
8	0	1	0	0	0	MCKI	26MHz	Type 1	15k	330n	100ms	
9	0	1	0	0	1	MCKI	27MHz	Type 1	10k	47n	20ms	
10	0	1	0	1	0	MCKI	13MHz	Type 2	10k	22n	20ms	
11	0	1	0	1	1	MCKI	26MHz	Type 2	10k	22n	20ms	
12	0	1	1	0	0	MCKI	19.8MHz	Type 3	10k	22n	20ms	
13	0	1	1	0	1	MCKI	27MHz	Type 4	10k	22n	20ms	
14	0	1	1	1	0	BICK	32fs	Table 6	6.8k	47n	20ms	
15	0	1	1	1	1	BICK	64fs	Table 6	6.8k	47n	20ms	
16	1	0	0	0	0	LRCK	fs	Table 6	6.8k	330n	80ms	
Others	Others					N/A						

Note 31. Refer to Table5 about Type1-4
Note 32 : Clock jitter is lower in Mode10-13 than Mode5/ 7/ 8/ 9 respectively
Note 33. Modes 14~16 are available at Slave Mode only.

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3	FS2	FS1	FS0	fs				
					Type 1	Type 2	Type 3	Type 4	
0	0	0	0	0	48kHz	48.0007kHz	47.9992kHz	47.9997kHz	
1	0	0	0	1	24kHz	24.0004kHz	23.9996kHz	23.9999kHz	
2	0	0	1	0	12kHz	12.0002kHz	11.9998kHz	11.9999kHz	
4	0	1	0	0	32kHz	32.0005kHz	31.9994kHz	31.9998kHz	
5	0	1	0	1	16kHz	16.0002kHz	15.9997kHz	15.9999kHz	
6	0	1	1	0	8kHz	8.0001kHz	7.9999kHz	7.9999kHz	
8	1	0	0	0	44.1kHz	44.0995kHz	44.0995kHz	44.0995kHz	(default)
9	1	0	0	1	22.05kHz	22.0498kHz	22.0498kHz	22.0498kHz	
10	1	0	1	0	11.025kHz	11.0249kHz	11.0249kHz	11.0249kHz	
3, 7, 11-15	Others				N/A	N/A	N/A	N/A	

Table 5. Setting of Sampling Frequency (PLL reference clock input is the MCKI pin) (N/A: Not available)

When PLL reference clock input is the LRCK or BICK pin, the sampling frequency is selected by FS3-0 bits. (Table 6)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	1	0	0	0	32kHz < fs ≤ 48kHz	(default)
1	1	0	0	1	24kHz < fs ≤ 32kHz	
2	1	0	1	0	16kHz < fs ≤ 24kHz	
3	1	0	1	1	12kHz < fs ≤ 16kHz	
4	1	1	0	0	8kHz ≤ fs ≤ 12kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency (PLL reference clock input is LRCK or BICK pin) (N/A: Not available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In master mode (M/S bits = "1"), the LRCK and BICK pins output "L" before the PLL is locked by setting PMPLL = PMDAC bits = "0" → "1". At that time, the MCKO pin outputs an irregular frequency clock at MCKO bit = "1". When MCKO bit = "0", the MCKO pin outputs "L". After the PLL is locked, the LRCK and BICK start outputting the clocks (Table 7).

	Master Mode (M/S bit = "1")		
	Power Up (PMDAC bit= PMPLL bit= "1")	Power Down (PMDAC bit= PMPLL bit= "0")	PLL Unlock
MCKI pin	Refer to Table 4.	Input or fixed to "L" or "H" externally	Refer to Table 4.
MCKO pin	MCKO bit = "0": "L" MCKO bit = "1": Output	L	MCKO bit = "0": L MCKO bit = "1": Unsettling
BICK pin	BF bit = "1": 64fs output BF bit = "0": 32fs output	L	L
LRCK pin	Output	L	L

Table 7. Clock Operation in Master mode (PLL mode)

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In slave mode (M/S bits = "0"), an invalid clock is output from the MCKO pin when MCKO bit = "1", before the PLL is locked by setting PMPLL = PMDAC bits = "0" → "1". When MCKO bit = "0", the MCKO pin outputs "L". After the PLL is locked, the MCKO pin starts outputting the clocks (Table 9).

	Slave Mode (M/S bit = "0")		
	Power Up (PMDAC bit= PMPLL bit= "1")	Power Down (PMDAC bit= PMPLL bit= "0")	PLL Unlock
MCKI pin	Refer to Table 4.	Input or fixed to "L" or "H" externally	Refer to Table 4.
MCKO pin	MCKO bit = "0": "L" MCKO bit = "1": Output	L	MCKO bit = "0": L MCKO bit = "1": Unsettling
BICK pin	Input	Fixed to "L" or "H" externally	Input or Fixed to "L" or "H" externally
LRCK pin	Input	Fixed to "L" or "H" externally	Input or Fixed to "L" or "H" externally

Table 8. Clock Operation in Slave mode (PLL mode)

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13MHz, 14.4MHz, 15.36MHz, 19.2MHz, 19.68MHz,19.8MHz, 26MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BF bit (Table 10).

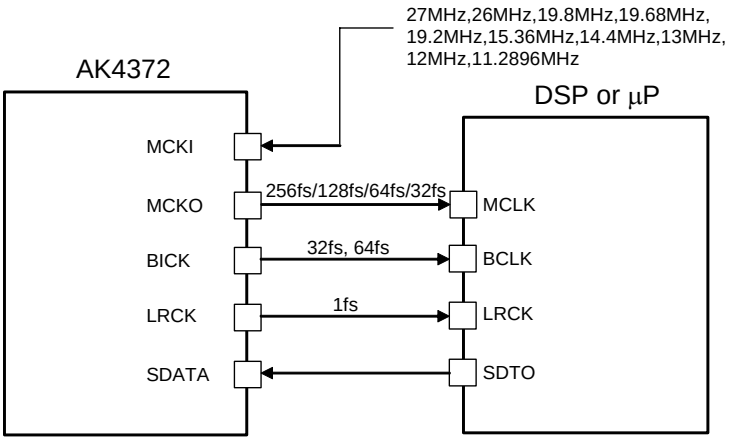


Figure 11. PLL Master Mode

PS1	PS0	MCKO	
0	0	256fs	(default)
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 9. MCKO Frequency (PLL mode, MCKO bit = "1")

BF bit	BICK Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock to the AK4372 is generated by an internal PLL circuit. Input frequency is selected by PLL4-0 bits (Table 4).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

The external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in operation (PMDAC bit = "1"). If these clocks are not provided, the AK4372 may draw excess current and will not possible to operate properly because it utilizes dynamic refreshed logic internally. If the external clocks are not present, the DAC should be in the power-down mode (PMDAC bits = "0").

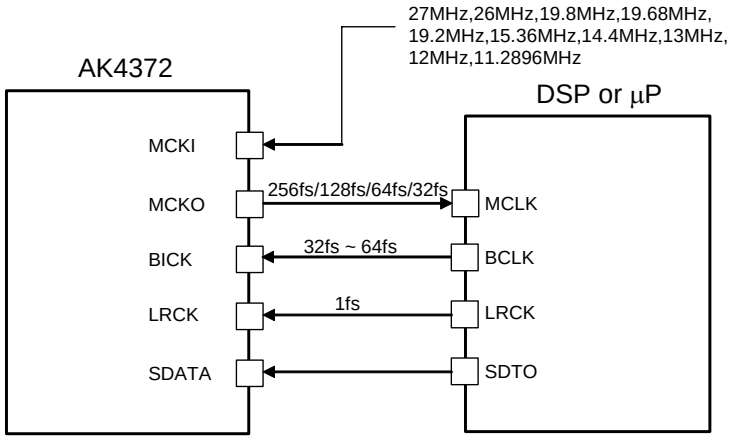


Figure 12. PLL Slave Mode (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK pin

Sampling frequency corresponds to 8kHz to 48kHz by changing FS3-0 bits (Table 6).

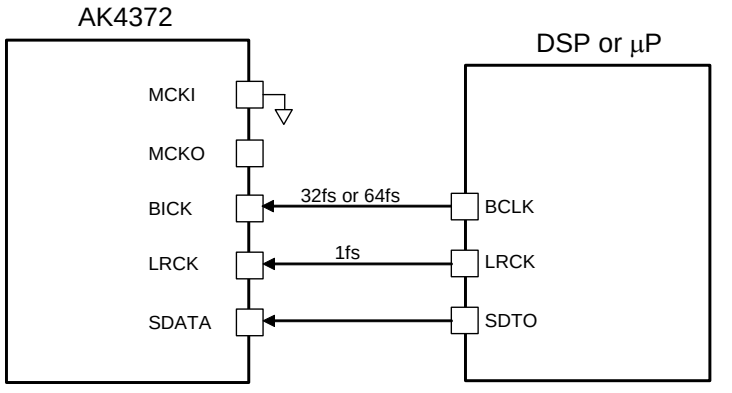


Figure 13. PLL Slave Mode (PLL Reference Clock: BICK pin)

c) PLL reference clock: LRCK pin

Sampling frequency corresponds to 8kHz to 48kHz by changing FS3-0 bits (Table 6).

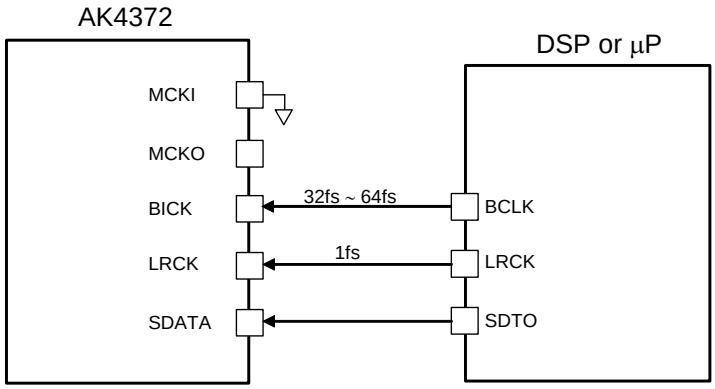


Figure 14. PLL Slave Mode (PLL Reference Clock: LRCK pin)

■ EXT Mode (PMPLL bit = "0": Default)

The AK4372 can be placed in external clock mode (EXT mode) by setting the PMPLL bit to "0". In EXT mode, the master clock can directly input to the DAC via the MCKI pin without going through the PLL. In this case, the sampling frequency and MCKI frequency can be selected by FS3-0 bits (Table 11). In EXT mode, PLL4-0 bits are ignored. MCKO output is enabled by MCKO bit. The MCKO output frequency can be controlled by PS1-0 bits. If the sampling frequency is changed during normal operation of the DAC (PMDAC bit = "1"), the input must be muted by SMUTE bit = "1", or set to "0" data.

LRCK and BICK are output from the AK4372 in master mode(Figure 15). The clock input to the MCKI pin should always be present whenever the DAC is in normal operation (PMDAC bit = "1"). If these clocks are not provided, the AK4372 may draw excessive current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = "0").

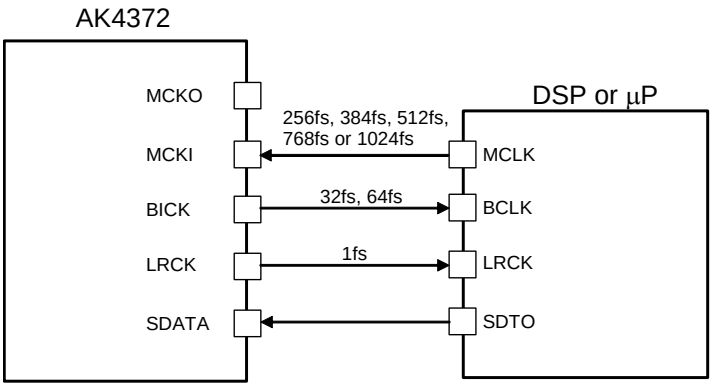


Figure 15. EXT Master Mode

The external clocks required to operate the AK4372 in slave mode are MCKI, LRCK and BICK(Figure 16). The master clock (MCKI) should be synchronized with the sampling clock (LRCK). The phase between these clocks does not matter. All external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PMDAC bit = "1"). If these clocks are not provided, the AK4372 may draw excessive current and will not operate properly, because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = "0").

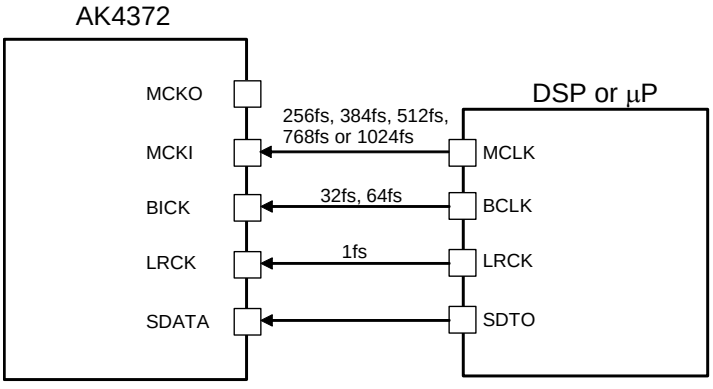


Figure 16. EXT Slave Mode

Mode	FS3	FS2	FS1	FS0	fs	MCKI	
0	0	0	0	0	8kHz ~ 48kHz	256fs	
1	0	0	0	1	8kHz ~ 48kHz	512fs	
2	0	0	1	0	8kHz ~ 24kHz	1024fs	
4	0	1	0	0	8kHz ~ 48kHz	256fs	
5	0	1	0	1	8kHz ~ 48kHz	512fs	
6	0	1	1	0	8kHz ~ 24kHz	1024fs	
8	1	0	0	0	8kHz ~ 48kHz	256fs	(default)
9	1	0	0	1	8kHz ~ 48kHz	512fs	
10	1	0	1	0	8kHz ~ 24kHz	1024fs	
12	1	1	0	0	8kHz ~ 48kHz	384fs	
13	1	1	0	1	8kHz ~ 24kHz	768fs	
Others	Others				N/A	N/A	

Table 11. Relationship between Sampling Frequency and MCKI Frequency (EXT mode) (N/A: Not available)

PS1	PS0	MCKO	
0	0	256fs	(default)
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 12. MCKO frequency (EXT mode, MCKO bit = "1")

	Master Mode (M/S bit = "1")	
	Power Up (PMDAC bit = "1")	Power Down (PMDAC bit = "0")
MCKI pin	Refer to Table 11	Input or fixed to "L" or "H" externally
MCKO pin	MCKO bit = "0": L MCKO bit = "1": Output	L
BICK pin	BF bit = "1": 64fs output BF bit = "0": 32fs output	L
LRCK pin	Output	L

Table 13. Clock Operation in Master mode (EXT mode)

	Slave Mode (M/S bit = "0")	
	Power Up (PMDAC bit = "1")	Power Down (PMDAC bit = "0")
MCKI pin	Refer to Table 11	Input or fixed to "L" or "H" externally
MCKO pin	MCKO bit = "0": L MCKO bit = "1": Output	L
BICK pin	Input	Fixed to "L" or "H" externally
LRCK pin	Input	Fixed to "L" or "H" externally

Table 14. Clock Operation in Slave mode (EXT mode)

For low sampling rates, DR and S/N degrade because of the out-of-band noise. DR and S/N are improved by using higher frequency for MCKI. Table 15 shows DR and S/N when the DAC output is to the HP-amp.

MCKI	DR, S/N (BW=20kHz, A-weight)	
	fs=8kHz	fs=16kHz
256fs/384fs/512fs	56dB	75dB
768fs/1024fs	75dB	90dB

Table 15. Relationship between MCKI frequency and DR (and S/N) of HP-amp (2.4V)

■ Serial Data Interface

The AK4372 interfaces with external systems via the SDATA, BICK and LRCK pins. Five data formats are available, selected by setting the DIF2, DIF1 and DIF0 bits (Table 16). Mode 0 is compatible with existing 16-bit DACs and digital filters. Mode 1 is a 20-bit version of Mode 0. Mode 4 is a 24-bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Modes 2 and 3 with BICK≥48fs, the following formats are also valid: 16-bit data followed by eight zeros (17th to 24th bits) and 20-bit data followed by four zeros (21st to 24th bits). In all modes, the serial data is MSB first and 2's complement format.

When master mode and BICK=32fs(BF bit = "0"), the AK4372 cannot be set to Mode 1 Mode 2 or Mode 4.

Mode	DIF2	DIF1	DIF0	Format	BICK	Figure	
0	0	0	0	0: 16bit, LSB justified	32fs ≤ BICK ≤ 64fs	Figure 17	
1	0	0	1	1: 20bit, LSB justified	40fs ≤ BICK ≤ 64fs	Figure 18	
2	0	1	0	2: 24bit, MSB justified	48fs ≤ BICK ≤ 64fs	Figure 19	(default)
3	0	1	1	3: I^2S Compatible	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 20	
4	1	0	0	4: 24bit, LSB justified	48fs ≤ BICK ≤ 64fs	Figure 18	

Table 16. Audio Data Format

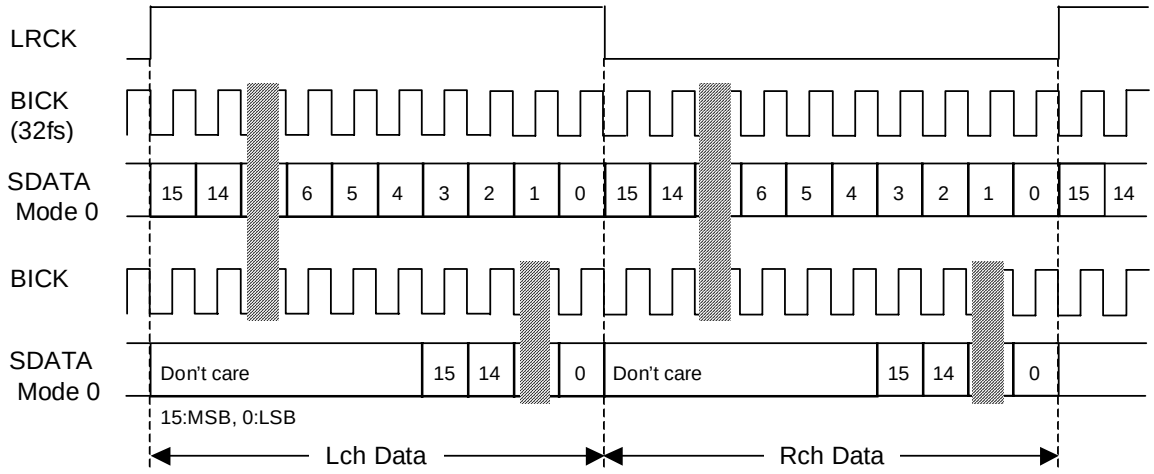


Figure 17. Mode 0 Timing (LRP = BCKP bits = "0")

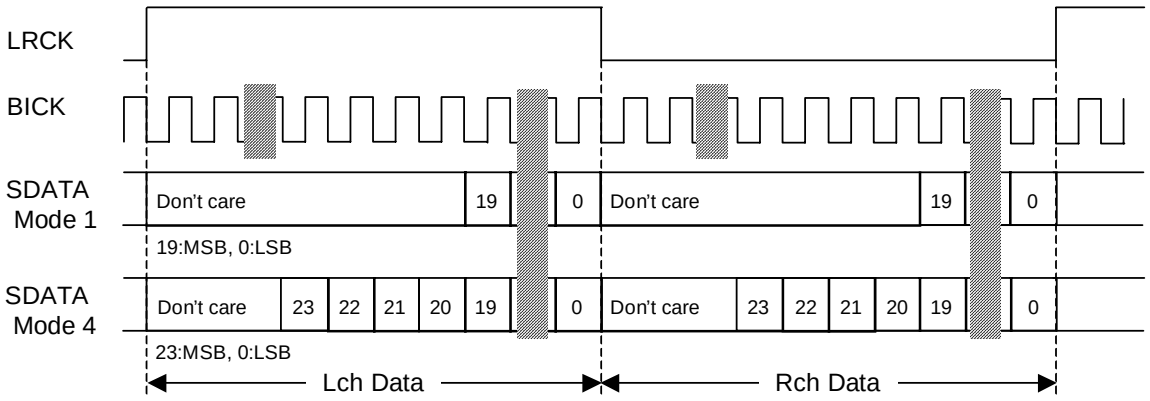


Figure 18. Mode 1, 4 Timing (LRP = BCKP bits = "0")

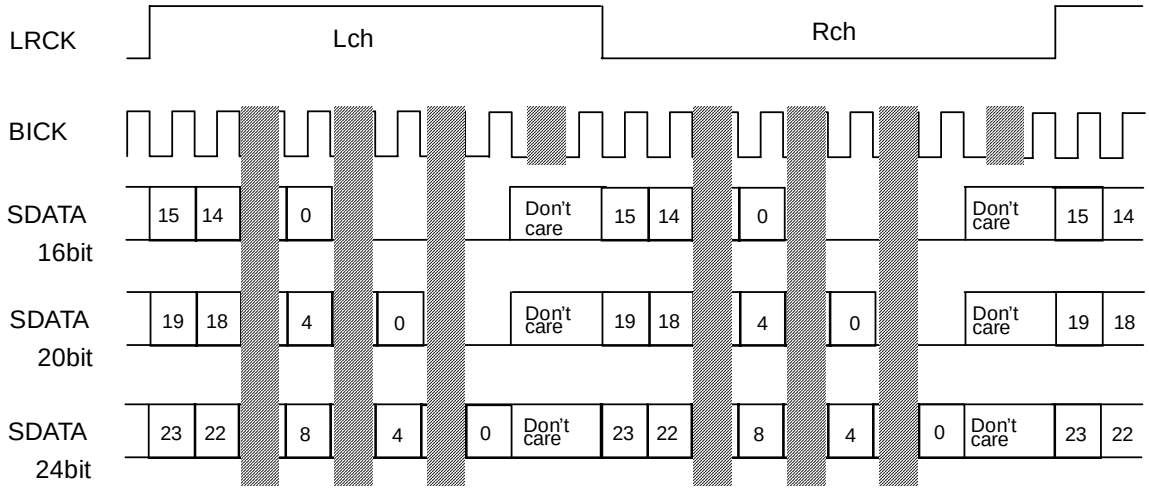


Figure 19. Mode 2 Timing (LRP = BCKP bits = "0")

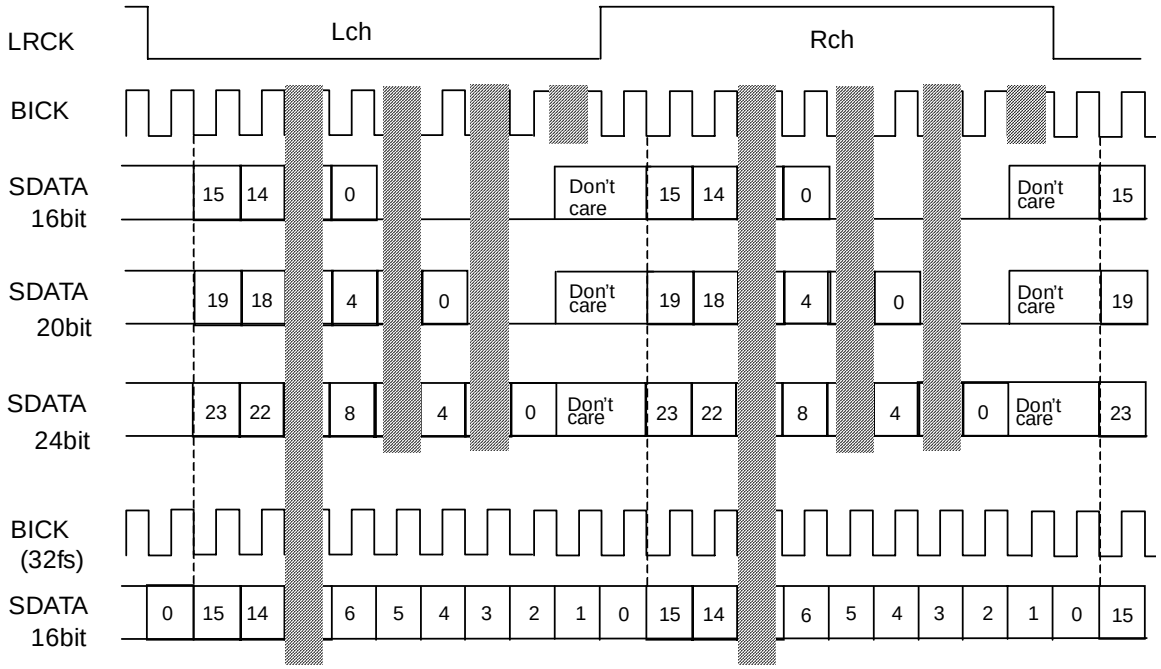


Figure 20. Mode 3 Timing (LRP = BCKP bits = "0")

■ Digital Attenuator

The AK4372 has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to −127dB or MUTE) for each channel (Table 17). At DATTC bit = "1", ATTL7-0 bits control both channel's attenuation levels. At DATTC bit = "0", ATTL7-0 bits control the left channel level and ATTR7-0 bits control the right channel level.

ATTL7-0 ATTR7-0	Attenuation	
FFH	0dB	
FEH	−0.5dB	
FDH	−1.0dB	
FCH	−1.5dB	
:	:	
02H	−126.5dB	
01H	−127.0dB	
00H	MUTE (−∞)	(default)

Table 17. Digital Volume ATT values

The ATS bit sets the transition time between set values of ATT7-0 bits as either 1061/fs or 7424/fs (Table 18). When the ATS bit = "0", a soft transition between the set values occurs(1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). The ATTs are 00H when the PMDAC bit is "0". When the PMDAC returns to "1", the ATTs fade to their current value. The digital attenuator is independent of the soft mute function.

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	(default)
1	7424/fs	29/fs	

Table 18. Transition time between set values of ATT7-0 bits

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit changes to "1", the output signal is attenuated by –∞ during the ATT_DATA×ATT transition time (Table 18) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and is returned to the ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

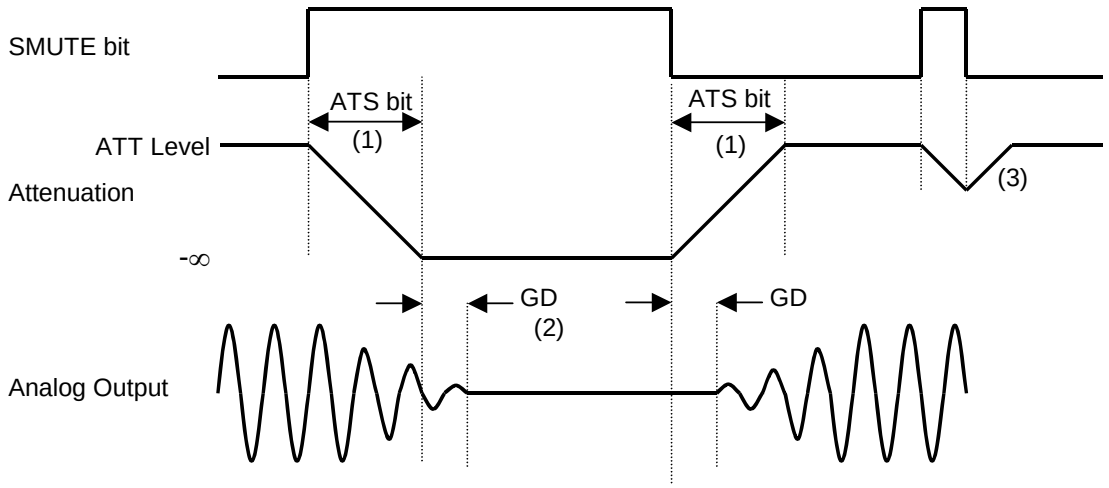


Figure 21. Soft Mute Function

Notes:

(1) ATT_DATA×ATT transition time (Table 18). For example, this time is 3712LRCK cycles (3712/fs) at ATS bit = "1" and ATT_DATA = "128"(-63.5dB).

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and it is returned to the ATT level by the same cycle.

■ De-emphasis Filter

The AK4372 includes a digital de-emphasis filter (tc = 50/15μs), using an IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting DEM1-0 bits (Table 19).

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 19. De-emphasis Filter Frequency Select

■ Bass Boost Function

By controlling the BST1-0 bits, a low frequency boost signal can be output from DAC. The setting value is common for both channels (Table 20).

BST1 bit	BST0 bit	BOOST	
0	0	OFF	(default)
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 20. Low Frequency Boost Select

■ Digital Mixing Function

MONO1-0 bits select the digital data mixing for the DAC (Table 21).

MONO1 bit	MONO0 bit	Lch	Rch	
0	0	L	R	(default)
0	1	L	L	
1	0	R	R	
1	1	(L+R)/2	(L+R)/2	

Table 21. Mixer Setting

■ System Reset

The PDN pin should be held to “L” upon power-up. The 4372 should be reset by bringing the PDN pin “L” for 150ns or more. All of the internal register values are initialized by the system reset. After exiting reset, VCOM, DAC, HPL, HPR, LOUT and ROUT switch to the power-down state. The contents of the control register are maintained until the reset is completed.

The DAC exits reset and power down states by MCKI after the PMDAC bit is changed to “1”. The DAC is in power-down mode until MCKI is input.

■ Headphone Output (HPL, HPR pins)

The power supply voltage for the headphone-amp is supplied from the AVDD pin and is centered on the MUTET voltage. The headphone-amp output load resistance is 16Ω (min). When the MUTEN bit is "1" at PMHPL=PMHPR= "1", the common voltage rises to 0.475 x AVDD. When the MUTEN bit is "0", the common voltage of the headphone-amp falls and the outputs (HPL and HPR pins) go to VSS1.

t_r: Rise Time up to VCOM/2	70k x C (typ)
t_f: Fall Time down to VCOM/2	60k x C (typ)

Table 22. Headphone-Amp Rise/Fall Time

[Example] : Capacitor between the MUTET pin and ground = 1μF:
Rise time up to VCOM/2: t_r = 70k x 1μ = 70ms(typ).
Fall time down to VCOM/2: t_f = 60k x 1μ = 60ms(typ).

When the PMHPL and PMHPR bits are "0", the headphone-amp is powered-down, and the outputs (HPL and HPR pins) go to VSS1.

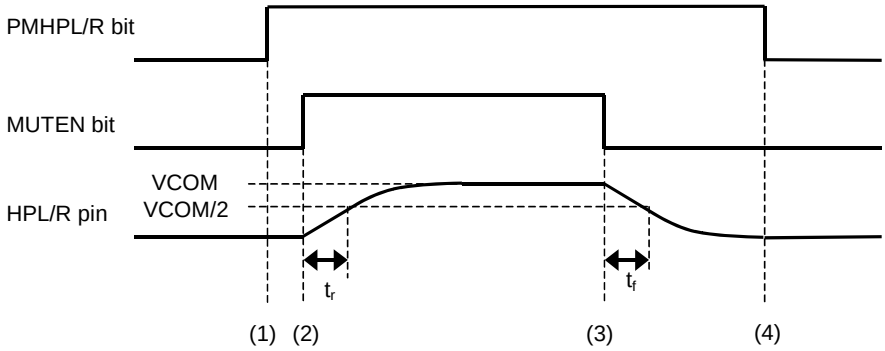


Figure 22. Power-up/Power-down Timing for the Headphone-Amp

(1) Headphone-amp power-up (PMHPL and PMHPR bits = "1"). The outputs are still at VSS1.
(2) Headphone-amp common voltage rises up (MUTEN bit = "1"). Common voltage of the headphone-amp is rising. This rise time depends on the capacitor value connected with the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ) when the capacitor value on MUTET pin is "C".
(3) Headphone-amp common voltage falls down (MUTEN bit = "0"). Common voltage of the headphone-amp is falling to VSS1. This fall time depends on the capacitor value connected with the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ) when the capacitor value on the MUTET pin is "C".
(4) Headphone-amp power-down (PMHPL, PMHPR bits = "0"). The outputs are at VSS1. If the power supply is switched off or the headphone-amp is powered-down before the common voltage settles to VSS1, some pop noise may occur.

< External Circuit of Headphone-Amp >

The cut-off frequency of the headphone-amp output depends on the external resistor and capacitor used. Table 23 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at AVDD = 2.4, 3.0 and 3.3V. The output voltage of the headphone-amp is 0.48 x AVDD (Vpp) @−3dBFS.

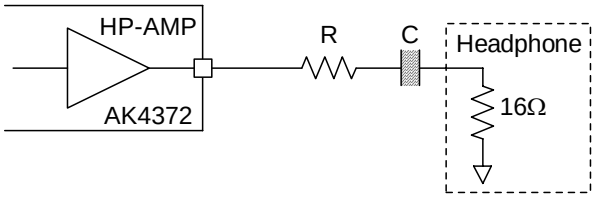


Figure 23. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN	Output Power [mW]		
				2.4V	3.0V	3.3V
0	220	45	17	21	33	40
	100	100	43			
6.8	100	70	28	10	16	20
	47	149	78			
16	100	50	19	5	8	10
	47	106	47			

Table 23. Relationship of external circuit, output power and frequency response

< Wired OR with External Headphone-Amp >

When PMVCM=PMHPL=PMHPR bits = "0" and HPZ bit = "1", Headphone-amp is powered-down and HPL/R pins are pulled-down to VSS1 by 200kΩ (typ). In this setting, it is able to connect headphone-amp of AK4372 and external single supply headphone-amp by "wired OR".

PMVCM	PMHPL/R	HPMTN	HPZ	Mode	HPL/R pins	
x	0	x	0	Power-down & Mute	VSS1	(default)
0	0	x	1	Power-down	Pull-down by 200kΩ	
1	1	0	x	Mute	VSS1	
1	1	1	x	Normal Operation	Normal Operation	

Table 24. HP-Amp Mode Setting (x: Don't care)

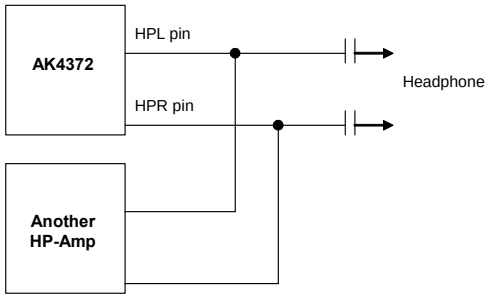


Figure 24. Wired OR with External HP-Amp

< Analog Mixing Circuit for Headphone Output >

DALHL, LINHL, RINHL and MINHL bits control each path switch of the HPL output. DARHR, LINHR, RINHR and MINHR bits control each path switch of the HPR output.
When LHM bit = "0", HPG1-0 bits = "00" (R_{1H}= R_{2H} = R_{DH}= 100k) and ATTH4-0 bits = "00H"(0dB), the mixing gain is +0.95dB(typ). When HPG1-0 bit = "01" (R_{DH}= 50k), the mixing gain of DAC path is +6.95dB(typ). When HPG1-0 bit = "10" (R_{DH}= 25k), the mixing gain of DAC path is +12.95dB(typ). When LHM bit is "1", LIN and RIN signals are output from the HPL/R pins as (L+R)/2 respectively.

When LDIF=LDIFH=LINL=RINR bits = "1", the LIN and RIN pins becomes IN+ and IN− pins, respectively. The IN+ and IN− pins can be used as full-differential mono line input for analog mixing for headphone-amp. In this case, LINHL, RINHL, LINHR and RINHR bits should be "0".

If the path is OFF and the signal is input to the input pin, the input pin should be biased to a voltage equivalent to VCOM voltage (= 0.475 x AVDD) externally. Figure 51 shows the external bias circuit example.

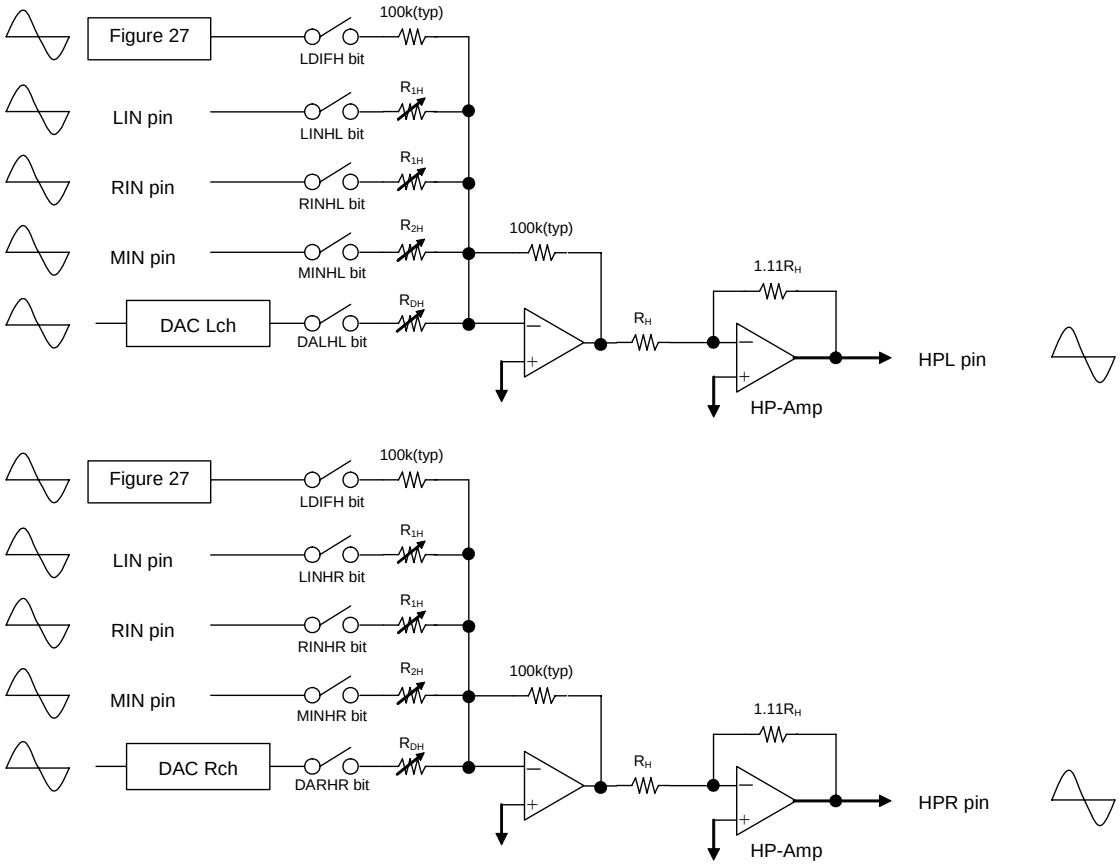


Figure 25. Summation circuit for HPL/R output

■ Headphone Output Volume

HPL/HPR volume is controlled by ATTH4-0 bits when HMUTE bit = "0" (+12dB ~ –51dB or +6dB ~ –57dB or 0dB ~ –63dB, 1.5dB or 3dB step, Table 25)

HMUTE	ATTH4-0	HPG1-0 bits = "10" (DAC Only)	HPG1-0 bits = "01" (DAC Only)	HPG1-0 bits = "00"	STEP	
0	00H	+12dB	+6dB	0dB	1.5dB	(default)
	01H	+10.5dB	+4.5dB	–1.5dB		
	02H	+9dB	+3dB	–3dB		
	03H	+7.5dB	+1.5dB	–4.5dB		
	:	:	:	:		
	12H	–15dB	–21dB	–27dB		
	13H	–16.5dB	–22.5dB	–28.5dB		
	14H	–18dB	–24dB	–30dB		
	15H	–21dB	–27dB	–33dB	3dB	
	16H	–24dB	–30dB	–36dB		
	:	:	:	:		
	1DH	–45dB	–51dB	–57dB		
	1EH	–48dB	–54dB	–60dB		
	1FH	–51dB	–57dB	–63dB		
1	x	MUTE	MUTE	MUTE		

Table 25. HPL/HPR Volume ATT values (x: Don't care)

■ Stereo Line Output (LOUT, ROUT pins)

The common voltage is 0.475 x AVDD. The load resistance is 10kΩ(min). When the PMLO bit is "1", the stereo line output is powered-up. DALL, LINL, RINL and MINL bits control each path switch of LOUT. DARR, LINR, RINR and MINR bits control each path switch of ROUT. When LM bit = "0", LOG bit = "0" ($R_{1L} = R_{2L} = R_{DL} = 100k$) and ATTS3-0 bits is "0FH"(0dB), the mixing gain is 0dB(typ) for all paths. When the LOG bit = "1"(R_{DL}= 50k), the DAC path gain is +6dB. When LM bit = "1", LIN and RIN signals are output from LOUT/ROUT pins as (L+R)/2 respectively.

If the path is OFF and the signal is input to the input pin, the input pin should be biased to a voltage equivalent to VCOM voltage (= 0.475 x AVDD) externally. Figure 51 shows the external bias circuit example.

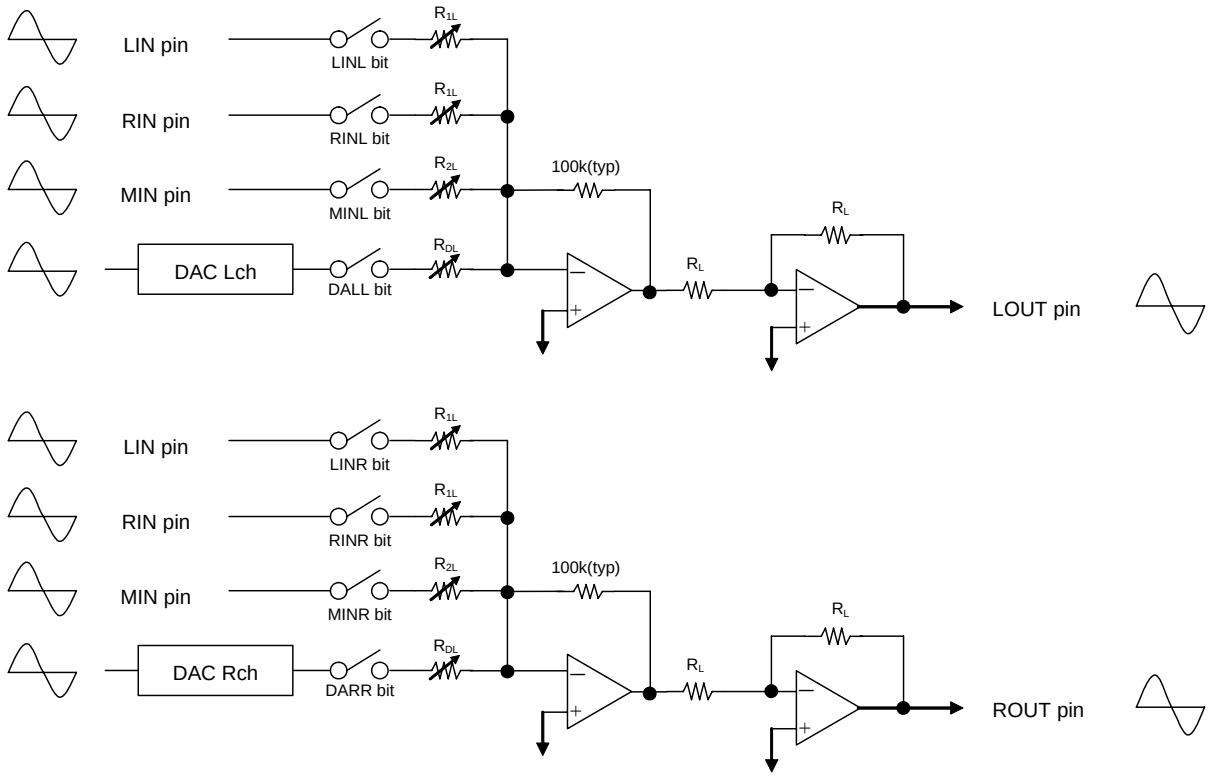


Figure 26. Summation circuit for stereo line output

< Analog Mixing Circuit of Full-differential Mono input >

When LDIF=LINL=RINR bits = "1", the LIN and RIN pins becomes IN+ and IN− pins, respectively. The IN− and IN+ pins can be used as full-differential mono line input for analog mixing of LOUT/ROUT pins. It is not available to mix with other signal source for LOUT/ROUT outputs.

If the path is OFF and the signal is input to the input pin, the input pin should be biased to a voltage equivalent to VCOM voltage (= 0.475 x AVDD) externally. Figure 51 shows the external bias circuit example.

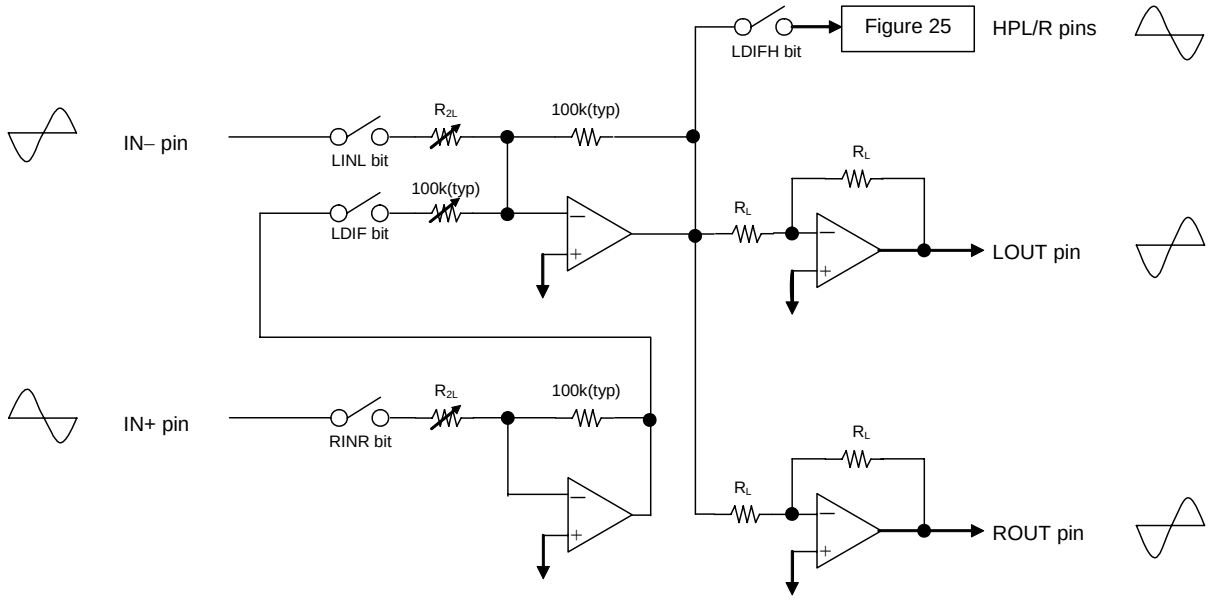


Figure 27. Summation circuit for stereo line output (Full-differential input)

■ Stereo Line Output (LOUT/ROUT pins) Volume

LOUT/ROUT volume is controlled by ATTS3-0 bits when LMUTE bit = "0" (+6dB ~ –24dB or 0dB ~ –30dB, 2dB step, Table 26). Pop noise occurs when ATTS3-0 bits are changed.

LMUTE	ATTS3-0	LOG bit = "1" (DAC Only)	LOG bit = "0"	
0	FH	+6dB	0dB	
	EH	+4dB	–2dB	
	DH	+2dB	–4dB	
	CH	0dB	–6dB	
	:	:	:	
	1H	–22dB	–28dB	
	0H	–24dB	–30dB	
1	x	MUTE	MUTE	(default)

Table 26. LOUT/ROUT Volume ATT values (x: Don't care)

■ Power-Up/Down Sequence (EXT mode)

1) DAC → HP-Amp

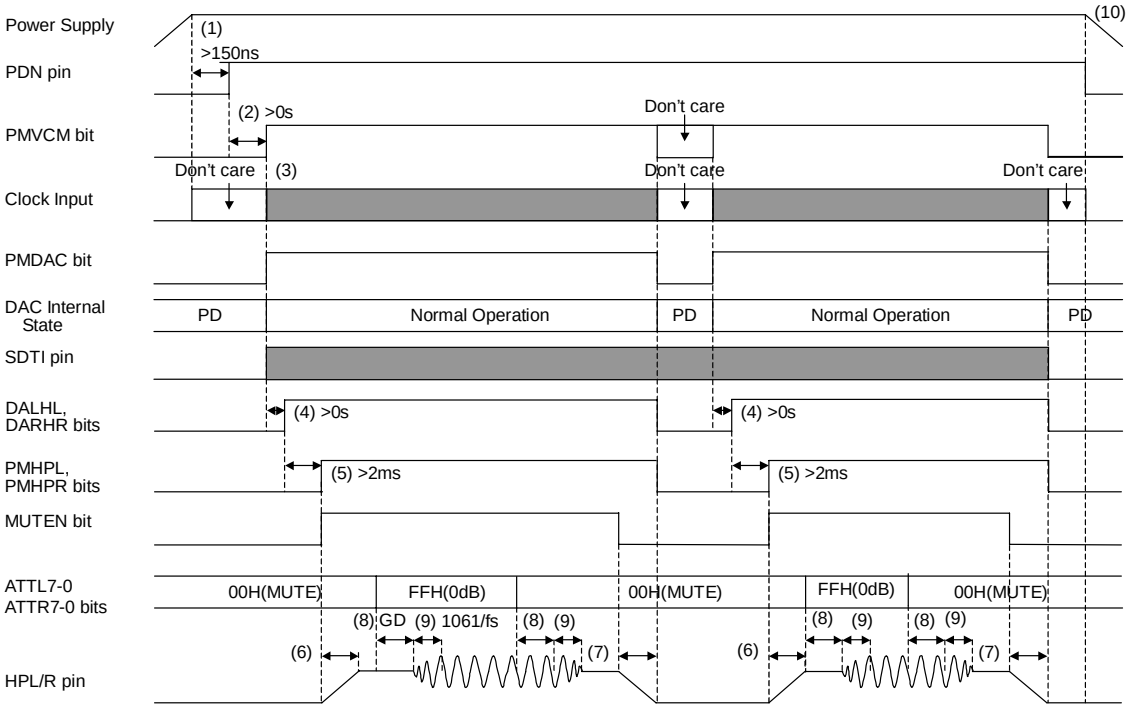


Figure 28. Power-up/down sequence of DAC and HP-amp (Don't care: except Hi-Z)

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM and PMDAC bits should be changed to "1" after the PDN pin is set to "H".
(3) External clocks (MCKI, BICK, LRCK) are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The headphone-amp can operate without these clocks.
(4) DALHL and DARHR bits should be changed to "1" after PMVCM and PMDAC bit is changed to "1".
(5) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after the DALHL and DARHR bits are changed to "1"
(6) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(7) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after the HPL and HPR pins settle to VSS1. After that, the DALHL and DARHR bits should be changed to "0".
(8) Analog output corresponding to the digital input has a group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(9) The ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(10) The power supply should be switched off after the headphone-amp is powered down (HPL/R pins become "L"). When AVDD and DVDD are supplied separately, DVDD should be powered-down at the same time or later than AVDD.

2) DAC → Lineout

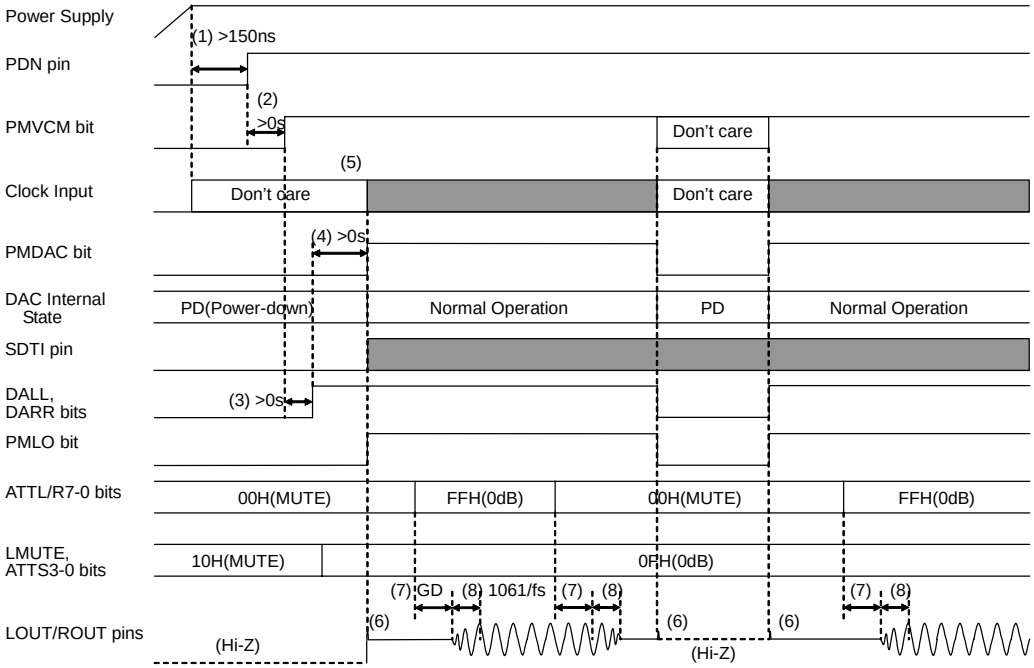


Figure 29. Power-up/down sequence of DAC and LOUT/ROUT (Don't care: except Hi-Z)

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) DALL and DARR bits should be changed to "1" after the PMVCM bit is changed to "1".
(4) PMDAC and PMLO bits should be changed to "1" after DALL and DARR bits is changed to "1".
(5) External clocks (MCKI, BICK, LRCK) are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The LOUT/ROUT buffer can operate without these clocks.
(6) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.
(7) Analog output corresponding to the digital input has a group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(8) The ATS bit sets the transition time of the digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-Amp

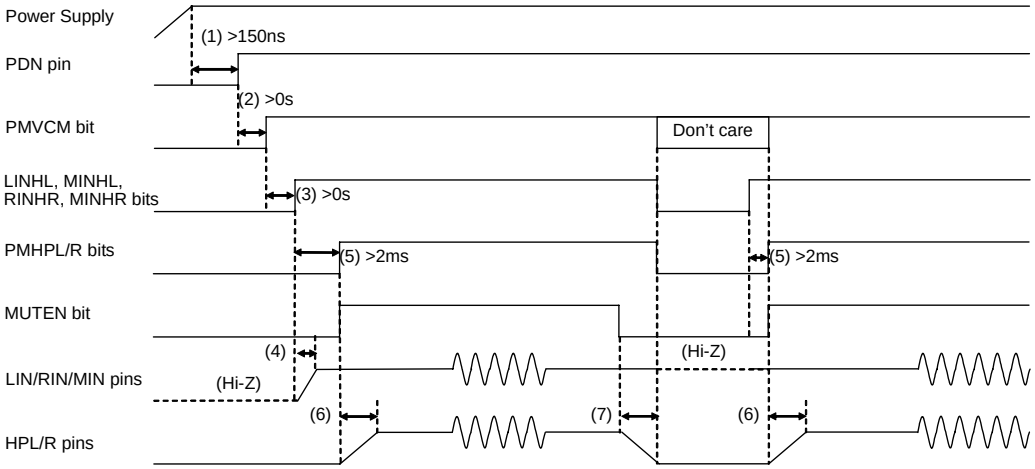


Figure 30. Power-up/down sequence of LIN/RIN/MIN and HP-Amp

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINHL, MINHL, RINHR or MINHR bit is changed to "1", the LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at the VCOM pin is 2.2μF) after LINHL, MINHL, RINHR and MINHR bits are changed to "1".
(6) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(7) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after the HPL and HPR pins settle to VSS1. After that, the LINHL, MINHL, RINHR and MINHR bits should be changed to "0".

4) LIN/RIN/MIN → Lineout

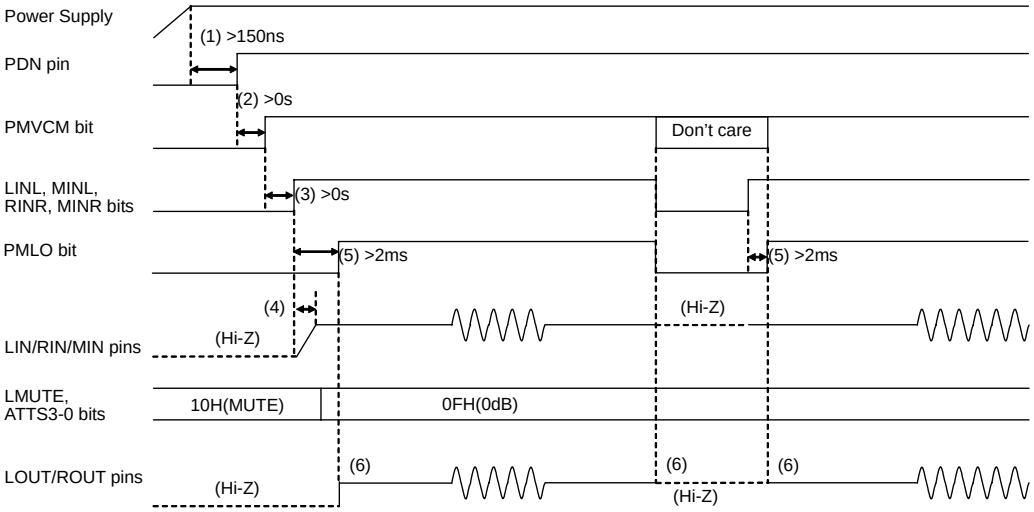


Figure 31. Power-up/down sequence of LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 and Lineout

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) LINL, MINL, RINR and MINR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR or MINR bit is changed to "1", the LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) PMLO bit should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINL, MINL, RINR and MINR bits are changed to "1".
(6) When the PMLO bit is changed, pop noise is output from the LOUT/ROUT pins.

■ Power-Up/Down Sequence (PLL Slave mode)

1) DAC → HP-Amp

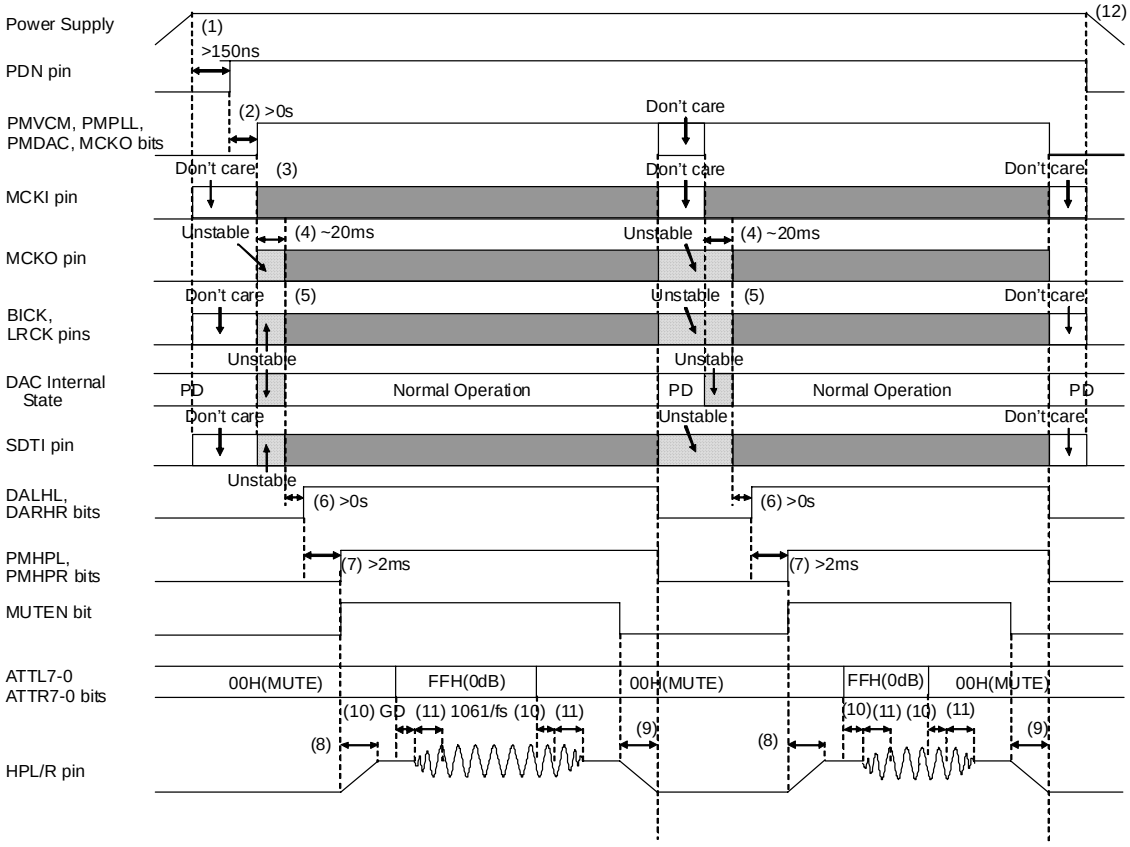


Figure 32. Power-up/down sequence of DAC and HP-amp (Don't care: except Hi-Z)

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC and MCKO bits should be changed to "1" after the PDN pin goes "H".
(3) The PLL operation is executed when the system clock is input to the MCKI pin.
(4) The PLL lock time is referred to Table 4. After the PLL is locked, the MCKO pin outputs the master clock.
(5) The clocks (BICK, LRCK) generated by MCKO are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The headphone-amp can operate without these clocks.
(6) DALHL and DARHR bits should be changed to "1" after the PLL is locked.
(7) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after the DALHL and DARHR bits are changed to "1".
(8) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(9) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, the DALHL/DARHR bits should be changed to "0".
(10) Analog output corresponding to the digital input has a group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(11) The ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(12) The power supply should be switched off after the headphone-amp is powered down (HPL/R pins become "L"). When AVDD and DVDD are supplied separately, DVDD should be powered-down at the same time or after AVDD.

2) DAC → Lineout

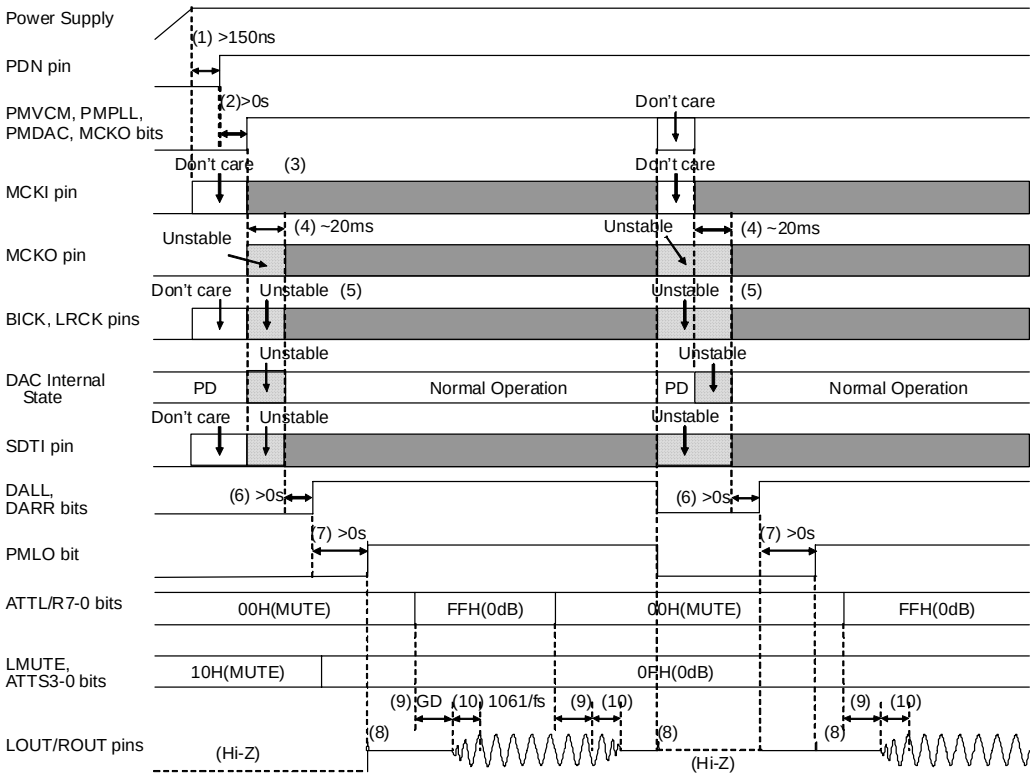


Figure 33. Power-up/down sequence of DAC and LOUT/ROUT (Don't care: except Hi-Z)

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC and MCKO bits should be changed to "1" after the PDN pin goes "H".
(3) The PLL operation is executed when the system clock is input to the MCKI pin.
(4) The PLL lock time is referred to Table 4. After the PLL is locked, the MCKO pin outputs the master clock.
(5) The clocks (BICK, LRCK) generated by MCKO are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The LOUT/ROUT buffer can operate without these clocks.
(6) DALL and DARR bits should be changed to "1" after the PLL is locked
(7) PMLO bit is changed to "1".
(8) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.
(9) Analog output corresponding to the digital input has group delay (GD) of 22fs(=499μs@fs=44.1kHz).
(10) The ATS bit sets the transition time of the digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-Amp

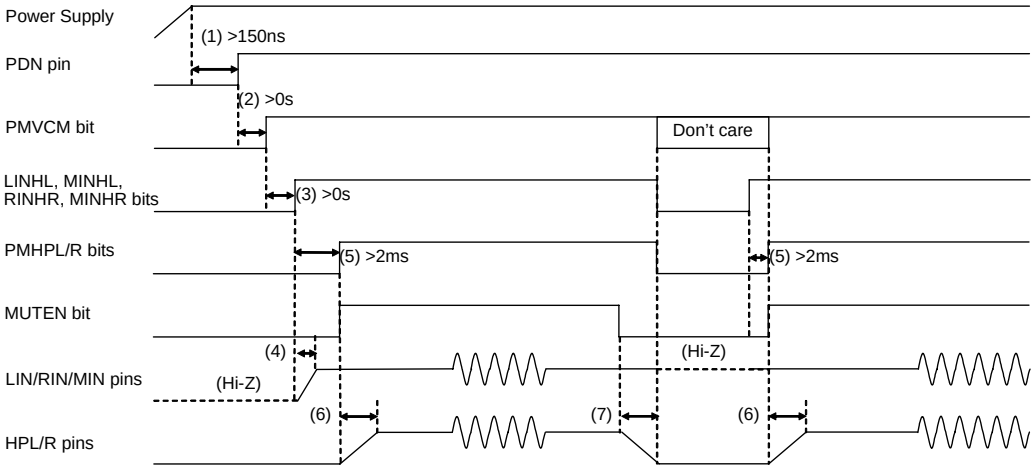


Figure 34. Power-up/down sequence of LIN/RIN/MIN and HP-Amp

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINHL, MINHL, RINHR or MINHR bit is changed to "1", the LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at the VCOM pin is 2.2μF) after LINHL, MINHL, RINHR and MINHR bits are changed to "1".
(6) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(7) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after the HPL and HPR pins settle to VSS1. After that, the LINHL, MINHL, RINHR and MINHR bits should be changed to "0".

4) LIN/RIN/MIN → Lineout

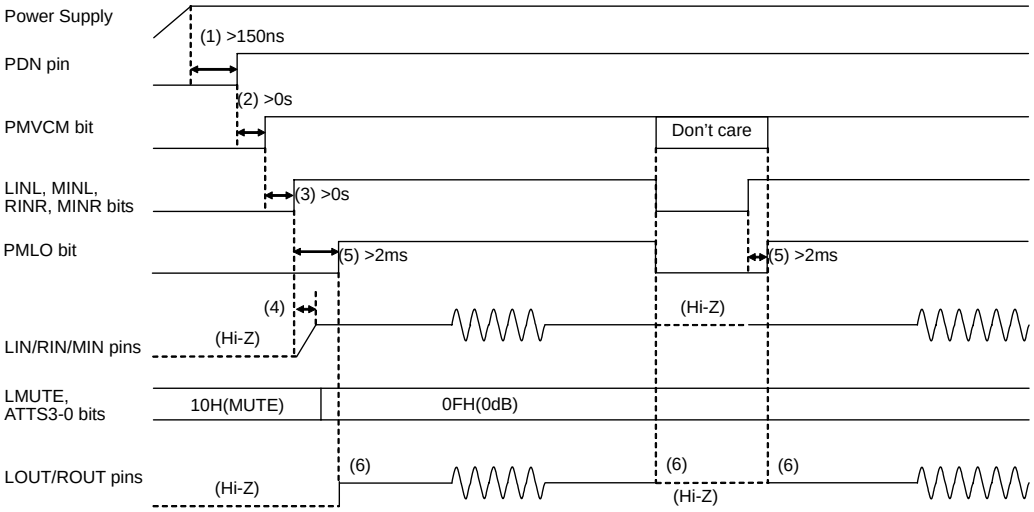


Figure 35. Power-up/down sequence of LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 and Lineout

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) LINL, MINL, RINR and MINR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR or MINR bit is changed to "1", the LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) PMLO bit should be changed to "1" at least 2ms (in case external capacitance at the VCOM pin is 2.2μF) after LINL, MINL, RINR and MINR bits are changed to "1".
(6) When the PMLO bit is changed, pop noise is output from the LOUT/ROUT pins.

■ Power-Up/Down Sequence (PLL Master mode)

1) DAC → HP-Amp

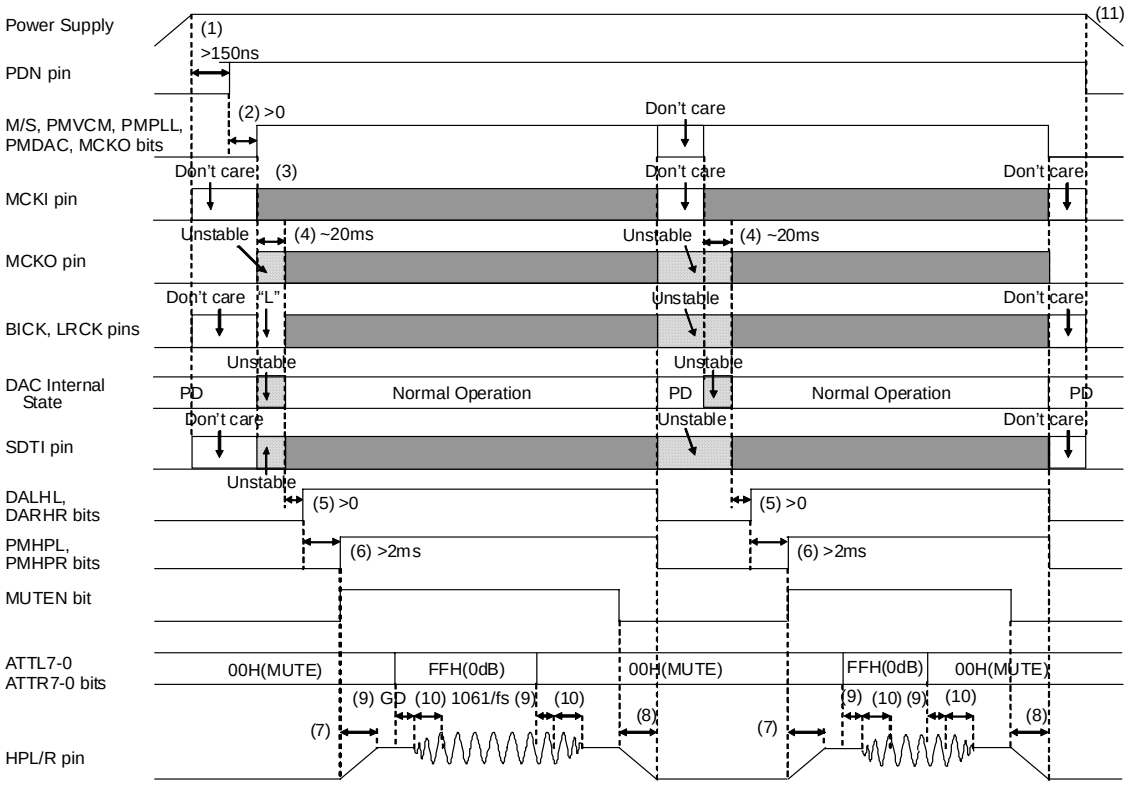


Figure 36 Power-up/down sequence of DAC and HP-amp (Don't care: except Hi-Z)

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC, MCKO and M/S bits should be changed to "1" after the PDN pin goes "H".
(3) The PLL operation is executed when the system clock is input to the MCKI pin.
(4) The PLL lock time is referred to Table 4. After the PLL is locked, each clock is output from BICK, LRCK and MCKO pins.
(5) DALHL and DARHR bits should be changed to "1" after the PLL is locked.
(6) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after the DALHL and DARHR bits are changed to "1".
(7) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(8) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, the DALHL/DARHR bits should be changed to "0".
(9) Analog output corresponding to the digital input has group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(10) The ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(11) The power supply should be switched off after the headphone-amp is powered down (HPL/R pins become "L"). When AVDD and DVDD are supplied separately, DVDD should be powered-down at the same time or after AVDD.

2) DAC → Lineout

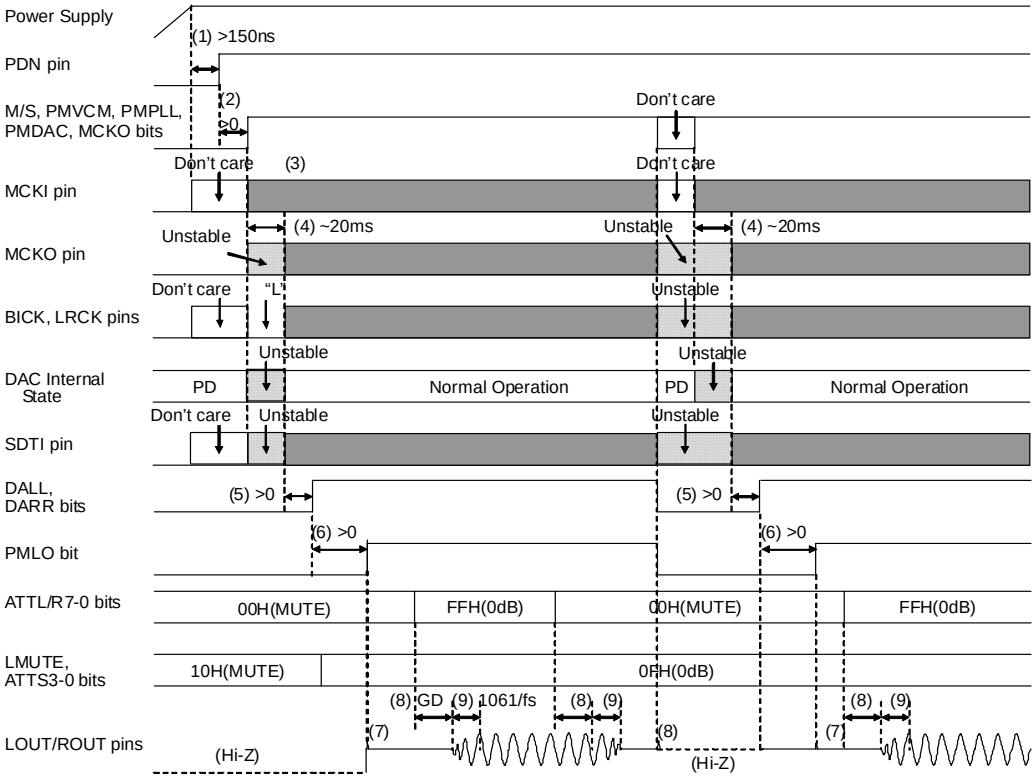


Figure 37. Power-up/down sequence of DAC and LOUT/ROUT(Don't care: except Hi-Z)

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC, MCKO and M/S bits should be changed to "1" after the PDN pin goes "H".
(3) The PLL operation is executed when the system clock is input to the MCKI pin.
(4) The PLL lock time is referred to Table 4. After the PLL is locked, each clock is output from BICK, LRCK and MCKO pins.
(5) DALL and DARR bits should be changed to "1" after the PLL is locked.
(6) PMLO bit is changed to "1".
(7) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.
(8) Analog output corresponding to the digital input has group delay (GD) of 22fs(=499μs@fs=44.1kHz).
(9) The ATS bit sets the transition time of the digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-Amp

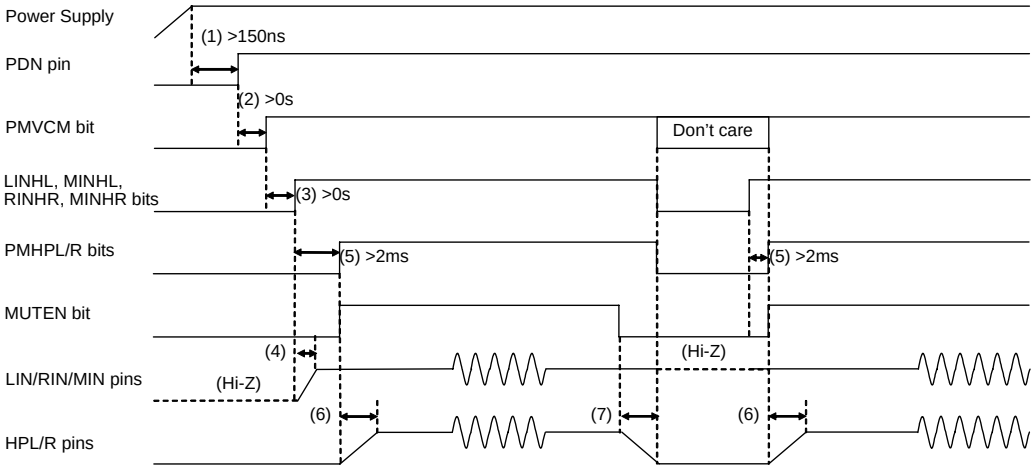


Figure 38. Power-up/down sequence of LIN/RIN/MIN and HP-Amp

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINHL, MINHL, RINHR or MINHR bit is changed to "1", the LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at the VCOM pin is 2.2μF) after LINHL, MINHL, RINHR and MINHR bits are changed to "1".
(6) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(7) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after the HPL and HPR pins settle to VSS1. After that, the LINHL, MINHL, RINHR and MINHR bits should be changed to "0".

4) LIN/RIN/MIN → Lineout

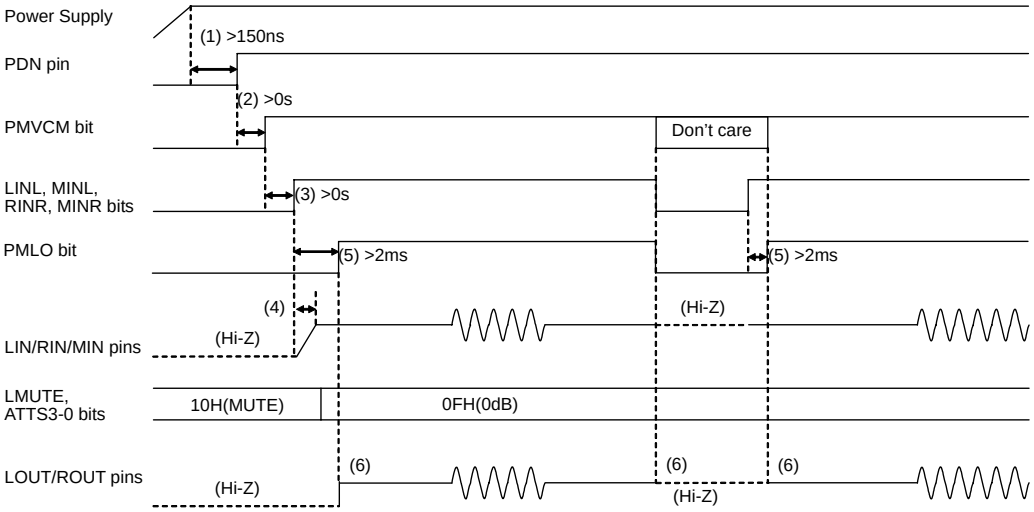


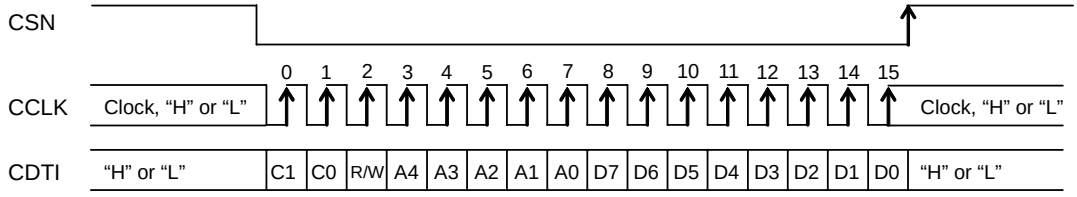
Figure 39. Power-up/down sequence of LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 and Lineout

(1) When AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. The PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after the PDN pin is set to "H".
(3) LINL, MINL, RINR and MINR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR or MINR bit is changed to "1", the LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) PMLO bit should be changed to "1" at least 2ms (in case external capacitance at the VCOM pin is 2.2μF) after LINL, MINL, RINR and MINR bits are changed to "1".
(6) When the PMLO bit is changed, pop noise is output from the LOUT/ROUT pins.

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = “L”)

Internal registers may be written to via the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of the Chip address (2-bits, Fixed to “01”), Read/Write (1-bit, Fixed to “1”, Write only), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). Address and data are clocked in on the rising edge of CCLK. For write operations, the data is latched after a low-to-high transition of the 16th CCLK. CSN should be set to “H” once after 16 CCLKs for each address. The clock speed of CCLK is 5MHz(max). The value of the internal registers is initialized at the PDN pin = “L”.



C1-C0: Chip Address (Fixed to “01”)
R/W: READ/WRITE (Fixed to “1”, Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 40. 3-wire Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")
The AK4372 supports fast-mode I²C-bus (max: 400kHz, Version 1.0).

(2)-1. WRITE Operations
Figure 41 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 47). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001000". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets this device address bit (Figure 42). If the slave address matches that of the AK4372, the AK4372 generates an acknowledgement and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 48). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4372. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 43). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 44). The AK4372 generates an acknowledgement after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 47).

The AK4372 can perform more than one byte write operation per sequence. After receiving the third byte the AK4372 generates an acknowledgement and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 13H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW(Figure 49) except for the START and STOP conditions.

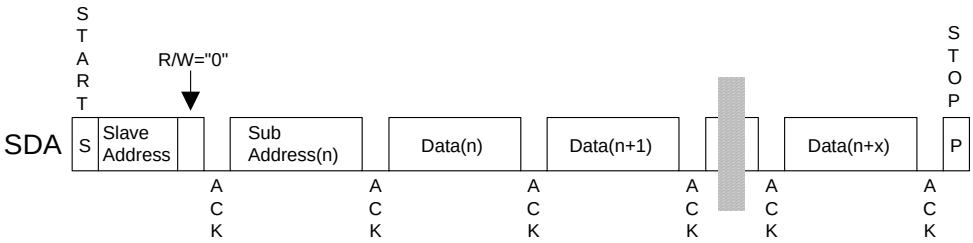


Figure 41. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	CAD0	R/W

(Those CAD0 should match with CAD0 pin)
Figure 42. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 43. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 44. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4372. After a transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the writing cycle after receiving the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 13H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4372 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4372 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receiving the slave address with R/W bit "1", the AK4372 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter, and increments the internal address counter by 1. If the master does not generate an acknowledgement but instead generates stop condition, the AK4372 ceases transmission.

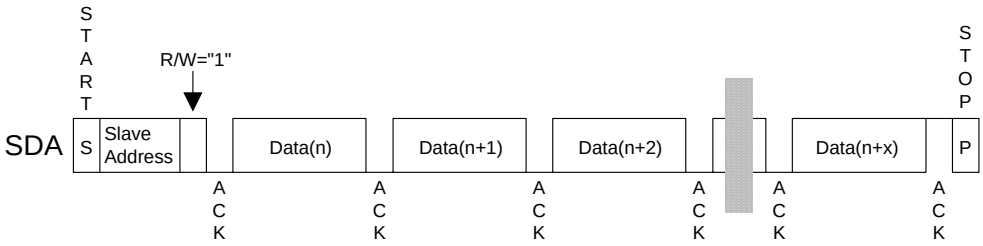


Figure 45. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4372 then generates an acknowledgement, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledgement but instead generates stop condition, the AK4372 ceases transmission.

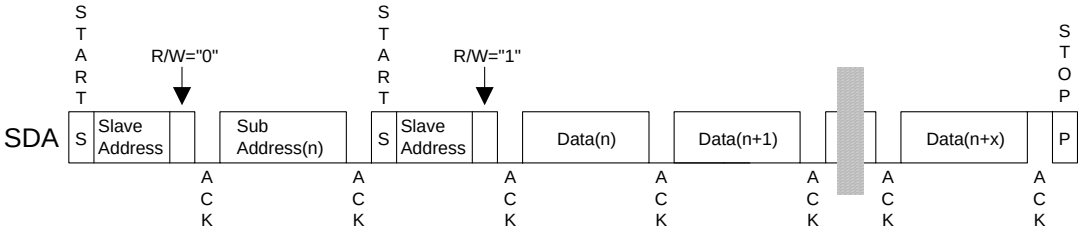


Figure 46. RANDOM ADDRESS READ

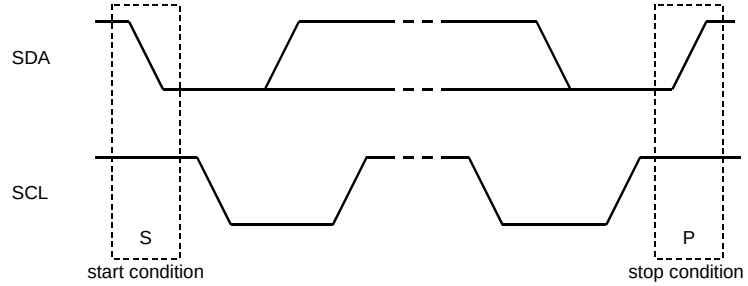


Figure 47. START and STOP Conditions

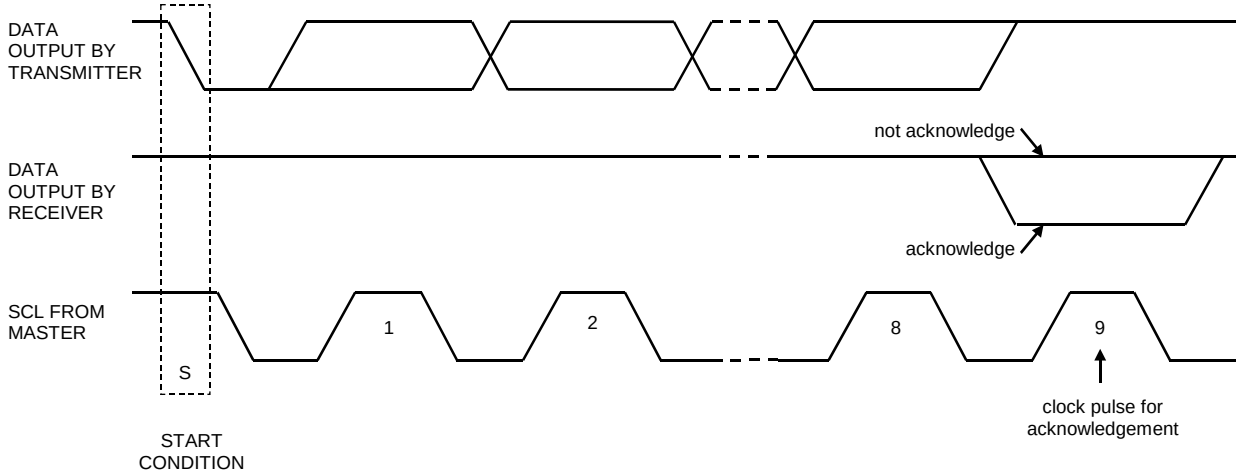


Figure 48. Acknowledge on the I^2C-Bus

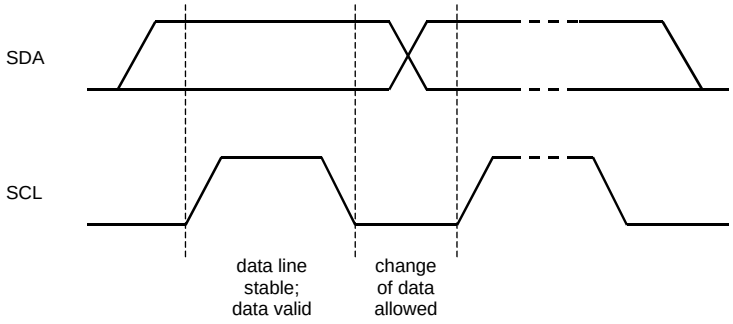


Figure 49. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	0	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	Clock Control	PLL4	0	M/S	MCKAC	BF	PS0	PS1	MCKO
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
07H	Headphone Out Select 0	HPG1	HPG0	MINHR	MINHL	RINHR	LINHL	DARHR	DALHL
08H	Lineout Select 0	0	LOG	MINR	MINL	RINR	LINL	DARR	DALL
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
0AH	Reserved	0	0	0	0	0	0	0	0
0BH	Reserved	0	0	0	0	0	0	0	0
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Headphone Out Select 1	0	0	0	0	0	0	LINHR	RINHL
0EH	Headphone ATT	0	HPZ	HMUTE	ATTH4	ATTH3	ATTH2	ATTH1	ATTH0
0FH	Lineout Select 1	0	0	0	0	0	0	LINR	RINL
10H	Mono Mixing	0	0	0	0	0	0	LM	LHM
11H	Differential Select	0	0	0	0	0	0	LDIFH	LDIF
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	1	0	0	0	0

All registers inhibit writing at PDN pin = "L".
PDN pin = "L" resets the registers to their default values.
For addresses from 14H to 1FH, data must not be written.
Unused bits indicated by "0" must contain a "0" value.
Unused bits indicated by "1" must contain a "1" value.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	0	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (default)
1: Power ON

PMDAC: Power Management for DAC Blocks
0: Power OFF (default)
1: Power ON
When the PMDAC bit is changed from "0" to "1", the DAC is powered-up to the current register values (ATT value, sampling rate, etc).

PMHPL: Power Management for the left channel of the headphone-amp
0: Power OFF (default). The HPL pin settles to VSS1(0V).
1: Power ON

PMHPR: Power Management for the right channel of the headphone-amp
0: Power OFF (default). The HPR pin settles to VSS1(0V).
1: Power ON

MUTEN: Headphone Amp Mute Control
0: Mute (default). The HPL and HPR pins settles to VSS1(0V).
1: Normal operation. HPL and HPR pins go to 0.475 x AVDD.

PMLO: Power Management for Stereo Output
0: Power OFF (default) LOUT/ROUT pins change to Hi-Z.
1: Power ON

PMPLL: Power Management for PLL
0: Power OFF: EXT mode (default)
1: Power ON: PLL mode

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless of setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMDAC, PMHPL, PMHPR, PMLO, PMMO, PMPLL and MCKO bits are "0", all blocks are powered-down. The register values remain unchanged. Power supply current is 20μA(typ) in this case. For fully shut down (typ. 1μA), the PDN pin should be "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

FS3-0: Select Sampling Frequency
PLL mode: Table 5
EXT mode: Table 11

PLL4-0: Select PLL Reference Clock
PLL mode: Table 3
EXT mode: PLL4-0 bits are disabled
(PLL4 bit is D7 bit of 02H.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock Control	PLL4	0	M/S	MCKAC	BF	PS0	PS1	MCKO
R/W		R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MCKO: Control of MCKO signal
0: Disable (default)
1: Enable

PS1-0: MCKO Frequency
PLL mode: Table 9
EXT mode: Table 12

BF: BICK Period setting in Master Mode. In slave mode, this bit is ignored.
0: 32fs (default)
1: 64fs

MCKAC: MCKI Input Mode Select
0: CMOS input (default)
1: AC coupling input

M/S: Select Master/Slave Mode
0: Slave mode (default)
1: Master mode

PLL4-0: Select PLL Reference Clock
PLL3-0 bits are D3-0 bits of 01H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF2-0: Audio Data Interface Format Select (Table 16)
Default: "010" (Mode 2)

LRP: LRCK Polarity Select in Slave Mode
0: Normal (default)
1: Invert

BCKP: BICK Polarity Select in Slave Mode
0: Normal (default)
1: Invert

MONO1-0: Digital Mixing Select (Table 21)
Default: "00" (LR)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select (Table 19)
Default: "01" (OFF)

BST1-0: Low Frequency Boost Function Select (Table 20)
Default: "00" (OFF)

SMUTE: Soft Mute Control
0: Normal operation (default)
1: DAC outputs soft-muted

LMUTE: Mute control for LOUT/ROUT (Table 26)
0: Normal operation. ATTS3-0 bits control attenuation value.
1: Mute. ATTS3-0 bits are ignored. (default)

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent (default)
1: Dependent
At DATTC bit = "1", ATTL7-0 bits control both channel attenuation levels, while register values of ATTL7-0 bits are not written to the ATTR7-0 bits. At DATTC bit = "0", the ATTL7-0 bits control the left channel level and the ATTR7-0 bits control the right channel level.

ATS: Digital attenuator transition time setting (Table 18)
0: 1061/fs (default)
1: 7424/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTL7-0: Setting of the attenuation value of output signal from DACL (Table 17)
ATTR7-0: Setting of the attenuation value of output signal from DACR (Table 17)
Default: "00H" (MUTE)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Headphone Out Select 0	HPG1	HPG0	MINHR	MINHL	RINHR	LINHL	DARHR	DALHL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DALHL: DAC left channel output signal is added to the left channel of the headphone-amp.
0: OFF (default)
1: ON

DARHR: DAC right channel output signal is added to the right channel of the headphone-amp.
0: OFF (default)
1: ON

LINHL: Input signal to LIN pin is added to the left channel of the headphone-amp.
0: OFF (default)
1: ON

RINHR: Input signal to RIN pin is added to the right channel of the headphone-amp.
0: OFF (default)
1: ON

MINHL: Input signal to MIN pin is added to the left channel of the headphone-amp.
0: OFF (default)
1: ON

MINHR: Input signal to MIN pin is added to the right channel of the headphone-amp.
0: OFF (default)
1: ON

HPG1-0: DAC → HPL/R Gain (Table 25)
Default: "00": +0.95dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Lineout Select 0	0	LOG	MINR	MINL	RINR	LINL	DARR	DALL
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DALL: DAC left channel output is added to the LOUT buffer amp.
0: OFF (default)
1: ON

DARR: DAC right channel output is added to the ROUT buffer amp.
0: OFF (default)
1: ON

LINL: Input signal to the LIN pin is added to the LOUT buffer amp.
0: OFF (default)
1: ON

RINR: Input signal to the RIN pin is added to the ROUT buffer amp.
0: OFF (default)
1: ON

MINL: Input signal to the MIN pin is added to the LOUT buffer amp.
0: OFF (default)
1: ON

MINR: Input signal to the MIN pin is added to the ROUT buffer amp.
0: OFF (default)
1: ON

LOG: DAC → LOUT/ROUT Gain
0: 0dB (default)
1: +6dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTS3-0: Analog volume control for LOUT/ROUT (Table 26)
Default: LMUTE bit = "1", ATTS3-0 bits = "0000" (MUTE)

Setting of ATTS3-0 bits is enabled at LMUTE bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Headphone Out Select	0	0	0	0	0	0	LINHR	RINHL
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

RINHL: RIN signal is added to the left channel of the Headphone-Amp
0: OFF (default)
1: ON

LINHR: LIN signal is added to the right channel of the Headphone-Amp
0: OFF (default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Headphone ATT	0	HPZ	HMUTE	ATTH4	ATTH3	ATTH2	ATTH1	ATTH0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTH4-0: Setting of the attenuation value of output signal from Headphone (Table 25)
Default: HMUTE bit = "0", ATTH4-0 bits = "00" (0dB)

Setting of ATTH4-0 bits is enabled at HMUTE bit is "0".

HMUTE: Mute control for Headphone-Amp (Table 25)
0: Normal operation. ATTH4-0 bits control attenuation value. (default)
1: Mute. ATTH4-0 bits are ignored.

HPZ: Headphone-Amp Pull-down Control
0: Shorted to GND (default)
1: Pulled-down by 200kΩ (typ)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Lineout Select	0	0	0	0	0	0	LINR	RINL
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

RINL: RIN signal is added to the left channel of the Lineout
0: OFF (default)
1: ON

LINR: LIN signal is added to the right channel of the Lineout
0: OFF (default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Mono Mixing	0	0	0	0	0	0	LM	LHM
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

LHM: LIN/RIN signal is added to Headphone-Amp as (L+R)/2.
0: OFF (default)
1: ON

LM: LIN/RIN signal is added to LOUT/ROUT as (L+R)/2.
0: OFF (default)
1: ON

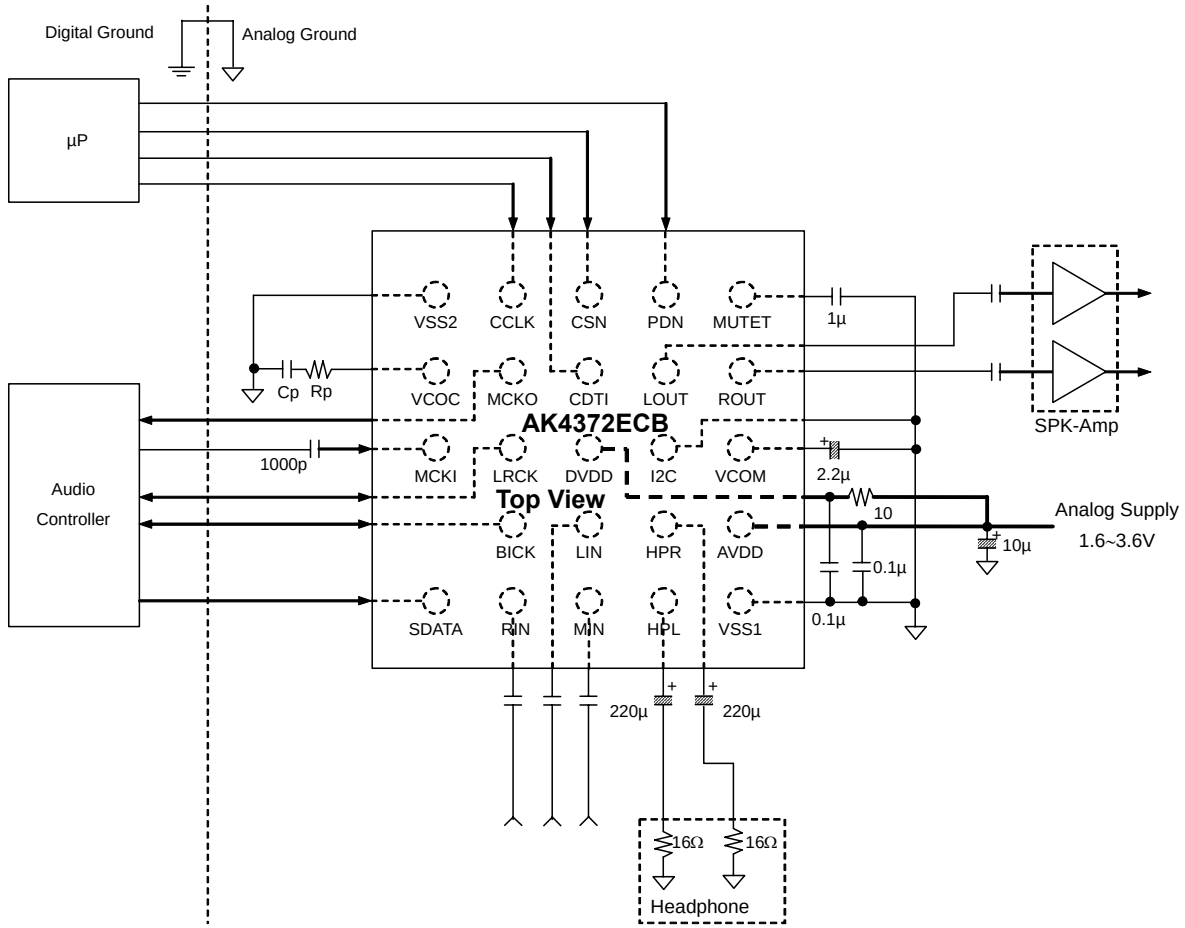
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Differential Select	0	0	0	0	0	0	LDIFH	LDIF
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

LDIF: Switch control from IN+/IN− pin to LOUT/ROUT.
0: OFF (default)
1: ON
When LDIF bit = "1", the LIN1 and RIN1 pins become IN+ and IN− pins respectively.

LDIFH: Switch control from the IN+/IN− pin to Headphone-Amp. (Setting of LIDFH bit is enable at LDIF bit = "1")
0: OFF (default)
1: ON

SYSTEM DESIGN

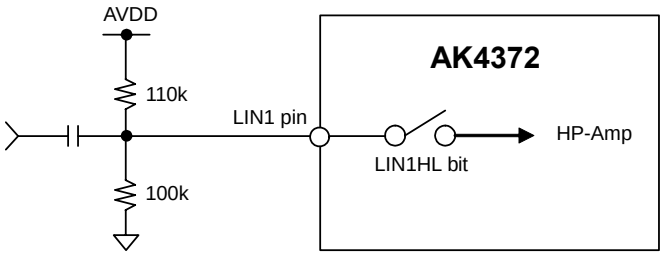
Figure 50 shows the system connection diagram. The evaluation board [AKD4372] demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- VSS1 and VSS2 of the AK4372 should be distributed separately from the ground of external controllers.
- All digital input pins (I2C, SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN) must not be left floating.
- When the AK4372 is in EXT mode (PMPLL bit = "0"), a resistor and capacitor for the VCOC pin are not needed.
- When the AK4372 is in PLL mode (PMPLL bit = "1"), a resistor and capacitor for the VCOC pin are shown in Table 4
- When the AK4372 is used in master mode, LRCK and BICK pins are floating before the M/S bit is changed to "1". Therefore, a 100kΩ pull-up resistor should be connected to the LRCK and BICK pins of the AK4372.
- When DVDD is supplied from AVDD via 10Ω series resistor, the capacitor larger than 0.1µF should not be connected between DVDD and the ground.

Figure 50. Typical Connection Diagram (In case of AC coupling to MCKI)



Note: If the path is OFF and the signal is input to the input pin, the input pin should be biased to a voltage equivalent to VCOM voltage (= 0.475 x AVDD) externally.

Figure 51. External Bias Circuit Example for Line Input Pin

1. Grounding and Power Supply Decoupling

The AK4372 requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the analog power supply in the system and DVDD is supplied from AVDD via a 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD should be powered-up after DVDD rises up to 1.6V or more. When the AK4372 is powered-down, DVDD should be powered-down at the same time or later than AVDD. VSS1 and VSS2 must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4372 as possible, with the small value ceramic capacitors being the nearest.

2. Voltage Reference

The input voltage to AVDD sets the analog output range. Usually a 0.1μF ceramic capacitor is connected between AVDD and VSS1. VCOM is a signal ground of this chip (0.475 x AVDD). The electrolytic capacitor around 2.2μF attached between VCOM anVSS1 eliminates the effects of high frequency noise, too. No load current may be drawn from the VCOM pin. All signals, especially clock, should be kept away from AVDD and VCOM in order to avoid unwanted coupling into the AK4372.

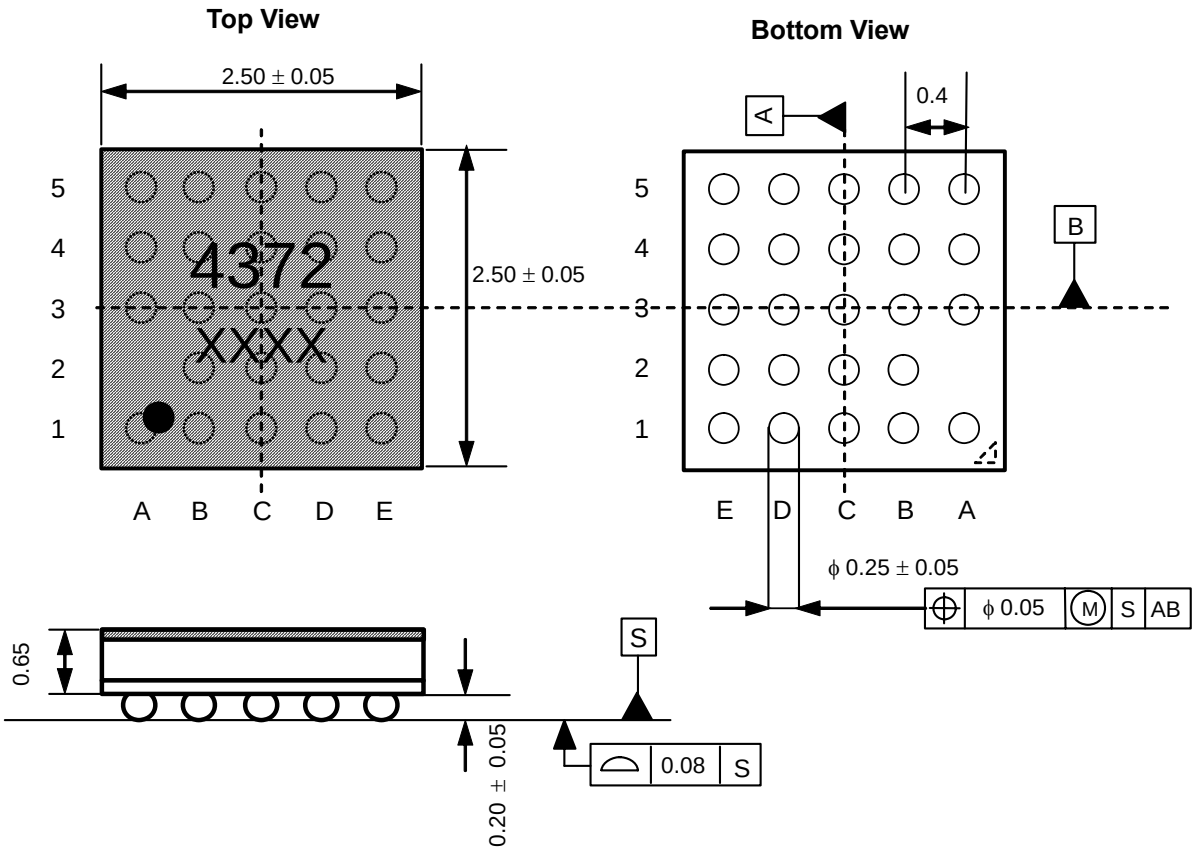
3. Analog Outputs

The analog outputs are single-ended outputs, and 0.48 x AVDD Vpp(typ)@−3dBFS for headphone-amp, 0.61xAVDD Vpp(typ) @0dBFS for LOUT/ROUT centered on the VCOM voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFFH(@24bit) and negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit).

DC offsets on the analog outputs should be eliminated by AC coupling since the analog outputs have a DC offset equal to VCOM plus a few mV.

PACKAGE

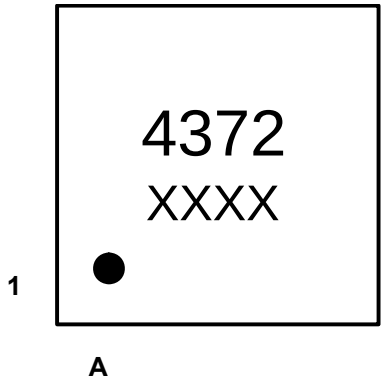
24pin CSP (Unit: mm)



■ Material & Lead finish

Package material: Epoxy resin, Halogen (bromine and chlorine) free
Solder ball material: SnAgCu

MARKING



XXXX: Date code (4 digit)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/10/30	00	First Edition		
08/12/04	01	Product Addition	1, 3, 4, 6	AK4372VCB was added. Ambient Temperature AK4372ECB: –30 ~ 85°C AK4372VCB: –40 ~ 85°C
		Specification Change	53	Package material was changed.
08/12/19	02	Description Addition	39-42	Power-Up/Down Sequence (PLL Slave mode, PLL Master mode) were added.