AK4365
DAC with built-in PLL & HP-AMP

GENERAL DESCRIPTION

The AK4365 is 20bit DAC with built-in PLL and Headphone Amplifier. The PLL input crystal frequency is matched to typical mobile phone clock frequencies. The AK4365 features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features “click-free” power-on/off, a mute control and delivers 10mW of power at 16Ω. The AK4365 is housed in a 28pin QFN package, making it suitable for portable applications.

FEATURE

- ☐ **Multi-bit ΔΣ DAC**
- ☐ **Sampling Rate**
  - **8kHz, 11.025kHz,16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz**
- ☐ **On chip perfect filtering 8 times FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.02dB**
  - **Stopband Attenuation: 57dB**
- ☐ **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
- ☐ **PLL:**
  - **Input Frequency: 19.8MHz, 19.68MHz, 19.2MHz, 15.36MHz, 14.4MHz, 13MHz, 12MHz and 11.2896MHz**
  - **Input Level: CMOS or 0.4Vpp Analog Input**
- ☐ **Audio I/F Format: MSB First, 2’s Compliment**
  - **I^2S, 20bit MSB justified, 20bit/16bit LSB justified**
  - **Master/Slave Mode**
- ☐ **Digital ATT**
- ☐ **Analog Mixing Circuit**
- ☐ **Mono Lineout**
- ☐ **µP Interface: 3-wire**
- ☐ **Low Frequency Boost Function**
- ☐ **Headphone Amplifier**
  - **Output Power: 10mW x 2ch @16Ω (THD+N=0.3%)**
  - **S/N: 88dB**
  - **Click Noise Free at Power-ON/OFF and Mute**
- ☐ **Power Supply: 3V±10%**
- ☐ **Power Supply Current: 11.5mA (@HP-AMP no-input)**
- ☐ **Ta: -30 ~ 85°C**
- ☐ **Small Package: 28pin QFN**

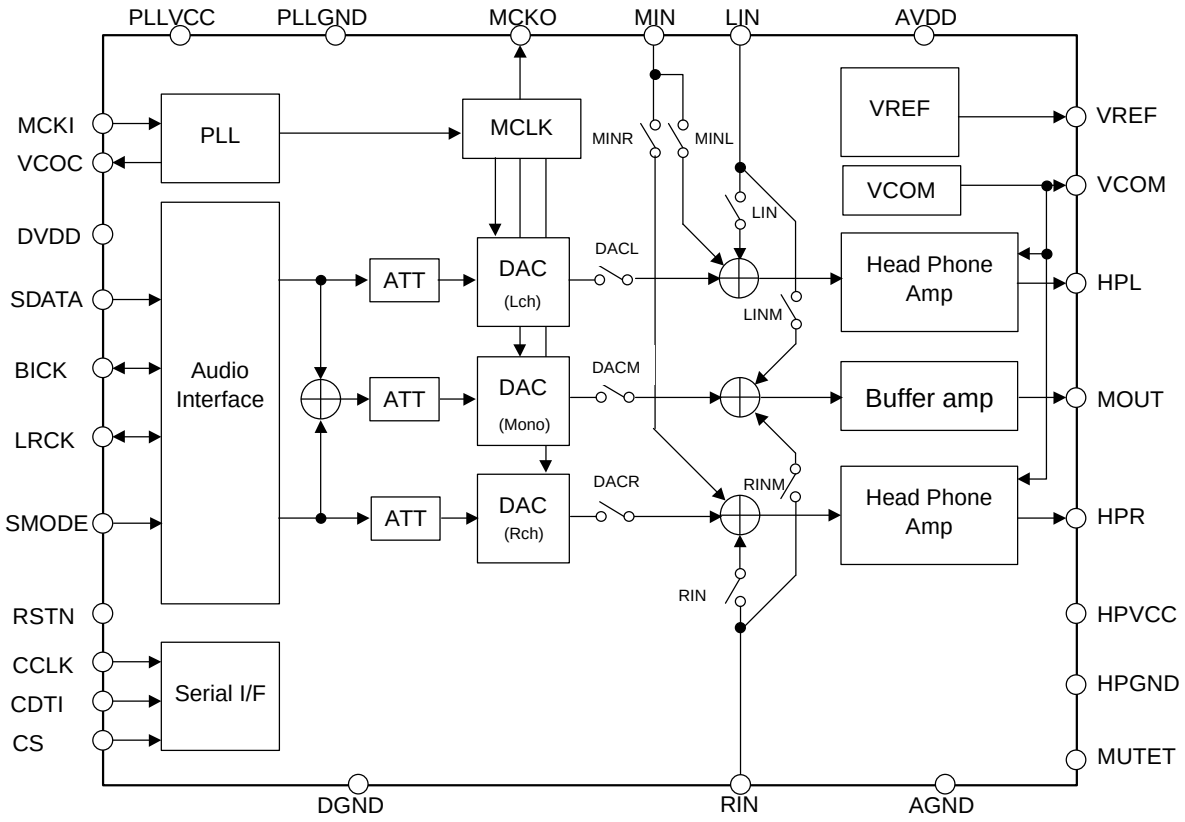
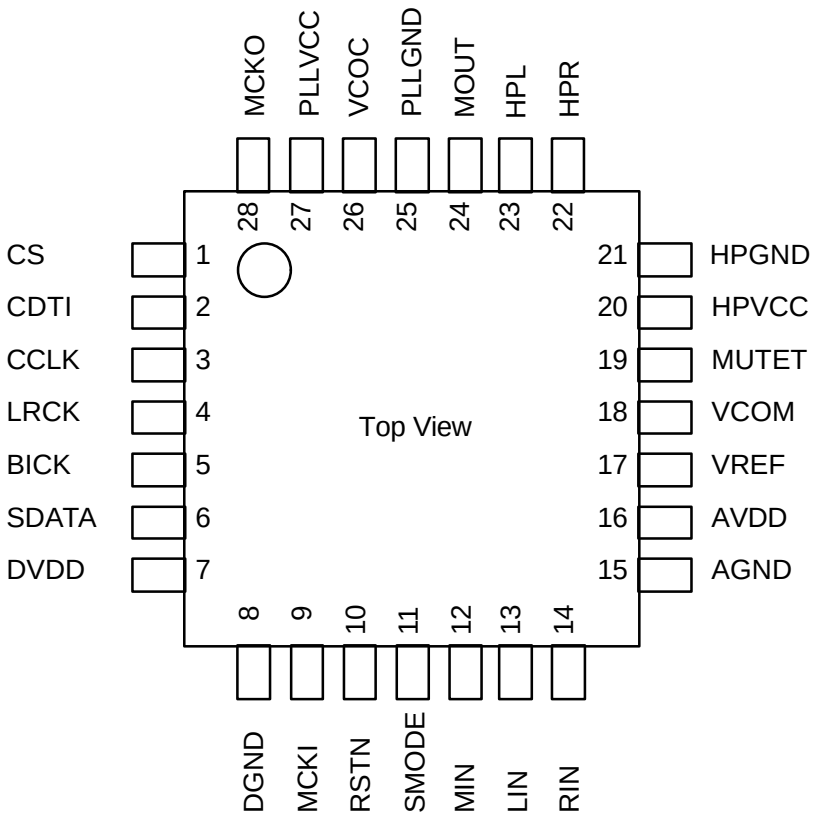


Figure 1. AK4365 Block Diagram

■ Ordering Guide

AK4365VN	-30 ~ +85°C	28pin QFN (0.5mm pitch)
AKD4365	Evaluation board for AK4365	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	CS	I	Control Data Chip Select Pin
2	CDTI	I	Control Data Input Pin
3	CCLK	I	Control Clock Input Pin
4	LRCK	I/O	L/R Clock Pin This clock determines which audio channel is currently being input on SDATA pin. When SMODE pin = "L", a clock with fs rate is output. This pin is fixed to "L" at power-down. When SMODE pin = "H", a L/R clock is input.
5	BICK	I/O	Serial Bit Clock Pin This clock is used to latch audio data. When SMODE pin = "L", a clock with 32fs or 64fs rate is output. This pin is fixed to "L" at power-down. When SMODE pin = "H", a bit clock is input.
6	SDATA	I	Audio Data Input Pin
7	DVDD	-	Digital Power Supply Pin
8	DGND	-	Digital Ground Pin
9	MCKI	I	Master Clock Input Pin
10	RSTN	I	Reset Pin When at "L", the AK4365 is in power-down mode and is held in reset. The AK4365 should always be reset upon power-up.
11	SMODE	I	Master/Slave Mode Select Pin "L": Master Mode, "H": Slave Mode
12	MIN	I	Mono Analog Input Pin
13	LIN	I	Lch Analog Input Pin
14	RIN	I	Rch Analog Input Pin
15	AGND	-	Analog Ground Pin
16	AVDD	-	Analog Power Supply Pin
17	VREF	O	Reference Voltage Output Pin, 2.0V (typ, respect to AGND) Normally connected to AGND pin with 0.1µF ceramic capacitor in parallel with a 10µF electrolytic capacitor.
18	VCOM	O	Common Voltage Output Pin, 1.0V (typ, respect to AGND) Normally connected to AGND pin with 0.1µF ceramic capacitor in parallel with a 1µF electrolytic capacitor.
19	MUTET	O	Mute Time Constant Control Pin Connected to AGND pin with a capacitor for mute time constant.
20	HPVCC	-	Power Supply Pin for Headphone Amplifier
21	HPGND	-	Ground Pin for Headphone Amplifier
22	HPR	O	Rch Headphone Amplifier Output Pin
23	HPL	O	Lch Headphone Amplifier Output Pin
24	MOUT	O	Monaural Analog Output Pin
25	PLLGND	-	Ground Pin for PLL. Connected to AGND.
26	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AGND with one resistor and one capacitor in series.
27	PLLVCC	-	Power Supply Pin for PLL. Normally connected to AVDD.
28	MCKO	O	Master Clock Output Pin

Note: All digital input pins must not be left floating.

ABSOLUATE MAXIMUM RATING

(AGND, DGND, HPGND, PLLGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
	PLL	PLLVCC	-0.3	4.6	V
	HP-AMP	HPVCC	-0.3	4.6	V
	|AGND – HPGND| (Note 2)	ΔGND1	-	0.3	V
	|AGND – DGND| (Note 2)	ΔGND2	-	0.3	V
	|AGND – PLLGND| (Note 2)	ΔGND3	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN, MIN pins)		VINA	-0.3	AVDD+0.3 or 4.6	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3 or 4.6	V
Ambient Temperature		Ta	-30	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. AGND, DGND, HPGND and PLLGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AGND, DGND, HPGND, PLLGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog (Note 3)	AVDD	2.7 or (HPVCC – 0.4)	2.9	3.3	V
	Digital	DVDD	2.7	2.9	3.3	V
	PLL	PLLVCC	2.7	2.9	3.3	V
	HP-AMP	HPVCC	2.7	2.9	3.3	V

Note 1. All voltages with respect to ground.

Note 3. Minimum value is higher value between 2.7V and (HPVCC - 0.4)V.

Note 4. Figure 24 and Figure 25 shows the sequence in case that only AVDD is powered ON/OFF when DVDD is powered ON.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=PLLVCC=DVDD=HPVCC=2.9V,AGND=PLLGND=DGND=HPGND=0V; fs=44.1kHz; EXT=1; BOOST OFF; Slave Mode; Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Load impedance is a serial connection with R_L =16Ω and C_L=220μF. (Refer to Figure 26); unless otherwise specified)

Parameter	min	typ	max	Units
DAC Resolution			20	bit
LINEIN: (LIN/RIN/MIN pins)				
Analog Input Characteristics				
Input Resistance	14	20	26	kΩ
Gain (Note 5)	+5	+6	+7	dB
Headphone-Amp: (HPL/HPR pins) (Note 6)				
Analog Output Characteristics				
THD+N (0dBFS Output)		-50	-40	dB
D-Range (-60dBFS Output, A-weighted)	82	88		dB
S/N (A-weighted)	82	88		dB
Interchannel Isolation	55	80		dB
DC Accuracy				
Interchannel Gain Mismatch		0.3	0.5	dB
Gain Drift	-	200	-	ppm/°C
Load Resistance (Note 7)	16			Ω
Load Capacitance			300	pF
Output Voltage	1.00	1.12	1.24	Vpp
Mono Output: (MOUT pin) (Note 8)				
Analog Output Characteristics:				
THD+N (0dBFS Output)		-80	-65	dB
S/N (A-weighted)	79	85		dB
DC Accuracy				
Gain Drift	-	200	-	ppm/°C
Load Resistance (Note 7)	10			kΩ
Load Capacitance			25	pF
Output Voltage	1.00	1.12	1.24	Vpp
Power Supplies				
Power Supply Current Normal Operation (DAC=HPL=HPR=MOUT= "1") AVDD + PLLVCC + DVDD + HPVCC (Note 9) Power-Down Mode (DAC=HPL=HPR=MOUT= "0") AVDD + PLLVCC + DVDD + HPVCC (Note 10)		 11.5 1	 18 100	 mA μA
Power Supply Rejection (Note 11)	-	50	-	dB

Note 5. Analog signal inputted from LIN/RIN/MIN pin is gained to +6dB internally.
Note 6. DACL=DACR= "1", MINL=MINR=LIN=RIN= "0"
Note 7. AC Load
Note 8. DACM= "1", LINM=RINM= "0"
Note 9. HP-Amp no output. MCKO = "0"
Note 10. MINL=MINR=LIN=RIN= "0". In power-down mode, all digital input pins including clock pins (MCKI, BICK and LRCK) are held at DVDD or DGND. RSTN pin is held at DGND.
In case of MINL, MINR, LIN, RIN, LINM or RINM = "1", the power supply current of AVDD pin is about 0.5mA (typ.).
Note 11. PSR is applied to AVDD, PLLVCC, DVDD and HPVCC with 1kHz, 100mVpp.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PLLVCC, HPVCC=2.7 ~ 3.3V; fs=44.1kHz; De-emphasis = "OFF")

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 12)							
Passband	-0.05dB (Note 13)		PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband (Note 13)			SB	24.1			kHz
Passband Ripple			PR			±0.02	dB
Stopband Attenuation			SA	57			dB
Group Delay (Note 14)			GD	-	19.1	-	1/fs
Group Delay Distortion			ΔGD		0		μs
DAC Digital Filter + Analog Filter: (Note 12)(Note 15)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
Analog Filter: (Note 16)							
Frequency Response	0 ~ 20.0kHz		FR	-	±1.0	-	dB
BOOST Filter: (Note 15) (Note 17)							
Frequency Response	MIN	20Hz	FR	-	-4.21	-	dB
		100Hz		-	-7.03	-	dB
		1kHz		-	-10	-	dB
	MID	20Hz	FR	-	-4.05	-	dB
		100Hz		-	-6.04	-	dB
		1kHz		-	-9.9	-	dB
	MAX	20Hz	FR	-	-4.34	-	dB
		100Hz		-	-5.35	-	dB
		1kHz		-	-9.7	-	dB

Note 12. BOOST OFF (BST1-0 = "00")

Note 13. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.05dB), SB=0.546*fs(@-57dB).

Note 14. This is the calculated delay time caused by digital filtering. This time is measured from the setting of the 20bit data of both channels to the input registers to the output of the analog signal.

Note 15. DACL → HPL, DACR → HPR, DACM → MOUT

Note 16. MIN → HPL/HPR, LIN → HPL/MOUT, RIN → HPR/MOUT

Note 17. These frequency responses are characteristics with BOOST ON and -10dBFS digital data input.

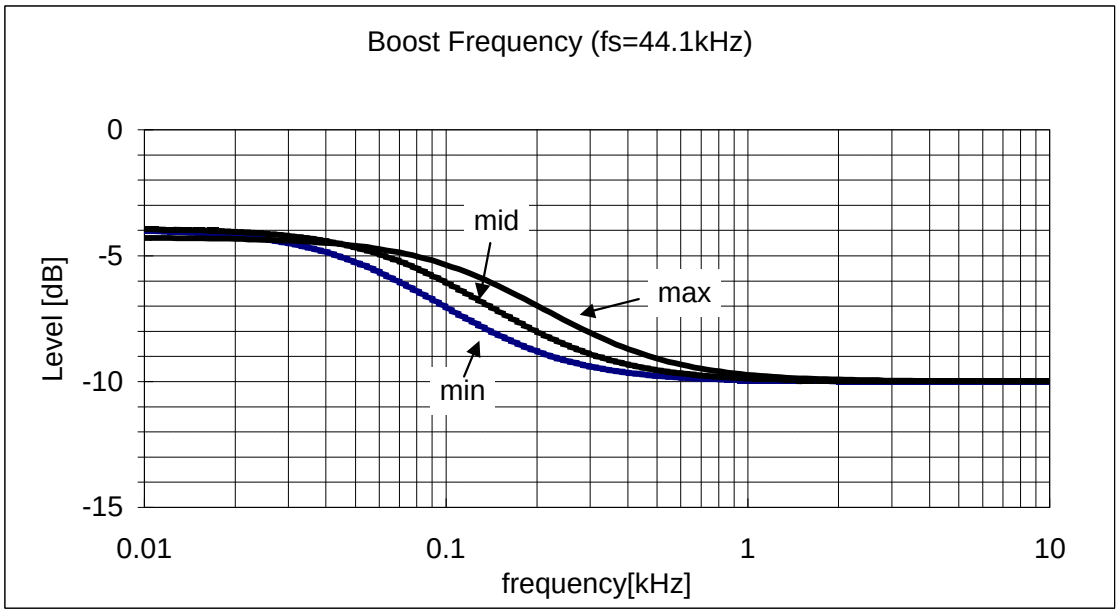


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PLLVCC = 2.7 ~ 3.3V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD		-	V
Low-Level Input Voltage	VIL	-		30%DVDD	V
Input Voltage at AC Coupling (Note 18)	VAC	0.4			Vpp
High-Level Output Voltage (Iout = -400µA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout = 400µA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

Note 18. Only MCKI pin. (Figure 26)

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PLLVCC = 2.7 ~ 3.3V: CL = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency (EXT= "0")	fCLK	11.2896		19.8	MHz
(EXT= "1")	fCLK	2.048		12.288	MHz
Pulse Width Low (Note 19)	tCLKL	0.4/fCLK			ns
Pulse Width High (Note 19)	tCLKH	0.4/fCLK			ns
AC Pulse Width (Note 23)	tACW	20			ns
LRCK					
Frequency	fs	8	44.1	48	kHz
Duty Cycle: Slave Mode	Duty	45		55	%
Master Mode	Duty		50		%
MCKO Output (PLL mode)					
Frequency	fCLKO	0.256		12.288	MHz
Duty Cycle (except fs=32kHz, PS1-0= "00")	dMCK	40		60	%
(fs=32kHz, PS1-0= "00")	dMCK	30		70	%
Serial Interface Timing (Note 20)					
Slave Mode (SMODE = "H"):					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	50			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	50			ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Master Mode (SMODE = "L"):					
BICK Frequency (BF = "0")	fBCK		64fs		Hz
(BF = "1")	fBCK		32fs		Hz
BICK Duty	dBCK		50		%
BICK "↓" to LRCK	tMBLR	-50		50	ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CS "H" Time	tCSW	150			ns
CS "L" Time	tCSW	150			ns
CS "↑" to CCLK "↑"	tCSS	150			ns
CCLK "↑" to CS "↑"	tCSH	50			ns
Reset Timing					
RSTN Pulse Width (Note 22)	tRST	300			ns

Note 19. Except AC coupling.

Note 20. Refer to "Serial Data Interface".

Note 21. BICK rising edge must not occur at the same time as LRCK edge.

Note 22. The AK4365 can be reset by bringing RSTN= "L" to "H" only upon power up.

Note 23. Pulse width to ground level when MCKI is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3.)

■ Timing Diagram

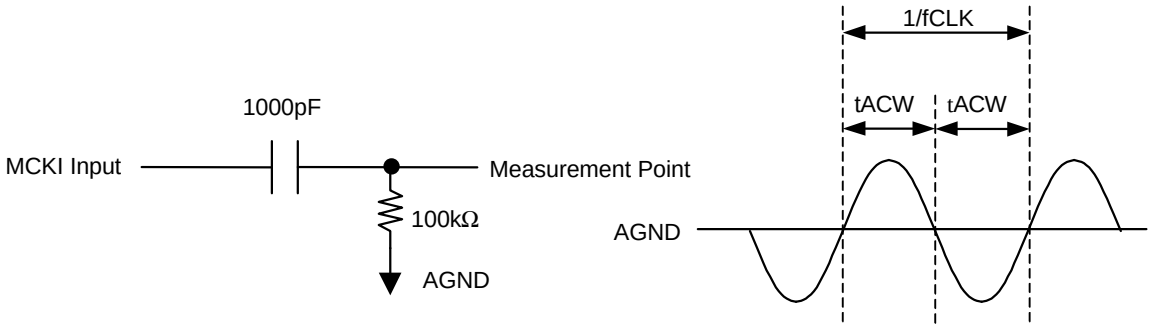


Figure 3. MCKI AC Coupling Timing

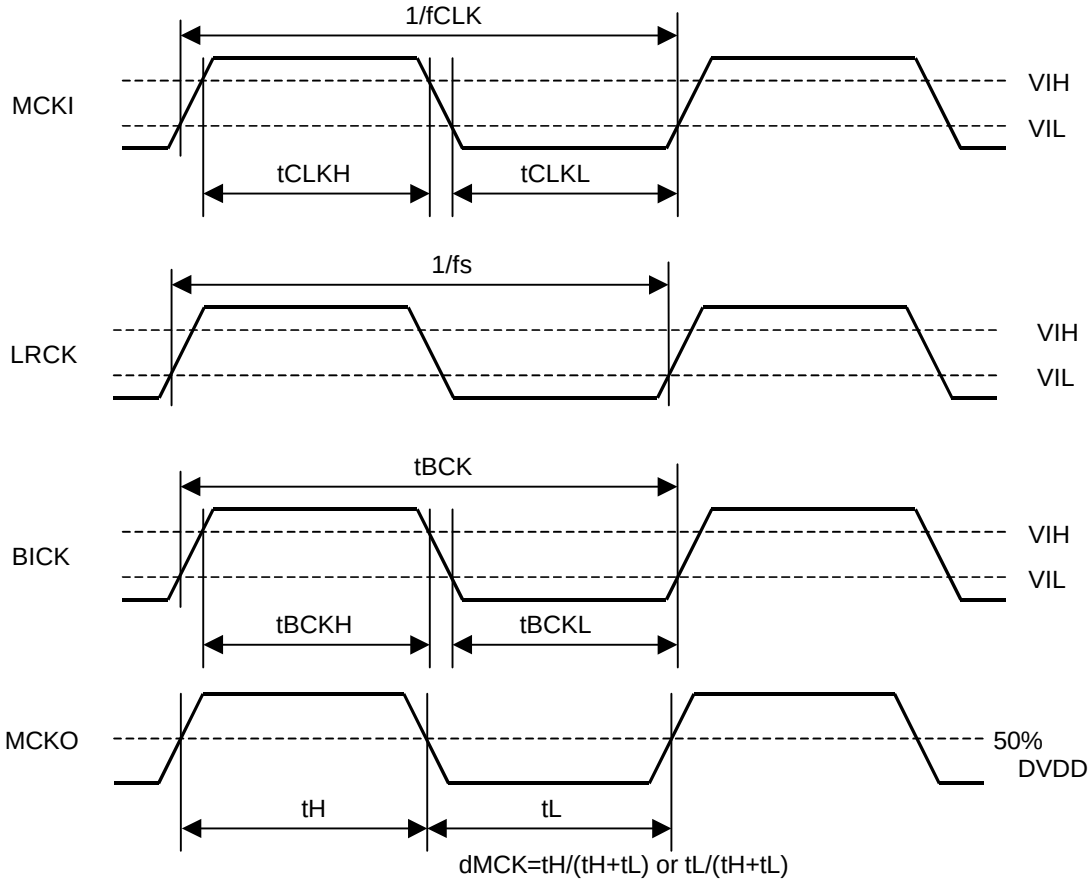


Figure 4. Clock Timing

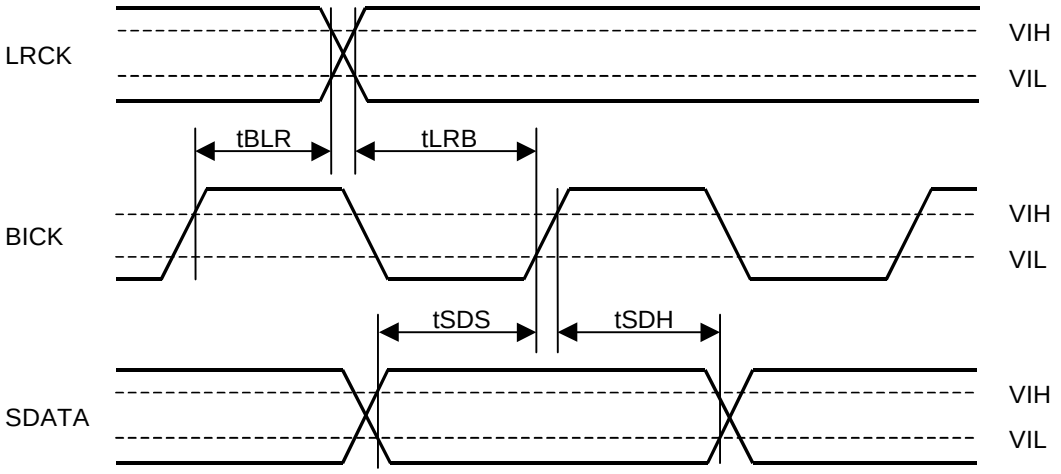


Figure 5. Serial Interface Timing (Slave Mode)

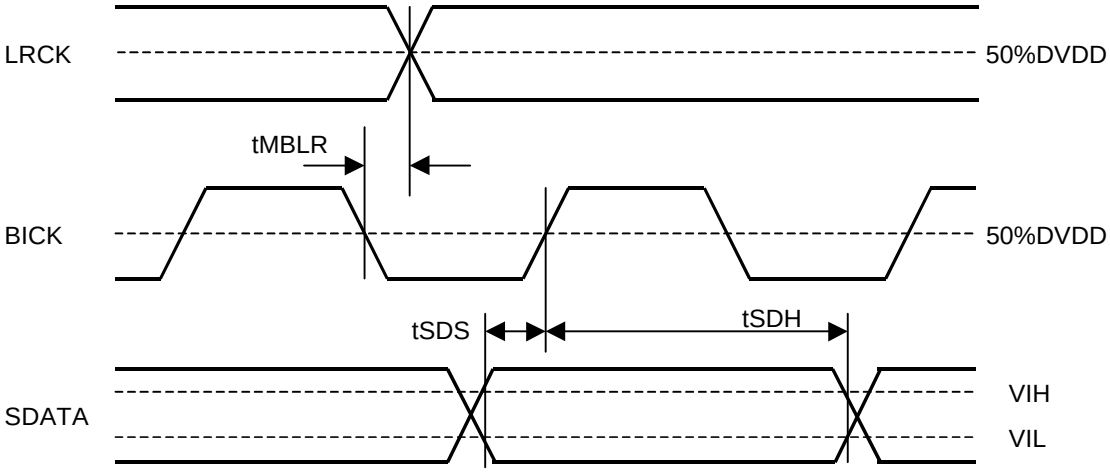


Figure 6. Serial Interface Timing (Master mode)

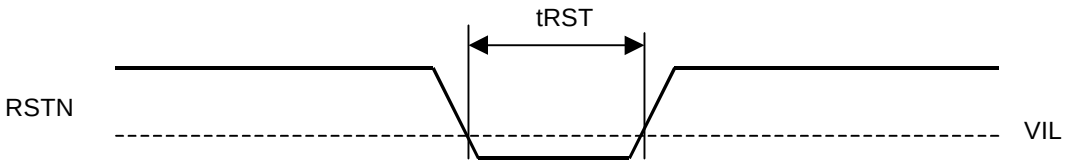


Figure 7. Power-down & Reset Timing

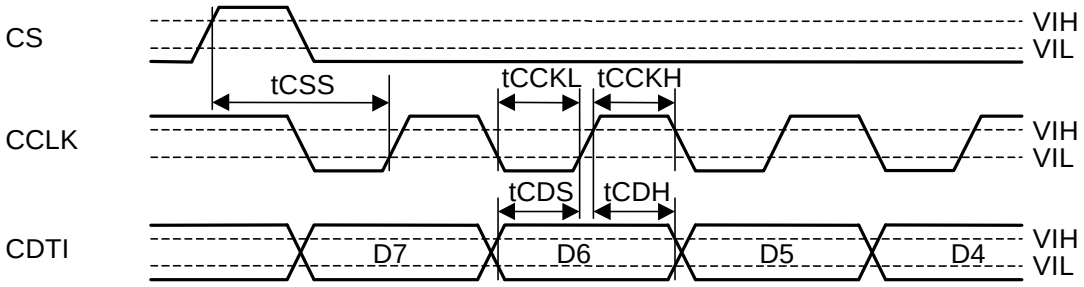


Figure 8. WRITE Command Input Timing

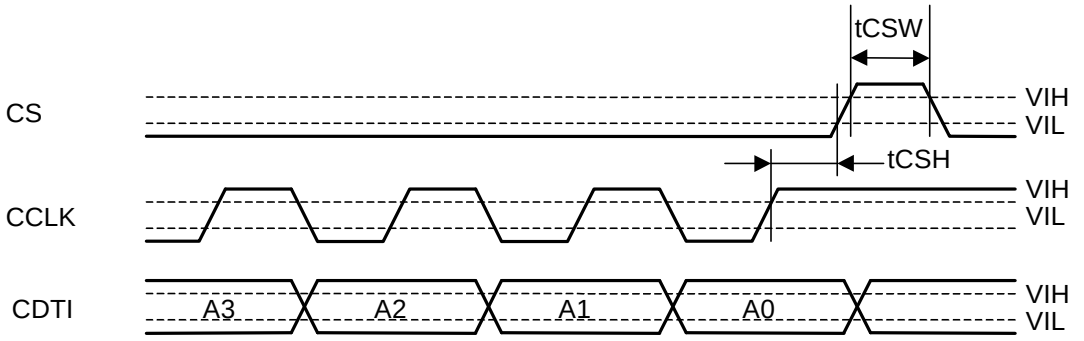


Figure 9. WRITE Data Input Timing

OPERATION OVERVIEW

■ System Clock

1) PLL mode (EXT bit = “0”)

A fully integrated analog phase locked loop (PLL) generates a clock that is selected by PLL2-0 and FS2-0 bits (refer to Table 1 and Table 2). MCKO output frequency can be controlled by PS1-0 bits (addr=8FH, Table 3). MCKO output can be enabled by controlling MCKO bit. The lock time of PLL is 20ms from the changing of sampling frequency, and it is also 20ms after a stable MCKI clock is attained after power-up. To decrease output noise from DAC, serial input data is zeroed internally when PLL is not locked. When DAC is powered-up (DAC bit = “1”) from power-down state (DAC bit = “0”), there is a 5ms delay before the internal circuit starts up. When changing the sampling frequency during normal operation (DAC bit = “1”), the change of sampling frequency should occur after the input is muted, or input to “0” data.

LRCK and BICK are output from the AK4365 in master mode. When the clock input to MCKI pin stops during normal operation (DAC bit = “1”), the internal PLL oscillates (freewheels) at a few MHz, and LRCK and BICK outputs go to “L” (refer to Table 4).

LRCK input should be synchronized with MCKI or MCKO at slave mode. LRCK and BICK should always be present whenever the AK4365 is in normal operation mode (DAC bit = “1”). If these clocks are not provided, the AK4365 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4365 should be placed in the power-down mode (DAC bit = “0”).

Mode	PLL2	PLL1	PLL0	MCKI	
0	0	0	0	11.2896MHz	Default
1	0	0	1	14.4MHz	
2	0	1	0	12MHz	
3	0	1	1	19.2MHz	
4	1	0	0	15.36MHz	
5	1	0	1	13MHz	
6	1	1	0	19.68MHz	
7	1	1	1	19.8MHz	

Table 1. MCKI Input Frequency (PLL mode)

Mode	FS2	FS1	FS0	fs	
0	0	0	0	48kHz	
1	0	0	1	24kHz	
2	0	1	0	32kHz	
3	0	1	1	16kHz	
4	1	0	0	44.1kHz	Default
5	1	0	1	22.05kHz	
6	1	1	0	11.025kHz	
7	1	1	1	8kHz	

Table 2. Sampling Frequency (PLL mode)

PS1	PS0	MCKO	
0	0	256fs	Default
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 3. MCKO frequency (PLL mode, MCKO bit = “1”)

	Master Mode (SMODE = “L”)		
	Power Up (DAC bit = “1”)	Power Down (DAC bit = “0”)	PLL Unlock
MCKI pin	Refer to Table 1	Don’t care	Refer to Table 1
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”	“L”
LRCK pin	Output	“L”	“L”

Table 4. Clock Operation at Master mode

	Slave Mode (SMODE = “H”)		
	Power Up (DAC bit = “1”)	Power Down (DAC bit = “0”)	PLL Unlock
MCKI pin	Refer to Table 1	Don’t care	Refer to Table 1
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”:Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	Input	Fixed to “L” or “H” externally	Input
LRCK pin	Input	Fixed to “L” or “H” externally	Input

Table 5. Clock Operation at Slave mode

2) EXT mode (EXT bit = “1”)

The AK4365 can be set to external clock mode (EXT mode) by setting EXT bit (control register: 8FH) to “1”. In EXT mode, the master clock can be directly input to DAC via MCKI pin without PLL. In this case, the sampling frequency and MCKI frequency can be selected by FS2-0 bits (refer to Table 6). In EXT mode, PLL2-0 bits are ignored. Table 6 shows typical sampling frequencies. The sampling frequency can be adjusted from 8kHz to 48kHz by leaving FS2-0 bits fixed and altering the MCKI frequency. For example, when MCKI=256fs, the sampling frequency can be changed from 8kHz to 48kHz. MCKO output is enabled by controlling MCKO bit. MCKO output frequency can be controlled by PS1-0 bits. When DAC is powered-up (DAC bit = “1”) from power-down state (DAC bit = “0”), there is a 5ms delay prior to internal circuit starting up. When changing the sampling frequency during normal operation (DAC bit = “1”), the change of sampling frequency should occur after the input is muted, or input to “0” data.

LRCK and BICK are output from the AK4365 in master mode. The clock input to MCKI pin should always be present whenever the AK4365 is in normal operation (DAC bit = “1”). If these clocks are not provided, the AK4365 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4365 should be placed in the power-down mode (DAC bit = “0”).

The external clocks required to operate the AK4365 in slave mode are MCKI, LRCK and BICK. The master clock (MCKI) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. All external clocks (MCKI, BICK and LRCK) should always be present whenever the AK4365 is in normal operation mode (DAC bit = “1”). If these clocks are not provided, the AK4365 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4365 should be placed in the power-down mode (DAC bit = “0”).

Mode	FS2	FS1	FS0	fs	MCKI	
0	0	0	0	48kHz	256fs	
1	0	0	1	24kHz	512fs	
2	0	1	0	32kHz	256fs	
3	0	1	1	16kHz	512fs	
4	1	0	0	44.1kHz	256fs	Default
5	1	0	1	22.05kHz	512fs	
6	1	1	0	11.025kHz	1024fs	
7	1	1	1	8kHz	1024fs	

Table 6. Relationship between Sampling Frequency and MCKI Frequency (EXT mode)

PS1	PS0	MCKO	
0	0	256fs	Default
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 7. MCKO frequency (EXT mode, MCKO bit = “1)

	Master Mode (SMODE = “L”)	
	Power Up (DAC bit = “1”)	Power Down (DAC bit = “0”)
MCKI pin	Refer to Table 6	Don’t care
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”
LRCK pin	Output	“L”

Table 8. Clock Operation at Master mode (EXT mode)

	Slave Mode (SMODE = “H”)	
	Power Up (DAC bit = “1”)	Power Down (DAC bit = “0”)
MCKI pin	Refer to Table 6	Don’t care
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	Input	Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally

Table 9. Clock Operation at Slave mode (EXT mode)

When low sampling rate, DR and S/N degrade because of the outband noise. DR and S/N are approved by using higher frequency for MCKI. Table 10 shows DR and S/N in the case DAC output to HP-amp.

MCKI	DR, S/N (A-weight)	
	fs=8kHz	fs=16kHz
256fs	63dB	81dB
512fs	81dB	88dB
1024fs	88dB	N/A

Table 10. Relationship between MCKI frequency and DR (and S/N) of HP-amp

■ Serial Data Interface

The AK4365 interfaces with external system by using SDATA, BICK and LRCK pins. Four data formats are available and are selected by setting DIF0 and DIF1 bits. Mode 0 is compatible with existing 16bit DACs and digital filters. Mode 1 is a 20bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Mode 2 and 3, 16bit data followed by four zeros also could be input, 18bit data followed by two zeros also could be input. In all modes, the serial data is MSB first and 2's complement format.

When master mode and BICK=32fs(BF bit = "0"), the AK4365 cannot be set to Mode 1 or Mode 2.

DIF1 bit	DIF0 bit	MODE	BICK	Figure
0	0	0: 16bit, LSB justified	≥ 32fs	Figure 10
0	1	1: 20bit, LSB justified	≥ 40fs	Figure 10
1	0	2: 20bit, MSB justified	≥ 40fs	Figure 11
1	1	3: I^2S Compatible	32fs or ≥ 40fs	Figure 12

Table 11. Audio Data Format

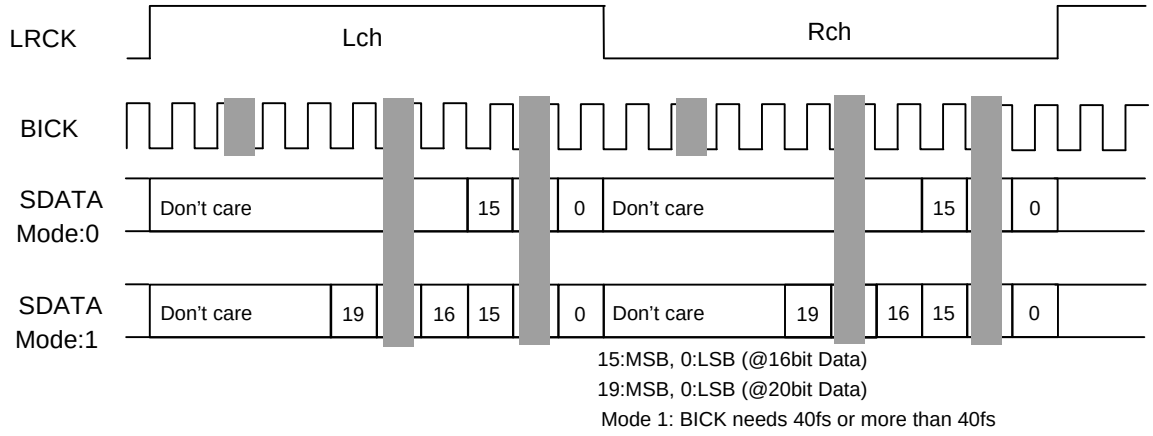


Figure 10. Mode 0,1 Timing

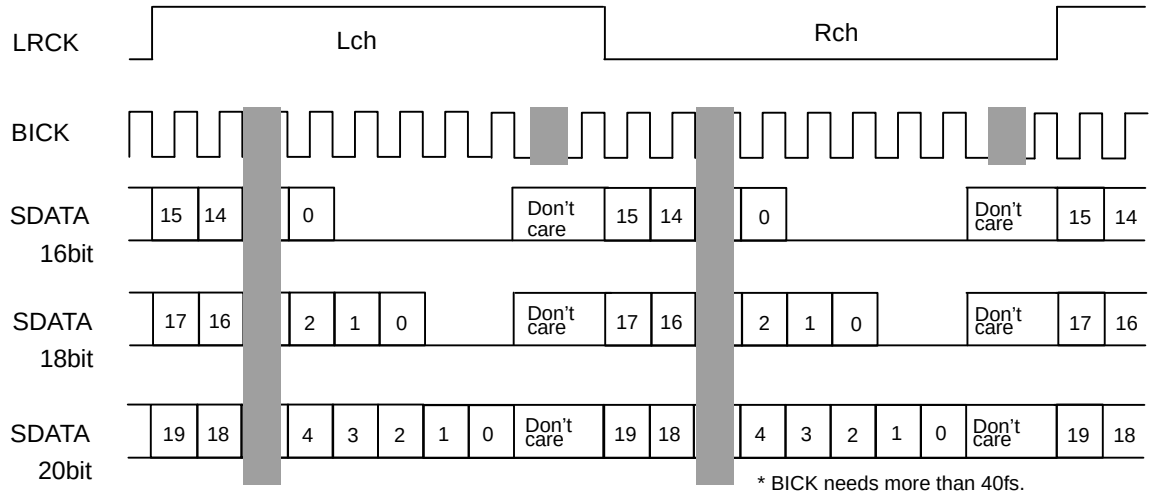


Figure 11. Mode 2 Timing

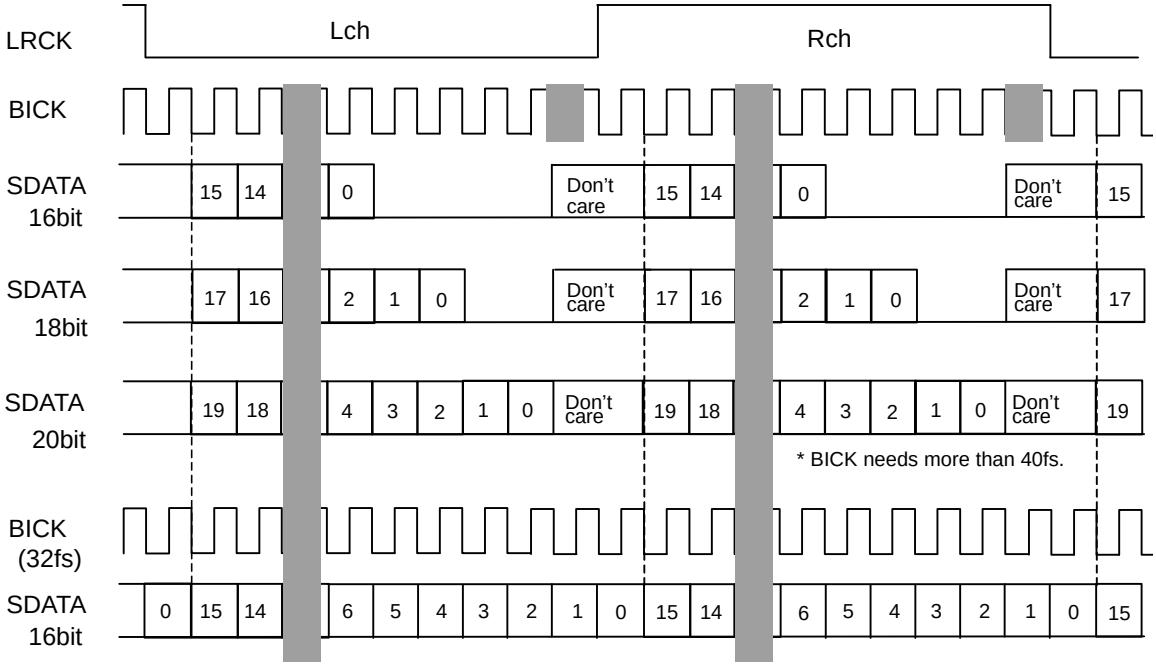
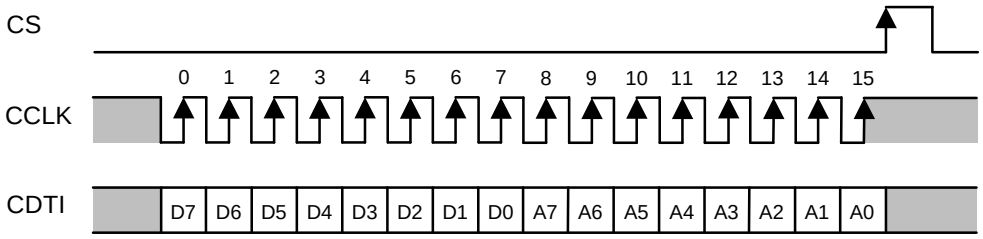


Figure 12. Mode 3 Timing

■ Serial Control Interface

Internal registers may be written to via the 3-wire µP interface pins (CS, CCLK and CDTI). The data on this interface consists of Control data (MSB first, 8bits) and Register address (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For WRITE operations, data is latched after a low-to-high transition of CS. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at RSTN = "L".



D7-D0: Control Data
A7-A0: Register Address

Figure 13. Control Interface

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
80H	PLL Mode & Timer	TM1	TM0	PLL2	PLL1	PLL0	FS2	FS1	FS0
81H	Mode Control	DIF1	DIF0	MCKO	DEM	LRMUTE	MMUTE	BST1	BST0
85H	Power Management	MINR	MINL	BF	MONO	MOUT	HPR	HPL	DAC
88H	Output Select 1	0	RINM	LINM	RIN	LIN	DACM	DACR	DACL
89H	HP-Amp Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
8BH	HP-Amp Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
8DH	MOUT ATT	ATTM7	ATTM6	ATTM5	ATTM4	ATTM3	ATTM2	ATTM1	ATTM0
8FH	Mode Control 2	0	0	PS0	PS1	CKP	LRP	0	EXT

■ Register Definitions

All registers inhibit writing at RSTN pin = "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
80H	PLL Mode & Timer	TM1	TM0	PLL2	PLL1	PLL0	FS2	FS1	FS0
Default		0	0	0	0	0	1	0	0

FS2-0: Select Sampling Frequency
PLL mode: Table 2
EXT mode: Table 6

PLL2-0: Select MCKI Frequency
PLL mode: Table 1
EXT mode: Disable

TM1-0: Soft Mute Time Setting. LRMUTE and MMUTE settings are linked together.

TM1	TM0	Cycle	
0	0	1024/fs	Default
0	1	512/fs	
1	0	256/fs	
1	1	128/fs	

Table 12. Soft Mute Time Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
81H	Mode Control	DIF1	DIF0	MCKO	DEM	LRMUTE	MMUTE	BST1	BST0
Default		0	0	0	0	0	0	0	0

BST1-0: Select Low Frequency Boost Function

BST1	BST0	Mode	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 13. Select Low Frequency Boost

MMUTE: The output data from DACM is soft-muted.
0: Disable (Default)
1: Enable

LRMUTE: The output data from DACL and DACR are soft-muted.
0: Disable (Default)
1: Enable

DEM: De-emphasis Filter Frequency Select
Sampling frequency of De-emphasis is selected by FS2-0 bits. Sampling frequency is enabled at 32kHz, 44.kHz and 48kHz only.

DEM	FS2	FS1	FS0	Sampling Frequency	De-emphasis	
0	-	-	-	-	OFF	Default
1	0	0	0	48kHz	ON: 48kHz	
	0	0	1	24kHz	OFF	
	0	1	0	32kHz	ON: 32kHz	
	0	1	1	16kHz	OFF	
	1	0	0	44.1kHz	ON: 44.1kHz	
	1	0	1	22.05kHz	OFF	
	1	1	0	11.025kHz	OFF	
	1	1	1	8kHz	OFF	

Table 14. De-emphasis Filter Frequency Select

MCKO: Control of MCKO signal
0: Disable (Default)
1: Enable

DIF1-0: Audio Data Interface Format

DIF1	DIF0	MODE	BICK	Figure	
0	0	0: 16bit, LSB justified	≥ 32fs	Figure 10	Default
0	1	1: 20bit, LSB justified	≥ 40fs	Figure 10	
1	0	2: 20bit, MSB justified	≥ 40fs	Figure 11	
1	1	3: I^2S Compatible	32fs or ≥ 40fs	Figure 12	

Table 15. Audio Data Interface Format

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
85H	Power Management	MINR	MINL	BF	MONO	MOUT	HPR	HPL	DAC
Default		0	0	0	0	0	0	0	0

DAC: Power management for DACL, DACR, DACM and PLL. When this bit changes from "0" to "1", DAC is powered-up to the current register values (ATT value, sampling rate, etc).
0: Power OFF (Default)
1: Power ON

HPL: Power management for Lch headphone amplifier.
0: Power OFF (Default). Output voltage becomes HPGND (0V).
1: Power ON

HPR: Power management for Rch headphone amplifier
0: Power OFF (Default). Output voltage becomes HPGND (0V).
1: Power ON

MOUT: Power management for monaural lineout
0: Power OFF (Default). Output voltage becomes Hi-z.
1: Power ON

MONO: Control of the signal output from DACL and DACR
0: Normal Output (Default)
1: (L+R)/2
In case of DAC bit = "0", MONO bit is not ignored.

When changing between Mono and Stereo modes, the headphone amplifiers should be powered-down. (HPL=HPR= "0").
When HPL/HPR bits are OFF ("0"), DAC and MOUT bits should also be OFF("0"). If HPL/HPR bits are changed to ON ("1") when DAC and MOUT are powered-up, the HP-AMP will remain off.

HPL bit	HPR bit	MONO bit	HPL pin	HPR pin	
0	0	0	HPGND	HPGND	Default
0	0	1	HPGND	HPGND	
0	1	0	HPGND	Normal output	
0	1	1	HPGND	(L+R)/2	
1	0	0	Normal output	HPGND	
1	0	1	(L+R)/2	HPGND	
1	1	0	Normal output	Normal output	
1	1	1	(L+R)/2	(L+R)/2	

Table 16. HPL/HPR pin Output Signal

BF: BICK Period setting at Master Mode. In slave mode, this bit is ignored.
0: 32fs (Default)
1: 64fs

MINL: The input signal from MIN pin is added to Lch of headphone amplifier.
0: OFF (Default)
1: ON

MINR: The input signal from MIN pin is added to Rch of headphone amplifier.
0: OFF (Default)
1: ON

*** When the paths of MINL and MINR are changed, outputs of HP-Amp and MOUT should be muted.**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
88H	Output Select 1	0	RINM	LINM	RIN	LIN	DACM	DACR	DACL
Default		0	0	0	0	0	0	0	0

DACL: Select an output path of DACL
0: OFF (Default)
1: ON

DACR: Select an output path of DACR
0: OFF (Default)
1: ON

DACM: Select an output path of DACM
0: OFF (Default)
1: ON

LIN: The input signal from LIN pin is added to Lch of headphone amplifier.
0: OFF (Default)
1: ON

RIN: The input signal from RIN pin is added to Rch of headphone amplifier.
0: OFF (Default)
1: ON

LINM: The input signal from LIN pin is added to MOUT amplifier.
0: OFF (Default)
1: ON

RINM: The input signal from RIN pin is added to MOUT amplifier.
0: OFF (Default)
1: ON

*** When these paths (DACL, DACR, DACM, LIN, RIN, LINM and RINM) are changed, outputs of HP-Amp and MOUT should be muted.**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
89H	HP-Amp Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
8BH	HP-Amp Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
8DH	MOUT ATT	ATTM7	ATTM6	ATTM5	ATTM4	ATTM3	ATTM2	ATTM1	ATTM0
Default		0	0	0	0	0	0	0	0

ATTR7-0: Setting of the attenuation value of output signal from DACR
ATTL7-0: Setting of the attenuation value of output signal from DACL
ATTM7-0: Setting of the attenuation value of output signal from DACM.

The internal calculation is attenuated by 10bit linear value, but the available ATT value is 8bit. Table 17 shows typical ATT values. The transition between ATT values uses the same mechanism as the soft mute operation. For example, if the current value is ATT1 and a new value is set as ATT2, ATT1 transitions to ATT2. The time that it takes for this transition to occur is set via the TM1-0 bits. If the new value (ATT3) is set before ATT1 reaches ATT2, the ATT value will transition directly to the ATT3 setting.

Equation of attenuation level:

FFH: **0dB**
FEH ~ 20H: **ATT = 20 x $\log_{10}$ ((Register Value x 4) – 60H) / 1023) [dB]**
1FH ~ 01H: **ATT = 20 x $\log_{10}$ ((Register Value) / 1023) [dB]**
00H: **MUTE**

DATA	ATT [dB]	DATA	ATT [dB]
FFH	0.0	25H	-25.877
FCH	-0.998	23H	-27.328
E3H	-2.006	22H	-28.156
CDH	-3.003	21H	-29.017
B9H	-4.020	20H	-30.095
A8H	-4.989	1DH	-30.950
98H	-6.012	1AH	-31.898
8AH	-7.018	16H	-32.963
7EH	-7.984	14H	-34.177
73H	-8.975	12H	-35.092
69H	-9.987	10H	-36.115
60H	-11.010	0EH	-37.275
58H	-12.033	0DH	-37.919
51H	-13.039	0BH	-39.370
4BH	-14.005	0AH	-40.198
45H	-15.092	09H	-41.113
41H	-15.901	08H	-42.136
3CH	-17.030	07H	-43.296
38H	-18.053	06H	-44.634
35H	-18.908	05H	-46.218
31H	-20.198	04H	-48.156
2FH	-20.922	03H	-50.655
2CH	-22.136	02H	-54.177
2AH	-23.051	01H	-60.198
28H	-24.074	00H	MUTE
26H	-25.234		

Table 17. Typical ATT values

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
8FH	Mode Control 2	0	0	0	0	0	0	0	EXT
Default		0	0	PS0	PS1	CKP	LRP	0	0

EXT: Master Clock Mode Select
0: PLL mode
1: EXT mode (External clock mode)

LRP: LRCK Polarity (enable at slave mode)
0: Normal
1: Invert

CKP: BICK Polarity (enable at slave mode)
0: Normal
1: Invert

PS1-0: MCKO Frequency
PLL mode: Table 3
EXT mode: Table 7

■ Soft Mute

Soft mute operation is performed in the digital domain. When LRMUTE or MMUTE bit go to "1", the output signal is attenuated by -∞ ("0") via the cycle set by TM1-0 bit (Table 12). When LRMUTE or MMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB via the cycle set of TM1-0 bits. LRMUTE and MMUTE bits operate independently. If the soft mute is cancelled within the cycle set by TM1-0 bits after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

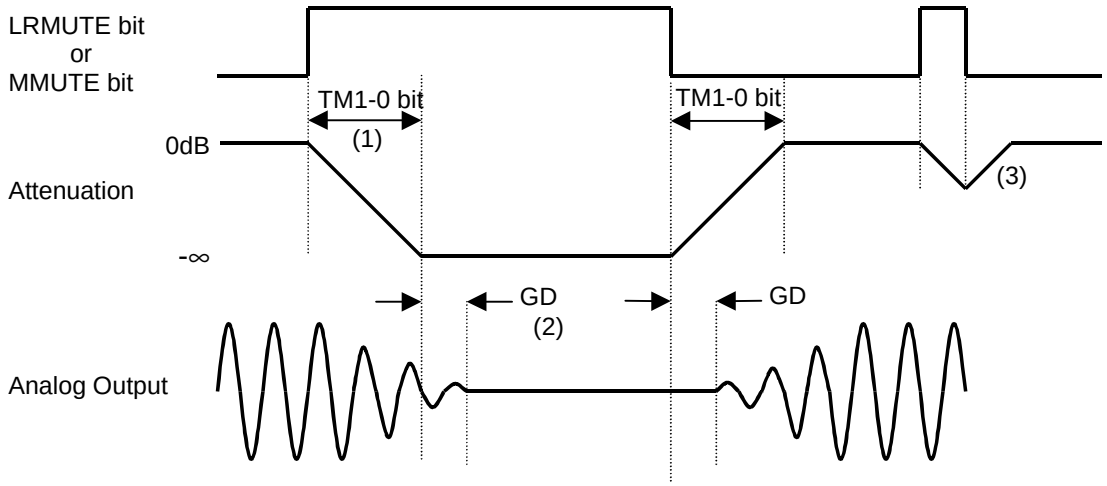


Figure 14. Soft Mute Function

NOTE:

(1) The output signal is attenuated until -∞ ("0") by the cycle set by TM1-0 bit
(2) Analog output corresponding to digital input have the group delay (GD).
(3) If the soft mute is cancelled within the cycle of setting TM1-0 bit, the attenuation is discontinued and returned to 0dB(the setting value).

■ De-emphasis Filter

The AK4365 includes a digital de-emphasis filter (tc = 50/15μs) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting FS2-0 and DEM bits.

■ Low Frequency Boost Function

By controlling BST1-0 bits, the low frequency boost signal can be output from DACL, DACR and DACM. The setting value is common in DACL, DACR and DACM.

Table 18 shows the relationship of external resistor, capacitor, fc(cut-off frequency) and output power, where load resistance of headphone is 16Ω.

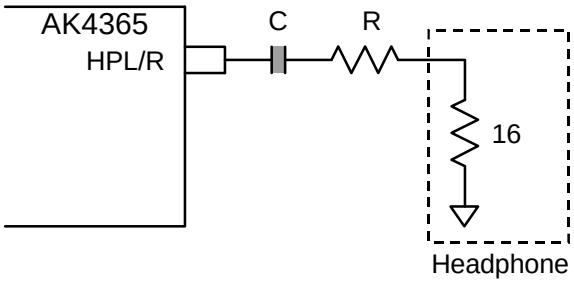


Figure 15. Headphone external circuit example

R[Ω]	C[μF]	Fc	Po	Figure
0Ω	220μF	45Hz	9.8mW	Figure 16
	100μF	100Hz		Figure 17
6.8Ω	100μF	70Hz	4.8mW	Figure 18
	47μF	149Hz		Figure 19
16Ω	100μF	50Hz	2.45mW	Figure 20
	47μF	106Hz		Figure 21

Table 18. Relationship of external circuit, output power and frequency response

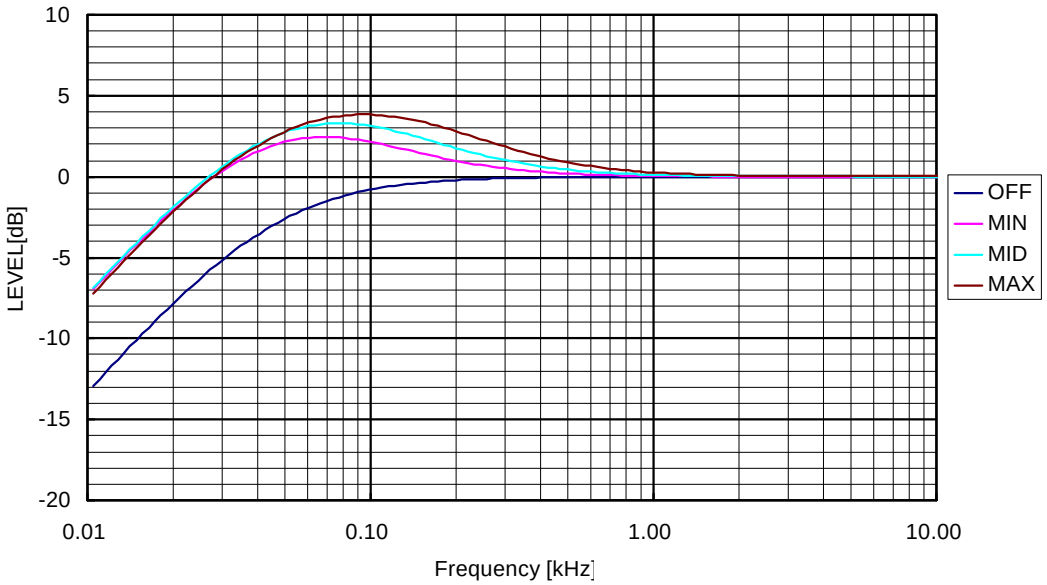


Figure 16. C=220µF, R = 0Ω, fs=44.1kHz

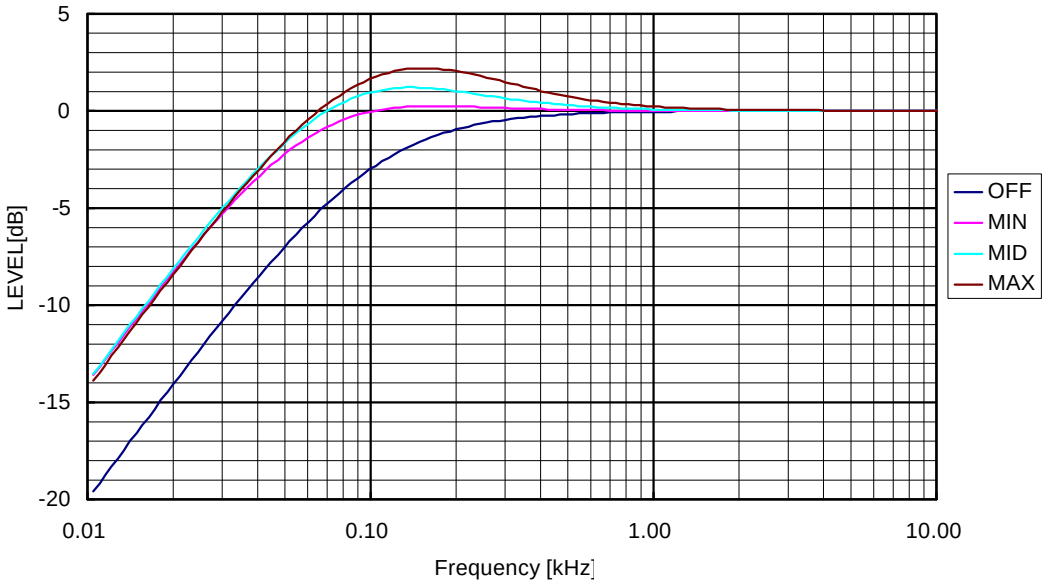


Figure 17. C=100µF, R = 0Ω, fs=44.1kHz

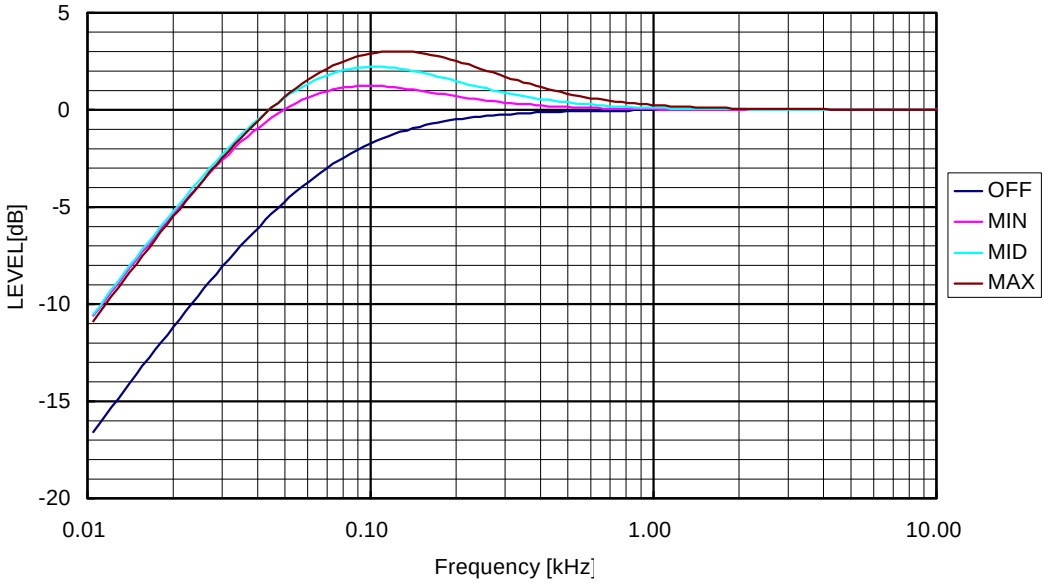


Figure 18. C=100µF, R = 6.8Ω, fs=44.1kHz

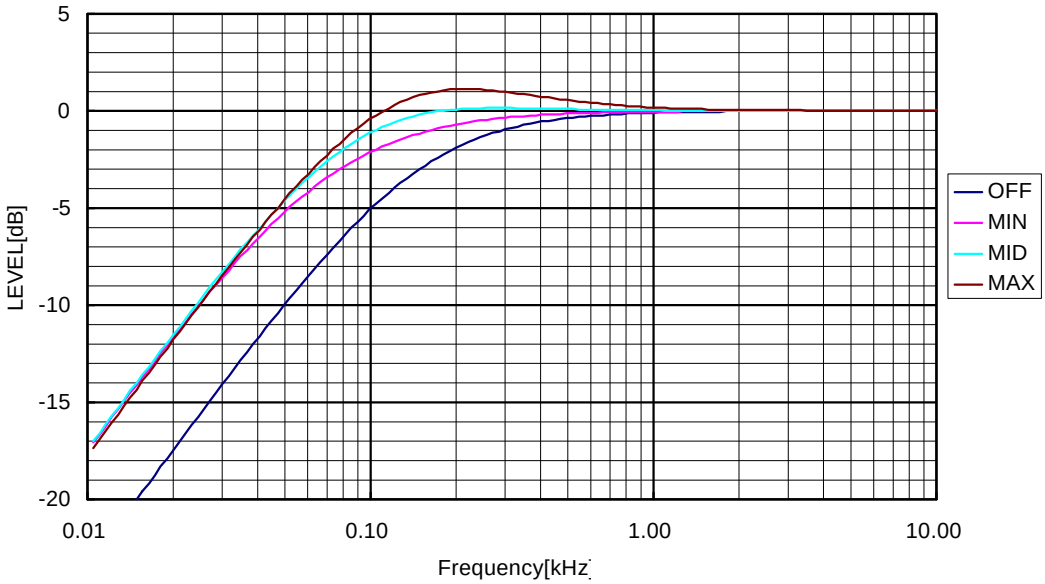


Figure 19. C=47µF, R = 6.8Ω, fs=44.1kHz

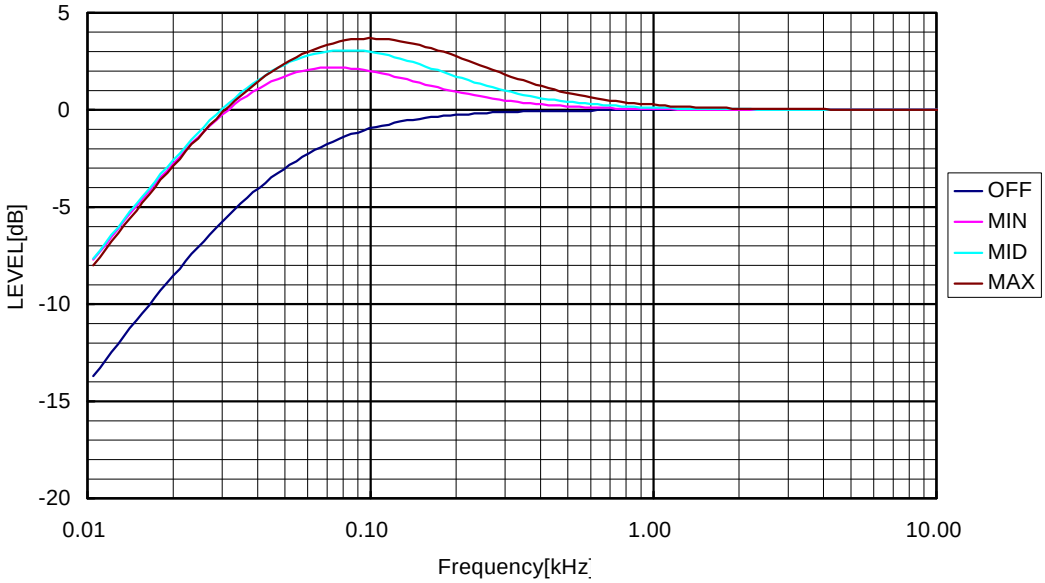


Figure 20. C=100µF, R = 16Ω, fs=44.1kHz

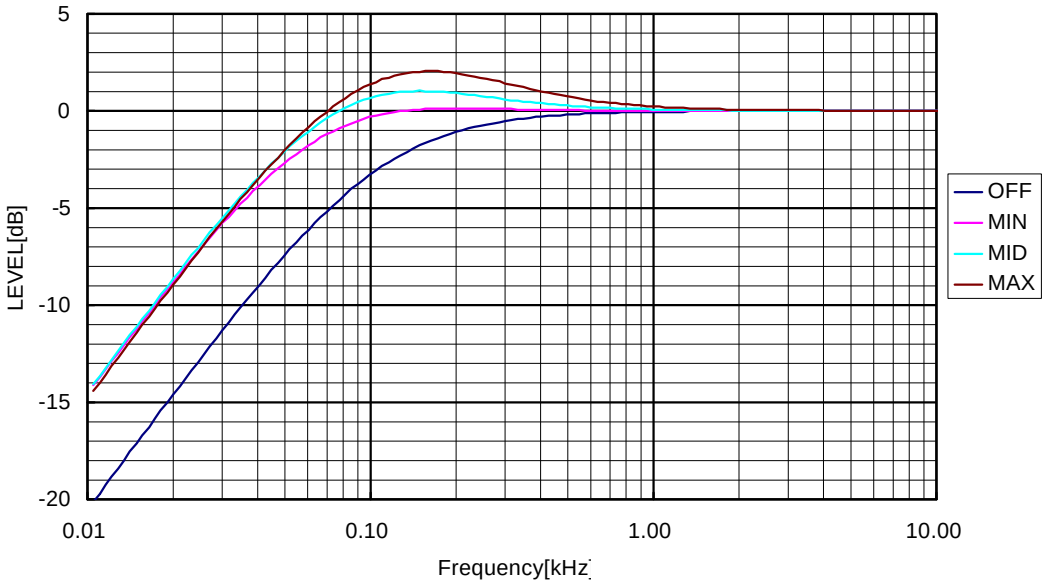


Figure 21. C=47µF, R = 16Ω, fs=44.1kHz

■ Polarity and gain of Line Input/Output

The input signal from LIN, RIN and MIN pins are gained to +6dB by headphone amplifier. The input signal from LIN, RIN and MIN pins are inverted by headphone amplifier. The output signal from DAC is a non-inverted signal.

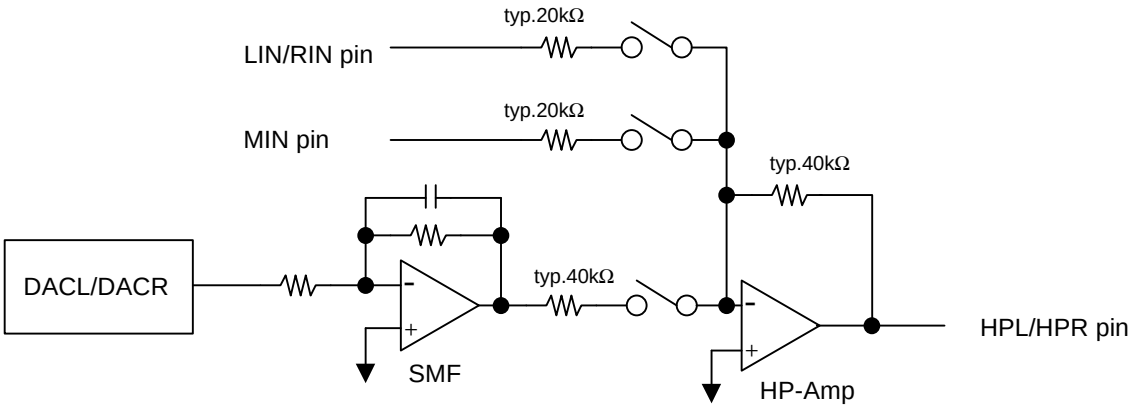


Figure 22. Internal equivalent circuit between DACL/DACR and HPL/HPR

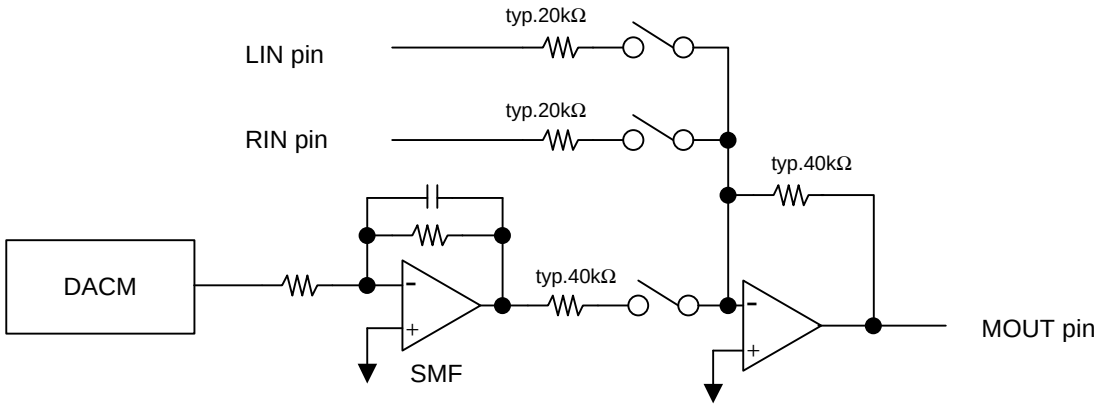


Figure 23. Internal equivalent circuit between DACM and MOUT

■ System Reset

The AK4365 should be reset once by bringing RSTN “L” upon power-up. After exiting reset, DAC, HPL, HPR and MOUT switch to the power-down state. The contents of the control register are maintained until the reset is done.

■ Power ON/OFF Sequence

1) In case of DAC output (Full-scale output) to HPL, HPR and MOUT pins (LIN, RIN and MIN: No input)

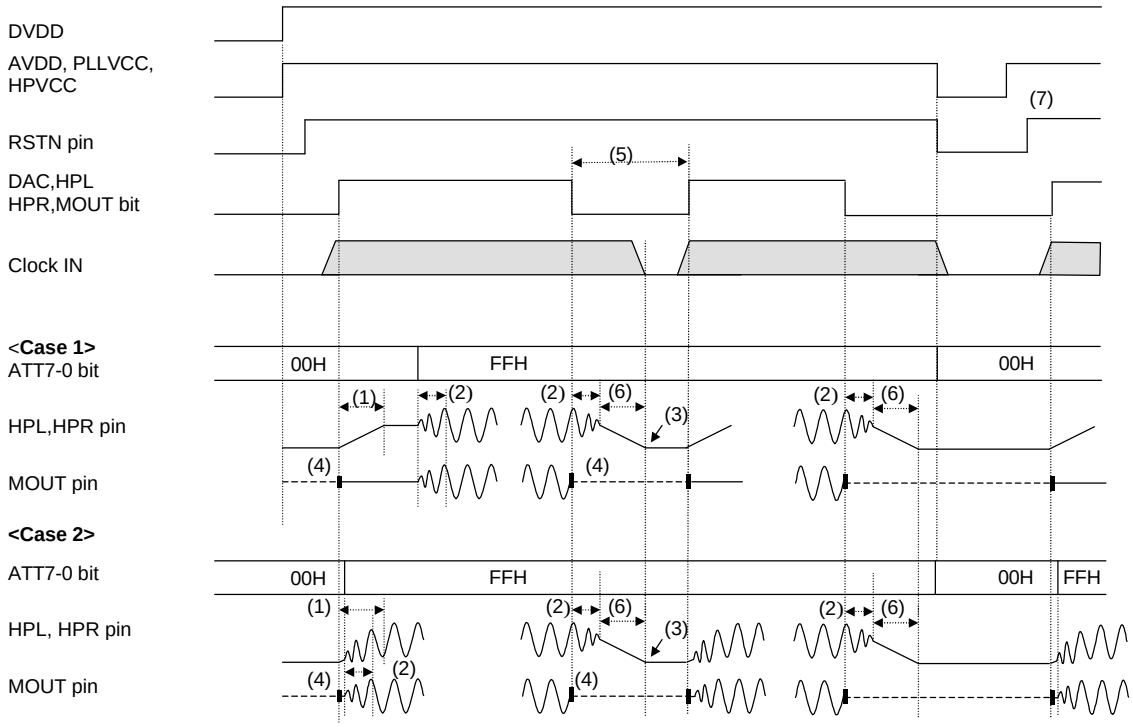


Figure 24. Power ON/OFF Sequence (1)

(1) Rise time of HP-Amp can be set by a capacitor connected to the MUTET pin. Rise time to 80% is 150ms(min), 300ms(typ) and 600ms(max) when the capacitor is 1µF, and 70ms(min), 140ms(typ) and 290ms(max) when 0.47µF. In case of 0.47µF, pop noise may be bigger.
(2) ATT7-0 bits are set to 00H on reset. When TM1-0 bits are "00", the attenuated signal is released by the cycle set by TM1-0 bits after ATT7-0 bits are set to FFH. (Same as soft mute)
(3) When HPL and HPR go to HPGND, the power supplies to DAC and HP-Amp are powered-down.
(4) When DAC and MOUT bits change to "1" or "0", click noise occurs from MOUT pin.
When MOUT bit is "0", output of MOUT becomes Hi-Z.
(5) After DAC, HPL, HPR and MOUT are powered-down once, it is necessary to wait this amount of time before they are powered-up again. (Time required prior to writing to DAC, HPL, HPR and MOUT bits.) **If HPL and HPR bits are changed to "1" within this time, HP-Amp may not be powered-up.** The time in which HP-Amp is not powered-up (this partial time is included in the time above) depends on a capacitor connected to the VCOM pin (C_2), 0.8k x C_2 (max).
(6) Fall time of HP-Amp can be set by a capacitor connected to the MUTET pin. Fall time to 0V is 200ms(min), 400ms(typ) and 860ms(max) when the capacitor is 1µF, and 90ms(min), 190ms(typ) and 410ms(max) when 0.47µF. In case of 0.47µF, pop noise may be bigger.
(7) If only AVDD, PLLVCC and HPVCC are powered ON/OFF when DVDD is powered ON, the RSTN pin should be changed from "L" to "H" after AVDD, PLLVCC and HPVCC are powered ON.

The time required prior to writing to DAC, HPL, HPR and MOUT bits(5) = Time(1) + Soft Mute Time(2)

For example,

MUTET pin = 1µF, VCOM pin = 1µF, fs = 44.1kHz, Soft mute time setting = 1024/fs (TM1-0 = "00")
Time (1): max. 860ms
Time (2): max. 23.2ms = 1024/fs + 1/fs @ fs=44.1kHz
Time (5): 883.2ms = 860ms + 23.2ms

For the example above, wait about 883.2ms before writing to DAC, HPL, HPR or MOUT bit.

*** If it is necessary to shorten the MUTE sequence time, an external mute circuit should be implemented. An example of an external mute circuit is shown in the AK4365 evaluation board manual. The external mute circuit should be released after the HP-Amp is powered up. If the external mute is released on the way of HP-Amp power-up, large pop noise will occur.**

*** Power supply AVDD is powered-up at the same time or earlier than power supply HPVCC. Power supply AVDD is powered-down at the same time or later than power supply HPVCC.**

2) In case of output from LIN, RIN and MIN pins (Full-scale output) to HPL, HPR and MOUT pins (DAC Power OFF)

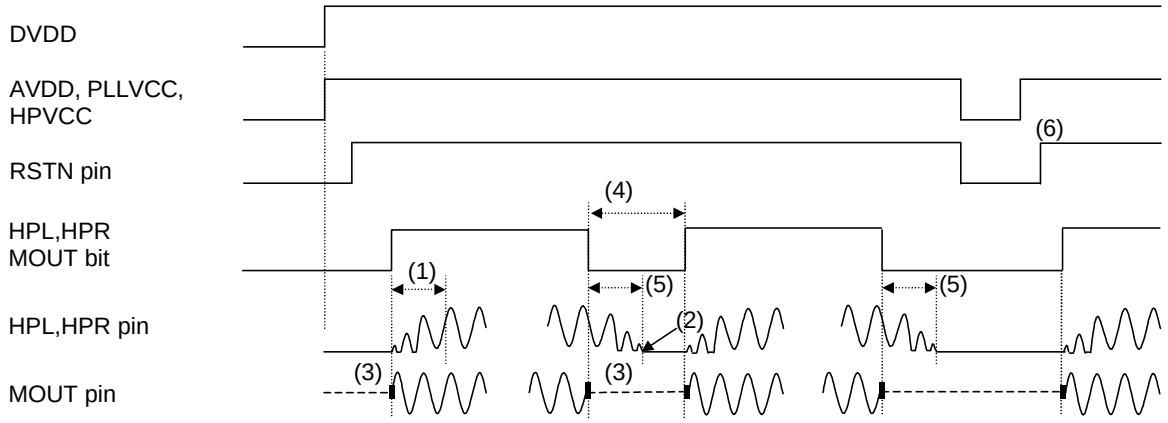


Figure 25. Power ON/OFF Sequence (2)

(1) Rise time of HP-Amp can be set by a capacitor connected to the MUTET pin. Rise time to 80% is 150ms(min), 300ms(typ) and 600ms(max) when the capacitor is 1µF, and 70ms(min), 140ms(typ) and 290ms(max) when 0.47µF. In case of 0.47µF, pop noise may be bigger. To rise common voltage, lower side of output signal is clipped.
(2) When HPL and HPR go to HPGND, the power supply of HP-Amp is powered-down.
(3) MOUT bit changes to "1" or "0", click noise occurs from MOUT pin.
When MOUT bit is "0", output of MOUT becomes Hi-Z.
(4) After DAC, HPL, HPR and MOUT are powered-down once, it is necessary to wait this amount of time before they are powered-up once again. (Time required prior to writing to DAC, HPL, HPR and MOUT bits.) **If HPL and HPR bits are changed to "1" within this time, HP-Amp may not be powered-up.** The time in which HP-Amp is not powered-up (this partial time is included in the time above) depends on a capacitor connected to the VCOM pin (C_2), 0.8k x C_2 (max).
(5) Fall time of HP-Amp can be set by a capacitor connected to the MUTET pin. Fall time to 0V is 200ms(min), 400ms(typ) and 860ms(max) when the capacitor is 1µF, and 90ms(min), 190ms(typ) and 410ms(max) when 0.47µF. In case of 0.47µF, pop noise may be bigger. To fall common voltage, lower side of output signal is clipped.
(6) If only AVDD, PLLVCC and HPVCC are powered ON/OFF when DVDD is powered ON, the RSTN pin should be changed from "L" to "H" after AVDD, PLLVCC and HPVCC are powered ON.

The time required prior to writing to DAC, HPL, HPR and MOUT bits (4) = Time (1)

For example,
MUTET pin = 1µF, VCOM pin = 10µF

Time (1): max. 860ms
Time (4) = Time (1) = 860ms

For the example above, wait about 860ms writing to DAC, HPL, HPR or MOUT bit.

*** If it is necessary to shorten the MUTE sequence time, an external mute circuit should be implemented. An example of an external mute circuit is shown in the AK4365 evaluation board manual. The external mute circuit should be released after the HP-Amp is powered up. If the external mute is released on the way of HP-Amp power-up, large pop noise will occur.**

*** Power supply of AVDD is powered-up at the same time or earlier than power supply of HPVCC. Power supply of AVDD is powered-down at the same time or later than power supply of HPVCC.**

SYSTEM DESIGN

Figure 26 shows the system connection diagram. An evaluation board [AKD4365] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

Capacitance values of VCOC pin

PLL Frequency: 19.8MHz, 19.68MHz, 19.2MHz, 15.36MHz, 14.4MHz, 12MHz, 11.2896MHz → C = 4.7nF

PLL Frequency: 13MHz →C = 470nF

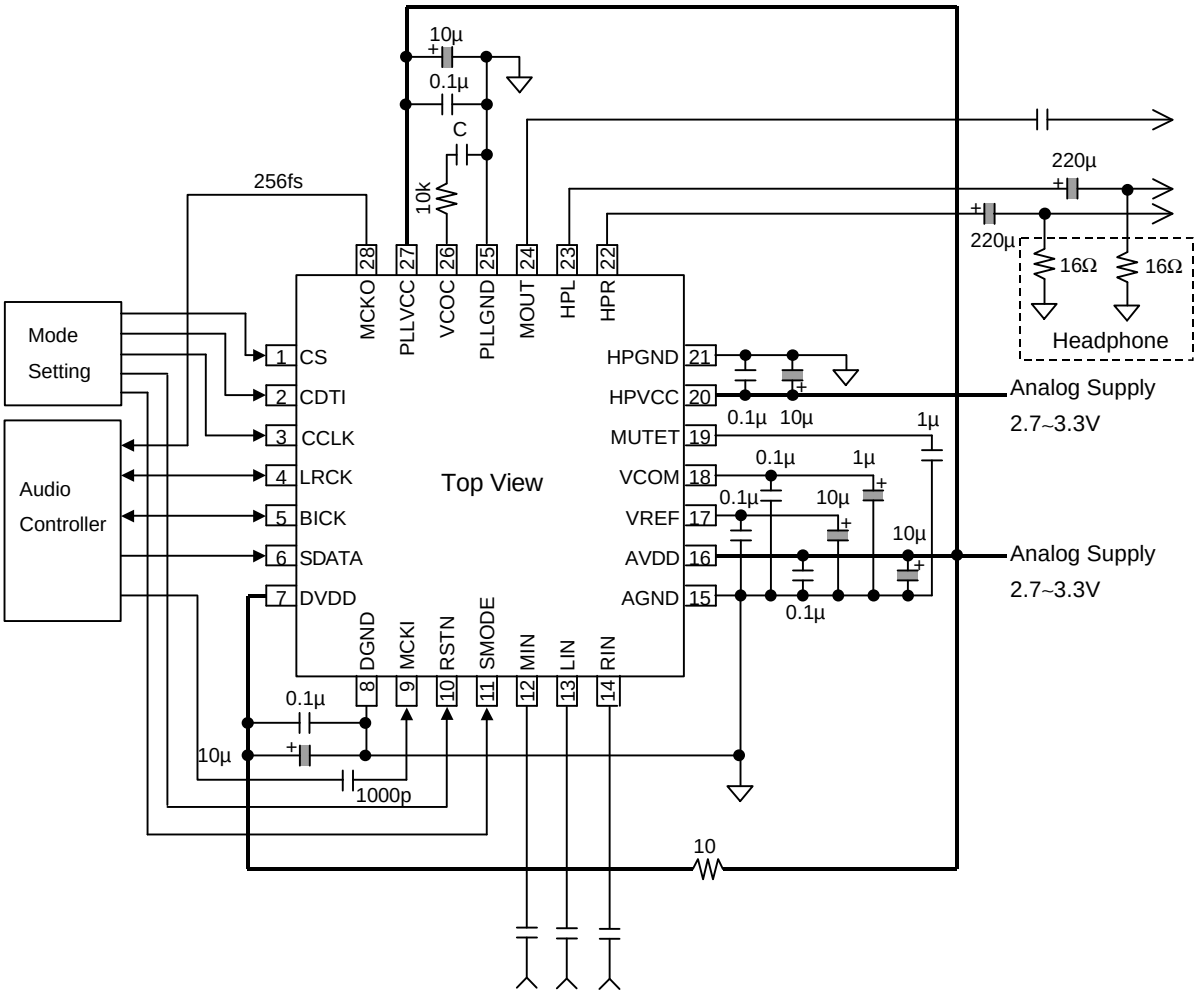


Figure 26. Typical Connection Diagram (In case of AC coupling to MCKI)

Note: The headphone amplifier output for the AK4365 may oscillate. This oscillation is caused by the load of a headphone cable. The following external circuit 1) or 2) should be used to avoid this oscillation.

1) Resistor (≥6.8Ω) in series. In this case, the voltage at the headphone will be attenuated by resistor divider.

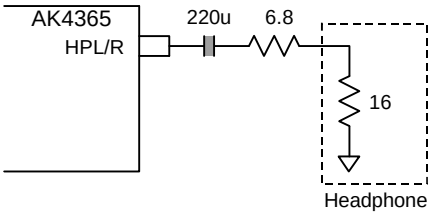


Figure 27. Headphone amp external circuit example 1

2) Capacitor (0.1μF±20%) and resistor (10Ω±20%) in series to ground.

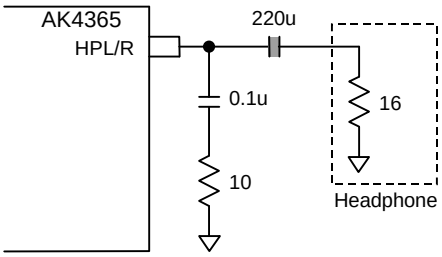


Figure 28. Headphone amp external circuit example 2

1. Grounding and Power Supply Coupling

The AK4365 requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the analog power supply in the system and DVDD is supplied from AVDD via a 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. When AVDD and HPVCC are supplied separately, AVDD is powered-up at the same time or earlier than HPVCC. When the AK4365 is powered-down, HPVCC is powered-down at the same time or later than AVDD. The power up sequence of PLLVCC is not critical. AGND, DGND, PLLGND and HPGND must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4365 as possible, with the small value ceramic capacitors being the nearest.

2. Internal Voltage Reference

Internal voltage reference is output on the VREF pin (typ. 2.0V). An electrolytic capacitor 10μF in parallel with a 0.1μF ceramic capacitor is attached between VREF and AGND to eliminate the effects of high frequency noise. VCOM is 1.0V(typ) and is a signal ground of this chip. A 1μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor should be connected between VCOM and AGND to eliminate the effects of high frequency noise. A ceramic capacitor should be connected to VCOM pin and located as close as possible to the AK4365. No load current may be drawn from VREF and VCOM pins. All signals, especially clocks, should be kept away from the VCOM and VREF pins in order to avoid unwanted coupling into the AK4365.

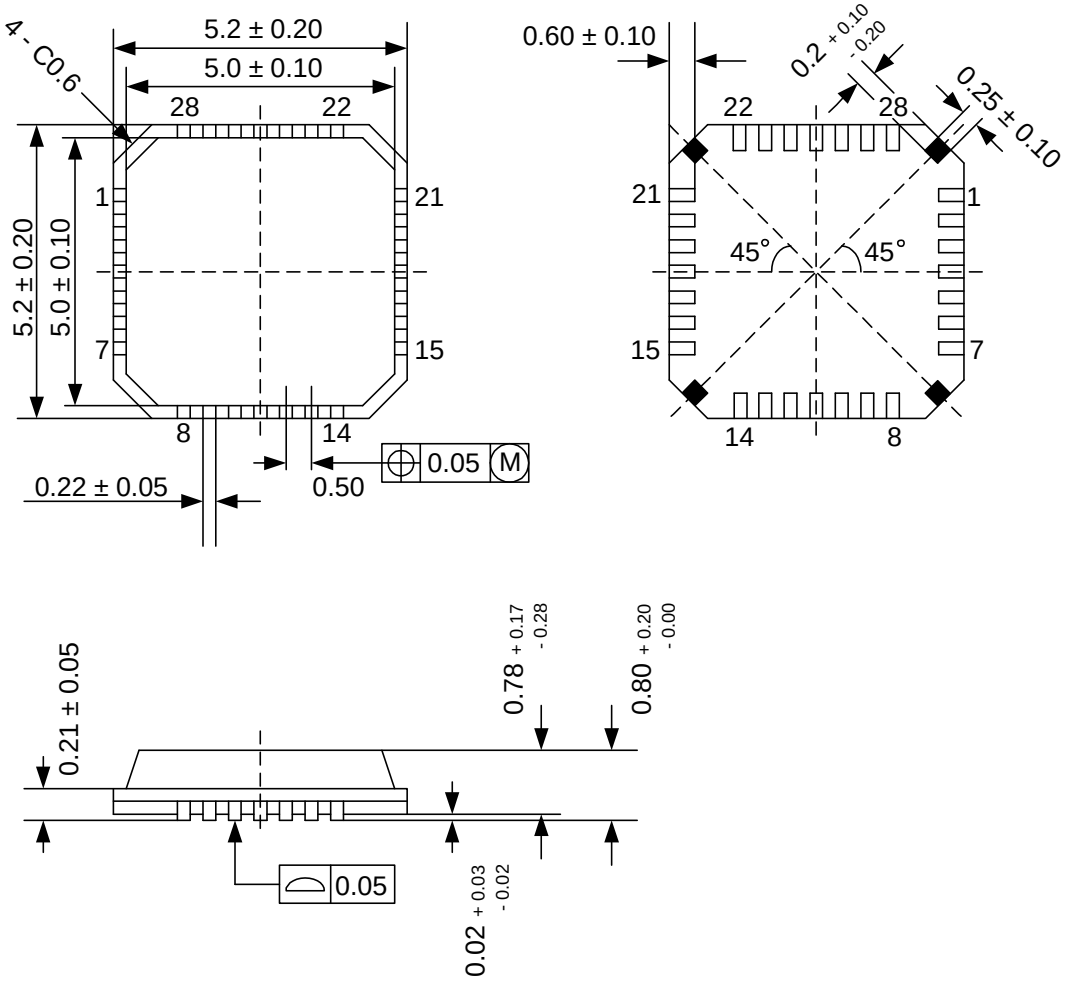
3. Analog Outputs

The analog outputs are single-ended outputs and 1.12Vpp(typ) centered around the VCOM voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFF(@20bit) and negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). If the noise generated by the delta-sigma modulator beyond the audio band causes problems, attenuation by an external filter is required.

DC offsets on the analog outputs is eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

● 28pin QFN (Unit: mm)

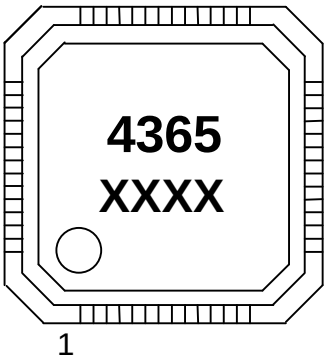


Note: The black parts of back package should be open.

■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXX : Date code identifier (4 digits)

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