AK4368
PLL & HP-AMP ″ DAC

A

AK4368 xPLL & ¿ ¯ ¥ ″ `h 24bit D/A fl »pb{ PLL x 3?Øw7 s ¯«Ø¿«t0 ` b{ hz ˇØ‹ '‡ ‹sˇ ″ `oS bwpz 3?Ø wf ^ ƒ I/F qw D pb{ AK4368 x3D Stereo Enhancement sˇ ″ ` b{ ¿¯ ¥ x 16 p50mW Z b \qUD pz?o ON/OFF z Æ ˜ w ¿ ° ¶xK d {˝¿› ·x w 41pin BGA >;`oS z » ;Mtx7&pb{

- ☐ ‰ˇ¿˜ ΔΣM **DAC**
- ☐ – ‹Ł ˜
  - **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz**
- ☐ **8 FIR** ^ ·» »″
  - Ła‹ **: 20kHz**
  - Ła‹ ¿ **: ±0.02dB**
  - ″ ›‹n0 **: 54dB**
- ☐ ^ ·» ^ ⁄ ‡ ″ **: 32kHz, 44.1kHz, 48kHz**
- ☐ **PLL:**
  - * **: : 27MHz, 26MHz, 19.8MHz, 19.68MHz, 19.2MHz, 15.36MHz, 14.4MHz, 13MHz, 12MHz, 11.2896MHz**
  - Ł **AC** Ş¿ D
- ☐ ƒ ^ ƒ **I/F** ¥ ¿˜ **: MSB First, 2's Compliment**
  - **I²S, 24bit** †g **, 24bit/20bit/16bit** g
  - » ¯ Ł ¯0
- ☐ '‡ ‹; **: LR, LL, RR, (L+R)/2**
- ☐ ^ ·» **ALC**
- ☐ ^ ·» Æ
- ☐ ˇØ‹ '‡ ‹sˇ
- ☐ **3D Stereo Enhancement**
- ☐ ´Łƒ Z
- ☐ fl » £ **: 3 ¢ /I²C**
- ☐ ˜″
- ☐ ¿¯ ¥ ″
  - ¤Z **: 50mW x 2ch @16Ω, 3.3V**
  - **S/N: 92dB@3.3V**
  - ?o **ON/OFF** S | Æ ˜ ¿ ° ¶
- ☐ ?o?y **: 1.6V ~ 3.6V**
- ☐ « ?v **: 4.0mA @2.4V (HP-AMP `Z)**
- ☐ **Ta: –30 ~ 85°C**
- ☐ ″¿› · **: 41pin BGA (4mm x 4mm, 0.5mm pitch)**

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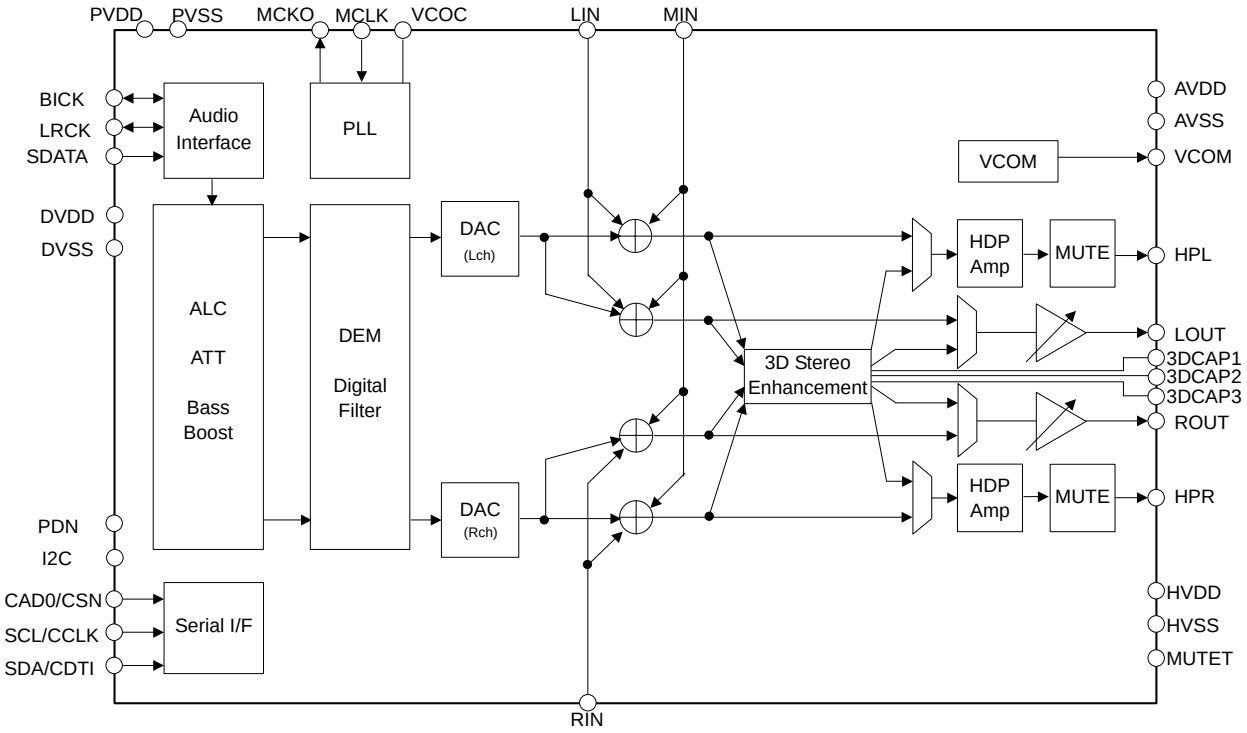

Figure 1. Ø ¿ « $

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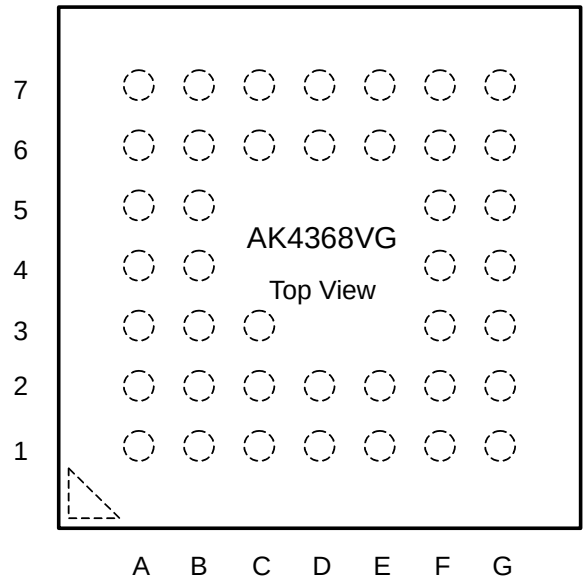
■ ƒ … ‹ ¤ -

AK4368VG	–30 ~ +85°C	41pin BGA (0.5mm pitch)
AKD4368	AK4368 ; A -	

■ –



7	NC	HPR	HVDD	AVDD	VCOM	LOUT	NC
6	HPL	HVSS	AVSS	MUTET	ROUT	3DCAP2	3DCAP3
5	MIN	NC	Top View			NC	3DCAP1
4	RIN	NC				PDN	NC
3	VCOC	LIN	NC			NC	CAD0/ CSN
2	PVDD	PVSS	DVSS	I2C	LRCK	SDATA	SCL/ CCLK
1	NC	MCKO	DVDD	MCKI	BICK	SDA/ CDTI	NC
	A	B	C	D	E	F	G

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■ **AK4365, AK4367 q w z – fl**

Ł	AK4365	AK4367	AK4368
PLL * :	19.8/19.68/19.2/15.36/ 14.4/13/12/11.2896MHz	N/A	27/26/19.8/19.68/19.2/ 15.36/14.4/13/12/11.2896 MHz
PLL 0 – ‹ * :	8/11.025/16/22.05/24/32/ 44.1/48kHz	N/A	8/11.025/12/16/22.05/24/ 32/44.1/48kHz
ƒ ^ ƒ I/F ¥ ¿ ~	20bit g 16/20bit † g I^2S	24bit g 16/20/24bit † g I^2S	←
» ¯	Available	N/A	Available
ALC	N/A	N/A	Available
3D Stereo Enhancement	N/A	N/A	Available
Z	Mono	Mono	Stereo
fl » £	3-wire	3-wire/I^2C	←
~	+6dB	+16dB	←
' ‡ ‹	(L+R)/2	(L+R)/2	LL, RR, (L+R)/2
¿ ¯ ¥ Z	10mW	50mW	50mW
? ○ ? y	2.7 ~ 3.3V	2.2 ~ 3.6V	1.6 ~ 3.6V
˝ ¿ › ·	28QFN(5.2mm x 5.2mm)	20QFN(4.2mm x 4.2mm)	41BGA(4mm x 4mm)

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– ;

No.	– ° ¶	I/O	;
B1	MCKO	O	» « Ø ¿ « Z –
C2	DVSS	-	^ · » ‹ ¯ –
C1	DVDD	-	^ · » ? o –
D2	I2C	I	fl ~ Ø ¯ ‹ R – "H": I²C , "L": 3 ¢ ‡
D1	MCKI	I	» « Ø ¿ « –
E2	LRCK	I/O	L/R « Ø ¿ « – ƒ ^ ƒ ^ » w ‰ > ' b {
E1	BICK	I/O	‡ ˇ ¿ ~ « Ø ¿ « – ƒ ^ ƒ ^ » ‡ ~ b h w « Ø ¿ « p b {
F2	SDATA	I	ƒ ^ ƒ ^ » –
F1	SDA	I/O	fl ~ Ø ^ » Z – (I2C pin = "H")
	CDTI	I	fl ~ Ø ^ » – (I2C pin = "L")
G2	SCL	I	fl ~ Ø « Ø ¿ « – (I2C pin = "H")
	CCLK	I	fl ~ Ø « Ø ¿ « – (I2C pin = "L")
G3	CAD0	I	‰ ¿ ¯ Ł 0 – (I2C pin = "H")
	CSN	I	fl ~ Ø ^ » ‰ ¿ • Ł « ~ – (I2C pin = "L")
F4	PDN	I	″ ° … ¢ & • ¿ ~ – \ w – "L" t b q ″ x ″ ° … ¢ ^ z • ¿ ~ 6 t s b { ? o q j ″ [t S "L" ' o < ^ M {
G5	3DCAP1	O	3D Stereo Enhancement ; fl ^ – 1 – 3DCAP2 pin q w t 4.7nF w fl ^ – » t ' o X i ^ M {
F6	3DCAP2	O	3D Stereo Enhancement ; fl ^ – 2 – 3DCAP1 pin q w t 4.7nF w fl ^ – » t z 3DCAP3 pin q w t 470nF w fl ^ – » t ' o < ^ M {
G6	3DCAP3	O	3D Stereo Enhancement ; fl ^ – 3 – 3DCAP3 pin q w t 470nF w fl ^ – » t ' o < ^ M {
F7	LOUT	O	Lch ˇ Ø ‹ Z –
E6	ROUT	O	Rch ˇ Ø ‹ Z –
E7	VCOM	O	fl ? y – AVSS pin q w t 2.2µF w ? r fl ^ – ' b {
D7	AVDD	-	ˇ Ø ‹ ? o –
C6	AVSS	-	ˇ Ø ‹ ‹ ¯ –
D6	MUTET	O	Æ ~ : fl ~ Ø – HVSS pin q w t : ; fl ^ – ' b {
C7	HVDD	-	¿ ¯ ¥ ; ? o –
B6	HVSS	-	¿ ¯ ¥ ; ‹ ¯ –
B7	HPR	O	Rch HP-Amp Z –
A6	HPL	O	Lch HP-Amp Z –
A5	MIN	I	° ˇ Ø ‹ –
A4	RIN	I	Rch ˇ Ø ‹ –
B3	LIN	I	Lch ˇ Ø ‹ –
A3	VCOC	O	PLL s ˇ w » Z – PVSS q w t ¯ q fl ^ – » t ' o < ^ M {
B2	PVSS	-	PLL ; ‹ ¯ – { AVSS q ' o < ^ M {
A2	PVDD	-	PLL ; ? o – { AVDD q ' o < ^ M {

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No.	— °¶	I/O	;
A1 A7 B4 B5 C3 F3 F5 G1 G4 G7	NC	-	No Connect Pin No internal bonding. These pins should be connected to ground

Note: ^ ·» — (I2C, SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN) xf t'sMp<^M{

Note: MCKI pin xz PDN pin = "L" w f D pb{

■ ;'sM— wrgtmMo

;'sM Z — x<Gw Mz&~trg'o<^M{

	— °	
Analog	LOUT, ROUT, MUTET, HPR, HPL, MIN, RIN, LIN	f
Digital	CAD0	DVSS t
	MCKO	f

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0 7 G ¤

(AVSS, DVSS, HVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	PLL	PVDD	–0.3	4.6	V
	HP-Amp	HVDD	–0.3	4.6	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – HVSS| (Note 2)	ΔGND2	-	0.3	V
	|AVSS – PVSS| (Note 2)	ΔGND3	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	–0.3	AVDD+0.3 or 4.6	V
Digital Input Voltage (Note 4)		VIND	–0.3	DVDD+0.3 or 4.6	V
Ambient Temperature		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. ? y x b o‹ ¯— t 0 b p b {

Note 2. AVSS, DVSS, HVSS qPVSS x ˜ Ø‹ ‹ ¯t ' o < ^ M {

Note 3. MIN, LIN, RIN pins.

Note 4. SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCLK, PDN, I2C pins.

« : \ w Q h E p ; ' h ø z ^ u b \ q U K b { h Ł w ^ x – ´ ^
d {

* ^ E

(AVSS, DVSS, HVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	typ	Max	Units
Power Supplies	Analog	AVDD	1.6	2.4	3.6	V
	Digital	DVDD	1.6	2.4	AVDD	V
	PLL	PVDD	1.6	2.4	3.6	V
	HP-Amp	HVDD	1.6	2.4	3.6	V
	Difference1	AVDD–PVDD	–0.3	0	+0.3	V
	Difference2	AVDD–HVDD	–0.3	0	+0.3	V

Note 1. ? y x b o‹ ¯— t 0 b p b {

« : ^ »‡ ˜ t G L ^ o M E w] ; t ' o x z p p x y M T v b w p G]
« < ^ M {

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˘Ø‹ Q

(GsV øx Ta=25°C; AVDD=PVDD=DVDD=HVDD=2.4V, AVSS=PVSS=DVSS=HVSS=0V; fs=44.1kHz; EXT mode; BOOST OFF; Slave Mode; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; Headphone-Amp: R_L =16Ω, C_L=220μF » 'h ø (Figure 45))

Parameter			min	typ	Max	Units
DAC Resolution			-	-	24	bit
Headphone-Amp: (HPL/HPR pins) (Note 5)						
Analog Output Characteristics						
THD+N		–3dBFS Output, 2.4V, Po=10mW@16Ω	-	–50	–40	dB
		–4.8dBFS Output, 3.3V, Po=50mW@16Ω HPG bit= "1"	-	–20	-	dB
D-Range		–60dBFS Output, A-weighted, 2.4V	82	90	-	dB
		–60dBFS Output, A-weighted, 3.3V	-	92	-	dB
S/N		A-weighted, 2.4V	82	90	-	dB
		A-weighted, 3.3V	-	92	-	dB
Interchannel Isolation			60	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.3	0.5	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 6)			16	-	-	Ω
Load Capacitance			-	-	300	pF
Output Voltage		–3dBFS Output (Note 7)	1.01	1.13	1.25	Vpp
		–4.8dBFS Output, 3.3V, Po=50mW@16Ω HPG bit= "1"	-	0.89	-	Vrms
Stereo Line Output: (LOUT/ROUT pins, R_L=10kΩ) (Note 8)						
Analog Output Characteristics:						
THD+N		0dBFS Output	-	–60	–50	dB
S/N		A-weighted	80	87	-	dB
DC Accuracy						
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 6)			10	-	-	kΩ
Load Capacitance			-	-	25	pF
Output Voltage		0dBFS Output (Note 9)	1.32	1.47	1.61	Vpp
Output Volume: (LOUT/ROUT pins)						
Step Size			1	2	3	dB
Gain Control Range			–30	-	0	dB

Note 5. DACHL=DACHR bits = "1", MINHL=MINHR=LINHL=RINHR bits = "0" w pb{

Note 6. AC Y{

Note 7. Z ?yx AVDD tz« ' b{ Vout = 0.47 x AVDD(typ)@–3dBFS.

Note 8. DACL=DACR bits = "1", MINL=MINR=LINL=RINR bits = "0" w w pb{

Note 9. Z ?yx AVDD tz« ' b{ Vout = 0.61 x AVDD(typ)@0dBFS.

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Parameter	min	typ	max	Units
LINEIN: (LIN/RIN/MIN pins)				
Analog Input Characteristics				
Input Resistance (Figure 23, Figure 24)				
LIN pin				
LINHL bit = “1”, LINL bit = “1”	35	50	-	kΩ
LINHL bit = “1”, LINL bit = “0”	-	100	-	kΩ
LINHL bit = “0”, LINL bit = “1”	-	100	-	kΩ
RIN pin				
RINHR bit = “1”, RINR bit = “1”	35	50	-	kΩ
RINHR bit = “1”, RINR bit = “0”	-	100	-	kΩ
RINHR bit = “0”, RINR bit = “1”	-	100	-	kΩ
MIN pin				
MINHL=MINHR=MINL=MINR bits = “1”	17	25	-	kΩ
MINHL bit = “1”, MINHR=MINL=MINR bits = “0”	-	100	-	kΩ
MINHR bit = “1”, MINHL=MINL=MINR bits = “0”	-	100	-	kΩ
MINL bit = “1”, MINHL=MINHR=MINR bits = “0”	-	100	-	kΩ
MINR bit = “1”, MINHL=MINHR=MINL bits = “0”	-	100	-	kΩ
Gain				
LIN/MIN→LOUT, RIN/MIN→ROUT	–1	0	+1	dB
LIN/MIN→HPL, RIN/MIN→HPR	–0.24	+0.76	+1.76	dB
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = “H”) (Note 10)				
AVDD+PVDD+DVDD	-	3.8	5.5	mA
HVDD	-	1.2	2.5	mA
Power-Down Mode (PDN pin = “L”) (Note 11)	-	1	100	μA

Note 10. PMDAC=PMHPL=PMHPR=PMLO bits = “1”, MUTEN bit = “1”, MCKO bit = “0”, HP-Amp ` Z {
PMDAC=PMHPL=PMHPR= “1”,PMLO bit= “0” , AVDD+PVDD+DVDD+HVDD= 4.0mA.

Note 11. i › z « Ø ¿ « (MCKI, BICK, LRCK) b o w ^ · » — x DVSS t { ' h ø
w p b {

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» Q

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=1.6 ~ 3.6V; fs=44.1kHz; De-emphasis = “OFF”)

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 12)							
Passband (Note 13)		–0.05dB	PB	0	-	20.0	kHz
		–6.0dB		-	22.05	-	kHz
Stopband (Note 13)			SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay (Note 14)			GD	-	22	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	µs
DAC Digital Filter + Analog Filter: (Note 12) (Note 15)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
Analog Filter: (Note 16)							
Frequency Response	0 ~ 20.0kHz		FR	-	±1.0	-	dB
BOOST Filter: (Note 15) (Note 17)							
Frequency Response		20Hz	FR	-	5.76	-	dB
	MIN	100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
		20Hz	FR	-	10.80	-	dB
	MID	100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
		20Hz	FR	-	16.06	-	dB
	MAX	100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 12. BOOST OFF (BST1-0 bit = “00”)

Note 13. Ł a ‹ z ˝ › ‹ w * : x fs (‡ ´ – ‹ Ł ˜) t z « ` b {
« Q y z PB=0.4535fs(@–0.05dB) z SB=0.546fs(@–54dB) p b {

Note 14. ^ · » » t p z ^ » U Ł · » t • ¿ ˜ ^ o T ˘ Ø ‹ Ł U
Z ^ p w p b {

Note 15. DAC → HPL, HPR, LOUT, ROUT p w Q

Note 16. MIN → HPL/HPR/LOUT/ROUT, LIN → HPL/LOUT, RIN → HPR/ROUT p w Q {

Note 17. * : Q x fs t z « ` b { › t x z ‹ p « ¿ ` b {

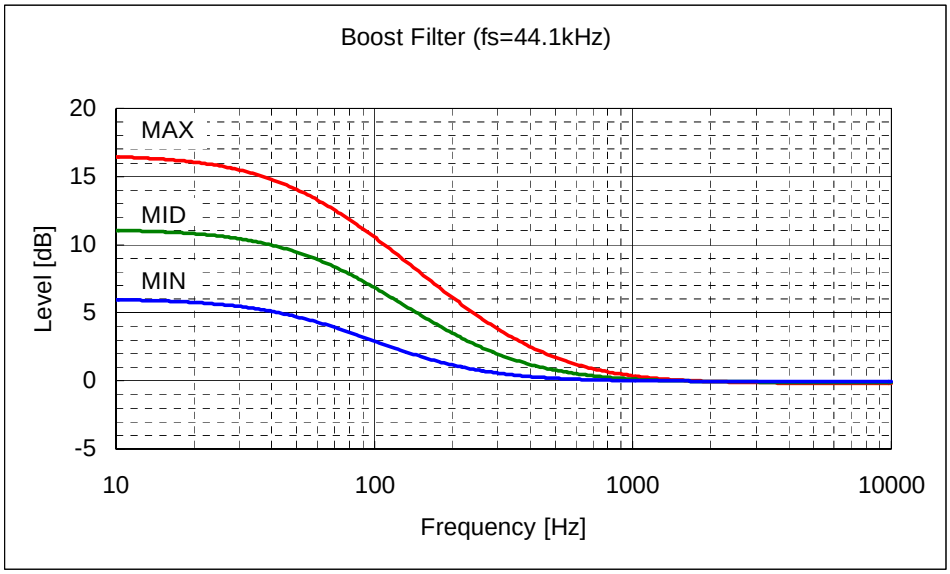

Figure 2. Boost Frequency (fs=44.1kHz)

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DC Q

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 18)		VAC	0.4	-	-	Vpp
High-Level Output Voltage (Iout=–200μA)		VOH	DVDD–0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout=200μA)		VOL	-	-	0.2	V
(SDA pin: Iout=3mA)		VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

Note 18. MCKI pin fl ^ – 'h ø{ (Figure 45)

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¿ ‰ ‹ Q

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=1.6 ~ 3.6V; CL = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Input Timing					
Frequency (PLL mode)	fCLK	11.2896	-	27	MHz
(EXT mode)	fCLK	2.048	-	12.288	MHz
Pulse Width Low (Note 19)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High (Note 19)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width (Note 20)	tACW	18.5	-	-	ns
LRCK Timing					
Frequency	fs	8	44.1	48	kHz
Duty Cycle: Slave Mode	Duty	45	-	55	%
Master Mode	Duty	-	50	-	%
MCKO Output Timing (PLL mode)					
Frequency	fCLKO	0.256	-	12.288	MHz
Duty Cycle (Except fs=32kHz, PS1-0= “00”)	dMCK	40	-	60	%
(fs=32kHz, PS1-0= “00”)	dMCK	-	33	-	%
Serial Interface Timing (Note 21)					
Slave Mode (M/S bit = “0”):					
BICK Period	tBCK	312.5	-	-	ns
BICK Pulse Width Low	tBCKL	100	-	-	ns
Pulse Width High	tBCKH	100	-	-	ns
LRCK Edge to BICK “↑” (Note 22)	tLRB	50	-	-	ns
BICK “↑” to LRCK Edge (Note 22)	tBLR	50	-	-	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Master Mode (M/S bit = “1”):					
BICK Frequency (BF bit = “1”)	fBCK	-	64fs	-	Hz
(BF bit = “0”)	fBCK	-	32fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK “↓” to LRCK	tMBLR	–50	-	50	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN “H” Time	tCSW	150	-	-	ns
CSN “↑” to CCLK “↑”	tCSS	50	-	-	ns
CCLK “↑” to CSN “↑”	tCSH	50	-	-	ns

Note 19. AC S ¿ ‹ X {

Note 20. MCKI t 0 ' o » t fl ^ – ' z ¯ ‹ ¯ t 0 ' o ' h ø w ‹ ¯ t 0 b

˝ { (Figure 3)

Note 21. ‡ ^ » » £ w ' o < ^ M {

Note 22. \ w F ¤ x LRCK w ⁄ ¿ · q BICK w “↑” U O s s M O t F ' o M b {

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Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 23)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 24)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 25)	tPD	150	-	-	ns

Note 23. I^2C xPhilips Semiconductors wJ "pb{

Note 24. ^ »x7 300ns (SCL wqj<U) w –¸^ sZ ys d {

Note 25. ?od x PDN pin "L" T "H" tb \qp •¿˜UTT b{

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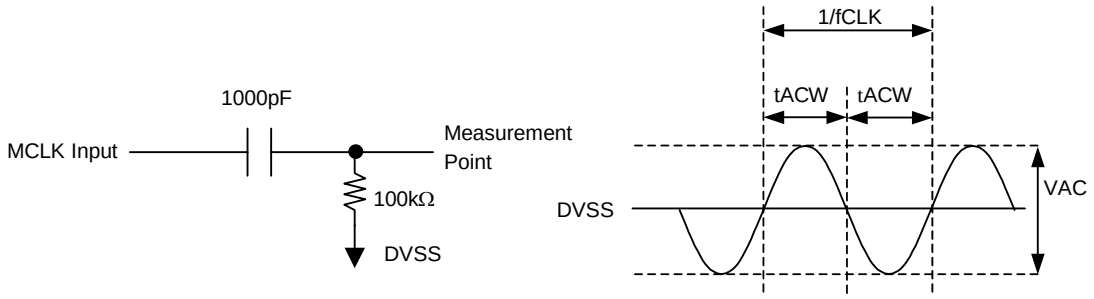

Figure 3. MCKI AC Coupling Timing

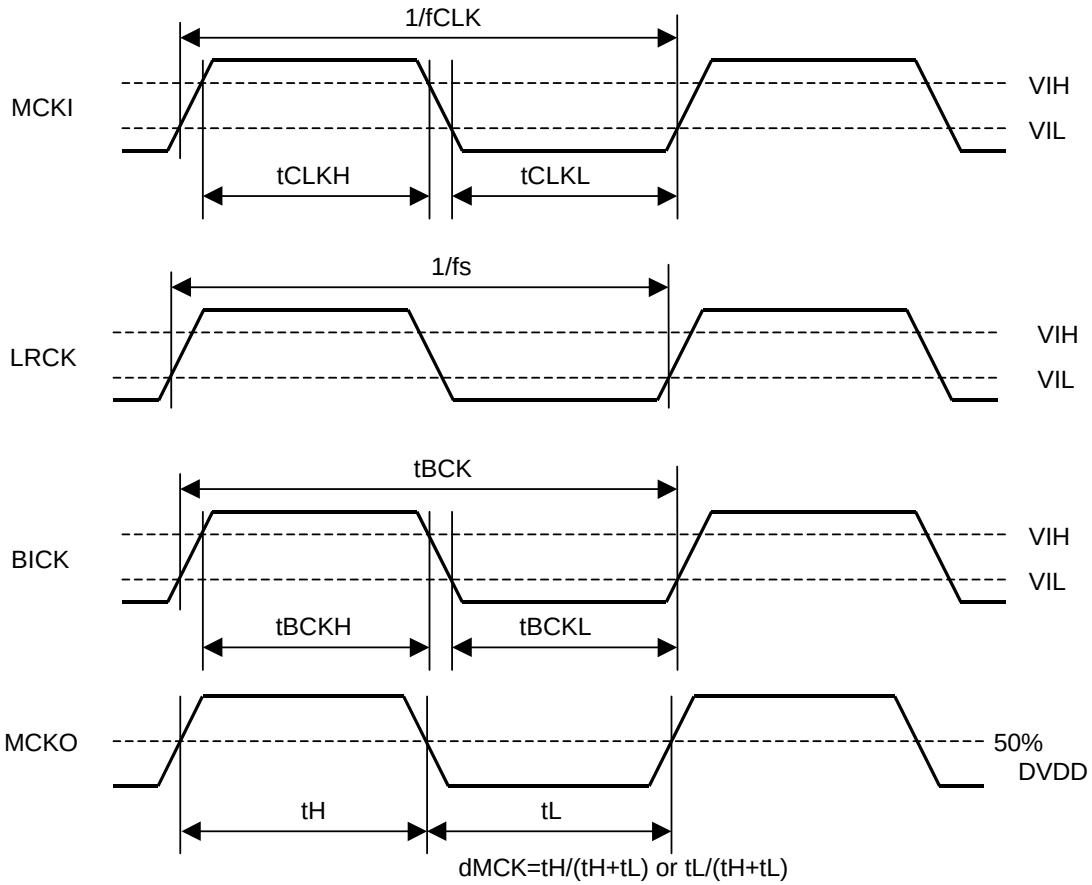

Figure 4. Clock Timing

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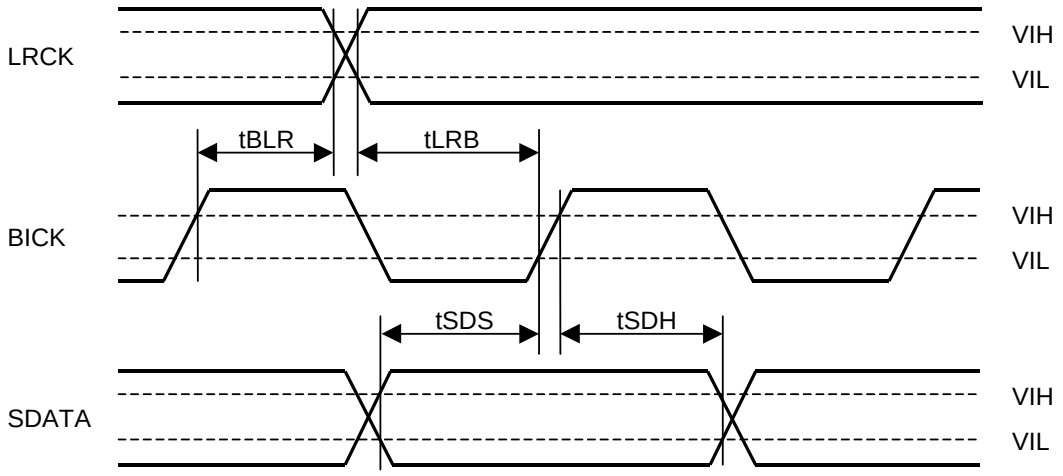

Figure 5. Serial Interface Timing (Slave Mode)

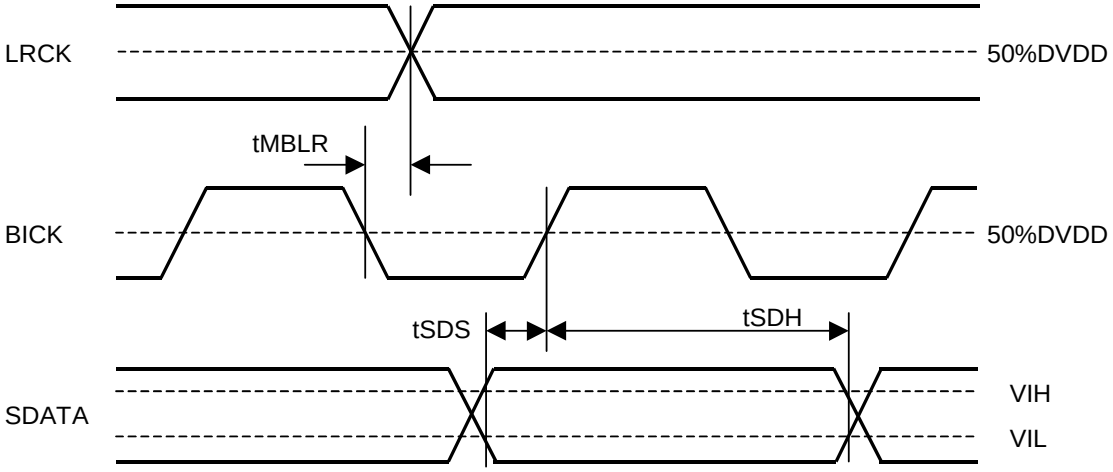

Figure 6. Serial Interface Timing (Master mode)

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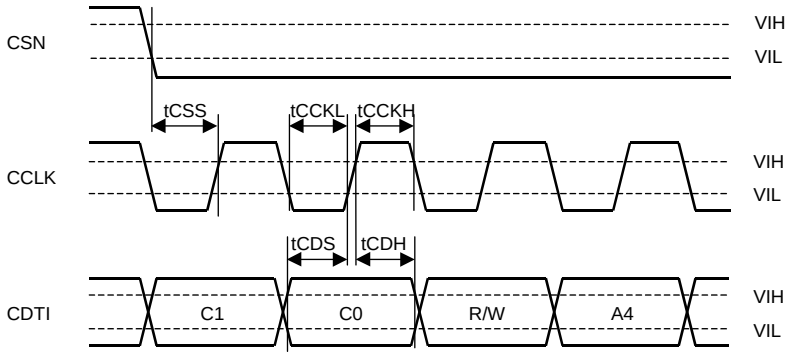

Figure 7. WRITE Command Input Timing

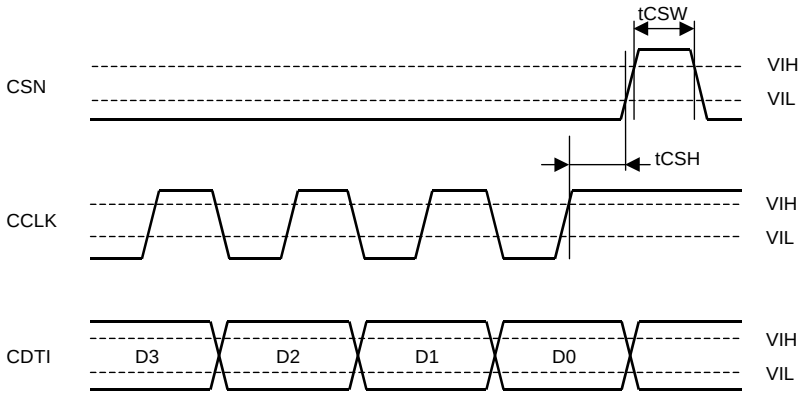

Figure 8. WRITE Data Input Timing

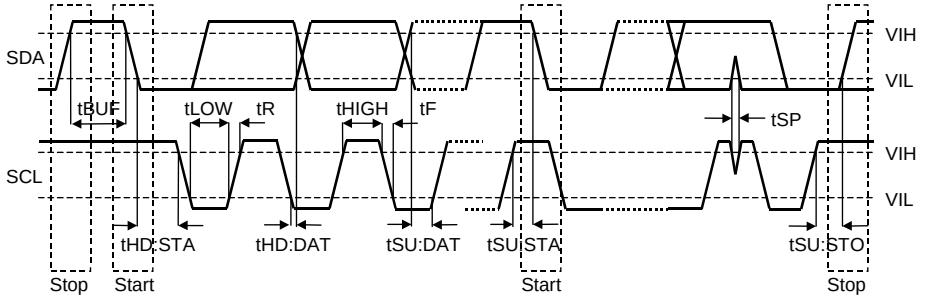

Figure 9. I^{2}C Bus Mode Timing

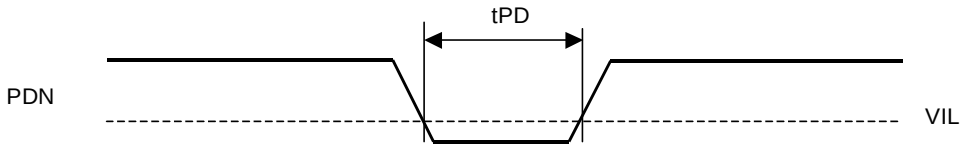

Figure 10. Power-down & Reset Timing

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■ ‡ ´ «Ø¿«

1) PLL ¯ (PMPLL bit = “1”)

″ w ^S ˘Ø‹ PLL xPLL3-0 bits, FS3-0 bits (Table 1, Table 2) p‹R`h«Ø¿«t ao ^` b{ MCKO wZ «Ø¿«x PS1-0 bits (Table 3) p ^ h* : Z `z MCKO bit to ON/OFF D pb{ PLL wØ¿« x Table 1 `oXi^M{ ^/ (PMDAC bit = “1”) t– ‹* : !¸b ØxZ„ ˜ Æ ˜ TZ TzK Mxl 0” ^ » `oT – ‹* :w!¸ l oXi^M{

» ¯q Ł ¯w~ 8Qx M/S bit p M b{ “1” p » ¯z “0” p Ł ¯ pb{ AK4368 x˝° …¢ (PDN pin = “L”) zt|˝° …¢ r x Ł ¯pb{˝° … ¢ r z M/S bit “1” t!¸b \qp » ¯ts b{

» ¯ z T 11.2896MHz, 12MHz, 13MHz, 14.4MHz, 15.36MHz, 19.2MHz, 19.68MHz, 19.8MHz, 26MHz, 27MHz w«Ø¿« `z” w PLL t z MCKO, BICK, LRCK «Ø¿« \R`Z ` b{ (Figure 11)

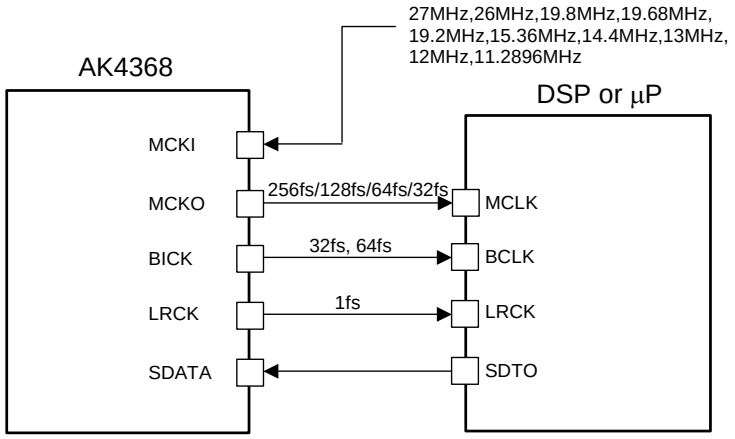

Figure 11. PLL Master Mode

» ¯p ;b øz M/S bit t “1” U{V pz AK4368 wLRCK, BICK pin x Ø ´ ‹w 6pb{fwh z AK4368 wLRCK, BICK pin t100kΩ Sw ¿ K Mx …¢ ¯ AUK b{

» ¯ (M/S bit = “1”) zPMPLL bit = “0” → “1” S | PMDAC bit = “0” → “1” t`h PLL UØ¿ «b pw z LRCK qBICK x“L” Z z MCKO bit = “1” wqV MCKO pin T xY psM* :w« Ø¿«UZ ^ b{ MCKO bit = “0” w øxz MCKO pin x“L” Z ` b{ PLL Ø¿« z LRCK q BICK UAK4368 T Z ^ b (Table 4) {

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Ł ¯ z BICK, LRCK pin ^ «Ø¿« ,jt" w PLL toz AK4368 t As«Ø¿« \R
`b{ \w ¯px MCKO t 8`h BICK, LRCK ` b{

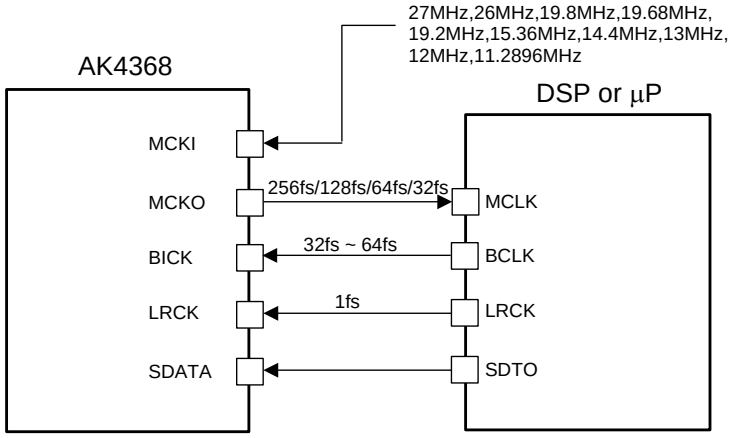

Figure 12. PLL Slave Mode

Ł ¯ (M/S bit = "0") zPMPLL bit = "0" → "1" S | PMDAC bit = "0" → "1" t`h PLL UØ ¿«b pw z MCKO bit = "1" wqV MCKO pin T xY psM* :w«Ø¿«UZ ^ b{f w z PLL UØ¿«b q MCKO pin T Table 3 p‹R^ h«Ø¿«UZ ^ b{ ^ (PMDAC bit = "1") xLRCK qBICK › oxMZ d {\ w«Ø¿«U ^ sM øz" t… ˘ ¿«s Ø·¿« ;`oM h za?vUv z ^U ts D QUK b{«Ø¿« › ø x˝° …¢ 6 (PMDAC bit = "0") t`o<^M{

Mode	PLL3	PLL2	PLL1	PLL0	MCKI	fs[kHz]	VCOC wR,C		PLL Ø¿« (typ £	
							R[Ω]	C[F]		
0	0	0	0	0	11.2896MHz	44.1, 48	10k	22n	20ms	Default
1	0	0	0	1	14.4MHz	44.1, 48	10k	22n	20ms	
2	0	0	1	0	12MHz	44.1, 48	10k	47n	20ms	
3	0	0	1	1	19.2MHz	44.1, 48	10k	22n	20ms	
4	0	1	0	0	15.36MHz	44.1, 48	10k	22n	20ms	
5	0	1	0	1	13MHz	44.1, 48	15k	330n	100ms	
6	0	1	1	0	19.68MHz	44.1, 48	10k	47n	20ms	
7	0	1	1	1	19.8MHz	44.1, 48	10k	47n	20ms	
8	1	0	0	0	26MHz	44.1, 48	15k	330n	100ms	
9	1	0	0	1	27MHz	44.1, 48	10k	47n	20ms	
10	1	0	1	0	13MHz	44.0995 48.0007	10k	22n	20ms	
11	1	0	1	1	26MHz	44.0995 48.0007	10k	22n	20ms	
12	1	1	0	0	19.8MHz	44.0995 47.9992	10k	22n	20ms	
13	1	1	0	1	27MHz	44.0995 47.9997	10k	22n	20ms	
14-15	Others				N/A	N/A	N/A	N/A	-	

Table 1. MCKI * : (PLL mode)

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Mode	FS3	FS2	FS1	FS0	fs	
0	0	0	0	0	48kHz	
1	0	0	0	1	24kHz	
2	0	0	1	0	12kHz	
4	0	1	0	0	32kHz	
5	0	1	0	1	16kHz	
6	0	1	1	0	8kHz	
8	1	0	0	0	44.1kHz	Default
9	1	0	0	1	22.05kHz	
10	1	0	1	0	11.025kHz	
3, 7, 11-15	Others				N/A	

Table 2. – ‹ * : (PLL mode)

PS1	PS0	MCKO	
0	0	256fs	Default
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 3. MCKO * : (PLL mode, MCKO bit = “1”)

	Master Mode (M/S bit = “1”)		
	Power Up (PMDAC bit= PMPLL bit= “1”)	Power Down (PMDAC bit= PMPLL bit= “0”)	PLL Unlock
MCKI pin	Refer to Table 1.	Input or fixed to “L” or “H”	Refer to Table 1.
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”	“L”
LRCK pin	Output	“L”	“L”

Table 4. Clock Operation in Master mode (PLL mode)

	Slave Mode (M/S bit = “0”)		
	Power Up (PMDAC bit= PMPLL bit= “1”)	Power Down (PMDAC bit= PMPLL bit= “0”)	PLL Unlock
MCKI pin	Refer to Table 1.	Input or fixed to “L” or “H”	Refer to Table 1.
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	Input	Fixed to “L” or “H” externally	Input or Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally	Input or Fixed to “L” or “H” externally

Table 5. Clock Operation in Slave mode (PLL mode)

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2) «Ø¿« ¯ (PMPLL bit = “0”: Default)

PMPLL bit “0” tb \qpz «Ø¿« ¯ (EXT mode) p ^'z MCKI pin T PLL p^ct DAC t »«Ø¿« pV b{\w øz FS3-0 bits p‹RpV «Ø¿«x Table 6 wŁ pb{ hz PLL3-0 bits w x`„^ b{ MCKO wZ x MCKO bit to ON/OFF D pzZ * :x PS1-0 bit t ^ b{ DAC ^⁄ (PMDAC bit = “1”) t– ‹* : !¸b øxz„ ~ Æ ~ TZ TzK Mx “0” ^ » 'oT – ‹* :w!¸ lo<^M{

» ¯ (M/S bit = “1”) xz LRCK qBICK UAK4368 T Z ^ b (Figure 13) { ^ (PMDAC bit = “1”) xMCKI pin w «Ø¿« › oxMZ d {\ w«Ø¿«U ^ sM øz” t… ˘ ¿«sØ·¿« ;'oM h za?vUv z ^U ts D QUK b{«Ø¿« › øx DAC ˝° …¢ 6 (PMDAC bit = “0”) t'o<^M{

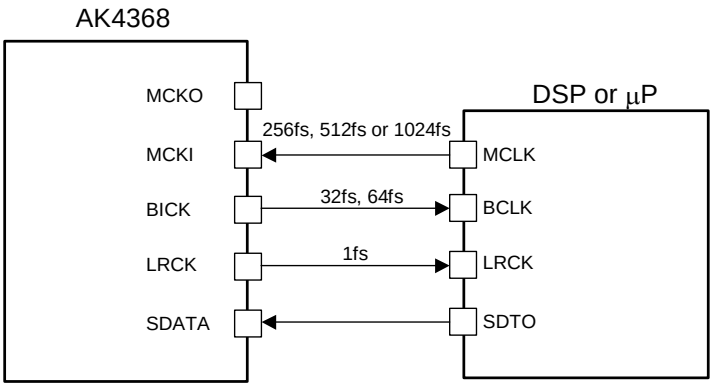

Figure 13. EXT Master Mode

Ł ¯ (M/S bit = “0”) t As«Ø¿«xz MCKI, BICK, LRCK pb (Figure 14) {MCKI qLRCK x 8b AUK bU ø d AxK d { DAC ^ (PMDAC bit = “1”) x⁄ «Ø¿« (MCKI, BICK, LRCK) › oxMZ d {\ w«Ø¿«U ^ sM øz” t… ˘ ¿«sØ·¿« ;'oM h za?vUv z ^U ts D QUK b{«Ø¿« › øx DAC ˝° …¢ 6 (PMDAC bit = “0”) t'o<^M{

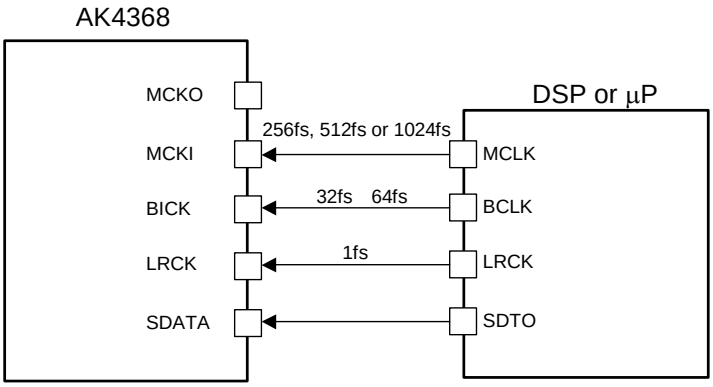

Figure 14. EXT Slave Mode

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Mode	FS3	FS2	FS1	FS0	fs	MCKI	
0	0	0	0	0	8kHz ~ 48kHz	256fs	
1	0	0	0	1	8kHz ~ 24kHz	512fs	
2	0	0	1	0	8kHz ~ 12kHz	1024fs	
4	0	1	0	0	8kHz ~ 48kHz	256fs	
5	0	1	0	1	8kHz ~ 24kHz	512fs	
6	0	1	1	0	8kHz ~ 12kHz	1024fs	
8	1	0	0	0	8kHz ~ 48kHz	256fs	Default
9	1	0	0	1	8kHz ~ 24kHz	512fs	
10	1	0	1	0	8kHz ~ 12kHz	1024fs	
3, 7, 11-15	Others				N/A	N/A	

Table 6. – ‹ * :q MCKI * :w (EXT mode)

PS1	PS0	MCKO	
0	0	256fs	Default
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 7. MCKO * : (EXT mode, MCKO bit = “1”)

	Master Mode (M/S bit = “1”)	
	Power Up (PMDAC bit = “1”)	Power Down (PMDAC bit = “0”)
MCKI pin	Refer to Table 6.	Input or fixed to “L” or “H”
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”
LRCK pin	Output	“L”

Table 8. Clock Operation in Master mode (EXT mode)

	Slave Mode (M/S bit = “0”)	
	Power Up (PMDAC bit = “1”)	Power Down (PMDAC bit = “0”)
MCKI pin	Refer to Table 6.	Input or fixed to “L” or “H”
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	Input	Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally

Table 9. Clock Operation in Slave mode (EXT mode)

– ‹ x3‹ ° ¶wh z DR, S/N U…=‘ b{ MCKI t ^ »«Ø¿«w*
: ˝[\qpz DR, S/N ~‡pV b{ Table 10 xDAC Z ¿¯ ¥ tŁ‘h øw DR, S/N pb{

MCKI	DR, S/N (BW=20kHz, A-weight)	
	fs=8kHz	fs=16kHz
256fs	56dB	75dB
512fs	75dB	90dB
1024fs	90dB	N/A

Table 10. MCKI q ¿¯ ¥ w DR, S/N w (2.4V)

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■ ‡ ˆ » » £

SDATA, BICK, LRCK w3pin ; ` o w ‡ ´ q » £ ` b { 5 ¤ w ˆ » ¥ ¿ ˜(Table 11) U DIF2-0 bits p ‹ R p V b { Mode 0 x 7 w 16bitDAC t | ˆ · » » q ı Q U K b { Mode 1 xMode 0 w20bit [p b { Mode 4 xMode 0 w24bit [p b { Mode 2 x p ADC w Z ; DSP w ‡ ˜ q ı Q U K b { Mode 3 xI²S » £ q ı Q U K b { BICK≥48fs Mode 2 q 3 p16bit ˆ » b ø x z LSB t Z o 17~24bit Ł t 8 x w “0” ` z 20bit ˆ » w ø x LSB t Z o 21~24bit Ł t 4 x w “0” ` b {

» ¯ p BICK=32fs(BF bit = “0”) w ø z ƒ ˆ ƒ ¥ ¿ ˜ w Mode 1, 2 t x 0 ` o M d {

Mode	DIF2	DIF1	DIF0	¥ ¿ ˜	BICK	$	
0	0	0	0	0: 16bit, g	32fs ≤ BICK ≤ 64fs	Figure 15	
1	0	0	1	1: 20bit, g	40fs ≤ BICK ≤ 64fs	Figure 16	
2	0	1	0	2: 24bit, † g	48fs ≤ BICK ≤ 64fs	Figure 17	Default
3	0	1	1	3: I²S ı	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 18	
4	1	0	0	4: 24bit, g	48fs ≤ BICK ≤ 64fs	Figure 16	

Table 11. ƒ ˆ ƒ ¥ ¿ ˜

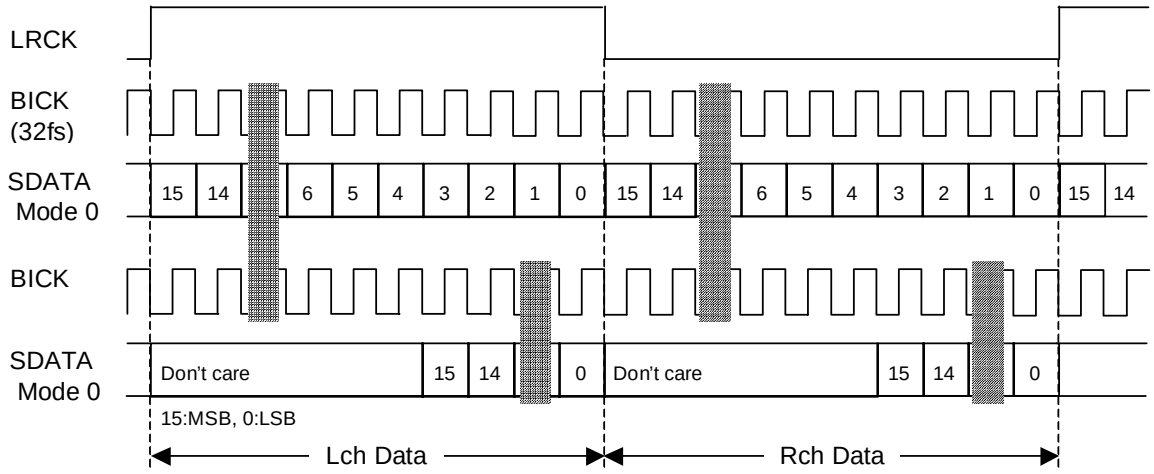

Figure 15. Mode 0 » ‹ (LRP = BCKP bits = “0”)

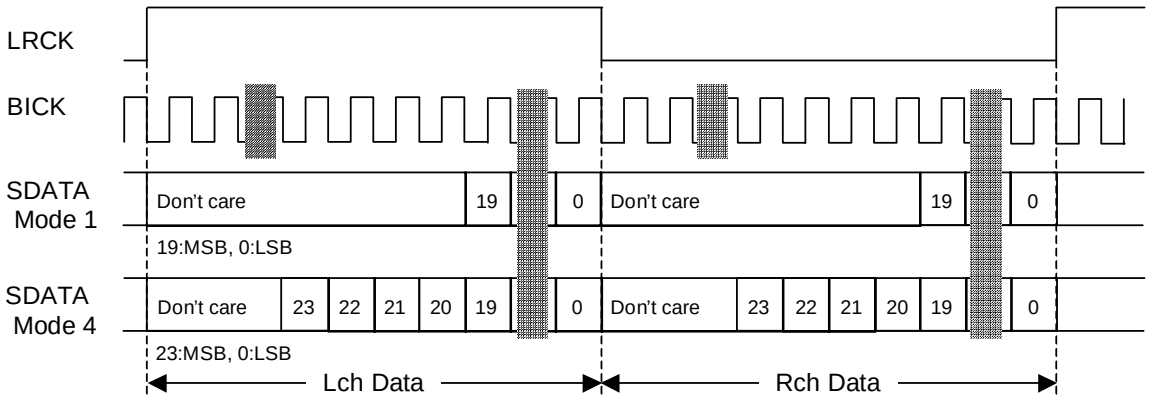

Figure 16. Mode 1, 4 » ‹ (LRP = BCKP bits = “0”)

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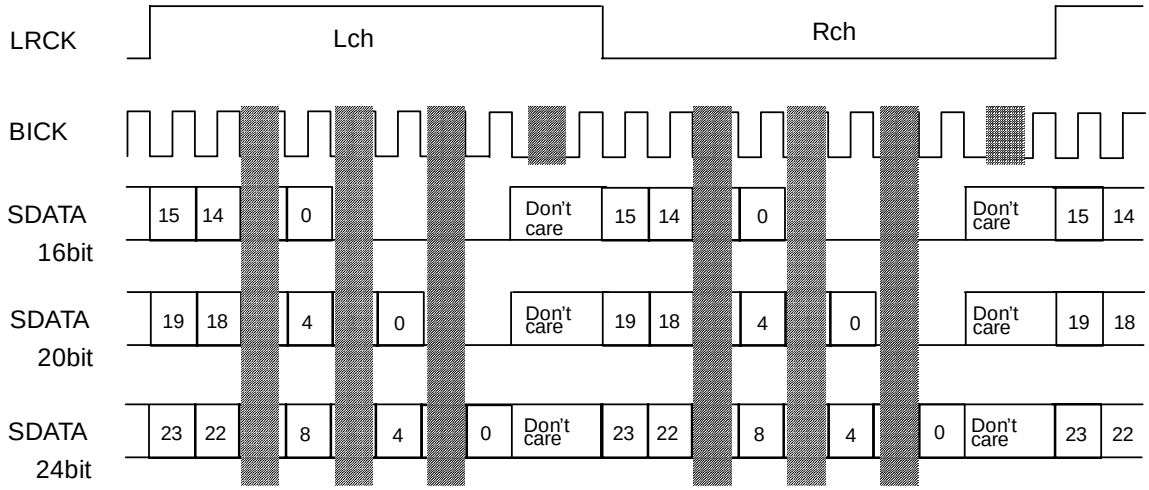

Figure 17. Mode 2 » ‹ (LRP = BCKP bits = "0")

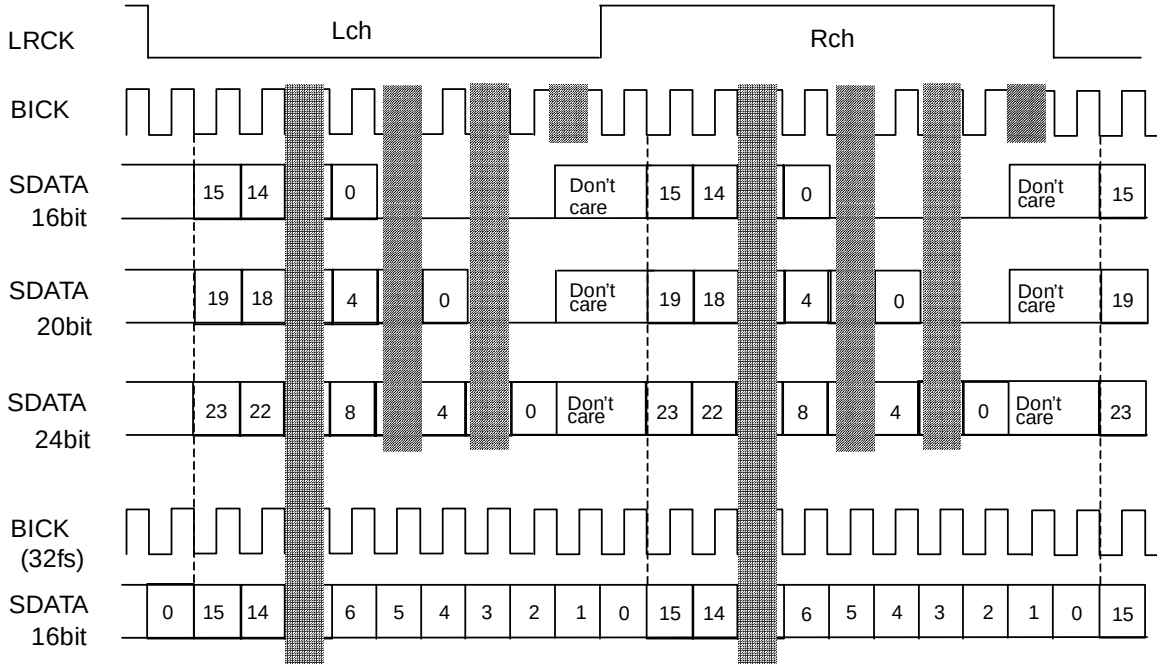

Figure 18. Mode 3 » ‹ (LRP = BCKP bits = "0")

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■ ALC ^

ALC bit = “1” t b qz ALC ^U ` b{ ALC bit = “0” wqVz ALC wfi x 0dB { pb{

[1] ALC ¿» ^

ALC ¿» ^pxz DAC wL/R ‰ w Ł Ur T mp ALC ¿»UZŁ (–6.0dBFS) Qh øz ALC ¿» ATT ´¿ (LMAT1-0 bits, Table 13) iZ $t Æ n0^d b{ ALC ¿» ^t Æ U!¸^ wxz L/R fg ,Ø«Ø b T,Ø «Ø » ¢˜`hqVpb{,Ø«Ø » ¢˜ x ROTM1-0 bits (Table 12) p ^ b{

ROTM1	ROTM0		ALC § 4; ,,Ø«Ø » ¢˜						
			fs=16kHz	fs=22.05kHz	fs=24kHz	fs=32kHz	fs=44.1kHz	fs=48kHz	
0	0	1024/fs	64ms	46ms	43ms	32ms	23ms	21ms	
0	1	2048/fs	128ms	93ms	85ms	64ms	46ms	43ms	Default
1	0	4096/fs	256ms	186ms	171ms	128ms	93ms	85ms	
1	1	Reserved	-	-	-	-	-	-	

Table 12. ALC § 4; ,,Ø«Ø » ¢˜

LMAT1	LMAT0	ALC ¿» ATT ´¿				
		ALC Output ≥ –6.0dBFS	ALC Output ≥ 0dBFS	ALC Output ≥ +6dBFS	ALC Output ≥ +12dBFS	
0	0	1	1	1	1	Default
0	1	2	2	2	2	
1	0	2	2	4	4	
1	1	2	4	4	8	

Table 13. ALC ¿» ATT ´¿

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[2] ALC § ^

ALC § ^xz ALC ¿» ^4 z ROTM1-0 bits p ^ h iZ4; Mz\w z DAC w Ł U § 4;§¢ » •¿˜Ł (–8.5dBFS) Q \qUsZ yz ALC § ^ s M b{\w ALC § ^xz ROTM1-0 bits (Table 12) p `h p,Ø«Ø UZ ^ MsU z Æ (L/R Ł) ^ h,jŁ (REF7-0 bits, Table 15) p RATT bit (Table 14) p ^ h ´¿ p $t C^d b{ h†sw 4;4 q t˝sw 4; b wpz ALC § ^x ROTM1-0 bits p `h*8p b{ ROTM1-0 bits p `h8 ⁄ t,Ø«Ø ^U4 `h øz ROTM1-0 bits p `h8 p4;`oz˝w § ^t b{

ALC § ^⁄ hx § 4;⁄z DAC wL/R ‰ w Ł Urj T Mp ALC ¿»UZŁ (–6.0dBFS) Qh øz jt ALC ¿» ^t b{

hz ALC § 4;⁄t
(ALC § 4;§¢ » •¿˜Ł) ≤ (DAC Ł) < (ALC ¿»UZŁ)
qsloM øz4;» x •¿˜^ b{fwh z
(ALC § 4;§¢ » •¿˜Ł) > (DAC Ł)
qslh T z4; w§¢ ˜U ^ b{

hz ˝ Qw° ¶U ^ h øz ROTM1-0 bits p ^ h ªM– « p § ^ M b{

RATT	GAIN STEP	
0	1	Default
1	2	

Table 14. ALC § fi ´¿

REF7-0	GAIN(dB)	
FFH : C2H	Reserved	
C1H	+18.0	
C0H	+17.625	
BFH	+17.25	
:	:	
92H	+0.375	
91H	0	Default
90H	–0.375	
:	:	
73H	–11.25	
72H	–11.625	
71H	–12.0	
70H : 00H	Reserved	

Table 15. ALC § ^ w,j w

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[3] ALC ^ q«

Register Name	Comment	fs=16kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
ROTM1-0	Zero crossing timeout period	00	64ms	01	46ms
REF7-0	Maximum gain at recovery operation	C1H	+18dB	C1H	+18dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RATT	Recovery GAIN step	0	1 step	0	1 step
ALC	ALC enable	1	Enable	1	Enable

Table 16. ALC «

ALC ^ / x z < w ˇ ¿ ˜ w ! ¸ — › ' b { \ w ˇ ¿ ˜ ! ¸ b ø x z ALC ^ 4 (ALC bit = "0" hx PMDAC bit = "0") 'oT lo<^M{

~LMAT1-0, ROTM1-0, RATT, REF7-0 w / ˇ ¿ ˜

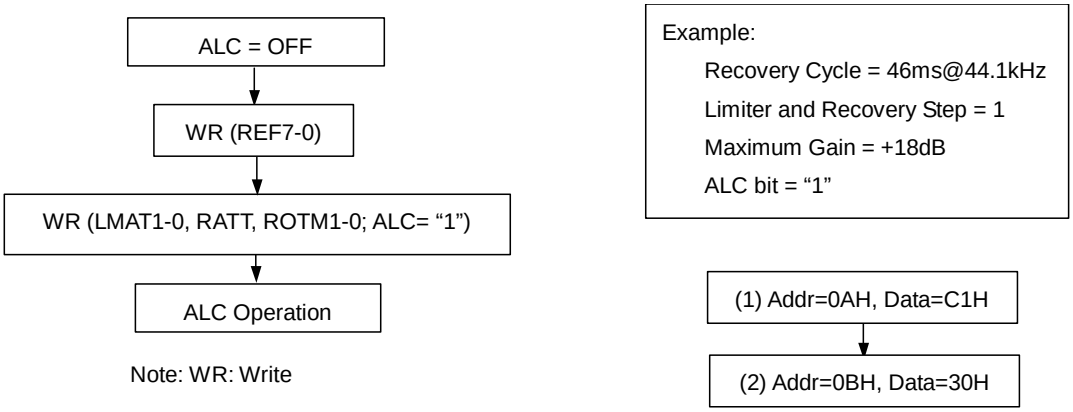

Figure 19. ALC ^ q«

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■ ˆ ·» Z Æ

AK4368 xMUTE 0.5dB ´¿ z 256 Ł w‰ qˆ ·» Z Æ (DATT) ″ ` b{\w Æ x DAC w† tK z ˆ » 0dB T –127dB pn0z hx Æ ˜` b (Table 17) {DATTC bit “1” tb qz ATTL7-0 bit pLch, Rch w Æ tfl ˜Ø pV b{ DATTC bit U “0” w øz Lch, Rch w Æ x qtfl ˜Ø pV b{

ATTL7-0 ATTR7-0	Attenuation	
FFH	0dB	
FEH	–0.5dB	
FDH	–1.0dB	
FCH	–1.5dB	
:	:	
:	:	
02H	–126.5dB	
01H	–127.0dB	
00H	MUTE (–∞)	Default

Table 17. Digital Volume ATT

ATT7-0 w› x ATS bit p1061/fs q7424/fs wrj T ‹RpV b (Table 18) {ATS bit = “0” wqV ATT w› x 1062 Ł p„ ˜› ` b{ FFH(0dB) T 00H(MUTE) ptx 1061/fs (24ms @fs=44.1kHz) TT b{ PDN pin “L” tb qz ATT7-0 x00H ts8=ˆ b{ ATT7-0 xPMDAC bit “0” tb q t 00H ts z PMDAC bit “1” t bq t loMV b{ˆ ·» Æ ; x„ ˜ Æ ˜; qx qt ^` b{

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	Default
1	7424/fs	29/fs	

Table 18. ˆ ·» Æ w ATT7-0 w›

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■ „ ˜ Æ ˜

„ ˜ Æ ˜ x ^ · » $ t ^ b { SMUTE bit “1” t b q f w : w ATT T ATT ×ATT › (Table 18) p ^ » U –∞ (“0”) p ´ ‡ª ^ b { SMUTE bit “0” t b q–∞ T ATT ×ATT › p ATT p < ` b { „ ˜ Æ ˜ z –∞ p ´ ‡ª ^ † t r ^ q ´ ‡ª U ⁄ ^ z a – « p ATT p < ` b { „ ˜ Æ ˜ ; x ł › c t ło ~ 8 Q ø s r t fip b {

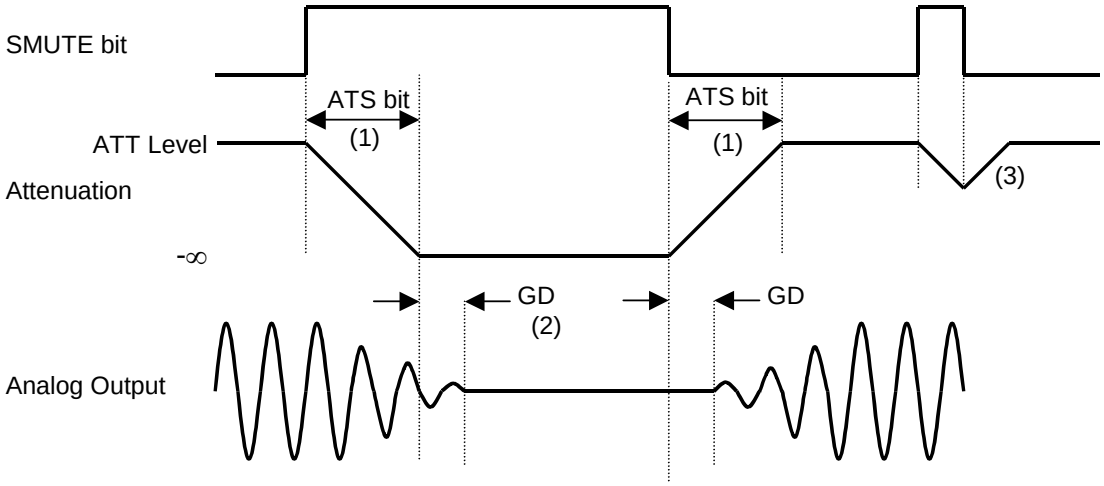

Figure 20. „ ˜ Æ ˜ ;

Notes:

(1) ATT ×ATT › (Table 18) { « Q y z ATS bit = “1” z ATT U “128”(–63.5dB) w ø x 3712/fs – « p b {

(2) ^ · » t 0 b ˘ Ø ‹ Z x (GD) ¸ j b {

(3) „ ˜ Æ ˜ z –∞ p ´ ‡ª ^ † t r ^ q ´ ‡ª U ⁄ ^ z a – « p ATT p < ` b {

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■ ˆ ⁄ ‡ »

IIR »t 3 * : (32kHz, 44.1kHz, 48kHz) 0 wˆ ⁄ ‡ » (50/15µs Q) ″ ` oM b{ DEM1-0 bit p‹ Rˆ hˆ ⁄ ‡ »U fits b (Table 19) {

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 19. ˆ ⁄ ‡ fl ˜Ø

■ ˜;

BST1-0 bit M b \qpz DAC T ˜ˆ h ł Z b \qUpV b (Table 20) { x ‰ Łpb{

BST1 bit	BST0 bit	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 20. ˜

■ '‡ ‹;

MONO1-0 bit t z DAC t ˆ ˆ ·» ˆ »t0 'o Lch/Rch ˆ »w~ 8Q M b (Table 21) {

MONO1 bit	MONO0 bit	Lch	Rch	
0	0	L	R	Default
0	1	L	L	
1	0	R	R	
1	1	(L+R)/2	(L+R)/2	

Table 21. '‡ ‹

■ ‡ ´ •¿˜

?oqj˝[txz PDN pin t S “L” 'o •¿˜'o<ˆM{ •¿˜r z VCOM, DAC, HPL, HPR, LOUT, ROUT x˝° …¢ 6pqj˝U b{ PDN pin p •¿˜ˆ sMv zfl ˜Ø Ł· »w″0x–¸ˆ oM b{

DAC w •¿˜t|˝° …¢ x PMDAC bit t“1” U{V h z MCKI pr ˆ z″ w» ‹U ˆ' b{ MCKI U ˆ p˝° …¢ 6pb{

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■ ¿ ¯ ¥ (HPL, HPR pins)

¿ ¯ ¥ w ? o x HVDD T ^ b { fl ? y x MUTET pin w ? y p z * Y ¯ x
16Ω ´ p b { PMHPL=PMHPR bits = “1” pMUTEN bit “1” t b q fl ? y VCOM(=0.475 x AVDD) t
q j ´ [b { MUTEN bit “0” t b q z ¿ ¯ ¥ w fl ? y HVSS t q j < [b {

t_r: q j ´ U	(VCOM/2 p)	70k x C (typ)
t_f: q j < U	(VCOM/2 p)	60k x C (typ)

Table 22. ¿ ¯ ¥ q j ´ U q j < U

« : MUTET pin w fl ^ – C=1µF w ø
~ ¿ ¯ ¥ q j ´ U (VCOM/2 p): t_r = 70k x 1µ = 70ms(typ)
~ ¿ ¯ ¥ q j < U (VCOM/2 p): t_f = 60k x 1µ = 60ms(typ)

PMHPL, PMHPR bits “0” t b \ q p z ¿ ¯ ¥ ¶ t ´ ° … ¢ b \ q U p V b { \
w z HPL, HPR pins x HVSS p b {

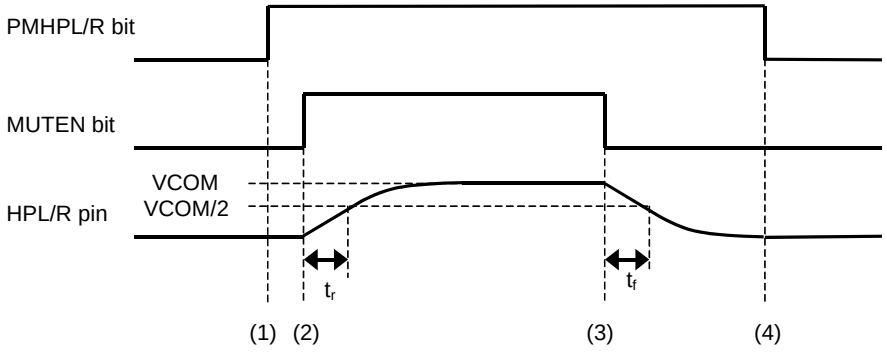

Figure 21. ¿ ¯ ¥ w ´ ° ¿ … ¢ ‡ ›

(1) ¿ ¯ ¥ w ´ ° ¿ (PMHPL, PMHPR bits = “1”) { Z x HVSS w p b {
(2) ¿ ¯ ¥ w fl ? y q j ´ [(MUTEN bit = “1”) { MUTET w fl ^ – q ″ ¯ w :
t fl ? y U ´ ¢ ` o V b { MUTET pin w fl ^ – w 0 “C” q ` h q V z VCOM/2 p
w q j ´ U (t_r) x70k x C(typ) q s b {
(3) ¿ ¯ ¥ w fl ? y q j < [(MUTEN bit = “0”) { MUTET w fl ^ – q ″ ¯ w :
t fl ? y U HVSS < æ ` o V b { MUTET pin w fl ^ – w 0 “C” q ` h q V z
VCOM/2 p w q j < U (t_f) x60k x C(typ) q s b {
(4) ¿ ¯ ¥ w ´ ° … ¢ (PMHPL, PMHPR bits = “1”) { Z x HVSS p b { ¿ ° ¶ w › w
h z ¿ ¯ ¥ w fl ? y U ¶ t < U l o T ´ ° … ¢ ` o < ^ M {

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¿ ¯ ¥ w ¯ qfl ^ –p§¿˜ƒ * : (fc) U> b{ Table 23 t ¯ qfl ^ –t|§¿˜ƒ * : (fc) w qfw wZ ˝° ` b{``z ¿ ¯ ¥ w R_L x16Ω q` b{Z ˝° x AVDD=2.4, 3.0, 3.3V w pb{ ¿ ¯ ¥ wZ x 0.47 x AVDD (Vpp) @–3dBFS pb{

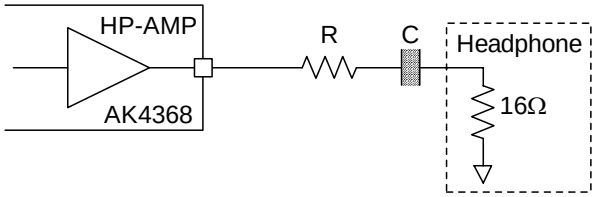

Figure 22. ¿ ¯ ¥ w ·Zs˘«

R [Ω]	C [µF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN	Output Power [mW]			
				HPG=0, 0dB			HPG=1, 4.8dB
				2.4V	3.0V	3.3V	3.3V
0	220	45	17	20	31	38	50
	100	100	43				
6.8	100	70	28	10	15	18	25
	47	149	78				
16	100	50	19	5	8	9	13
	47	106	47				

Table 23. s˘, Z ˝° q f w

/˝ w ON/OFF xf g DACHL, LINHL, MINHL, DACHR, RINHR, MINHR bits p ` b{ HPG bit = "0" (R_1=100k) wqVC fi xMc w˝ +0.76dB(typ) pb{ HPG bit = "1" (R_1= 50k) wqV DAC Z ł wC fi +6.76dB(typ) t~ 8Q b{

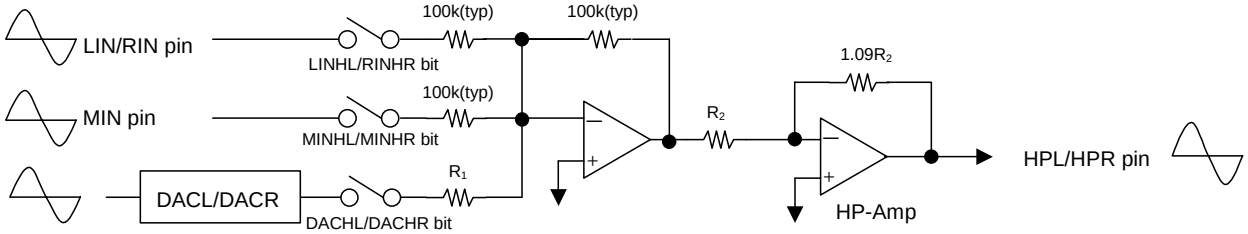

Figure 23. ¿ ¯ ¥ Z wC s˘ (HPG bit = "0" wqV)

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■ ´Ł ƒ Z (LOUT, ROUT pins)

fl ?yx 0.475 x AVDD ?ypz Y ¯x 10kΩ ´pb{ PMLO bit = “1” p´° ¿ ` b{ ⁄´ w ON/OFF xf g DACL, LINL, MINL, DACR, RINR, MINR bits p ` b{ LOG bit = “0”(R_1=100k), ATTS3-0 bits = “0FH”(0dB) wqVC fi xMc w´ 0dB(typ) pb{ LOG bit = “1” (R_1= 50k) wqV DAC Z ŁwC fi +6dB t~ 8Q b{

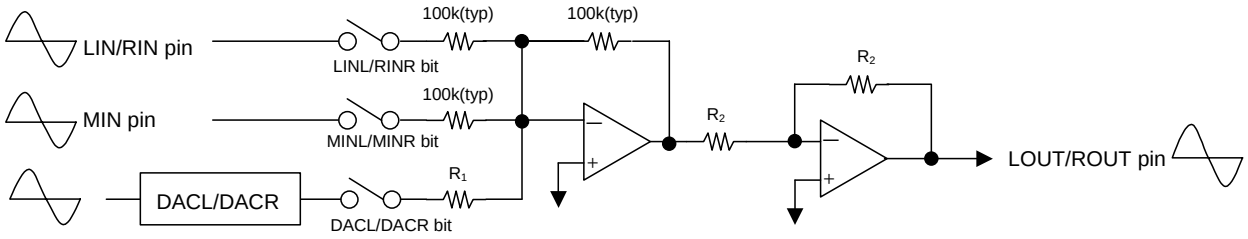

Figure 24. LOUT/ROUT wC s ˇ (LOG bit = “0” wqV)

■ ¯Ø‹ Z Æ

LOUT/ROUT Z xz LMUTE bit = “0” w zATTS3-0 bit p Æ fl ˜Ø D pb (0dB ~ –30dB, 2dB step, Table 24) {LOUT/ROUT Z w Æ ~ 8Q z ¿ ° ¶UC\ ` b{

LMUTE	ATTS3-0	Attenuation	
0	0FH	0dB	
	0EH	–2dB	
	0DH	–4dB	
	0CH	–6dB	
	:	:	
	:	:	
	01H	–28dB	
	00H	–30dB	
1	x	MUTE	Default

Table 24. LOUT/ROUT Volume ATT (x: Don’t care)

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■ 3D Stereo Enhancement

AK4368 x ´Łƒ Z t 3D fiL ¸hd ; (3D Stereo Enhancement) ″ ` b{ 3D1-0 bits t 3D ; w˝° · ˜ M (Table 25) z3D fiLwŁ x DP1-0 bits p ` b (Table 26) {3D1-0 bits {V pT 50ms w xz ¿ ;w›wh z 3D1-0 bits S | MUTEN bit !¸`sMp<^M{

hz 3DCAP1, 3DCAP2, 3DCAP3 pins t x Figure 25 w Otz 4.7nF q470nF w fl ^ – `oX i^M{ fl ^ –w^Sx ±20% ″w w ;`oXi^M{ 3DCAP1, 3DCAP2, 3DCAP3 pins w/ 0 Yx 20pF ″t`oXi^M{

3D1 bit	3D0 bit	3D ;	3D fiLZ	″	
0	0	OFF			Default
0	1	ON	LOUT, ROUT	¢˜C s˘	
1	0	ON	HPL, HPR	¿¯ ¥ C s˘	
1	1	ON	LOUT, ROUT, HPL, HPR	¿¯ ¥ C s˘	

Table 25. 3D ; w˝° · ˜

DP1 bit	DP0 bit	3D Depth	
0	0	0%	Default
0	1	50%	
1	0	70%	
1	1	100%	

Table 26. 3D fiLŁ

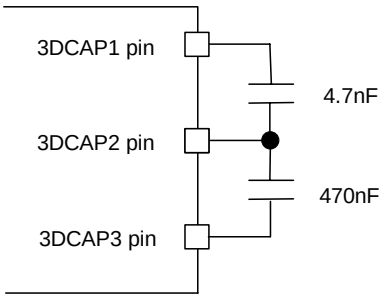

Figure 25. 3D ; ·Zs˘

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■ ˝ ° ¿ …¢ ‡ › **(EXT mode)**

1) DAC → HP-Amp

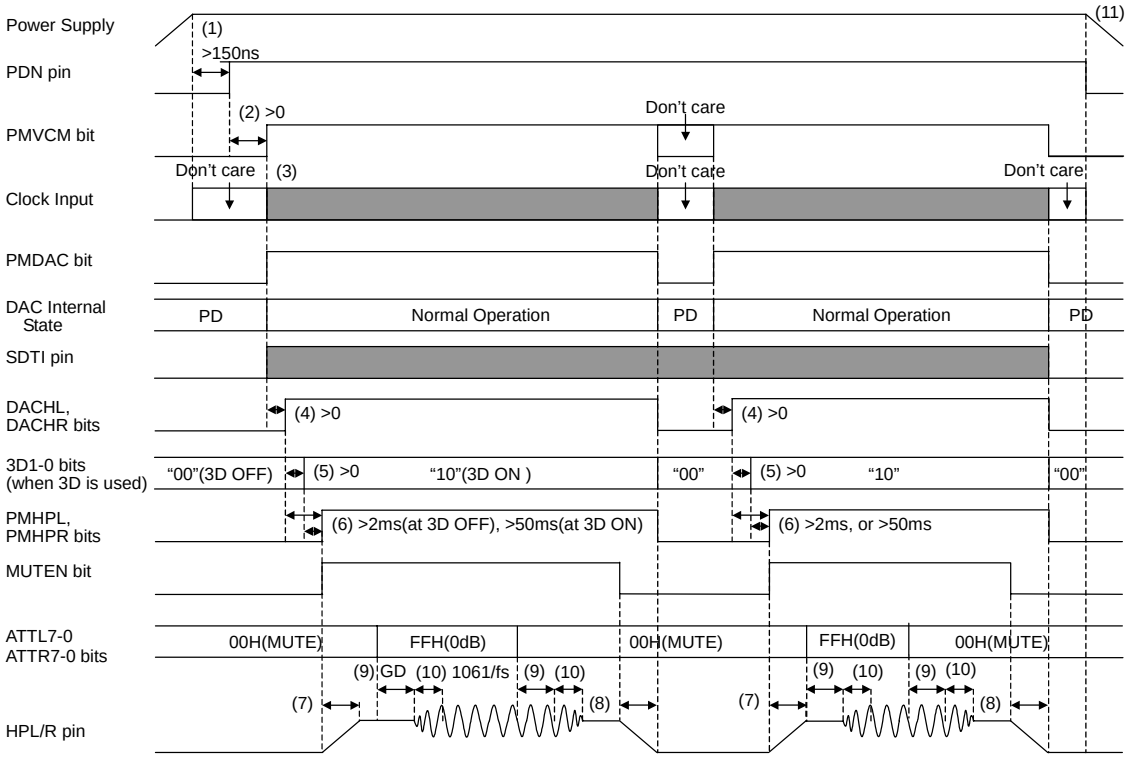

Figure 26. DAC S | HP-amp w ˝ ° ¿ …¢ ‡ › (Don't care: Hi-Z X)

(1) ?oqj˝[z 150ns ˝&loT PDN pin "H" t'o<^M{
(2) PDN pin "H" t'oT PMVCM, PMDAC bit t "1" {V p<^M{
(3) DAC w ^tx⁄«Ø¿« (MCKI, BICK, LRCK) U Apb{ PMDAC bit = "0" w x⁄«Ø¿« › \qUpV b{ ¿¯ ¥ x«Ø¿«U ^ oMsXo ^' b{
(4) PMVCM, PMDAC bits t "1" {V pT DACHL, DACHR bits t "1" {V p<^M{
(5) 3D ; ;b qVxz DACHL, DACHR bits t"1" {V pT 3D1-0 bits t"10" {V pX i^M{
(6) 3D ; ;'sM øxz DACHL, DACHR bits t "1" {V p 2ms ˝(VCOM pin wfl ^ – 2.2µF w ø) &loT PMHPL, PMHPR, MUTEN bits t "1" {V p<^M{ 3D ; ;b ø xz3D1-0bits t"10" {V p 50ms ˝&loT PMHPL, PMHPR, MUTEN bits t "1" {V p<^M{
(7) ¿¯ ¥ wqj˝U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj˝U (t_r) x70k x C(typ) pb{ C=1µF w øz t_r x70ms(typ) pb{
(8) ¿¯ ¥ wqj<U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj<U (t_f) x60k x C(typ) pb{ C=1µF w øz t_f x60ms(typ) pb{
¿¯ ¥ U ¶tqj<UloT PMHPL, PMHPR t "0" {V zfw DACL, DACR bits t "0" z 3D1-0bits t"00" {V p<^M{
(9) ^ ·» t0b ˘Ø‹Z x 22/fs(=499µs@fs=44.1kHz) w (GD) ¸j b{
(10) ^ ·» Æ w› x ATS bit p pV b{s8 x 1061/fs(=24ms@fs=44.1kHz) pb{
(11) ¿¯ ¥ U ¶tqj<UloT ?o OFF 'o<^M{

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2) DAC → Lineout

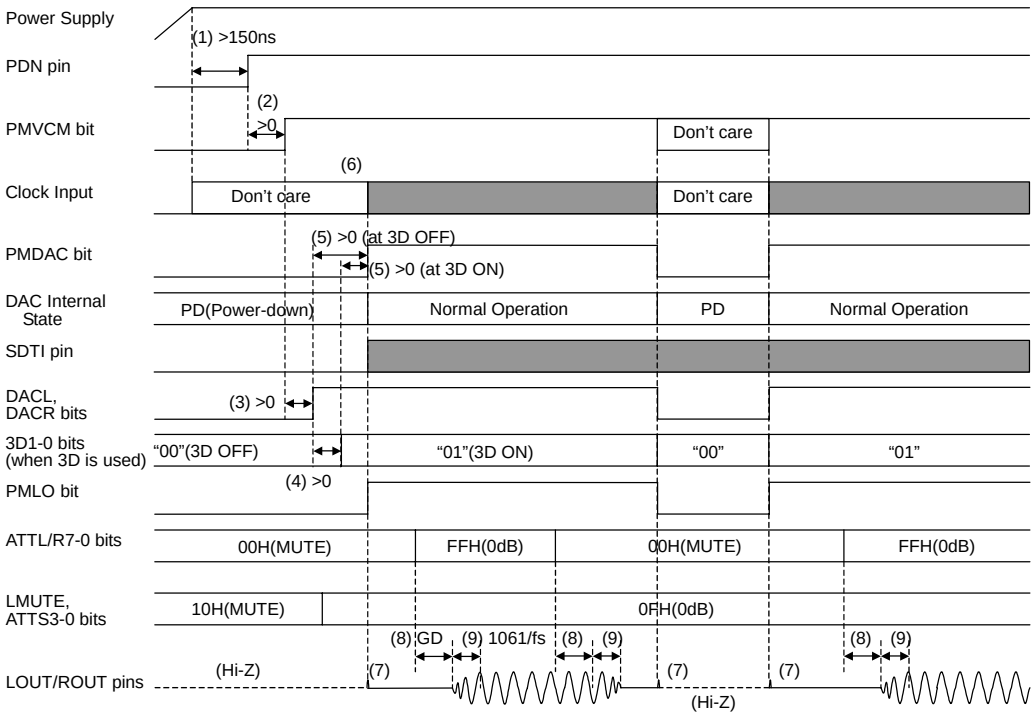

Figure 27. DAC S | Lineout w˝ ° ¿ …¢ ‡ › (Don't care: Hi-Z X)

(1) ?oqj˝[z 150ns ˝&loT PDN pin "H" t'o<^M{
(2) PDN pin "H" t'oT PMVCM bit t "1" {V p<^M{
(3) PMVCM bit t "1" {V pT DACL, DACR bits t "1" {V p<^M{
(4) 3D ; ;b qVxz DACL, DACR bits t"1" {V pT 3D1-0 bits t"01" {V pXi^M{
(5) 3D ; ;'sM øxz DACL, DACR bits t "1" {V pT PMDAC, PMLO bits t "1" {V p<^M{ 3D ; ;b øxz 3D1-0bits t"01" {V pT PMDAC, PMLO bits t "1" {V p<^M{
(6) DAC w ^txヘ«Ø¿« (MCKI, BICK, LRCK) U Apb{ PMDAC bit = "0" w xヘ«Ø¿« › \qUpV b{ LOUT/ROUT Z x«Ø¿«U ^ oMsXo ^' b{
(7) PMLO bit ~ 8Q q LOUT, ROUT pins t ¿ ° ¶UZ ^ b{
(8) ^ ·» t0b ˘Ø‹Z x 22/fs(=499µs@fs=44.1kHz) w (GD) ¸j b{
(9) ^ ·» Æ w› x ATS bit p pV b{s8 x 1061/fs(=24ms@fs=44.1kHz) pb{

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3) LIN/RIN/MIN → HP-Amp, Lineout

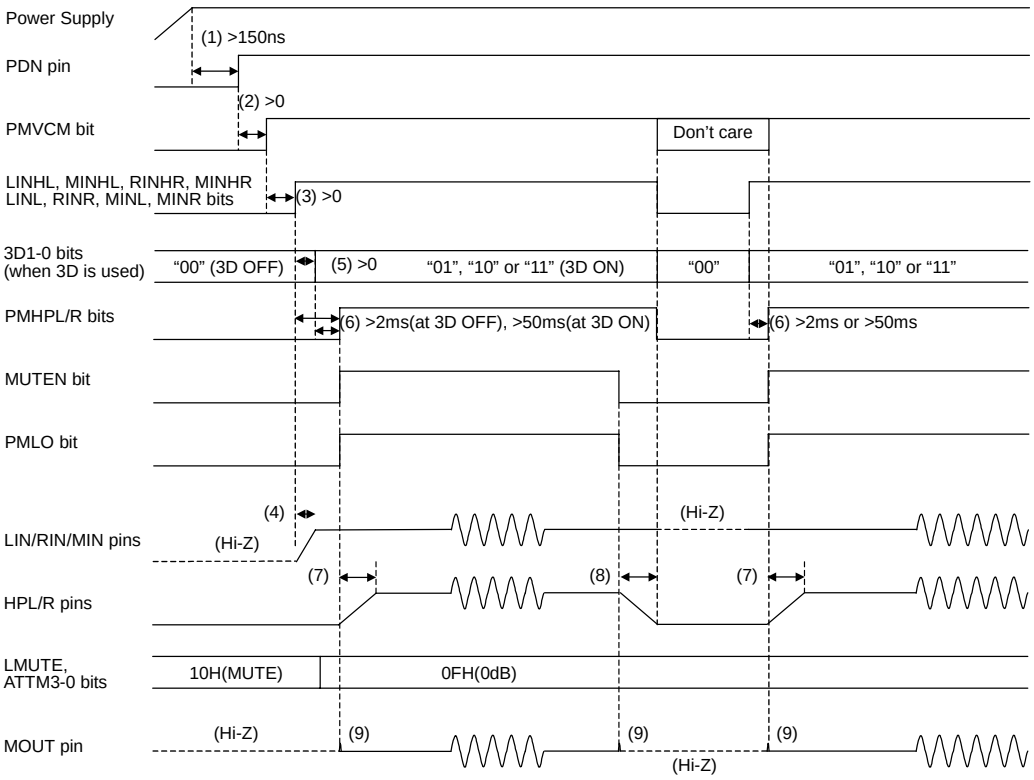

Figure 28. LIN/RIN/MIN, HP-amp S | LOUT/ROUT w´° ¿ …¢ ‡ ›
(Don't care: Hi-Z X)

(1) ?oqj´[z 150ns ´&loT PDN pin "H" t`o<^M{ DAC ;`sM øz⁄«Ø¿ «(MCLK, BICK, LRCK) x˘Apb{

(2) PDN pin "H" t`oT PMVCM bit t "1" {V p<^M{

(3) PMVCM bit t "1" {V pT LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V p<^M{

(4) LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V q LIN, RIN, MIN w⁄pin x0.475 x AVDD t ^ b{

(5) 3D ; ;b qVxz LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V pT 3D1-0bits t"01", "10" hx "11" {V pXi^M{ (Refer to Table 25)

(6) 3D ; ;`sM øxz LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V p 2ms ´(VCOM pin wfl ^ – 2.2µF w ø) &loT PMHPL, PMHPR, MUTEN, PMLO bits t "1" {V p<^M{ 3D ; ;b øz 3D1-0bits t"01", "10" hx "11" {V p 50ms ´&loT PMHPL, PMHPR, MUTEN, PMLO bits t "1" {V p<^M{

(7) ¿¯¥ wqj´U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj´U (t_r) x70k x C(typ) pb{ C=1µF w øz t_r x70ms(typ) pb{

(8) ¿¯¥ wqj<U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj<U (t_f) x60k x C(typ) pb{ C=1µF w øz t_f x60ms(typ) pb{
¿¯¥ U ¶tqj<UloT PMHPL, PMHPR bits t "0" {V zfw LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "0" {V p<^M{

(9) PMLO bit ~ 8Q q LOUT, ROUT pins t ¿ ° ¶UZ ^ b{

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■ ˝ ° ¿ …¢ ‡ › **(PLL Slave mode)**

1) DAC → HP-Amp

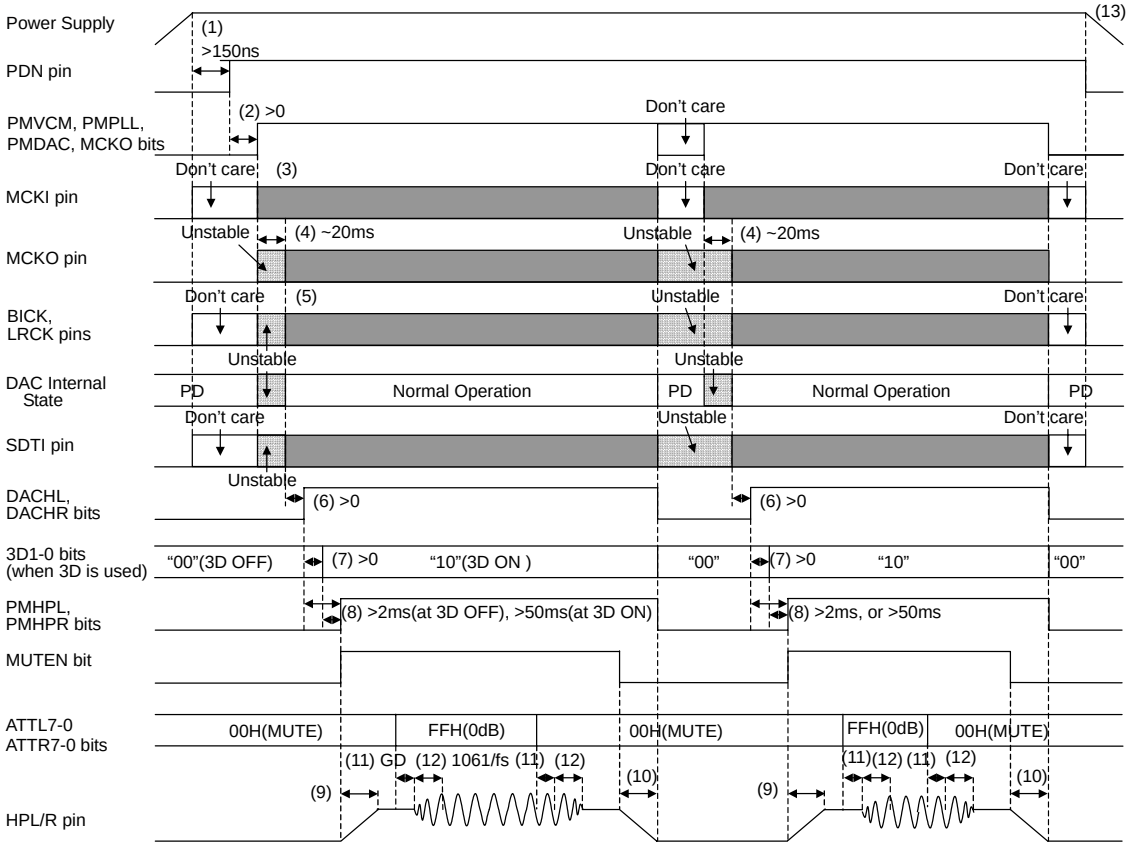

Figure 29. DAC S | HP-amp w ˝ ° ¿ …¢ ‡ › (Don't care: Hi-Z X)

(1) ?oqj˝[z 150ns ˝&loT PDN pin "H" t'o<^M{
(2) PDN pin "H" t'oT PMVCM, PMPLL, PMDAC, MCKO bits t"1" {V p<^M{
(3) MCKI pin t‡ ´ «Ø¿« b q PLL U ^ ' b{
(4) PLL wØ¿« x Table 1 { PLL UØ¿«b q MCKO pin T »«Ø¿«UZ ^ b{
(5) DAC w ^tx MCKO p *'h/«Ø¿« (BICK, LRCK) U Apb{ PMDAC bit = "0" w x/ «Ø¿« › \qUpV b{ ¿¯¥ x«Ø¿«U ^ oMsXo ^' b{
(6) PLL UØ¿«'oT DACHL, DACHR bits t"1" {V p<^M{
(7) 3D ; ;b qVxz DACHL, DACHR bits t"1" {V pT 3D1-0 bits t"10" {V pX i^M{
(8) 3D ; ;'sM øxz DACHL, DACHR bits t"1" {V p 2ms ˝(VCOM pin wfl ^ − 2.2µF w ø) &loT PMHPL, PMHPR, MUTEN bits t"1" {V p<^M{ 3D ; ;b ø xz3D1-0bits t"10" {V p 50ms ˝&loT PMHPL, PMHPR, MUTEN bits t"1" {V p< ^M{
(9) ¿¯¥ wqj˝U x MUTET pin wfl ^ − (C) p> z VCOM/2 pwqj˝U (t_r) x70k x C(typ) pb{ C=1µF w øz t_r x70ms(typ) pb{
(10) ¿¯¥ wqj<U x MUTET pin wfl ^ − (C) p> z VCOM/2 pwqj<U (t_f) x60k x C(typ) pb{ C=1µF w øz t_f x60ms(typ) pb{
¿¯¥ U ¶tqj<UloT PMHPL, PMHPR t"0" {V zfw DACL, DACR bits t"0" z 3D1-0bits t"00" {V p<^M{
(11) ^ ·» t0b ˘Ø‹Z x 22/fs(=499µs@fs=44.1kHz) w (GD) ¸j b{
(12) ^ ·» Æ w› x ATS bit p pV b{s8 x 1061/fs(=24ms@fs=44.1kHz) pb{
(13) ¿¯¥ U ¶tqj<UloT ?o OFF 'o<^M{

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2) DAC → Lineout

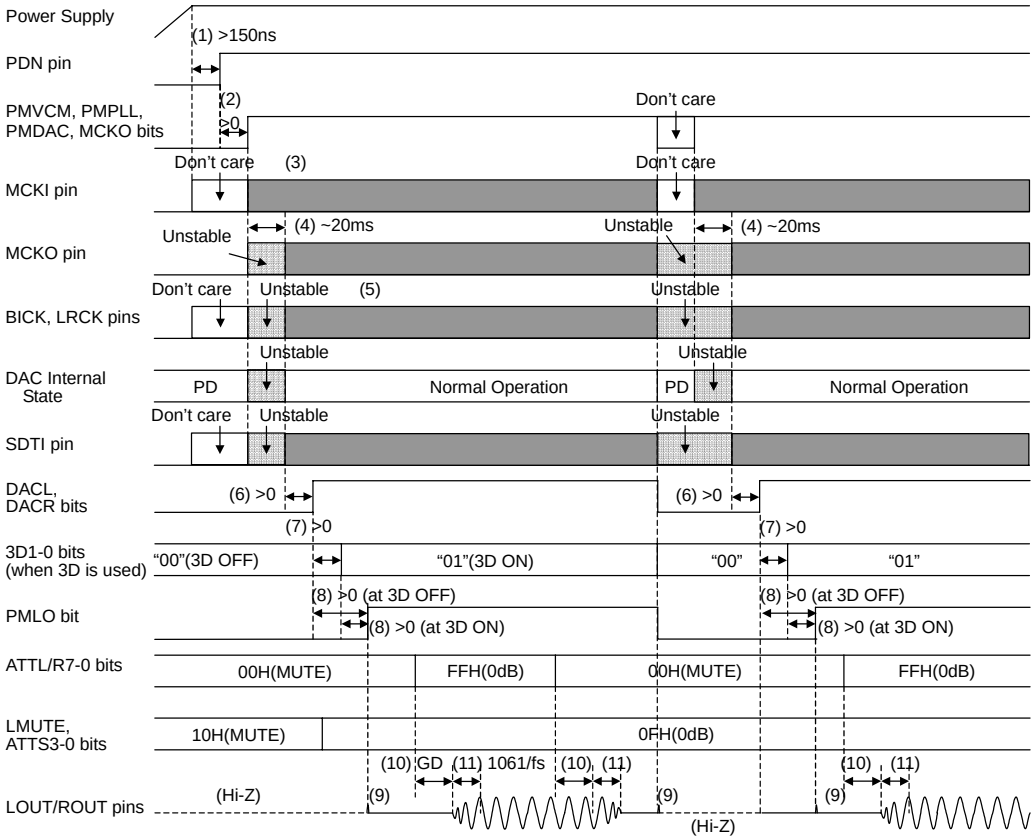

Figure 30. DAC S | Lineout w ˝ ° ¿ … ¢ ‡ › (Don't care: Hi-Z X)

(1) ? o q j ˝ [z 150ns ˝ & l o T PDN pin "H" t ' o < ^ M {
(2) PDN pin "H" t ' o T PMVCM, PMPLL, PMDAC, MCKO bits t "1" { V p < ^ M {
(3) MCKI pin t ‡ ´ « Ø ¿ « b q PLL U ^ ' b {
(4) PLL w Ø ¿ « x Table 1 { PLL U Ø ¿ « b q MCKO pin T » « Ø ¿ « U Z ^ b {
(5) DAC w ^ t x MCKO p * ' h ⁄ « Ø ¿ « (BICK, LRCK) U A p b { PMDAC bit = "0" w x ⁄ « Ø ¿ « › \ q U p V b { LOUT/ROUT Z x « Ø ¿ « U ^ o M s X o ^ ' b {
(6) PLL U Ø ¿ « ' o T DACL, DACR bits t "1" { V p < ^ M {
(7) 3D ; ; b q V x z DACL, DACR bits t"1" { V p T 3D1-0 bits t"01" { V p X i ^ M {
(8) PMLO bit t "1" { V p < ^ M {
(9) PMLO bit ~ 8 Q q LOUT, ROUT pins t ¿ ° ¶ U Z ^ b {
(10) ^ · » t 0 b ˘ Ø ‹ Z x 22/fs(=499µs@fs=44.1kHz) w (GD) ¸ j b {
(11) ^ · » Æ w › x ATS bit p p V b { s 8 x 1061/fs(=24ms@fs=44.1kHz) p b {

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3) LIN/RIN/MIN → HP-Amp, Lineout

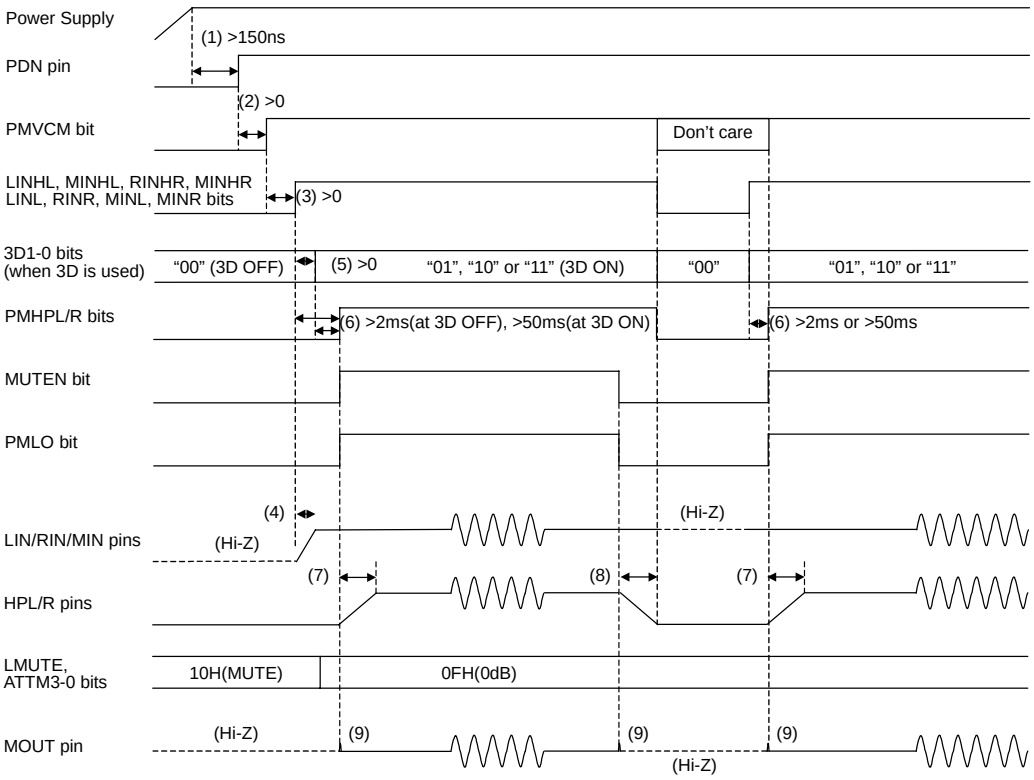

Figure 31. LIN/RIN/MIN, HP-amp S | LOUT/ROUT w´° ¿ …¢ ‡ ›
(Don't care: Hi-Z X)

(1) ?oqj´[z 150ns ´&loT PDN pin "H" t`o<^M{ DAC ;`sM øz⁄«Ø¿ «(MCLK, BICK, LRCK) x˘Apb{

(2) PDN pin "H" t`oT PMVCM bit t "1" {V p<^M{

(3) PMVCM bit t "1" {V pT LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V p<^M{

(4) LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V q LIN, RIN, MIN w⁄pin x0.475 x AVDD t ^ b{

(5) 3D ; ;b qVxz LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V pT 3D1-0bits t"01", "10" hx "11" {V pXi^M{ (Refer to Table 25)

(6) 3D ; ;`sM øxz LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V p 2ms ´(VCOM pin wfl ^ – 2.2µF w ø) &loT PMHPL, PMHPR, MUTEN, PMLO bits t "1" {V p<^M{ 3D ; ;b øz 3D1-0bits t"01", "10" hx "11" {V p 50ms ´&loT PMHPL, PMHPR, MUTEN, PMLO bits t "1" {V p<^M{

(7) ¿¯¥ wqj´U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj´U (t_r) x70k x C(typ) pb{ C=1µF w øz t_r x70ms(typ) pb{

(8) ¿¯¥ wqj<U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj<U (t_f) x60k x C(typ) pb{ C=1µF w øz t_f x60ms(typ) pb{

¿¯¥ U ¶tqj<UloT PMHPL, PMHPR bits t "0" {V zfw LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "0" {V p<^M{

(9) PMLO bit ~ 8Q q LOUT, ROUT pins t ¿ ° ¶UZ ^ b{

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■ AK4368 ˝ ° ¿ …¢ ‡ › (PLL Master Mode)

1) DAC → HP-Amp

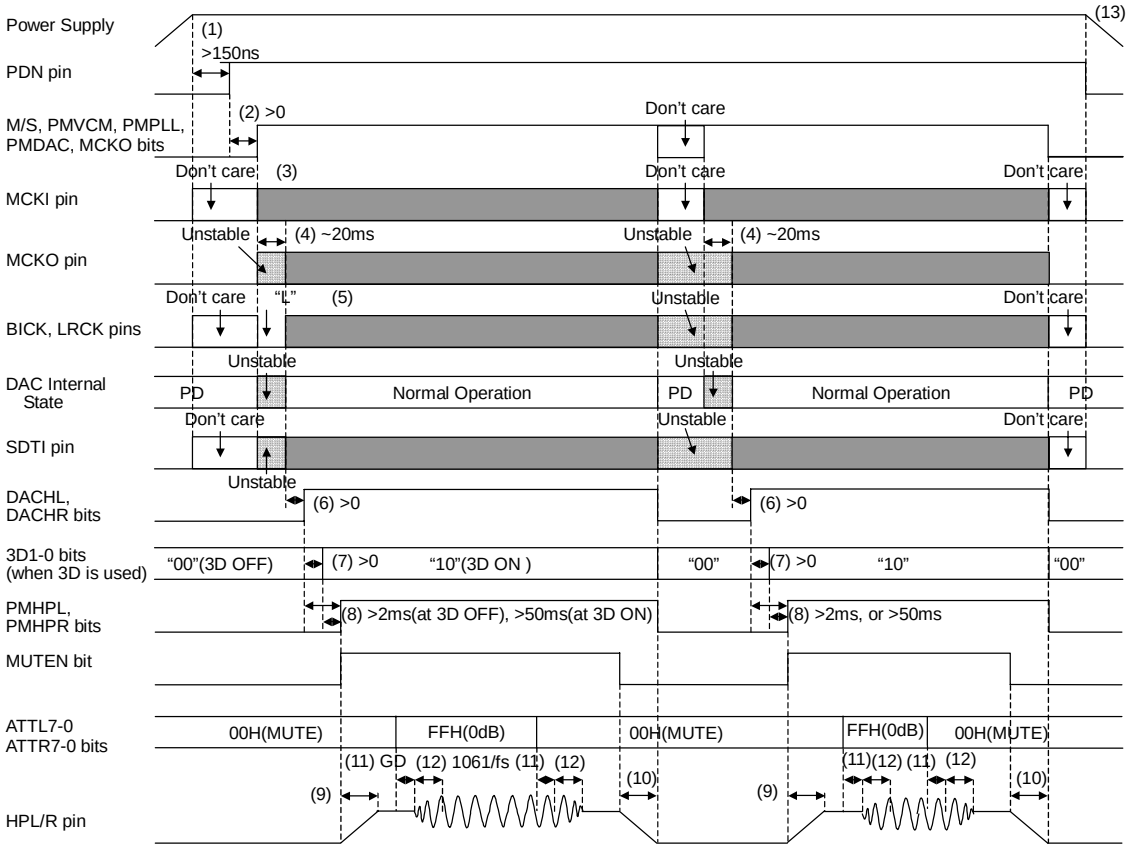

Figure 32 DAC S | HP-amp w ˝ ° ¿ …¢ ‡ › (Don't care: Hi-Z X)

(1) ?oqj˝[z 150ns ˝&loT PDN pin "H" t'o<^M{
(2) PDN pin "H" t'oT PMVCM, PMPLL, PMDAC, MCKO, M/S bits t "1" {V p<^M{
(3) MCKI pin t‡ ´ «Ø¿« b q PLL U ^ ' b{
(4) PLL wØ¿« x Table 1 { PLL UØ¿«b q BICK, LRCK, MCKO pin T ⁄«Ø¿« Z ^ b{
(5) PLL UØ¿«'oT DACHL, DACHR bits t "1" {V p<^M{
(6) 3D ; ;b qVxz DACHL, DACHR bits t"1" {V pT 3D1-0 bits t"10" {V pX i^M{
(7) 3D ; ;'sM øxz DACHL, DACHR bits t "1" {V p 2ms ˝(VCOM pin wfl ^ – 2.2µF w ø) &loT PMHPL, PMHPR, MUTEN bits t "1" {V p<^M{ 3D ; ;b ø xz3D1-0bits t"10" {V p 50ms ˝&loT PMHPL, PMHPR, MUTEN bits t "1" {V p<^M{
(8) ¿¯¥ wqj˝U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj˝U (t_r) x70k x C(typ) pb{ C=1µF w øz t_r x70ms(typ) pb{
(9) ¿¯¥ wqj<U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj<U (t_f) x60k x C(typ) pb{ C=1µF w øz t_f x60ms(typ) pb{
¿¯¥ U ¶tqj<UloT PMHPL, PMHPR t "0" {V zfw DACL, DACR bits t "0" z 3D1-0bits t"00" {V p<^M{
(10) ^ ·» t0b ˘Ø‹Z x 22/fs(=499µs@fs=44.1kHz) w (GD) ¸j b{
(11) ^ ·» Æ w› x ATS bit p pV b{s8 x 1061/fs(=24ms@fs=44.1kHz) pb{
(12) ¿¯¥ U ¶tqj<UloT ?o OFF 'o<^M{

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2) DAC → Lineout

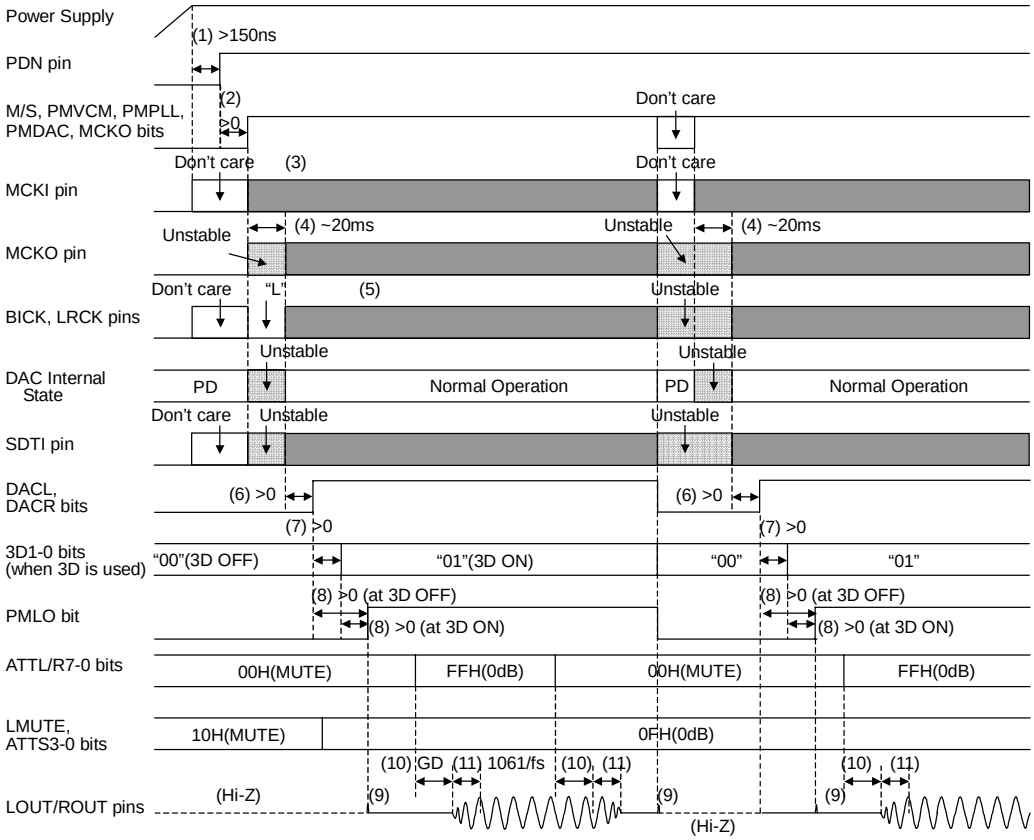

Figure 33. DAC S | Lineout w ˝ ° ¿ … ¢ ‡ › (Don't care: Hi-Z X)

(1) ? o q j ˝ [z 150ns ˝ & l o T PDN pin "H" t ' o < ^ M {
(2) PDN pin "H" t ' o T PMVCM, PMPLL, PMDAC, MCKO, M/S bits t "1" { V p < ^ M {
(3) MCKI pin t ‡ ´ « Ø ¿ « b q PLL U ^ ' b {
(4) PLL w Ø ¿ « x Table 1 { PLL U Ø ¿ « b q BICK, LRCK, MCKO pin T ⁄ « Ø ¿ « Z ^ b {
(5) PLL U Ø ¿ « ' o T DACL, DACR bits t "1" { V p < ^ M {
(6) 3D ; ; b q V x z DACL, DACR bits t "1" { V p T 3D1-0 bits t "01" { V p X i ^ M {
(7) PMLO bit t "1" { V p < ^ M {
(8) PMLO bit ~ 8 Q q LOUT, ROUT pins t ¿ ° ¶ U Z ^ b {
(9) ^ · » t 0 b ˘ Ø ‹ Z x 22/fs(=499µs@fs=44.1kHz) w (GD) ¸ j b {
(10) ^ · » Æ w › x ATS bit p p V b { s 8 x 1061/fs(=24ms@fs=44.1kHz) p b {

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3) LIN/RIN/MIN → HP-Amp, Lineout

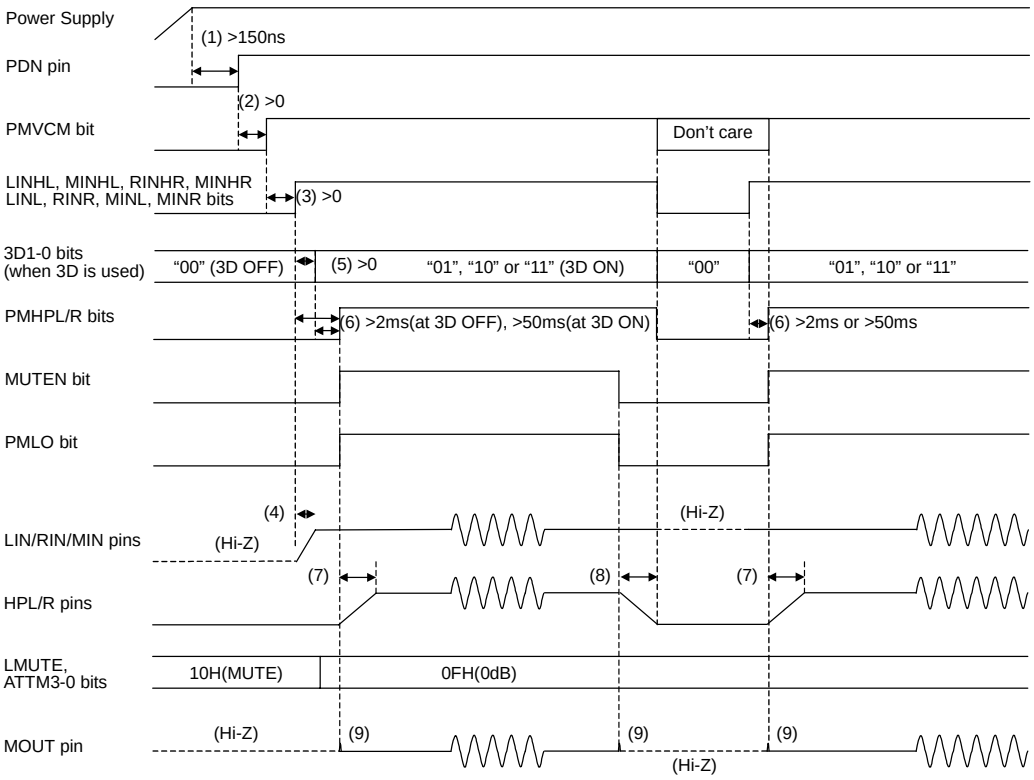

Figure 34. LIN/RIN/MIN, HP-amp S | LOUT/ROUT w´° ¿ …¢ ‡ ›
(Don't care: Hi-Z X)

(1) ?oqj´[z 150ns ´&loT PDN pin "H" t`o<^M{ DAC ;`sM øz⁄«Ø¿ «(MCLK, BICK, LRCK) x˘Apb{

(2) PDN pin "H" t`oT PMVCM bit t "1" {V p<^M{

(3) PMVCM bit t "1" {V pT LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V p<^M{

(4) LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V q LIN, RIN, MIN w⁄pin x0.475 x AVDD t ^ b{

(5) 3D ; ;b qVxz LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V pT 3D1-0bits t"01", "10" hx "11" {V pXi^M{ (Refer to Table 25)

(6) 3D ; ;`sM øxz LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "1" {V p 2ms ´(VCOM pin wfl ^ – 2.2µF w ø) &loT PMHPL, PMHPR, MUTEN, PMLO bits t "1" {V p<^M{ 3D ; ;b øz 3D1-0bits t"01", "10" hx "11" {V p 50ms ´&loT PMHPL, PMHPR, MUTEN, PMLO bits t "1" {V p<^M{

(7) ¿¯¥ wqj´U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj´U (t_r) x70k x C(typ) pb{ C=1µF w øz t_r x70ms(typ) pb{

(8) ¿¯¥ wqj<U x MUTET pin wfl ^ – (C) p> z VCOM/2 pwqj<U (t_f) x60k x C(typ) pb{ C=1µF w øz t_f x60ms(typ) pb{
¿¯¥ U ¶tqj<UloT PMHPL, PMHPR bits t "0" {V zfw LINHL, MINHL, RINHR, MINHR, LINL, MINL, RINR, MINR bits t "0" {V p<^M{

(9) PMLO bit ~ 8Q q LOUT, ROUT pins t ¿ ° ¶UZ ^ b{

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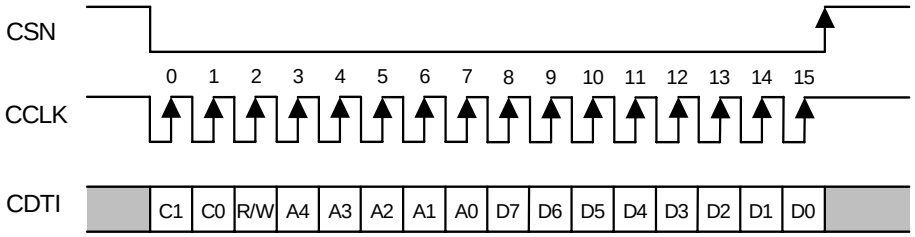
■ ‡ fl ˜ Ø » £

(1) 3 ¢ ‡ fl ˜ Ø ¯ (I2C pin = "L")

Ł · » x 3 ¢ ‡ I/F — : CSN, CCLK, CDTI p { V M b { I/F ˝ w ^ » x Chip address(2bits, "01" {), Read/Write(1bit, Fixed to "1", Write only), Register address(MSB first, 5bits), Control data(MSB first, 8bits) p ˇ R ^ b { ^ » x CCLK w q j ˝ U ⁄ ¿ · p b { ^ » w { V xCCLK w16 « Ø ¿ « Ł w q j ˝ U ⁄ ¿ · p fit s b { CCLK w « Ø ¿ « — ¯ x 5MHz(max) p b { PDN pin = "L" p Ł · » w x • ¿ ˜ ^ b {



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 35. 3 ¢ ‡ fl ˜ Ø I/F » ‹

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(2) I²C fl ~Ø - (I2C pin = "H")
AK4368 wI²C -w ¥ ¿~xz - (max:400kHz, Ver1.0) t0 'oM b{

(2)-1. WRITE ¸'
I²C -tSZ ^ »{V ‡ › x Figure 36 t ^ b{ ˝w IC w «• txz
7st E (Start Condition) ' b{ SCL U "H" w t SDA "H" T "L" tb qz
EU^ b (Figure 42) { Ew z Ł -Ł Uø ^ b{\w -Ł x 7bit T
˘R^ z 8bit Łtx^ »M†˘¿~ (R/W) U V b{˝ 6bit x "001000" { z˝w 1bit x «• b
IC ‹ h w -Ł ˘¿~pz CAD0 pin t ^ b (Figure 37) { -Ł U 'h øz
AK4368 x‹ t (Acknowledge) \R'z¸'U ^ b{ »x‹ t;w«Ø¿«˝
\R'z SDA rL'sZ ys d (Figure 43) {R/W ˘¿~U "0" w øx^ »{V z R/W
˘¿~U "1" w øx^ »¡ Z' M b{

H2 ~x- -Ł (Ł· » -Ł) pb{- -Ł x 8bit zMSB first p˘R^ z˝ 3bit x "0"
{ pb (Figure 38) {H 3 ~ æxfl ~Ø ^ »pb{fl ~Ø ^ »x 8bit zMSB first p˘R
^ b (Figure 39) {AK4368 xz/ ~w! b h|t‹ t \R' b{^ »8øxz
c »U\Rb › E (Stop Condition) t lo4 ' b{ SCL U "H" w t SDA
"L" T "H" tb qz › EU^ b (Figure 42) {

AK4368 x :w ~w^ » St{V \qUpV b{^ » 1 ~ølh z › E
ø c¸t^ » ø qz- -Ł U $t « ~^ z˝w^ »x˝w- -Ł
t¤ ^ b{ -Ł "0CH" Q ^ » ø qz" Ł· »t0 b -Ł §¢ »xØ
ƒ 'z -Ł "00H" T qt¤ ^ b{

«Ø¿«U "H" w xz SDA w 6x psZ ys d {^ » U "H" q"L" w p
6 !¸pV wxz SCL w«Ø¿« ŁU "L" w tv b (Figure 44) {SCL U "H" w
tSDA !¸b wxz Ez › E b qVw pb{

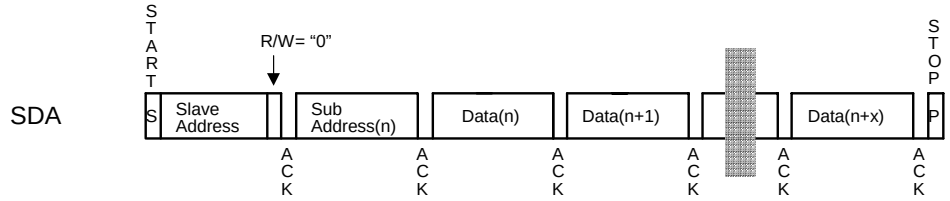

Figure 36. I²C -w^ »{V ‡ ›

0	0	1	0	0	0	CAD0	R/W

(CAD0 xpin t)
Figure 37. H1 ~w˘R

0	0	0	A4	A3	A2	A1	A0

Figure 38. H2 ~w˘R

D7	D6	D5	D4	D3	D2	D1	D0

Figure 39. H3 ~ æw˘R

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(2)-2. READ ¸'

R/W ˜¿˜U "1" w øz AK4368 xREAD ^ M b{ƒ ^ h ¯Ł w^ »UZ ^ h z
»U › E ø c‹ t \Rb qz– ¯Ł U $t « ˜^ z˝w ¯
Ł w^ » ¡ Zb\qUpV b{ ¯Ł "0CH" w^ » ¡ Z'h z^ t˝w ¯Ł
¡ Zb øtx ¯Ł "00H" w^ »U¡ Z^ b{

AK4368 x§Ł ˜ ¯Ł ¯q … ¯w 2 mw READ ¸' ¸loM b{

(2)-2-1. §Ł ˜ ¯Ł ¯
AK4368 x" t ¯Ł §¢ » ¸loS z §Ł ˜ ¯Ł ¯px\w§¢ »pƒ ^ h
¯Ł w^ » ¡ Z' b{" w ¯Ł §¢ »x7 t «• 'h ¯Ł w˝w ¯Ł
–¸'oM b{«Qyz7 t «• (READ p WRITE p) 'h ¯Ł U "n" pK zfw §Ł
˜ ¯Ł ¯ lh øz ¯Ł "n+1" w^ »U¡ Z^ b{§Ł ˜ ¯Ł ¯p
xz AK4368 xREAD ¸'w Ł ¯Ł (R/W = "1") w t0'o‹ t \R'z˝w«Ø¿«T
" w ¯Ł §¢ »pƒ ^ h^ » Z 'hwj" §¢ » 1m « ˜' bG^
»UZ ^ h J »U‹ t \Rdc › E ø qz READ ^x4 ' b{

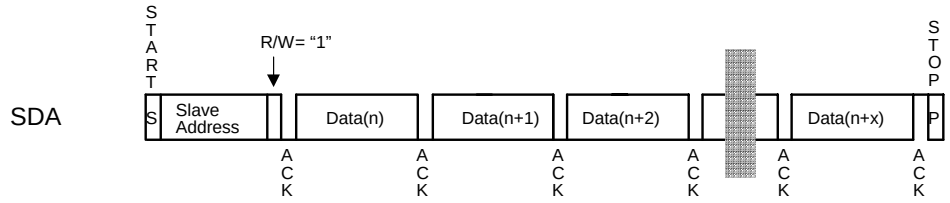

Figure 40. CURRENT ADDRESS READ ¸'

(2)-3-2. … ¯Ł ¯
… ¯Ł ¯t w ¯Ł w^ » ¡ Zb\qUpV b{ … ¯Ł
¯x READ ¸'w Ł ¯Ł (R/W bit= "1") b †tz… w WRITE ¸' b AUK
b{ … ¯Ł ¯px7st E 'z˝t WRITE ¸'w Ł ¯Ł (R/W =
"0") z¡ Zb ¯Ł q˝ ' b{ AK4368 U\w ¯Ł t0'o‹ t \R'h z6
ø Ez READ ¸'w Ł ¯Ł (R/W bit= "1") ' b{ AK4368 x\w Ł ¯Ł w
t0'o‹ t \R'zƒ ^ h ¯Ł w^ » Z 'z" ¯Ł §¢ » 1m «
˜' b{^ »UZ ^ h z »U «° ¿· \Rdc › E ø qz READ ^x4
' b{

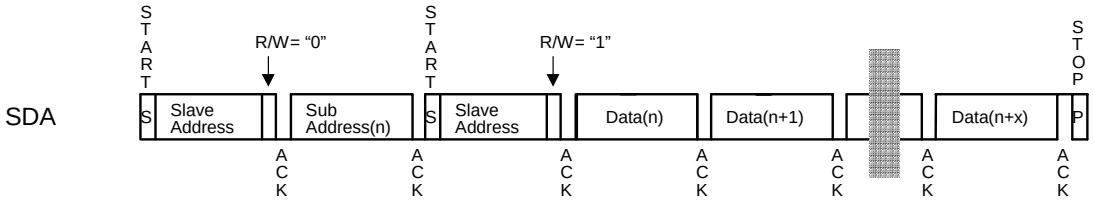

Figure 41. RANDOM ADDRESS READ ¸'

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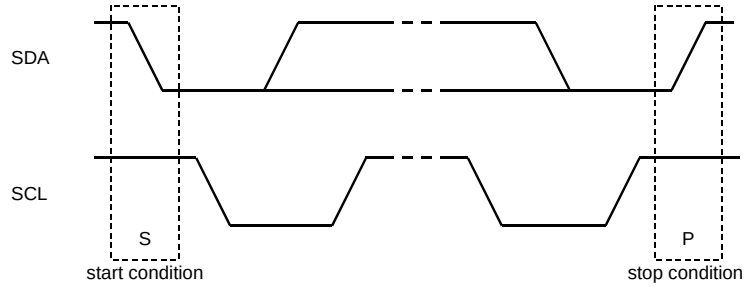

Figure 42. E q › E

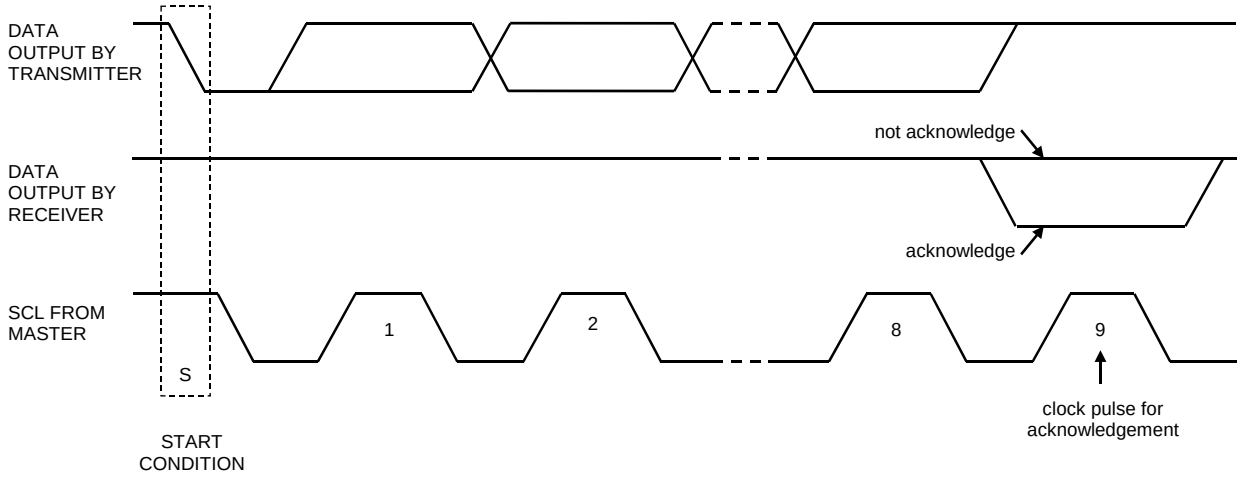

Figure 43. I²C p w ‹ t

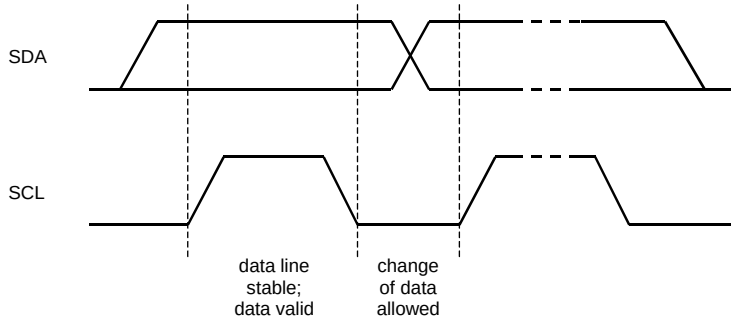

Figure 44. I²C p w ˘ ¿ ˜ 8 ø

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■ Ł· » ¿

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	Clock Control	0	0	M/S	MCKAC	BF	PS0	PS1	MCKO
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
07H	Headphone Out Select	0	HPG	MINHR	MINHL	RINHR	LINHL	DACHR	DACHL
08H	Lineout Select	0	LOG	MINR	MINL	RINR	LINL	DACR	DACL
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
0AH	ALC Mode Control 1	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0BH	ALC Mode Control 2	0	0	ALC	ROTM1	ROTM0	LMAT1	LMAT0	RATT
0CH	3D Control	0	0	0	0	DP1	DP0	3D1	3D0

PDN pin = "L" z¶Ł· »x{V ˇDpb{

PDN pin "L" tb qzŁ· » xs8=^ b{

0DH T 1FH px{V ˇDpb{

"0" pƒ ^ hˇ¿˜ w "1" w{V x—›pb{

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■ ˜I

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: VCOM w ″ ° · ˜
0: Power OFF (Default)
1: Power ON

PMDAC: DAC w ″ ° · ˜
0: Power OFF (Default)
1: Power ON
OFF T ON t ! ¸ ` h ø x ^ h ATT s w Ł · » w ″ 0 p ″ ° ¿ ^ b {

PMHPL: Lch ¿ ¯ ¥ w ″ ° · ˜
0: Power OFF (Default)
1: Power ON

PMHPR: Rch ¿ ¯ ¥ w ″ ° · ˜
0: Power OFF (Default)
1: Power ON

MUTEN: ¿ ¯ ¥ w Æ ˜ fl ˜ Ø
0: Æ ˜ (Default) { Z x HVSS(0V) t s b {
1: Ł ^ { Z w DC ? y x 0.475 x AVDD t s b {

PMLO: ´ Ł ƒ ¢ ˜ w ″ ° · ˜
0: Power OFF (Default) { Z x Hi-Z t s b {
1: Power ON

PMPLL: PLL w ″ ° · ˜
0: Power OFF: EXT mode (Default)
1: Power ON: PLL mode

\ w ¯ Ł w ˇ ¿ ˜ ON/OFF ¢ “1” /“0” £ b \ q p $ t ″ ° … ¢ b \ q U p V b {
h z PDN pin “L” t b \ q p z Ł · » w t c ¶ s ˇ S t ″ ° … ¢ p V b { \
w ø z Ł · » x s 8 = ^ b {
h z PMVCM, PMDAC, PMHPL, PMHPR, PMLO, PMPLL, MCKO bits b o “0” t b \ q p z ¶ s ˇ
S t ″ ° … ¢ b \ q U p V b { \ w q V Ł · » w ″ 0 x − ¸ ^ o M b { « ? v x
20µA(typ) s w p z ¶ t ‡ ¿ ˜ … ¢ (typ. 1µA) b t x PDN pin = “L” q ` o < ^ M {

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

FS3-0: − ‹ * : w ‹ R
PLL mode: Table 2
EXT mode: Table 6

PLL3-0: MCKI * : w ‹ R
PLL mode: Table 1
EXT mode: ` fi

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock Control	0	0	M/S	MCKAC	BF	PS0	PS1	MCKO
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MCKO: MCKO ł M ` b{
0: Disable (Default)
1: Enable

PS1-0: MCKO * :
PLL mode: Table 3
EXT mode: Table 7

BF: » ¯ w BICK * :w { Ł ¯ z\w˘¿˜x`fits b{
0: 32fs (Default)
1: 64fs

MCKAC: MCLK ¯
0: CMOS (Default)
1: AC S¿ ‹

M/S: » / Ł ¯
0: Ł ¯ (Default)
1: » ¯

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF2-0: ƒ ^ ƒ^ » » £ ¥ ¿˜w (Table 11)
Default: “010” (Mode 2)

LRP: LRCK ^Q (Ł ¯)
0: Ł (Default)
1: S8

BCKP: BICK ^Q (Ł ¯)
0: Ł (Default)
1: S8

MONO1-0: '‡ ‹ (Table 21)
Default: “00” (LR)

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	1

DEM1-0: ^ ⁄ ‡ »wR (Table 19)
Default: “01” (OFF)

BST1-0: ~ (Table 20)
Default: “00” (OFF)

SMUTE: DAC T Z ^ ^ » „ ~ Æ ~ ' b{
0: Ł ^ (Default)
1: DAC Z U„ ~ Æ ~^ b{

LMUTE: LOUT/ROUT T Z ^ łw Æ ~ (Table 24)
0: Ł ^{ ATTS3-0 bits p ^ hn0 pZ ^ b{
1: Mute {ATTS3-0 bits w tTT c Æ ~^ b{ (Default)

DATTC: ^ ·» Æ wfl ~Ø
0: Independent (Default)
1: Dependent
“0” pLch, Rch w^ ·» Æ qt ^^dz “1” pLch wATT t¨ 'o Rch wATT != ' b{'' DATTC bit = “1” w øz ATTR7-0 bit tx ATTL7-0 bit w x{V d {

ATS: ^ ·» Æ › (Table 18)
0: 1061/fs (Default)
1: 7424/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTL7-0: DACL T Z ^ łwn0 w (Table 17)
ATTR7-0: DACR T Z ^ łwn0 w (Table 17)
Default: “00H” (MUTE)

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Headphone Out Select	0	HPG	MINHR	MINHL	RINHR	LINHL	DACHR	DACHL
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACHL: DAC wLch w Z ł ¿ ¯ ¥ w Lch t C ` b {
0: OFF (Default)
1: ON

DACHR: DAC wRch w Z ł ¿ ¯ ¥ w Rch t C ` b {
0: OFF (Default)
1: ON

LINHL: LIN pin T ^ h ł ¿ ¯ ¥ w Lch t C ` b {
0: OFF (Default)
1: ON

RINHR: RIN pin T ^ h ł ¿ ¯ ¥ w Rch t C ` b {
0: OFF (Default)
1: ON

MINHL: MIN pin T ^ h ł ¿ ¯ ¥ w Lch t C ` b {
0: OFF (Default)
1: ON

MINHR: MIN pin T ^ h ł ¿ ¯ ¥ w Rch t C ` b {
0: OFF (Default)
1: ON

HPG: DAC → HPL/R Gain
0: +0.76dB (Default)
1: +6.76dB

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Lineout Select	0	LOG	MINR	MINL	RINR	LINL	DACR	DACL
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACL: DAC wLch w Z ł LOUT Z t C ` b{
0: OFF (Default)
1: ON

DACR: DAC wRch w Z ł ROUT Z t C ` b{
0: OFF (Default)
1: ON

LINL: LIN pin T ^ h ł LOUT Z t C ` b{
0: OFF (Default)
1: ON

RINR: RIN pin T ^ h ł ROUT Z t C ` b{
0: OFF (Default)
1: ON

MINL: MIN pin T ^ h ł LOUT Z t C ` b{
0: OFF (Default)
1: ON

MINR: MIN pin T ^ h ł ROUT Z t C ` b{
0: OFF (Default)
1: ON

LOG: DAC → LOUT/ROUT Gain
0: 0dB (Default)
1: +6dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTS3-0: LOUT/ROUT T Z ^ ł w n 0 w (Table 24)
Default: LMUTE bit = “1”, ATTS3-0 bits = “0000” (MUTE)

ATTS3-0 bit w x LMUTE bit U “0” w q V t fi t s b{

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Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Mode Control 1	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

REF7-0: ALC § ^ w , j w , 0.375dB step, 81 level, Default: “91H” (Table 15)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 2	0	0	ALC	ROTM1	ROTM0	LMAT1	LMAT0	RATT
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

RATT: ALC § fi ´ ¿ (Table 14)

LMAT1-0: ALC ¿ » ATT ´ ¿ (Table 13)

ROTM1-0: ALC § 4 ; , , Ø « Ø » ¢ ˜ (Table 12)

ALC: ALC
0: ALC Disable (Default)
1: ALC Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	3D Control	0	0	0	0	DP1	DP0	3D1	3D0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

3D1-0: 3D Stereo Enhancement Enable (Table 25)
Default: “00” (Disable)

DP1-0: 3D Depth (Table 26)
Default: “00” (0%)

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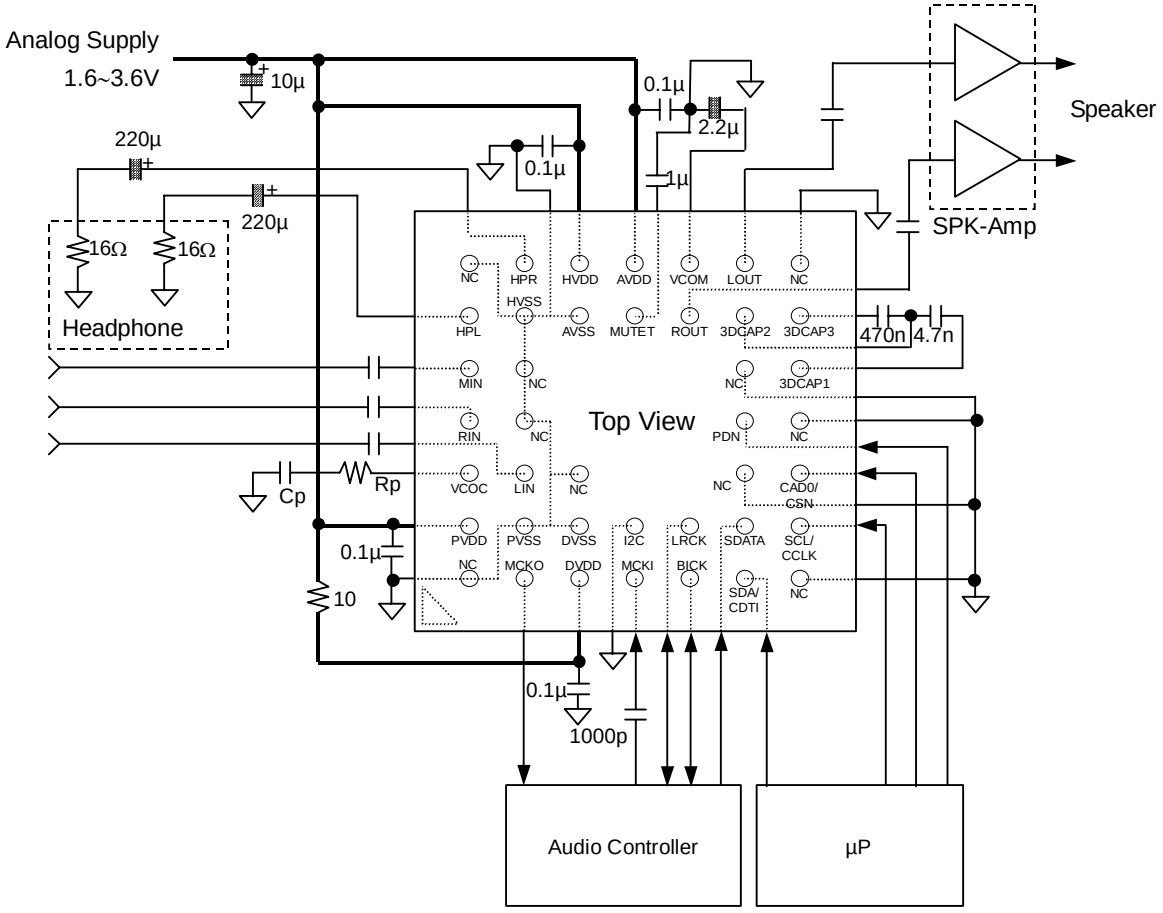
‡ ´ –

‡ ´ « Figure 45 t ` b{Ø.$ss˘mMox A; ¯ `o<^M{



«:

- AK4368 wAVSS, PVSS, DVSS, HVSS q*%fl ˜Ø sw‹ ¯x Zo ¢`o<^M{
- ^ ·» – xƒ t`sMp<^M{
- EXT ¯ (PMPLL bit = “0”) w øz VCOC pin xƒ p˘M d {
- PLL ¯ (PMPLL bit = “1”) w øz Cp qRp xTable 1 w Ot`o<^M{
- » ¯p ;b øz M/S bit t “1” U{V pz AK4368 wLRCK, BICK pins x Ø ´ ‹w 6pb{fwh z AK4368 wLRCK, BICK pins t100kΩ Sw ¿ K Mx …¢ ¯ AUK b{

Figure 45. ‡ ´ $ (MCLK tAC §¿ ‹p `h ø)

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1. ‹ ¯q?ow^§¿ ‹

?oq‹ ¯w MtxG « 'o<^M{Ł z AVDD, PVDD, HVDD x‡ ´ w ˘Ø‹?oz DVDD tx AVDD T 10Ω w‡ ¶ ¯ Ł'h‡ ´ w ˘Ø‹?o ' b{ AVDD qDVDD U ?op ^ øp z?oqj˝[‡ › b AxK d { AVDD qHVDD ?op b øz AVDD xHVDD q hx tqj˝[o<^M{ hz?o OFF xz HVDD q hx tqj<[o<^M{ PVDD x?oqj˝[‡ › b AxK d { AVSS, DVSS, PVSS, HVSS x‡ ´ w ˘Ø‹‹ ¯t 'o<^M{ ‡ ´ w‹ ¯x ˘Ø‹q^ ·» p Zo ¢'z PC ¯˝w?ot Mq\ p 'o<^M{ 0 w^§¿ ‹fl ^ -xs X?o— w Xt 'o<^M{

2. ,j?y

AVDD t ^ ?yU ˘Ø‹Z Ł · ' b{Ł AVDD xAVSS qw t 0.1µF w• ¿ «fl ^ - ' b{ VCOM x0.475 x AVDD ?y (typ) Z 'oS z ˘Ø‹ łwfl ?yq 'o b{\w— t * ° ¶ b h t 2.2µF Sw?rfl ^ - AVSS qw t 'o<^M{ hz VCOM pin T ?v qloxMZ d {^ ·» łz t«Ø¿«x!—+ w§¿ ‹ Z h z AVDD pin S | VCOM pin T pV iZm'o<^M{

3. ˘Ø‹Z

DAC Z x‡ ‹ ⁄ ¯tsloS zZ Ł ·x VCOM ?y ⁄œtz ¿¯ ¥ wZ Ł ·x VCOM ?y ⁄œt 0.47xAVDD(typ)@–3dBFS zLOUT/ROUT wZ Ł ·x VCOM ?y ⁄œt 0.61xAVDD(typ)@0dBFS pb{ fl ¯w ¥ ¿˜x 2's fl ˜ (2w4:)pz7FFFFFH(@24bit) t0'oxYw › z 800000H(@24bit) t0'ox w › z 000000H(@24bit) pwg xVCOM ?yUZ ^ b{ ΔΣ !—+UC\b 3‹ ° ¶ (‡£ — ‹ ° ¶)U>ts øxz ˙Zw »pn0^do<^M{

˘Ø‹Z x VCOM+ :mV Sw DC ƒ •¿˜ ¸mh zŁ w ;pxfl ^ -p DC R §¿ ˜' b{

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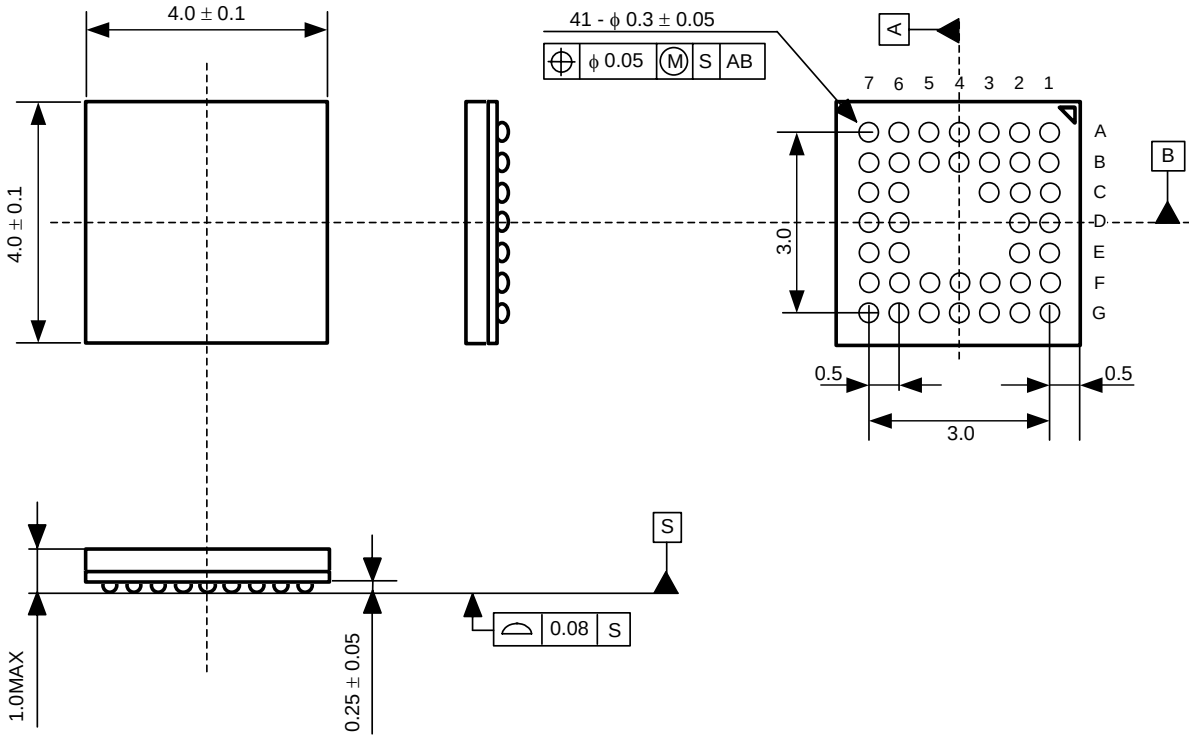
˝ ¿ › ·



■ P ~ ¿' 7

˝ ¿ › ·P : ⁄ '‡%%·
» † P : BT Ł·
R> P : SnAgCu

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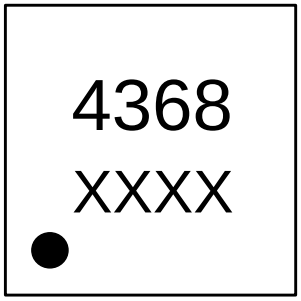
' ‹



XXXX: Date code (4 digit)
Pin #1 indication

~ d″

Date (YY/MM/DD)	Revision	Reason	Page	Contents
05/08/29	00	s [		
05/08/31	01	G \ ! ¸	5	fl ? y — fiAVSS pin q w t 2.2µF w ? r fl ^ – q 0.1µF w • ¿ « fl ^ – ' b { fl → fiAVSS pin q w t 2.2µF w ? r fl ^ – ' b { fl
			55	2. , j ? y fi \ w — t * ° ¶ b h t 2.2µF S w ? r fl ^ – q » t 0.1µF w • ¿ « fl ^ – AVSS q w t ' o < ^ M { fl → fi \ w — t * ° ¶ b h t 2.2µF S w ? r fl ^ – AVSS q w t ' o < ^ M { fl

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OAs« ˜

- {tGL^ ha…zt|za…w 7tmV ‘oxza…~‡wh t’ sX!¸b \ qUK b{HM ‘oz] ; U|wMtxz {t L‘h CU7 w wpK \q rpzK Mx 3 rpt]‹ <^M{
- {t L^ h C~$ w ;tI…‘hH~ wt b Vz» t Vzfw wV bt0b ı tmV ‘oxzp xfwy O wpxK d wpz] <^M{
- {GLa…Uz 8t|z u gOt tœ¿ (¿)t pb øz Zb Mt Ot,nX Z DU Apb{
- ' ;+z ¶ z ƒ;;+zj M ;;+srzfw ~;+w ¸ ^˘ Uz hx cz\¸z .zR s OGs t b\qUŁ ’ ^ Os^ o M TQ A{^ ;Mt a… ;^ øxz c˜†t Efl w{ t S <^M{
- \w { ct\O‘h;Mt a… ;^ h øz xzfw ;T \c swy ~ O wpxK d wp] <^M{
- Sl7w8 st \w« ˜ w O ct˝G;Mt a…U ;^ zfw ;T sU\ah øx¶oSl7to] r hx4 ‘o V bwp] <^M {

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