

Active SCSI Terminator

GENERAL DESCRIPTION

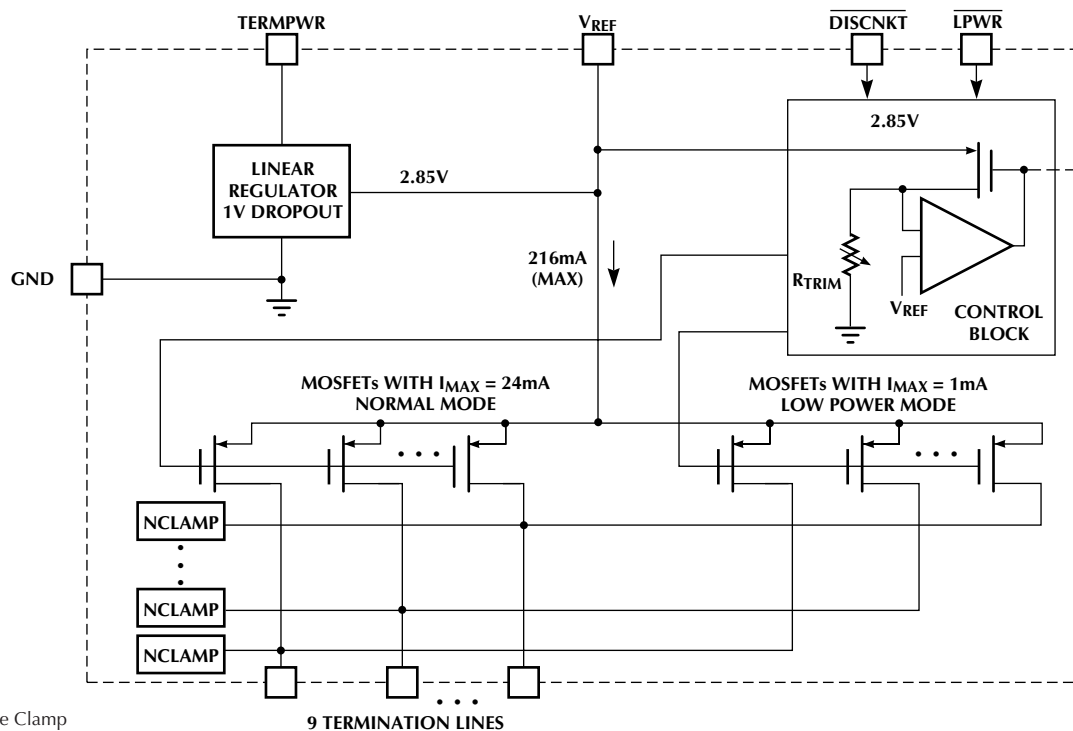
The ML6509 BiCMOS SCSI terminator provides active termination in a SCSI system with single ended drivers and receivers, in full compliance with the SCSI-1, SCSI-2 and SCSI-3 recommendations. It provides a 2.85V reference through an internal 1V dropout linear regulator. Active SCSI termination helps the system designer to effectively control analog transmission line effects like ringing, noise, crosstalk, ground bounce, etc. In addition it provides greater immunity to voltage drops on the TERMPWR line of the SCSI bus. The desired V-I characteristics for signal negation requires that the terminator source 0–24mA while maintaining 2.85V and for signal assertion preferably follow a linear slope of 110Ω. The ML6509 attempts to provide a V-I characteristic optimized to minimize the transmission line effects during both signal assertion and negation, using a MOSFET based architecture. The desired V-I characteristic is achieved by trimming one resistor in the control block. It provides negative clamping for signal assertion transients and current sink capability, to handle active negation driver overshoots above 2.85V, which is currently accomplished with external components in SCSI subsystems today. It provides a disconnect mode, where the terminator is completely disconnected from the SCSI bus and the output capacitance is < 5pF, typically.

FEATURES

- Fully monolithic IC solution providing active termination for 9 lines of the SCSI bus
- Low dropout voltage (1V) linear regulator, trimmed for accurate termination current, with 300mA current source capability
- Output capacitance typically <5pF
- Disconnect mode — logic pin to disconnect terminator from the SCSI bus, <100μA
- Lowpower mode — for power conscious, portable system & peripheral applications, using less than 6" cables. (Equivalent to a 1mA current drive with a 2.5kΩ termination)
- Current sinking — can sink current >10mA per line to handle active negation driver overshoots above 2.85V
- Negative clamping on all lines to handle signal assertion transients
- Regulator can source 200mA and sink 50mA while maintaining regulation
- Current limit & thermal shutdown protection
- Small and low profile package options; 16-pin SOIC (300 mil), 20-pin TSSOP (1 mil height)

* Some Packages Are End Of Life As Of August 1, 2000

BLOCK DIAGRAM

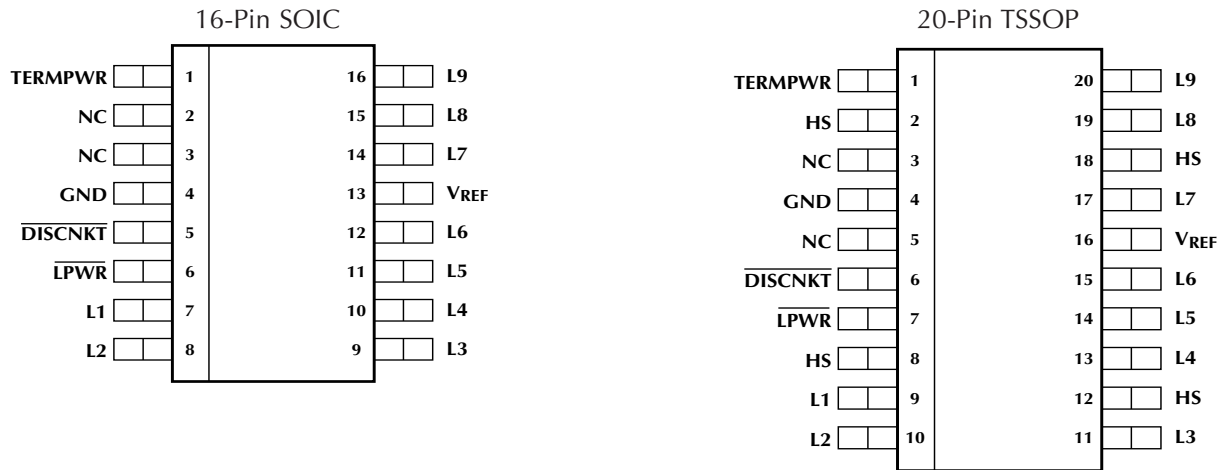


GENERAL DESCRIPTION (Continued)

One unique feature of the ML6509 is its support for a Low Power mode, for use in Notebook and portable computer applications, where it provides a 1mA (approximately 2.5K Ω termination) for less than 6" cable lengths. This minimizes the battery drain significantly in such systems.

Current limiting and thermal shutdown protection are also provided. The nine line configuration is optimal for wide SCSI's 18, 27, or 45 line termination needs.

PIN CONFIGURATION



PIN DESCRIPTION

NAME	DESCRIPTION
TERMPWR	Termination Power. Should be connected to the SCSI TERMPWR line. A 10 μ F tantalum local bypass capacitor is recommended per system, as shown in the application diagram
L1	Signal Termination 1. SCSI bus line 1
L2	Signal Termination 2. SCSI bus line 2
L3	Signal Termination 3. SCSI bus line 3
L4	Signal Termination 4. SCSI bus line 4
L5	Signal Termination 5. SCSI bus line 5
L6	Signal Termination 6. SCSI bus line 6
L7	Signal Termination 7. SCSI bus line 7
L8	Signal Termination 8. SCSI bus line 8
L9	Signal Termination 9. SCSI bus line 9

NAME	DESCRIPTION
V _{REF}	2.85V _{REF} Output. External decoupling with a 10 μ F tantalum in parallel with a 0.1 μ F ceramic capacitor is recommended, as shown in the application diagram.
DISCNKT	Disconnect Terminator. Logic input to disconnect the terminator from the bus when the SCSI device no longer needs termination due to not being the last device on the bus or otherwise. Active low input.
LPWR	Low Power Mode. Logic input to switch the terminator mode to a ~2.5k Ω termination, with a 1mA drive capability, meant for power conscious battery applications which use SCSI devices supporting cable lengths less than six inches. Active low input.
GND	Ground. Signal Ground (0V)
HS	Heat Sink Ground. Should be connected to GND.

NOTE: The DISCNKT and LPWR lines have 200k Ω internal pullup resistors connected to the supply. These pins should be left floating for normal operation and should be connected to ground to enable the function.

ABSOLUTE MAXIMUM RATINGS

Signal Line Voltage.....	-0.3 to TERMPWR +0.3V
Regulator Output Current.....	-100 to 300mA
TERMPWR Voltage.....	-0.3 to 7V
Storage Temperature	-65°C to 150°C
Soldering Temperature	260°C for 10 sec
Thermal Impedance (θ_{JA})	
SOIC	95°C/W
TSSOP	110°C/W

OPERATING CONDITIONS

TERMPWR Voltage.....	4V to 5.25V
Operating Temperature	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for 4V - TERMPWR - 5.25V, and $T_A = 0^\circ\text{C}$ to 70°C (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
TERMPWR Supply Current	L1-L9 = open, $\overline{\text{DISCNKT}}$ = open		3.5	5	mA
	L1-L9 = 0.2 V, $\overline{\text{DISCNKT}}$ = open		225	250	mA
	$\overline{\text{DISCNKT}}$ = 0 (active)		70	100	μA
$\overline{\text{DISCNKT}}$					
Input Low Voltage	$\overline{\text{LPWR}}$, $\overline{\text{DISCNKT}}$			1.0	V
Input High Voltage	$\overline{\text{LPWR}}$, $\overline{\text{DISCNKT}}$	TERMPWR -1.0			V
OUTPUT					
Output High Voltage	Measuring each signal line while other eight are high	2.8	2.85	2.9	V
Maximum Output Current (Normal Mode)	$V_{\text{OUT}} = 0.2\text{V}$, Measuring each signal line while the other eight are high	20		24	mA
Maximum Output Current (Lowpower Mode)	$V_{\text{OUT}} = 0.2\text{V}$, $\overline{\text{LPWR}} = 0$, and measuring each signal line while the other eight are high	0.8	1	1.2	mA
Output Clamp Level	$I_{\text{OUT}} = -30\text{mA}$	-0.15	0	0.15	V
Current Sink Capability	$V_{\text{OUT}} = 3.2\text{V}$ (per line)	7	12		mA
Output Capacitance (ML Method)	L1 thru L9, $\overline{\text{DISCNKT}} = 0$ 2V _{P-P} 100kHz square wave applied biased at 1V D.C.		4	5	pF
Output Capacitance (X3T9.2/855D method)	L1 thru L9, $\overline{\text{DISCNKT}} = 0$ 0.4V _{P-P} , 1MHz square wave applied biased at 0.5V D.C.		6	7	pF
REGULATOR					
Output Voltage	Sourcing 0-200mA	2.8	2.85	2.9	V
	Sinking 0-50mA	2.8	2.85	2.95	V
Dropout Voltage	L1-L9 = 0.2V, $V_{\text{OUT}} = 2.85\text{V}$		1.0	1.2	V
Short Circuit Current	Regulator output = 0V		100		mA
	Regulator output = 5V		300		mA
Thermal Shutdown			170		°C

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

FUNCTIONAL DESCRIPTION

The SCSI terminator helps in decreasing the transmission line effects with precise termination. Termination is conventionally provided at the beginning and end of the SCSI bus, however when additional peripherals are added, the termination needs to be disabled from the current device and enabled on the last device on the bus. Existing termination schemes use a SIP (Single-In-Line package) which is plugged into a socket on the PC board of the SCSI peripheral. To remove the termination, the user needs to pull the resistor SIP out of its socket. With the higher levels of system integration, this is no longer a simple task. With the increasing use of higher data rates and cable lengths in SCSI subsystems, the need for active termination is becoming necessary. Active termination also minimizes power dissipation and can be activated or deactivated under software control, thus eliminating the need for end user intervention. The V-I characteristics of popular SCSI termination schemes are shown in Figure 3. Theoretically the desired V-I characteristics are the Boulay type for signal assertion (high to low) and the Ideal type for signal negation. The ML6509 with its MOSFET based nonlinear termination element attempts to provide the most optimum V-I characteristics — optimized for both signal assertion and negation.

The ML6509 provides active termination for nine signal lines, thus accommodating basic SCSI which requires 18 lines to be terminated and wide SCSI which requires 27, 36 or 45 lines to be terminated. The ML6509 integrates an accurate voltage reference (1V dropout voltage) and nine MOSFET based termination lines. A single internal resistor is trimmed to tune the V-I characteristic of the MOSFETs as shown in figure 1. The voltage reference circuit produces a precise 2.85V level and is capable of sourcing at least 24mA into each of the nine terminating lines when low (active). When the signal line is negated (driver turns off), the terminator pulls the signal line to 2.85V (quiescent state). When all signal lines are inactive, the regulator will source about 200mA.

The ML6509 SCSI Terminator provides two control signals, $\overline{\text{DISCNKT}}$ & $\overline{\text{LPWR}}$ which are active low signals and have an internal 200k Ω pull-up resistor. The $\overline{\text{DISCNKT}}$ input when asserted low, isolates the ML6509 from the signal lines and effectively removes the terminator from the SCSI bus with a disconnect mode current of less than 100 μA . The $\overline{\text{LPWR}}$ input, when asserted low, puts the ML6509 in the low power termination mode by providing only a 1mA drive capability with an effective termination impedance of 2.5k Ω . This is intended for power conscious portable systems and peripheral applications where the cable lengths are small, thus resulting in fast signal transitions and practically no transmission line effects, while consuming minimum power (9mA worst case if all lines were active). At the same time, if this portable system were connected with an external SCSI peripheral, over a long cable, the normal terminator mode could be enabled to ensure compliance with the SCSI standard and maintain data integrity. In addition the ML6509 provides for negative clamping of signal transients and also supports current sink capability in excess of 10mA per signal line to handle active negation driver overshoot above 2.85V, a common occurrence with SCSI transceivers. These functions need to be handled with external components in SCSI subsystems today. Thus the ML6509 helps in eliminating a number of external components.

Disconnect mode capacitance is a very critical parameter in SCSI systems. The ML6509 provides the lowest capacitance contribution of maximum 5pF which is guaranteed by production test.

Figure 2 gives an application diagram showing a typical SCSI bus configuration. To ensure proper operation, the TERMPWR pin must be connected to the SCSI TERMPWR line. Each ML6509 requires parallel 0.1 μF and 10 μF capacitors connected between V_{REF} and GND pins and the TERMPWR line needs a 10 μF bypass capacitor per SCSI system.

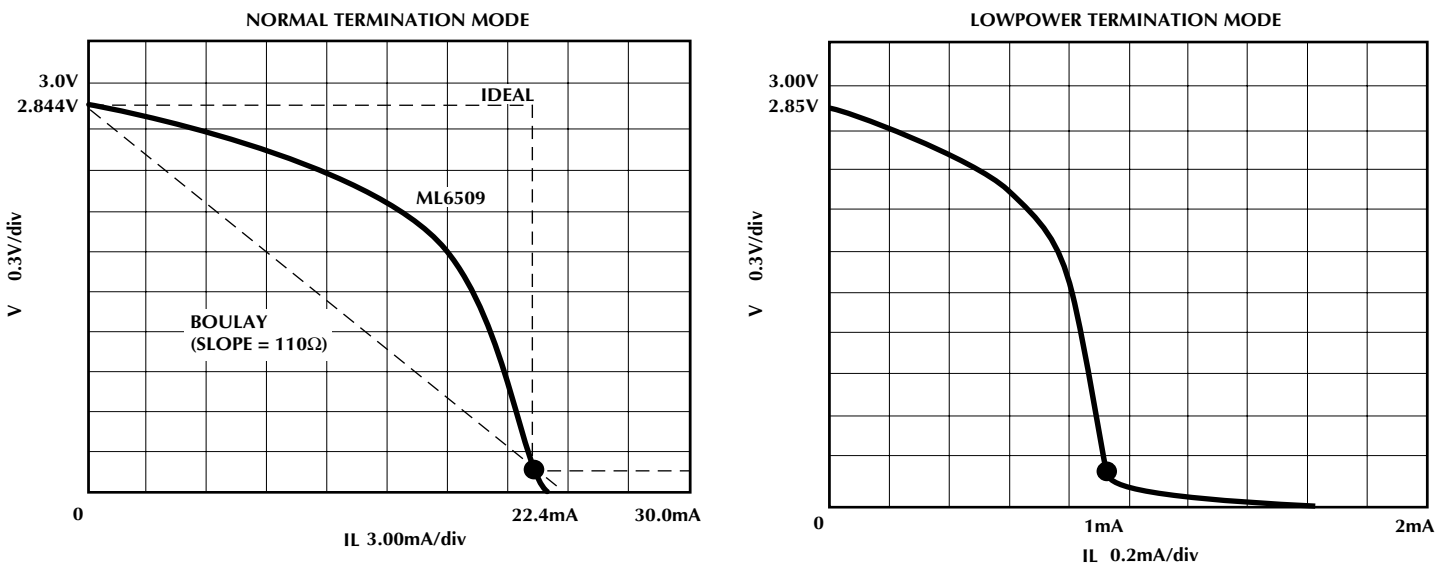


Figure 1. Trimmed V-I Characteristic of the ML6509

Thus in an 8-bit wide SCSI bus arrangement ("A" cable), two ML6509s would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. 16-bit wide SCSI would use three ML6509s, while 32-bit wide SCSI bus would require five ML6509s.

In a typical SCSI subsystem, the open collector driver in the SCSI transceiver, when asserted, pulls low and when negated, the termination resistance serves as the pull-up. Shown in figure 2 is a typical cable response to a pulse. The receiving end of the cable will exhibit a single time delay. When negated, the initial step will reach an intermediate level defined as V_{STEP} . With the higher SCSI data rates, sampling could occur during this step portion. In order to get the most noise margin, the step needs to be as high as possible to prevent false triggering. For this reason the regulator voltage and the resistor defining the MOSFETs characteristic is trimmed to ensure that the I_O is as close as possible to the SCSI max current specification. V_{STEP} is defined as follows :

$$V_{STEP} = V_{OL} + (I_O \times Z_O)$$

where

- V_{OL} is the Driver output low voltage,
- I_O is current from receiving terminator
- Z_O is characteristic impedance of cable.

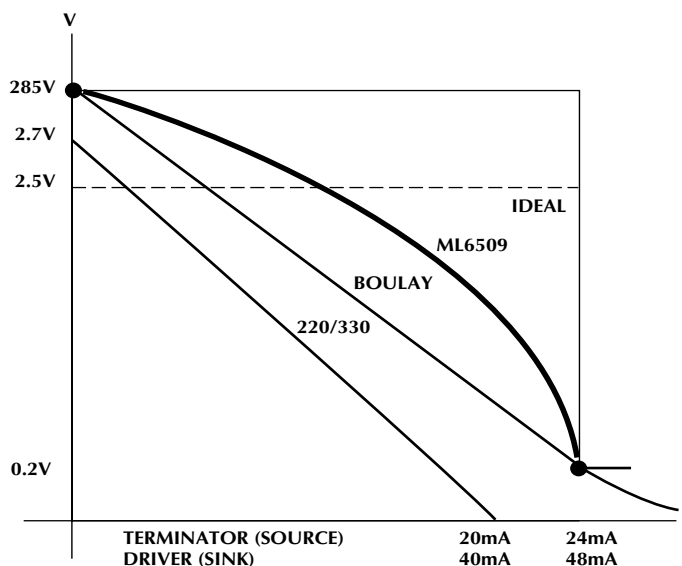


Figure 3. V-1 Characteristics of Various SCSI Termination Schemes

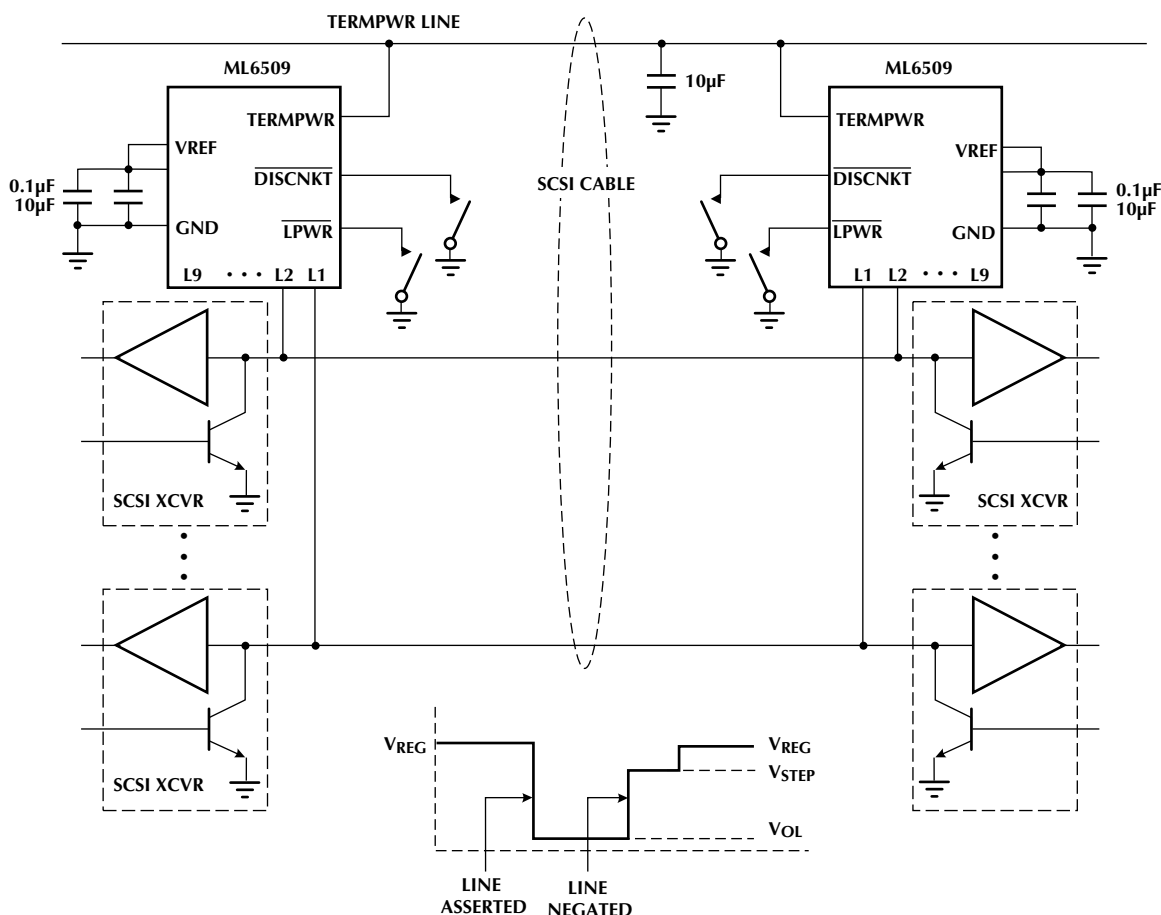


Figure 2. Application Diagram Showing Typical SCSI Bus Configuration with the ML6509

This is a very important characteristic that the terminator helps overcome by increasing the noise margin and boosting the step as high as possible. This capability for the ML6509 implementation is illustrated in the attached simulation graphs which show the terminator performance under different cable impedance situations and a comparison is shown with the standard Boulay terminator, under identical conditions.

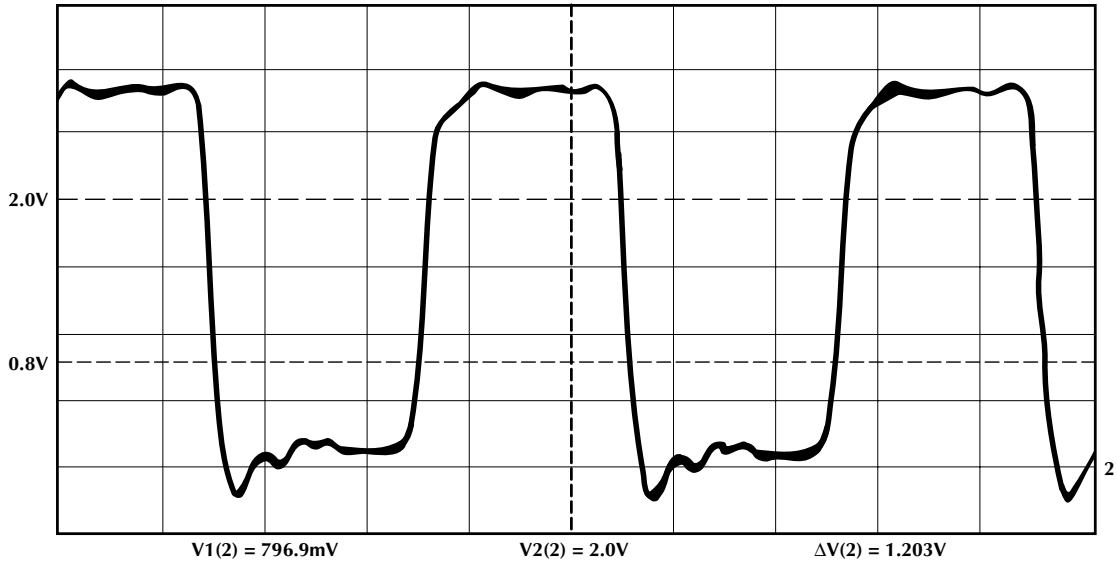


Figure 4. Transient Response (Actual)
(Approximately 110Ω , 10 feet long, ribbon cable stock)

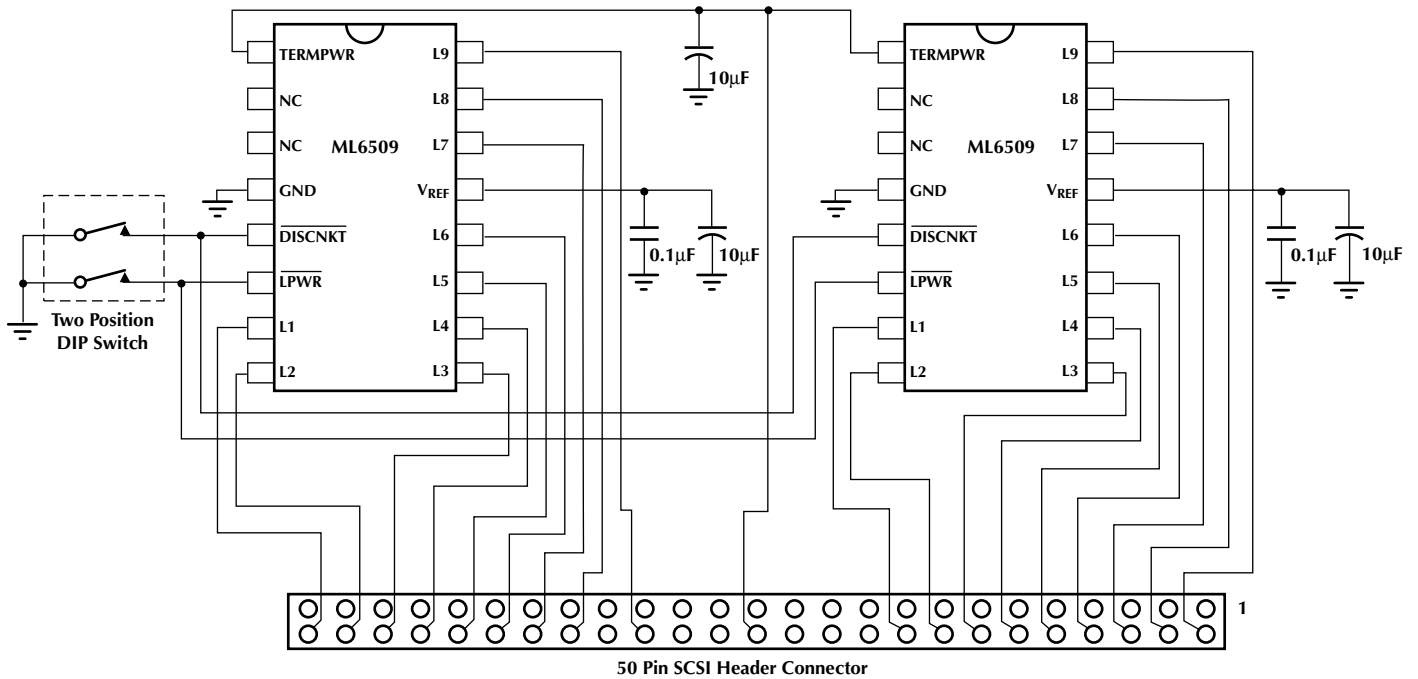
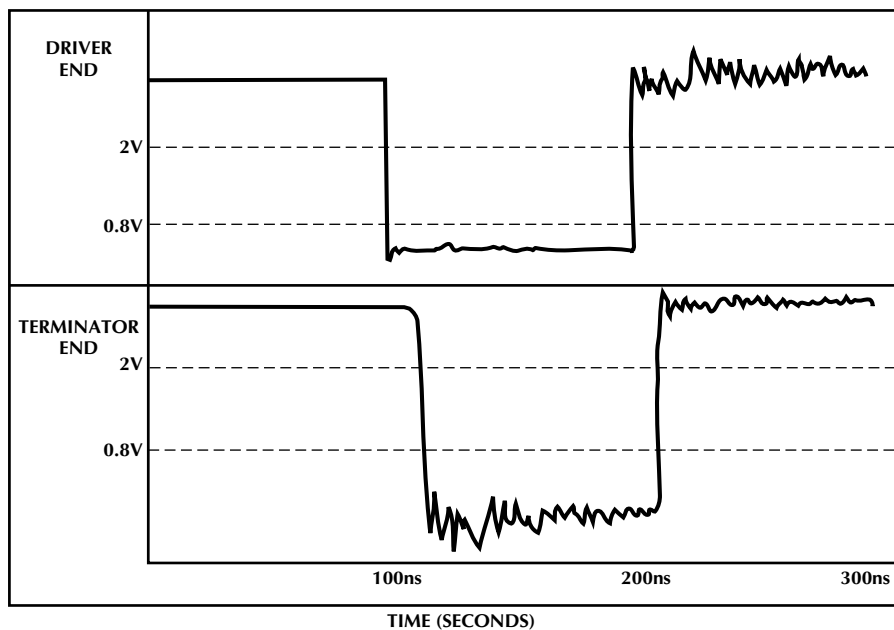
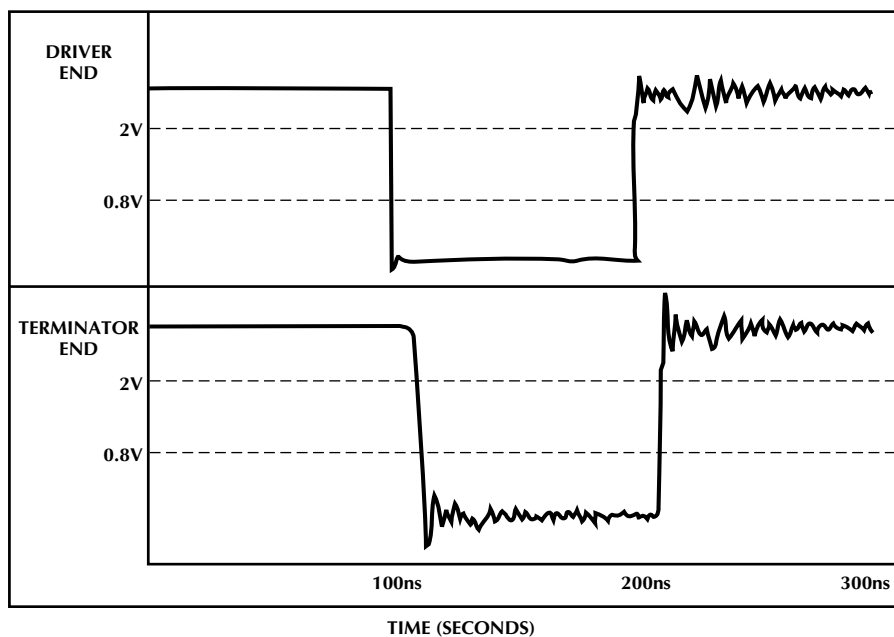


Figure 5. Typical Application Circuit

ML6509 SCSI TERMINATOR



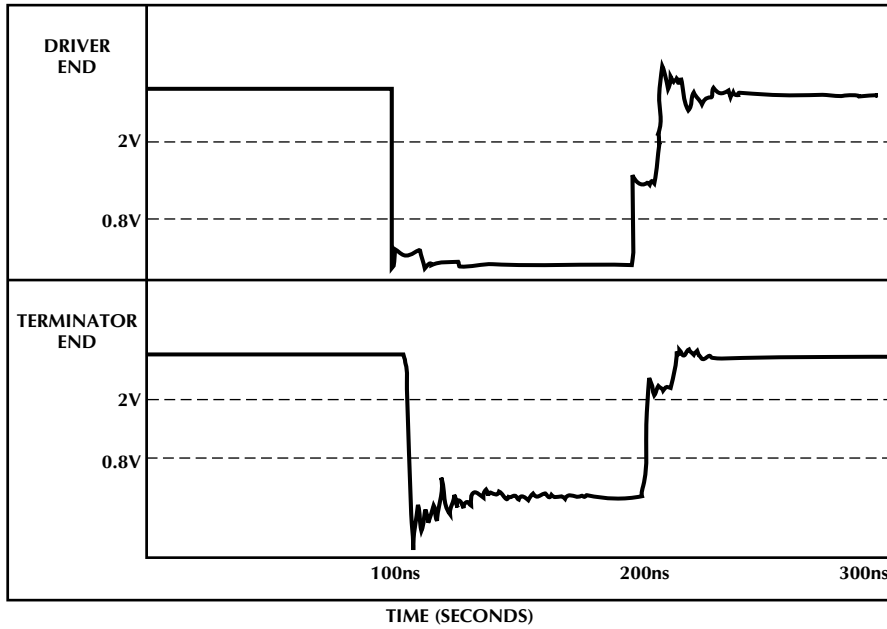
BOULAY TERMINATOR



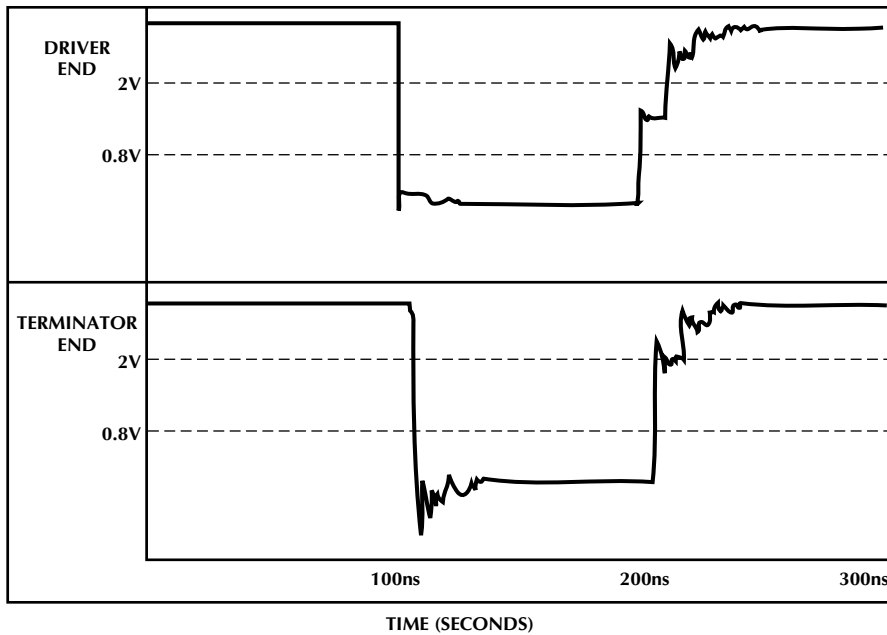
Conditions Low Cable impedance of 110Ω (worst case)
 $t_D = 10\text{ns}$
 10 segment distributed L-C, SCSI Bus Model
 Driver end of cable not terminated

Figure 6. Signal Assertion/Negation Waveforms (Simulated)

ML6509 SCSI TERMINATOR



BOULAY TERMINATOR

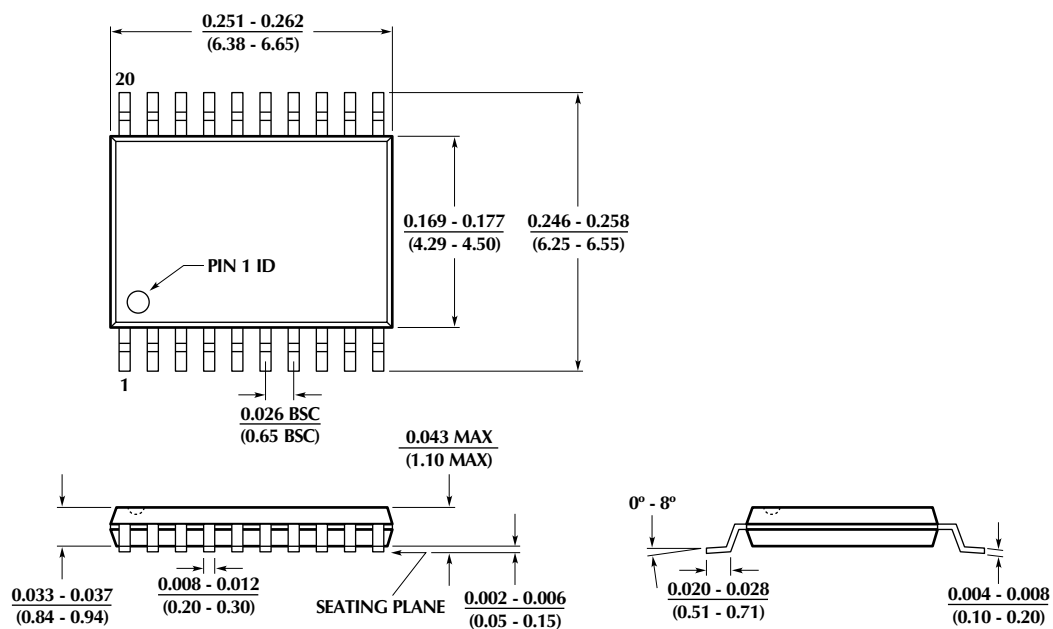


Conditions Low Cable impedance of 55Ω (worst case)
 $t_D = 10\text{ns}$
 10 segment distributed L-C, SCSI Bus Model
 Driver end of cable not terminated

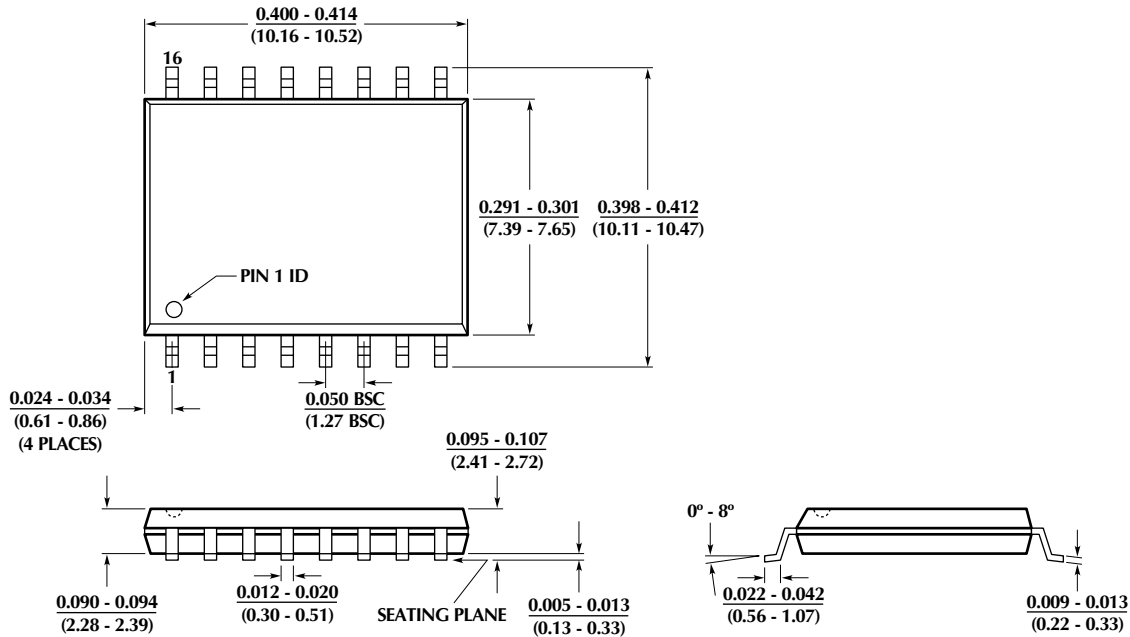
Figure 6a. Signal Assertion/Negation Waveforms (Simulated)

PHYSICAL DIMENSIONS inches (millimeters)

Package: T20
20-Pin TSSOP



**Package: S16W
16-Pin Wide SOIC**



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6509CS	0°C to 70°C	16-pin SOIC (S16W)
ML6509CT (EOL)	0°C to 70°C	20-pin TSSOP (T20)

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