AK5385A
24Bit 192kHz ΔΣ ADC

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AK5385A,ÍƒnƒCƒGƒ“ƒhƒI•[ƒfƒBƒIƒVƒXƒeƒ€,É•Å“K,È8kHz ~ 216kHzƒTƒ“ƒvƒŠƒ“ƒOŽü”g•”‘Î‰ž,ÌƒXƒeƒŒƒI A/DƒRƒ“ƒo•[ƒ^,Å,·•BAK5385A,ÍƒGƒ“ƒnƒ“ƒXƒg•Eƒfƒ…ƒAƒ‹ƒrƒbƒg ΔΣ Z π_ π ′ ⊗ ♦ ⎛ A ÷ ξ ♥ ℜ 〈 P Ξ γ ℵ ≈ ∝ ⊗ ′ ⇐ • B ⇐ ⎜ A A ι O ⎞ ⊆ ⊆ → Σ • → ¯ → ⊃ ∪ ℑ ⊗ ♠ AVƒAƒ“ƒvX A Γ η ⊂ AVƒŒƒR•[ƒ_,â“dŽqŠyŠí—p“r,É•Å“K,Å,·•BAK5385A,Í 28pin VSOP,Ü,½,Í 28pin SOPƒpƒbƒP•[ƒW,É,ÄŽÀ‘•,³,ê•AŠî”ÂƒXƒy•[ƒX,ð•íŒ¸,µ,Ü,·•B

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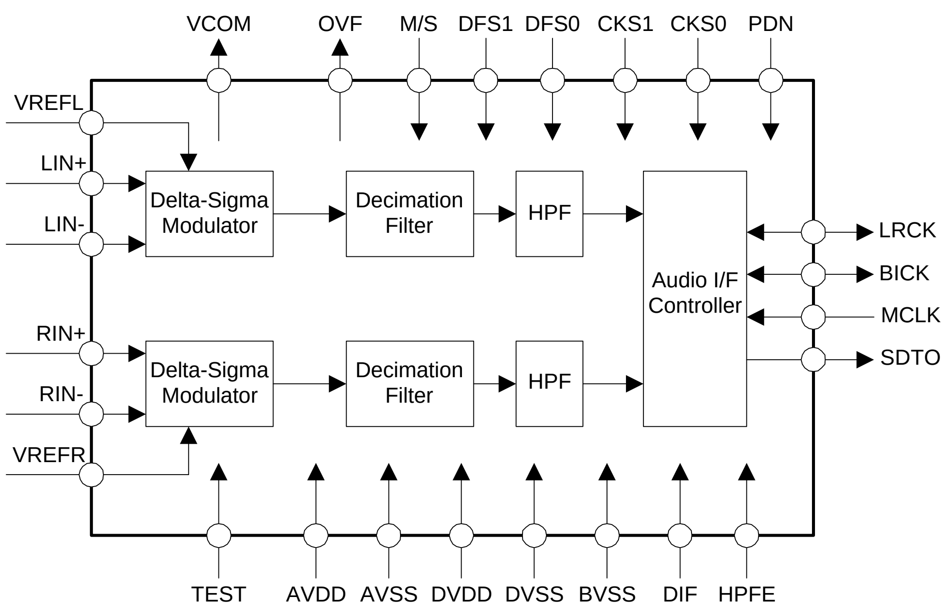
- ƒTƒ“ƒvƒŠƒ“ƒOƒŒ•[ƒg: 8kHz ~ 216kHz
-
- S/(N+D): 103dB
- DR: 114dB
- S/N: 114dB
-
  : 0•`21.768kHz (@fs=48kHz)
  ’Ê‰ß‰æƒŠƒbƒvƒ‹: 0.005dB
  ‘jŽ~‰æŒ¸•Š—Ê: 100dB
- HPF“à‘
- 5V ± 5%(ƒAƒiƒ•ƒO), 3.0 ~ 5.25V(ƒfƒBƒWƒ^ƒ‹)
- 183mW (@fs=48kHz)
- 28ƒsƒ“SOP, 28ƒsƒ“VSOP
- AK5383/AK5393/AK5394A•€ƒsƒ“ŒÝŠ·



Block diagram

■ ƒI•[ƒ_ƒŠƒ“ƒOƒKƒCƒh

AK5385AVS	–10 ~ +70°C	28pin SOP (1.27mm pitch)
AK5385AVF	–40 ~ +85°C	28pin VSOP (0.65mm pitch)
AKD5385A	AK5385A•]‰¿—pƒ{•[ƒh	

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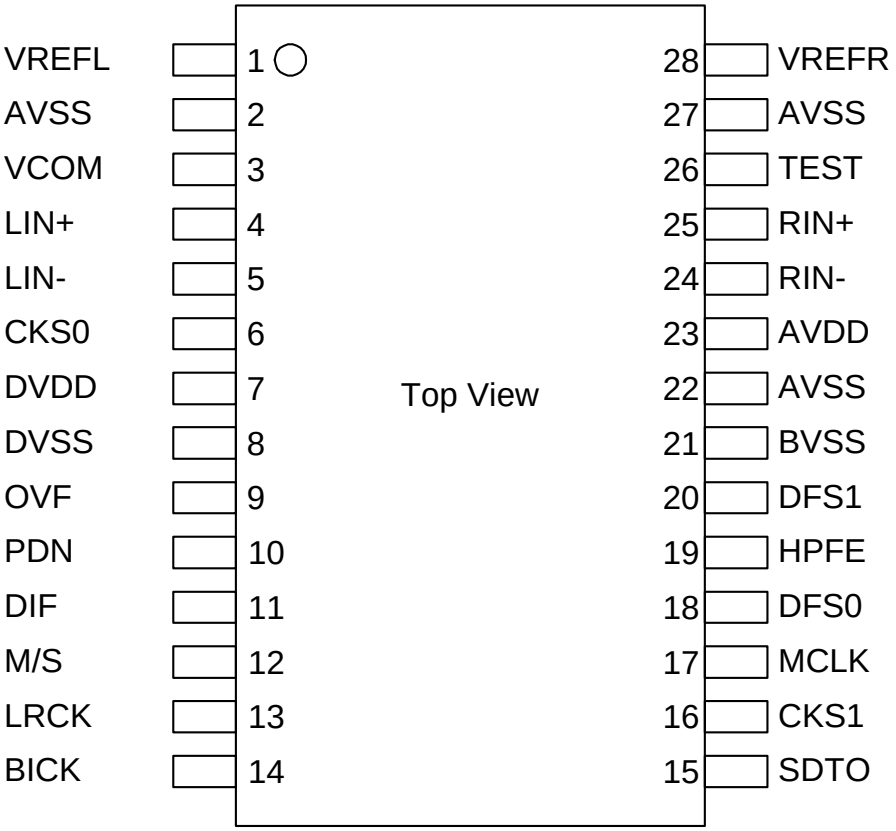
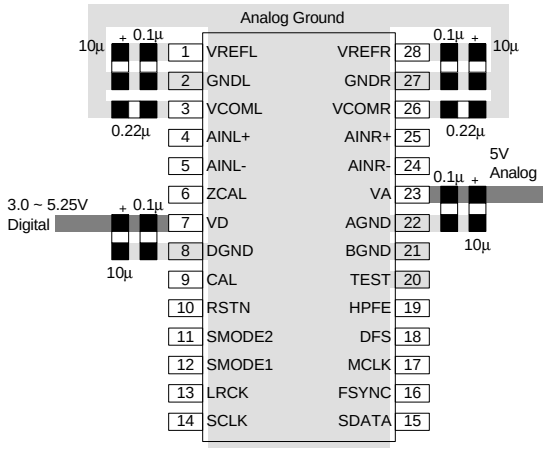


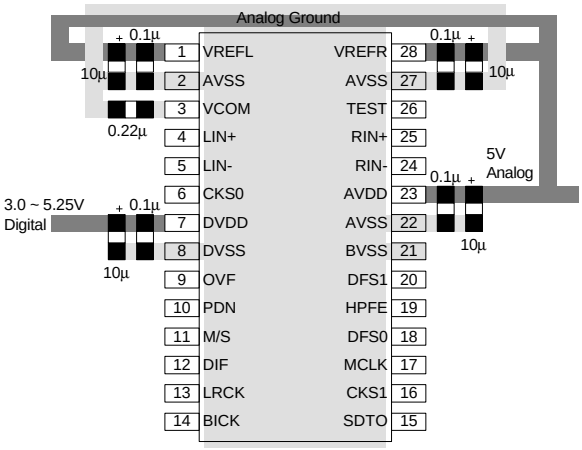
■ AK5383/AK5394A,Æ,ÌŒÝŠ·•«

	AK5385A	AK5383	AK5394A
Pin 1	VREFL	VREFL	VREFL+
Pin 2	AVSS	GNDL	VREFL–
Pin 3	VCOM	VCOML	VCOML
Pin 6	CKS0	ZCAL	ZCAL
Pin 9	OVF	CAL	CAL
Pin 11	DIF	SMODE2	SMODE2
Pin 12	M/S	SMODE1	SMODE1
Pin 16	CKS1	FSYNC	FSYNC
Pin 18	DFS0	DFS	DFS0
Pin 20	DFS1	TEST	DFS1
Pin 26	TEST	VCOMR	VCOMR
Pin 27	AVSS	GNDR	VREFR–
Pin 28	VREFR	VREFR	VREFR+
fs	8kHz ~ 216kHz	1kHz ~ 108kHz	1kHz ~ 216kHz
MCLK at 48kHz	256/384/512fs	256fs	256fs
MCLK at 96kHz	256fs	128fs	128fs
MCLK at 192kHz	128fs	Not Available	64fs
DR, S/N	114dB	110dB	123dB
Input Voltage	±2.9Vpp	±2.45Vpp	±2.4Vpp
Offset Calibration	Not Available	Available	Available

■ AK5383,Æ,ÌƒŒƒCƒAƒEƒg”äŠr



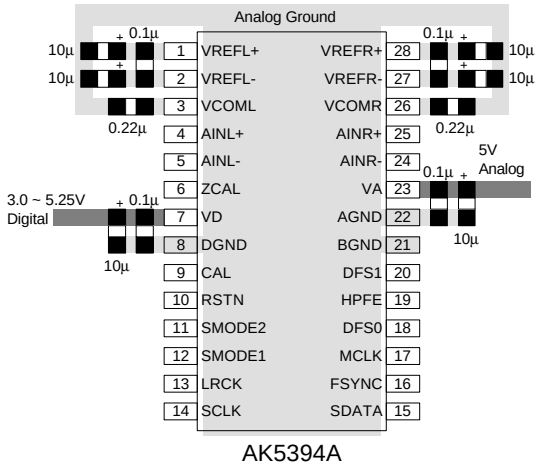
AK5383



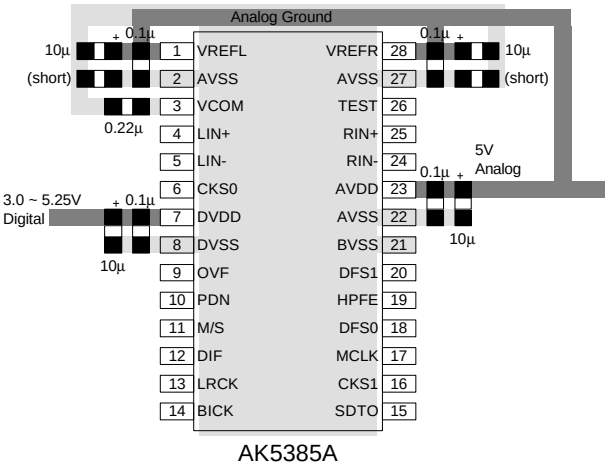
AK5385A

Pin #	AK5383	AK5385A
1	VREFL Lch Voltage Reference **Output** Pin, 3.75V Normally, connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.	VREFL Lch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
6	ZCAL Zero Calibration Control Pin This pin controls the calibration reference signal.	CKS0 Master Clock Select 0 Pin (Internal Pull-down Pin, typ. 100kΩ)
9	CAL Calibration Active Signal Pin	OVF Analog Input Overflow Detect Pin
11	SMODE2 Serial Interface Mode Select Pin	DIF Audio Interface Format Pin
12	SMODE1 Serial Interface Mode Select Pin	M/S Master / Slave Mode Pin
16	FSYNC Frame Synchronization Signal Pin	CKS1 Master Clock Select 1 Pin (Internal Pull-down Pin, typ.100kΩ)
18	DFS Double Speed Sampling Mode Pin	DFS0 Sampling Speed Select 0 Pin
20	TEST Test Pin (Internal Pull-down Pin)	DFS1 Sampling Speed Select 1 Pin
26	VCOMR Rch Common Voltage Pin, 2.75V	TEST Test Pin (Internal Pull-down Pin, typ. 100kΩ)
28	VREFR Rch Voltage Reference **Output** Pin, 3.75V Normally, connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.	VREFR Rch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.

■ AK5394A,Æ,ÌƒŒƒCƒAƒEƒg"äŠr



AK5394A



AK5385A

Pin #	AK5394A	AK5385A
1	VREFL+ Lch Positive Voltage Reference **Output** Pin, 3.75V Normally connected to AGND with a large electrolytic capacitor and connected to VREFL– with a 0.22µF ceramic capacitor.	VREFL Lch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
2	VREFL– Lch Negative Voltage Reference **Output** Pin, 1.25V Normally connected to AGND with a large electrolytic capacitor and connected to VREFL+ with a 0.22µF ceramic capacitor.	AVSS Analog Ground Pin
6	ZCAL Zero Calibration Control Pin This pin controls the calibration reference signal.	CKS0 Master Clock Select 0 Pin (Internal Pull-down Pin, typ. 100kΩ)
9	CAL Calibration Active Signal Pin	OVF Analog Input Overflow Detect Pin
11	SMODE2 Serial Interface Mode Select Pin	DIF Audio Interface Format Pin
12	SMODE1 Serial Interface Mode Select Pin	M/S Master / Slave Mode Pin
16	FSYNC Frame Synchronization Signal Pin	CKS1 Master Clock Select 1 Pin (Internal Pull-down Pin, typ. 100kΩ)
27	VREFR– Rch Negative Voltage Reference **Output** Pin, 1.25V Normally connected to AGND with a large electrolytic capacitor and connected to VREFR+ with a 0.22µF ceramic capacitor.	AVSS Analog Ground Pin
26	VCOMR Rch Common Voltage Pin, 2.75V	TEST Test Pin (Internal Pull-down Pin, typ. 100kΩ)
28	VREFR+ Rch Positive Reference **Output** Voltage, 3.75V Normally connected to AGND with a large electrolytic capacitor and connected to VREFR– with a 0.22µF ceramic capacitor.	VREFR Rch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.

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No.	Pin Name	I/O	Function
1	VREFL	I	Lch Voltage Reference Input Pin, AVDD Normally, connected to AVSS with a 10μF electrolytic capacitor and a 0.1μF ceramic capacitor.
2	AVSS	-	Analog Ground Pin
3	VCOM	O	Common Voltage Output Pin, AVDD/2
4	LIN+	I	Lch Analog Positive Input Pin
5	LIN–	I	Lch Analog Negative Input Pin
6	CKS0	I	Master Clock Select 0 Pin (Internal Pull-down Pin, typ. 100kΩ)
7	DVDD	-	Digital Power Supply Pin, 3.0 ~ 5.25V
8	DVSS	-	Digital Ground Pin
9	OVF	O	Analog Input Overflow Detect Pin This pin goes to "H" if analog input overflows.
10	PDN	I	Power Down Mode Pin "H": Power up, "L": Power down
11	DIF	I	Audio Interface Format Pin "H" : 24bit I^2S Compatible, "L" : 24bit MSB justified
12	M/S	I	Master / Slave Mode Pin "H" : Master Mode, "L" : Slave Mode
13	LRCK	I/O	Output Channel Clock Pin "L" Output in Master Mode at Power-down mode.
14	BICK	I/O	Audio Serial Data Clock Pin "L" Output in Master Mode at Power-down mode.
15	SDTO	O	Audio Serial Data Output Pin "L" Output at Power-down mode.
16	CKS1	I	Master Clock Select 1 Pin (Internal Pull-down Pin, typ. 100kΩ)
17	MCLK	I	Master Clock Input Pin
18	DFS0	I	Sampling Speed Select 0 Pin
19	HPFE	I	High Pass Filter Enable Pin "H" : Enable, "L" : Disable
20	DFS1	I	Sampling Speed Select 1 Pin
21	BVSS	-	Substrate Ground Pin
22	AVSS	-	Analog Ground Pin
23	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
24	RIN–	I	Rch Analog Negative Input Pin
25	RIN+	I	Rch Analog Positive Input Pin
26	TEST	I	Test Pin (Internal Pull-down Pin, typ. 100kΩ)
27	AVSS	-	Analog Ground Pin
28	VREFR	I	Rch Voltage Reference Input Pin, AVDD Normally, connected to AVSS with a 10μF electrolytic capacitor and a 0.1μF ceramic capacitor.

Note: All digital input pins except pull-down pins should not be left floating.

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Analog	LIN+, LIN–	AVSS,É•Ú‘±
	RIN+, RIN–	AVSS,É•Ú‘±
	VREFL, VREFR	AVDD,É•Ú‘±
Digital	OVF	ƒI•[ƒvƒ“
	TEST	DVSS,É•Ú‘±

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(AVSS, BVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	|BVSS – DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (LIN+/–, RIN+/–, VREFL/R pins)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (All digital input pins)		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (Power applied)	28SOP Package	Ta	–10	70	°C
	28VSOP Package	Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. “dˆ³,Í‘S,ÄƒOƒ‰ƒ“ƒhƒsƒ“,É‘Î,·,é’l,Å,·•B
Note 2. AVSS, BVSS, DVSS,Í“¯,¶ƒAƒiƒƒOƒOƒ‰ƒ“ƒh,É•Ú‘±,µ,Ä‰º,³,¢•B

’•ˆÓ: ,±,Ì’l,ð´,¦,½•ðŒ•,ÅŽg—p,µ,½•ê•‡•Aƒƒƒ‚ƒCƒX,ð”j‰ó,·,é,±,Æ,ª, ,è,Ü,·•B
,Ü,½•A’Ê•í,Ì“®•ì,Í•Û•Ø,³,ê,Ü,¹,ñ•B

•„•§“®•ì•ðŒ•

(AVSS, BVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	3.0	3.3	AVDD	V
Voltage Reference (VREFL/R pins)		VREF	3.0	-	AVDD	V

Note 1. “dˆ³,Í‘S,ÄƒOƒ‰ƒ“ƒhƒsƒ“,É‘Î,·,é’l,Å,·•B
Note 3. AVDD,ÆDVDD,Ì“dŒ¹—§,¿•ã,°ƒV•[ƒPƒ“ƒX,ð•l—¶,·,é•K—v,Í, ,è,Ü,¹,ñ•B

’•ˆÓ: –{ƒf•[ƒ^ƒV•[ƒg,É‹L•Ú,³,ê,Ä,¢,é•ðŒ•ˆÈŠO,Ì,²Žg—p,ÉŠÖ,µ,Ä,Í•A“–ŽÐ,Å,Í•Ó”C•‰,¢,©,Ë,Ü,·,Ì,Å •\•ª,²’•ˆÓ‰º,³,¢•B

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(Ta=25°C; AVDD=5.0V, DVDD=3.3V; AVSS=BVSS=DVSS=0V; VREFL=VREFR=AVDD; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz, 40Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			**min**	**typ**	**max**	**Units**
Analog Input Characteristics:						
Resolution					24	Bits
Input Voltage		(Note 4)	±2.7	±2.9	±3.1	Vpp
S/(N+D)		–1dBFS (Note 5)	-	103		dB
	fs=48kHz BW=20kHz	–1dBFS	92	100		dB
		–20dBFS	-	91		dB
		–60dBFS	-	51		dB
	fs=96kHz BW=40kHz	–1dBFS	90	98		dB
		–20dBFS	-	86		dB
		–60dBFS	-	46		dB
	fs=192kHz BW=40kHz	–1dBFS	-	98		dB
		–20dBFS	-	86		dB
		–60dBFS	-	46		dB
Dynamic Range		(–60dBFS with A-weighted)	107	114		dB
S/N		(A-weighted)	107	114		dB
Input Resistance			9	13		kΩ
Interchannel Isolation			100	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Power Supply Rejection		(Note 6)		50	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
AVDD				30	45	mA
DVDD		(fs=48kHz)		10	15	mA
DVDD		(fs=96kHz)		17	25	mA
DVDD		(fs=192kHz)		20	30	mA
Power down mode (PDN pin = "L")		(Note 7)				
AVDD+DVDD				10	100	µA

Note 4. (LIN+)–(LIN–)‹y,Ñ(RIN+)–(RIN–),Ì'l,Å,·•B VREFL, VREFR,Ì"dˆ³,É"ä—á,µ,Ü,·•B
Vin = 0.58 × VREF (Vpp)• B
Note 5. VREFL pin,ÆAVSSŠÔ‹y,ÑVREFR pin,ÆAVSSŠÔ,É,»,ê,¼,ê 100µF,ð•Ú'±,µ,½•ê•‡,Å,·•B
Note 6. VREFL, VREFR pin,Ì"dˆ³,ðˆê'è,É,µ,Ä AVDD, DVDD,É1kHz, 20mVpp,Ì•³Œ·"g,ð•d•ô,µ,½•ê•‡,Å,·•B
Note 7. 'S,Ä,ÌƒfƒBƒWƒ^ƒ‹"ü—Íƒsƒ",ð DVDD,Ü,½,Í DVSS,ÉŒÅ'è,µ,½ŽžŽ,Ì'l,Å,·•B

ƒtƒBƒ‹ƒ^“Á•« **(fs=48kHz)**

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; DFS1 pin = “L”, DFS0 pin = “L”)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	−0.005dB	PB	0		21.5	kHz
	−0.02dB		-	22.038	-	kHz
	−0.06dB		-	22.2	-	kHz
	−6.0dB		-	24.0	-	kHz
Stopband		SB	26.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 9)		GD		43.2		1/fs
Group Delay Distortion		ΔGD		0		µs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	−3dB	FR		1.0		Hz
	−0.1dB			6.5		Hz

ƒtƒBƒ‹ƒ^“Á•« **(fs=96kHz)**

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; DFS1 pin = “L”, DFS0 pin = “H”)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	−0.005dB	PB	0		43.0	kHz
	−0.02dB		-	44.081	-	kHz
	−0.06dB		-	44.5	-	kHz
	−6.0dB		-	48.0	-	kHz
Stopband		SB	53.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 9)		GD		43.1		1/fs
Group Delay Distortion		ΔGD		0		µs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	−3dB	FR		2.0		Hz
	−0.1dB			13.0		Hz

Note 8. Še•U••“Á•«,ÌŽü”g•”ƒ‰ƒ(ƒVƒXƒefƒ€ƒTƒ“ƒvƒŠƒ“ƒOƒŒ•[ƒg,ª”ä—á,µ,Ü,·•BŠe‰ž“š,ÍkHz,ðŠî•€,É,µ,Ü,·•B

Note 9. ƒfƒBƒWƒ^ƒ‹ƒtƒBƒ‹ƒ^,É,æ,é’x‰„‰ŽZ,Å•AƒAƒiƒ•ƒO•M•†,ª“ü—Í,³,ê,Ä,©,ç—¼ƒ`ƒƒƒlƒ‹,Ìbƒgƒf•[ƒ^,ª ADC•o—ÍƒŒƒWƒXƒ^,ÉƒZƒbƒg,³,ê,é,Ü,Å,ÌŽžŠÔ,Å,·•B

ƒtƒBƒ‹ƒ^“Á•« (fs=192kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; DFS1 pin = “H”, DFS0 pin = “L”)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	−0.005dB	PB	0		86.0	kHz
	−0.02dB		-	88.183	-	kHz
	−0.06dB		-	89.0	-	kHz
	−6.0dB		-	96.0	-	kHz
Stopband		SB	106.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 9)		GD		38.2		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	−3dB	FR		4.0		Hz
	−0.1dB			26.0		Hz

Note 8. Še•U••“Á•«,ÌŽü”g•”ŧ(ƒVƒXƒeƒ€ƒTƒ“ƒvƒŠƒ“ƒOƒŒ•[ƒg,É”ä—á,µ,Ü,··BŠe‰ž“š,ÍkHz,ðŠî•€,É,µ,Ü,··B

Note 9. ƒƒBƒWƒ^ƒ‹ƒtƒBƒ‹ƒ^,É,æ,é’x‰„‰ŽZ,Å•AƒAƒiƒƒO•M•†,ª“ü—Í,³,ê,Ä,©,ç—¼ƒ`ƒƒƒlƒ‹,Ìbƒgƒf•[ƒ^,ª ADC•o—ÍƒŒƒWƒX^,ÉƒZƒbƒg,³,ê,é,Ü,Å,ÌŽžŠÔ,Å,··B

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(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
High-Level Output Voltage	(Iout=−400μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage	(Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current	(Note 10)	Iin	-	-	±10	μA

Note 10. CKS1-0 pin, TEST pin,Í“à•”,Åƒvƒ‹ƒ_ƒEƒ“,³,ê,Ä,¢,Ü,··B (typ. 100kΩ)

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(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; C_L=20pF)

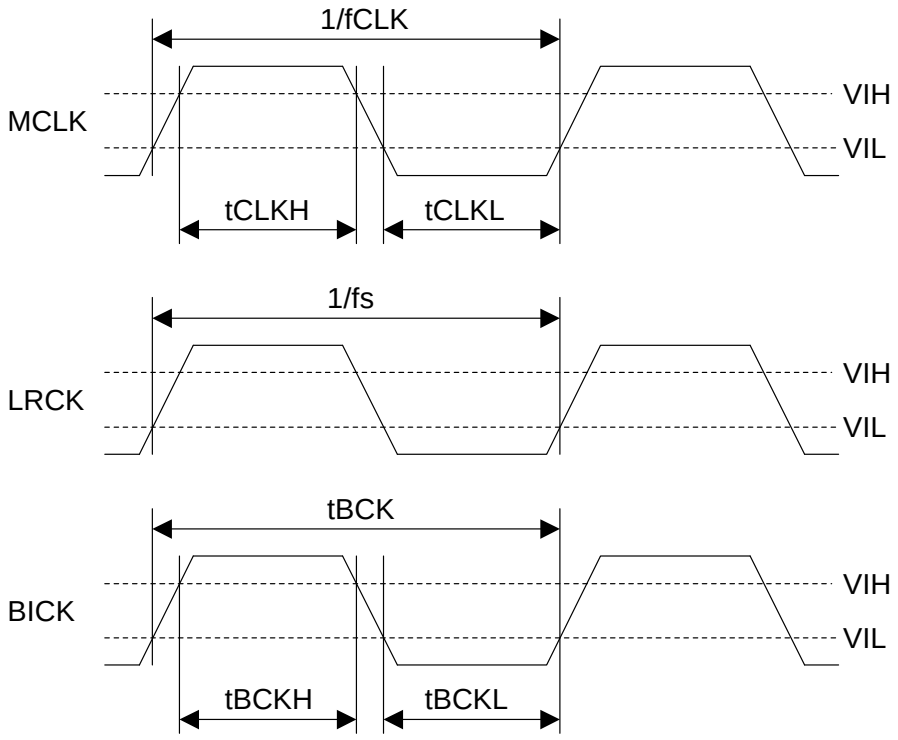
Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	2.048		27.648	MHz
Pulse Width Low		tCLKL	14.5			ns
Pulse Width High		tCLKH	14.5			ns
LRCK Frequency						
Normal Speed Mode		fsn	8		54	kHz
Double Speed Mode		fsd	54		108	kHz
Quad Speed Mode		fsq	108		216	kHz
Duty Cycle	Slave mode		45		55	%
	Master mode			50		%
Audio Interface Timing						
Slave mode						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			ns
Double Speed Mode		tBCK	1/64fsd			ns
Quad Speed Mode		tBCK	1/64fsq			ns
BICK Pulse Width Low		tBCKL	33			ns
Pulse Width High		tBCKH	33			ns
LRCK Edge to BICK "↑"	(Note 11)	tLRB	20			ns
BICK "↑" to LRCK Edge	(Note 11)	tBLR	20			ns
LRCK to SDTO (MSB)	(Except I^2S mode)	tLRS			20	ns
BICK "↓" to SDTO		tBSD			20	ns
Master mode						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	−20		20	ns
BICK "↓" to SDTO		tBSD	−20		20	ns
Reset Timing						
PDN Pulse Width	(Note 12)	tPD	150			ns
PDN "↑" to SDTO valid	(Note 13)	tPDV		516		1/fs

Note 11. ,±,Ì‹KŠi'l,Í LRCK,ÌƒGƒbƒW,ÆBICK,Ì "↑",ª•d,È,ç,È,¢,æ,¤,É‹K'è,µ,Ä,¢,Ü,·•B

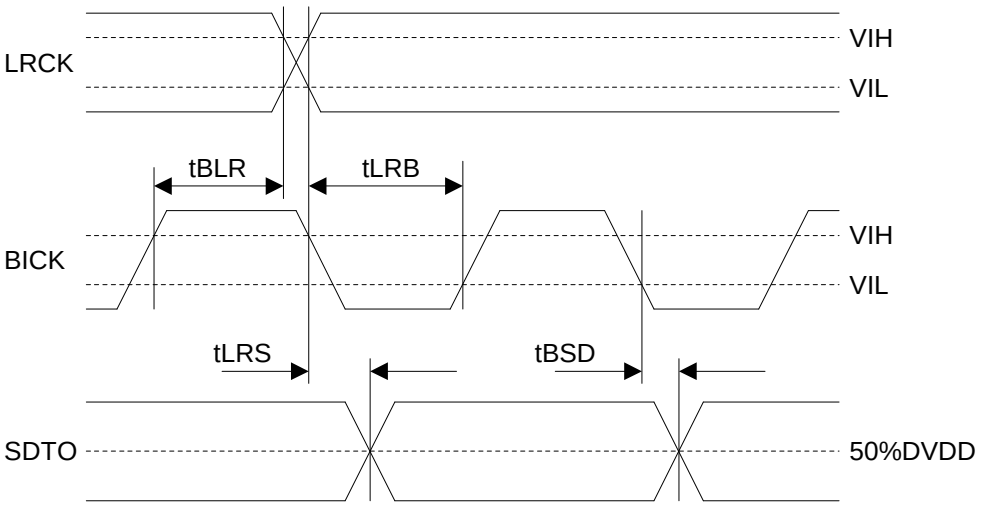
Note 12. AK5385A,Í PDN pin = "L",ÅƒŠƒZƒbƒg,³,ê,Ü,·•B

Note 13. PDN pin,ð—§,¿•ã,°,Ä,©,ç,Ì LRCKƒNƒ•ƒbƒN,ª↑",Ì‰ñ•",Å,·•B‹KŠi'l,Íƒ}ƒXƒ^ƒ•[ƒh,Å,Ì'l,Å,·•B
ƒXƒŒ•[ƒuƒ•[ƒh,Å,ÍLRCKƒNƒ•ƒbƒN(1/fs)'·,-,È,è,Ü,·•B

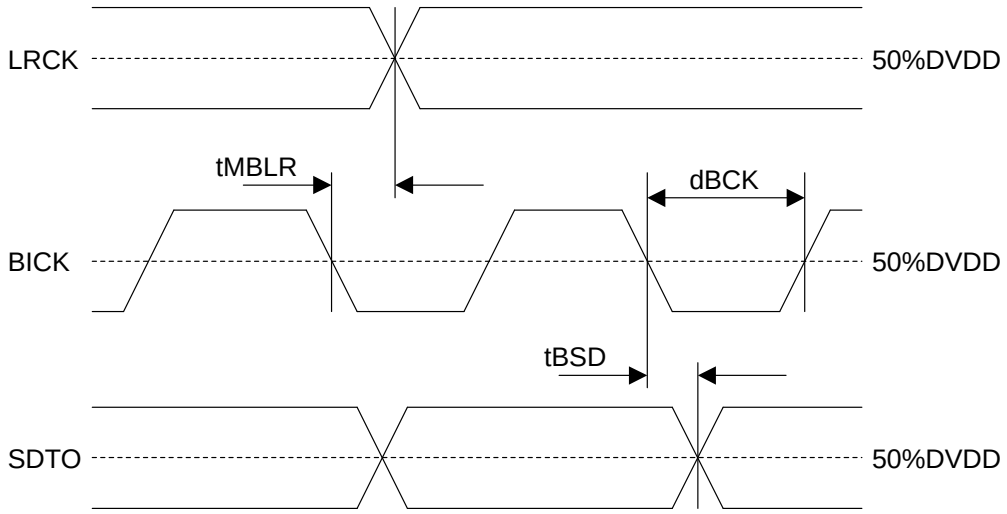
■ ƒ^ƒCƒ~ƒ“ƒO”gŒ`



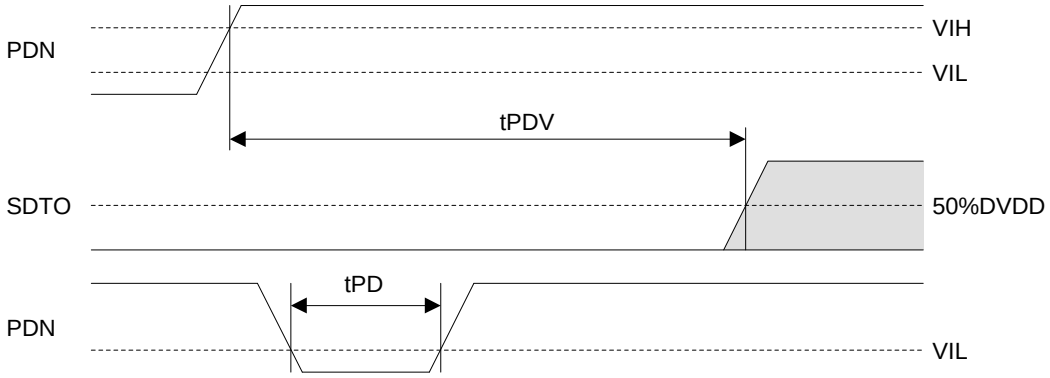
Clock Timing



Audio Interface Timing (Slave mode)



Audio Interface Timing (Master mode)



Power Down & Reset Timing

“®•ì•à–¾

■ ƒVƒXƒefƒ€ƒNƒ•ƒbƒN

AK5385A,É•K—v,Æ,³,ê,éƒNƒ•ƒbƒN,ÍMCLK, BICK, LRCK,Å,·•BMCLK,ÆLRCK,Í“¯Šú,·,é•K—v,Í ,è,Ü,·,ª•Aˆê‘Š,ð•‡,í,¹,é•K—v,Í, ,è,Ü,¹,ñ•B Table 1,É•W•€,ÌƒI•[ƒfƒBƒIƒŒ•[ƒg,É‘Î,µ,ÄAK5385A,É•K—v,Æ,³,ê,éŠeƒNƒ•ƒbƒN,ÌŽü”g•”,ðŽ¦,µ,Ü,·•BAK5385A,Ìƒ}ƒXƒ^ƒNƒ•ƒbƒNŽü”g•”,ÍCKS1-0 pin (Table 2),Å•Ý’è,µ•AƒTƒ“ƒvƒŠƒ“ƒOŽü”g•”,ÍDFS1-0 pin (Table 3),Å•Ý’è,µ,Ü,·•B

ƒXƒŒ•[ƒuƒ,•[ƒhŽž,É,Í•AK5385A,Í LRCK,É,æ,éˆÊ‘ŠŒŸ•o‰ñ˜H,ð“à‘ ,µ,Ä,¢,é,½,ß•A“®•ì’†,ÉŠeƒNƒ•ƒbƒN,ÌŽü”g•”•Ï•X™,Å“à•”ƒ^ƒCƒ~ƒ“ƒO,ª,¸,ê,½•ê•‡,É,ÍŽ©“®“I,ÉƒŠƒZƒbƒg,ª,©,©,è•AˆÊ‘Š•‡,í,¹,ª•s,í,ê,Ü,·•B

ƒXƒŒ•[ƒuƒ,•[ƒh,Å,Ì“®•ì(PDN pin = “H”),Í•AŠeŠO•”ƒNƒ•ƒbƒN(MCLK, BICK, LRCK),ðŽ~,ß,Ä,Í,¢,¯,Ü,¹,ñ•B ,±,ê,ç,ÌƒNƒ•ƒbƒN,ª‹Ÿ‹¤,³,ê,È,¢•ê•‡•A“à•”,Éƒ_ƒCƒiƒbƒN,Èƒ•ƒWƒbƒN,ðŽg—p,µ,Ä,¢,é,½,ß•A‰ß“d—¬,ª—¬,ê“®•ì,ªˆÙ•í,É,È,é‰Â”\•«,ª, ,è,Ü,·•BƒNƒ•ƒbƒN,ðŽ~,ß,é•ê•‡,Íƒpƒ••[ƒ_ƒEƒ“•ó‘Ô(PDN pin = “L”),É,µ,Ä‰º,³,¢•Bƒ}ƒXƒ^,•[ƒh,Å,Íƒpƒ••[ƒ_ƒEƒ“ŽžˆÈŠO,Í•AŠO•”ƒNƒ•ƒbƒN(MCLK),ð‹Ÿ‹¤,µ,Ä‰º,³,¢•B

fs	MCLK			
	128fs	256fs	384fs	512fs
32kHz	N/A	8.192MHz	12.288MHz	16.384MHz
44.1kHz	N/A	11.2896MHz	16.9344MHz	22.5792MHz
48kHz	N/A	12.288MHz	18.432MHz	24.576MHz
96kHz	N/A	24.576MHz	N/A	N/A
192kHz	24.576MHz	N/A	N/A	N/A

Table 1. System Clock Example

CKS1 pin	CKS0 pin	MCLK Frequency
L	L	256fs
L	H	128fs
H	L	512fs
H	H	384fs

Table 2. MCLK Frequency

DFS1 pin	DFS0 pin	LRCK Frequency
L	L	8kHz ≤ fs ≤ 54kHz
L	H	54kHz < fs ≤ 108kHz
H	L	108kHz < fs ≤ 216kHz
H	H	N/A

Table 3. Sampling Speed

[ƒTƒ“ƒvƒŠƒ“ƒOŽü”g•”•Ï•XŽž,Ì’•ˆÓ“_

- ƒXƒŒ•[ƒuƒ,•[ƒh,Íƒ}ƒXƒ^,•[ƒh‹¤,É•AMCLKŽü”g•”,ð•Ï•X,·,é•ê•‡,ÍPDN pin = “L”,Åƒ‚ƒZƒbƒg,µ,Ä‰º,³,¢•B
  [—á] 12.288MHz(@fs=48kHz),©,ç24.576MHz(@fs=96kHz),É•Ï•X,·,é•ê•‡•B

- ƒXƒŒ•[ƒuƒ,•[ƒh,Íƒ}ƒXƒ^,•[ƒh‹¤,É•AMCLKŽü”g•”,ðŒÅ’è,µ,ÄCKS1-0, DFS1-0 pin,Åƒ‚ƒf“ƒvƒŠƒ“ƒOŽü”g•”,ð•Ï•X,·,é•ê•‡,Í PDN pin = “L”,Åƒ‚ƒZƒbƒg,·,é•K—v,Í, ,è,Ü,¹,ñ•B
  [—á] MCLKŽü”g•”,ª24.576MHz,Ì ,Ü,Ü•Afs,ð48kHz,©,ç96kHz,É•Ø,è‘Ö,¦,é•ê•‡•B

■ ƒI•[ƒƒBƒIƒCƒ“ƒ^ƒtƒF•[ƒXƒtƒH•[ƒ}ƒbƒg

2Ží—Þ,Ìƒf•[ƒ^ƒtƒH•[ƒ}ƒbƒg,ªDIF pin (Table 4),Å‘I‘ð,Å,«,Ü,·•B—¼ƒ,•[ƒh,Æ,ÌMSBƒtƒ@•[ƒXƒg•2Asƒ Rƒ“ƒvƒŠ ƒ•ƒ“ƒg,Ìƒf•[ƒ^ƒtƒH•[ƒ}ƒbƒg,ÅSDTO,Í BICK,Ì—§,¿‰º,ª,è,Å•o—Í,³,ê,Ü,·•BƒI•[ƒƒBƒIƒCƒ“ƒ^ƒtƒF•[ƒX,Íƒ} ƒXƒ^ƒ,•[ƒh,ÆƒXƒŒ•[ƒuƒ,•[ƒh,É‘Î‰ž,µ,Ü,·•Bƒ}ƒXƒ^ƒ,•[ƒh,ÅRCK,ÆBICK,Í•o—Í,É,È,è•AƒXƒŒ•[ƒuƒ,•[ƒh ,Å,Í“ü—Í,É,È,è,Ü,·•Bƒ}ƒXƒ^ƒ,•[ƒhŽž,ÌLRCKŽü”g•”,ÆBICKŽü”g•”,Í,»,ê,¼,ê fs,Æ64fs,Å,·•B

Mode	DIF pin	SDTO	LRCK	BICK	Figure
0	L	24bit, MSB justified	H/L	≥ 48fs	Figure 1
1	H	24bit, I^{2}S Compatible	L/H	≥ 48fs	Figure 2

Table 4. Audio Interface Format

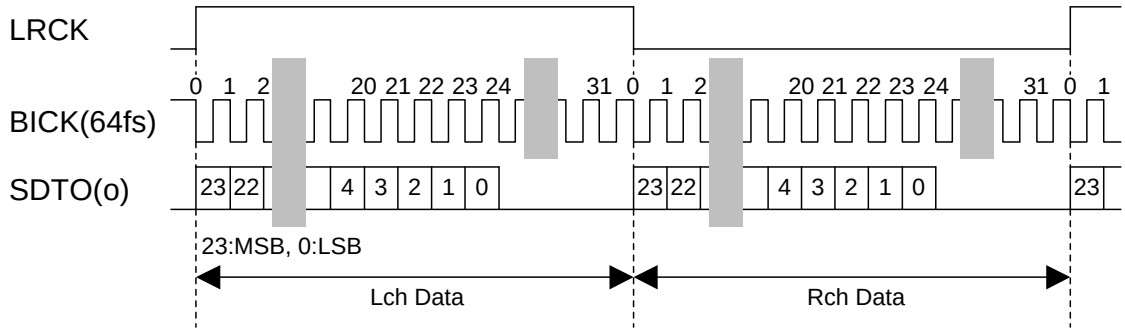


Figure 1. Mode 0 Timing

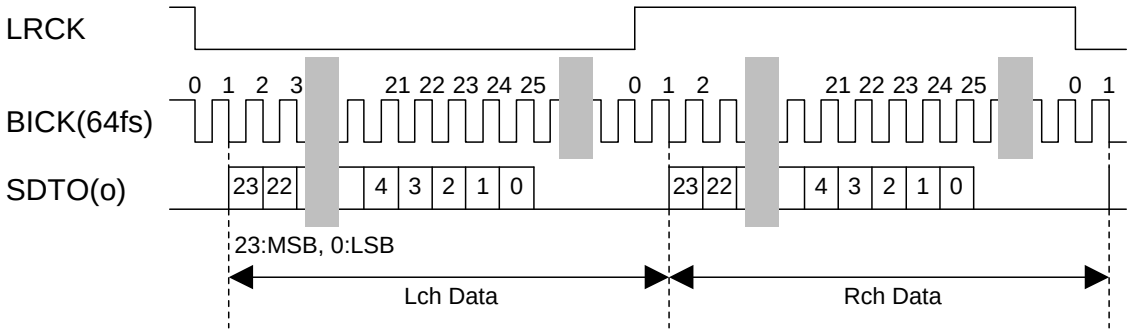


Figure 2. Mode 1 Timing

■ ƒ}ƒXƒ^ƒ,•[ƒh,ÆƒXƒŒ•[ƒuƒ,•[ƒh,Ì•Ø,è‘Ö,¦

ƒ}ƒXƒ^ƒ,•[ƒh,ÆƒXƒŒ•[ƒuƒ,•[ƒh,Ì•Ø,è‘Ö,¦,ÍM/S pin,Å•s,¢,Ü,·•B‘H”,Åƒ}ƒXƒ^ƒ,•[ƒh•ÆL”,ÅƒXƒŒ•[ƒuƒ,•[ƒh ,Å,·•BAK5385A,ªƒ}ƒXƒ^ƒ,•[ƒh,ÌŽž,É,Í•AAK5385A,ÉMCLK,ð‹Ÿ‹,·,é,Æ BICK, LRCK,ª•o—Í,³,ê,Ü,·•B AK5385A,ªƒXƒŒ•[ƒuƒ,•[ƒh,ÌŽž,É,Í•AMCLK, BICK, LRCK,ð‹Ÿ‹,µ,Ä‰º,³,¢•B

M/S pin	Mode	BICK, LRCK
L	Slave Mode	BICK = Input LRCK = Input
H	Master Mode	BICK = Output LRCK = Output

Table 5. Master mode/Slave mode

■ ƒƒƒBƒWƒ^ƒ‹HPF

ADC,Í DCƒIftƒZƒbƒgƒLƒƒƒ“ƒZƒ‹,Ì,½,ß,ÉƒƒƒBƒWƒ^ƒ‹ HPF,ð“à‘ ,µ,Ü,·•B HPF,Ì fc,Í•Afs=48kHzŽž1.0Hz,É,È,Á ,Ä,¨,è•AŽü”g•”‰ž“šƒß,É”ä—á,µ,Ü,·•B

HPFE pin,Ì•Ý’è,É,æ,è•AHPF,Ì ON/OFF,ð•§Œä,·,é,±,Æ,ª,Å,«,Ü,·•B’A,µ•A“®•ì’†,É HPF,Ì ON/OFF•Ý’è,ð•Ï•X ,·,é,Æ•ADCƒIftƒZƒbƒg’l,Ì•Ï‰»,É,æ,éƒNƒŠƒbƒN‰¹”-•¶,ÌŒ´ˆö,Æ,È,è,Ü,·•B•Ý’è•Ï•X,Íƒpƒ••[ƒ_ƒEƒ“ (PDN pin = “L”)Žž,É•s,¤,±,Æ,ð•„•§,µ,Ü,·•B

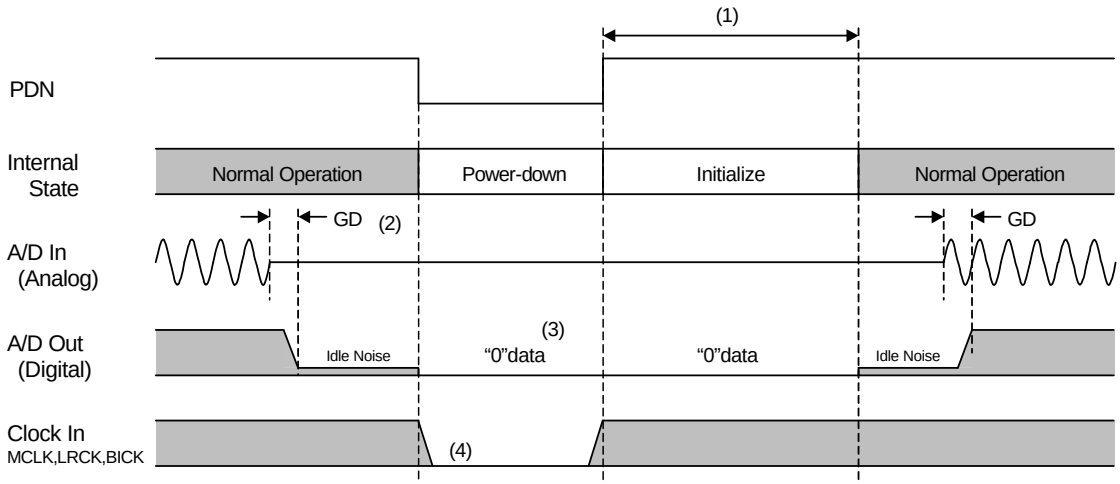
■ ƒI•[ƒoftƒ••[ŒŸ•o‹@”\

AK5385A,ÍƒAfiƒ•ƒO“ü—Í,ÌƒI•[ƒoftƒ••[ŒŸ•o‹@”\,ðŽ•,¿,Ü,·•B,Ü,½,Í Rch,ÌƒAfiƒ•ƒO“ü—Í,ªƒI•[ƒoftƒ••[,·,é,Æ (–0.3dBFSˆÈ•ã)• AOVF pin,ª “H”,É,È,è,Ü,·•BƒI•[ƒoftƒ••[,µ,½ƒAfiƒ•ƒO“ü—Í,É‘Î,·,é OVF•o—Í,ÍADC ,Æ“¯,¶ŒQ’x‰„ŽžŠÔ (GD = 43.2/fs = 0.9ms@fs=48kHz),ðŽ•,¿,Ü,·•Bƒpƒ••[ƒ_ƒEƒ“‰ð•úŒã (PDN pin = “L” → “H”)• A 516/fs(=10.75ms@fs=48kHz),ÌŠÔOVF pin,Í “L”,Å•A,»,ÌŒãƒI•[ƒoftƒ••[ŒŸ•o‹@”\,ª—LŒø,É,È,è,Ü,·•B

■ ƒpƒ••[ƒ_ƒEƒ“,Æƒ‚ƒZƒbƒg

AK5385A,Í PDN pin,ð“L”,É,·,é,±,Æ,Åƒpƒ••[ƒ_ƒEƒ“ƒ,•[ƒh,É,Å,«,Ü,·•B,±,ÌŽž•A“¯Žž,Éƒƒƒ^ƒ‹ƒtƒBƒ‹ƒ^ ,ªƒŠƒZƒbƒg,³,ê,Ü,·•B,±,ÌƒŠƒZƒbƒg,Í“dŒ¹“Š“üŽž,É•K,¸ê“x,s,Á,Ä‰º,³,¢•Bƒpƒ••[ƒ_ƒEƒ“ƒ,•[ƒhŽž,ÍVCOM ,Í AVSS,Ì“d³,É,È,è,Ü,·•Bƒpƒ••[ƒ_ƒEƒ“ƒ,•[ƒh,ª‰ð,³,ê,é,Æ•‰Šú‰»ƒTƒCƒNƒ‹,ªŠJŽn,³,ê,Ü,·•B,»,Ì,½,ß•A •o—Íƒf•[ƒ^SDTO,Í 516 × LRCKƒTƒCƒNƒ‹ŒãŠm’è,µ,Ü,·•B‰Šú‰»’†,Í—¼ƒ`ƒƒƒlƒ‹ADC•o—Íƒf•[ƒ^,Í2’sƒRƒ“ƒvƒŠƒ•ƒ“ƒg,Ì“0”,Å•A•‰Šú‰»•I—¹ŒãADC•o—Í,ÍƒAfiƒ•ƒO“ü—Í•M†,É‘Š“–,·,éƒf•[ƒ^,ÉƒZƒgƒŠƒ“ƒO,µ,Ü,·•B ƒZƒgƒŠƒ“ƒO,ÍŒQ’x‰„ŽžŠÔ‘ö“x,©,©,è,Ü,·•B

“dŒ¹“Š“üŽž•Aˆê’UPDN pin,ð“L”,É,µ,ÄƒŠƒZƒbƒg,µ,Ä‰º,³,¢•B,»,ÌŒã•APDN pin,ð“H”,É,·,é,ƒŠƒZƒbƒg‹y,Ñƒpƒ••[ƒ_ƒEƒ“,ÍMCLK,Å‰ð•œ,³,ê•ALRCK,Ì—§,¿•ã,ª,èGƒbƒW•o—Íƒtƒ‰ƒbƒg,ªMode 1,ÌŽž,Í—§,¿‰º,ª,èGƒbƒW,É“¯Šú,µ,Ä“à•”,Ìƒ^ƒCƒ~ƒ“ƒO,ª®•ì,µ,Ü,·•B



Notes:

(1) ƒXƒŒ•[ƒuƒ,•[ƒhŽž5Í17/fs•Aƒ}ƒXƒ^ƒ,•[ƒhŽž5Í16/fs,Å,·•B

(2) ƒAfiƒ•ƒO“ü—Í,É‘Î,·,éƒƒƒBƒWƒ^ƒ‹•o—Í,ÍŒQ’x‰„ŽžŠÔ (GD),ðŽ•,¿,Ü,·•B

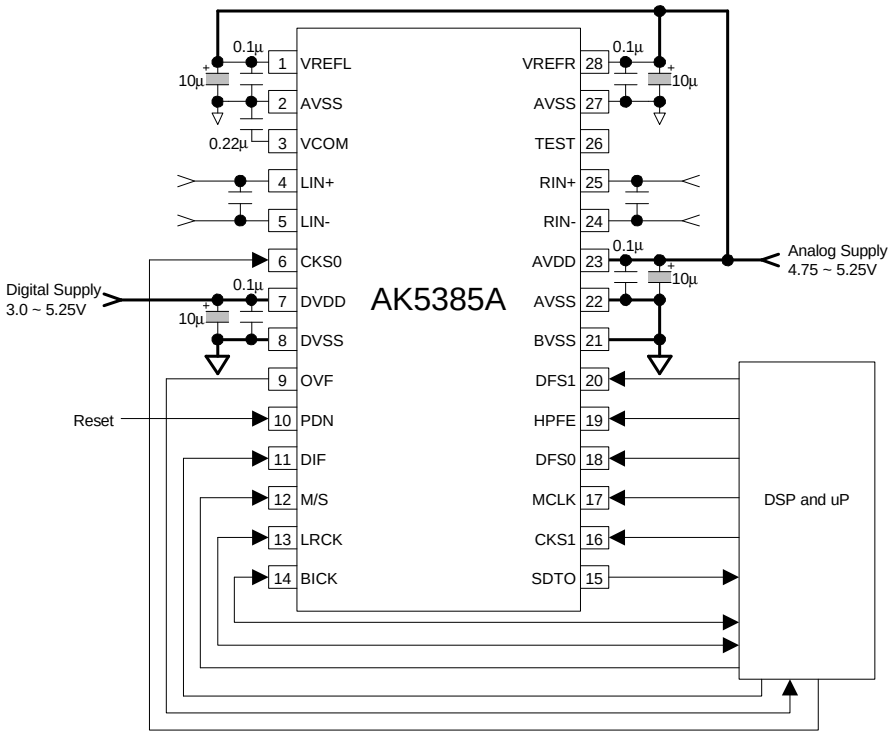
(3) ƒpƒ••[ƒ_ƒEƒ“ŽžADC•o—Í,Í“0”ƒf•[ƒ^,Å,·•B

(4) ŠeƒNƒ•ƒbƒN(MCLK, BICK, LRCK),Ì“ü—Í,ðŽ~,ß,é•ê•‡,Íƒpƒ••[ƒ_ƒEƒ“,µ,Ä‰º,³,¢•B

Figure 3. Power-down/up sequence example

ƒVƒXƒeƒ€•ÝŒv

Figure 4,ÍƒVƒXƒeƒ€•Ú‘±—á,Å,·•B‹ï‘Ì“I,È‰ñ˜H,Æ‘ª’è—á,É,Â,¢,Ä,Í•]‰¿ƒ{•[ƒh(AKD5385A),ðŽQ•Æ,µ,Ä‰º,³,¢•B



’•:

- AK5385A,Ì AVSS, BVSS, DVSS,ÆŽü•ÓƒRƒ“ƒgƒ•[ƒ‰“™,ÌƒOƒ‰ƒ“ƒh,Í•ª,¯,Ä”z•ü,µ,Ä‰º,³,¢•B
- ƒvƒ‹ƒ_ƒEƒ“ƒs“ (CKS0, CKS1, TEST pin)ˆÈŠO,ÌƒfƒBƒWƒ^ƒ‹“—ƒs“,ÍƒI•[ƒv“,É,µ,È,¢,Å‰º,³,¢•B

Figure 4. Typical Connection Diagram

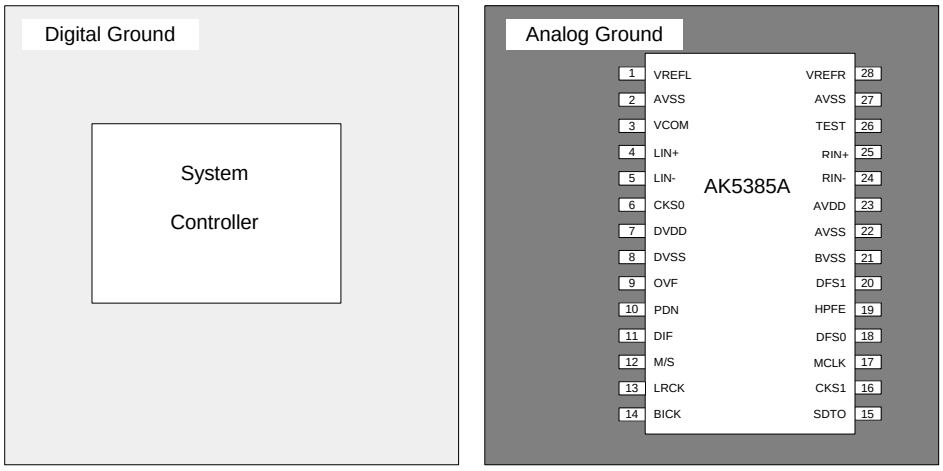


Figure 5.Ground Layout

’•:

- AVSS, BVSS, DVSS,Í“¯,¶ƒAƒiƒ•ƒOƒOƒ‰ƒ“ƒh,É•Ú‘±,µ,Ä‰º,³,¢•B

1. ƒOƒ‰ƒ“ƒh,Æ“dŒ¹,ÌƒƒJƒbƒvƒŠƒ“ƒO

“dŒ¹,ÆƒOƒ‰ƒ“ƒh,ÌŽæ,è•û,É,Í•\•ª’•ˆÓ,µ,Ä‰º,³,¢•B AVDD, DVDD,ª•Ê“dŒ¹,Å‹Ÿ‹‹,³,ê,é•ê•‡,É,Í•A“dŒ¹—§,¿•ã,°ƒV•[ƒPƒ“ƒX,ð•l,¦,é•K—v,Í, ,è,Ü,¹,ñ•B **AVSS, BVSS, DVSS,ÍƒAƒiƒ•ƒOƒOƒ‰ƒ“ƒh,É•Ú‘±,µ,Ä‰º,³,¢•BƒVƒXƒeƒ€,ÌƒOƒ‰ƒ“ƒh,ÍƒAƒiƒ•ƒO,ÆƒfƒBƒWƒ^ƒ‹,Å•ª,¯,Ä”z•ü,µ**,Ä PC ƒ{•[ƒh•ã,Ì“dŒ¹,É‹ß,¢,Æ,±,ë,Å•Ú‘±,µ,Ä‰º,³,¢•B •¬—e—Ê,ÌƒƒJƒbƒvƒŠƒ“ƒOƒRƒ“ƒfƒ“ƒT,Í,È,é,×,-“dŒ¹ƒsƒ“,Ì‹ß,-,É•Ú‘±,µ,Ä‰º,³,¢•B

2. Šî•€“dˆ³

A/D•ÏŠ·,ÌŠî•€“dˆ³,Í VREFL/R pin,Ì“dˆ³,Æ AVSS pin,Ì“dˆ³,Ì•·,Å,·•B AVSS pin,ÍƒAƒiƒ•ƒOƒOƒ‰ƒ“ƒh,É•Ú‘±,µ•A VREFL/R pin,É,Í“dŒ¹,Æ“¯—l•A•‚Žü”gƒmƒCƒY,ð•œ‹Ž,·,é,½,ß,É 0.1µF,ÌƒZƒ‰ƒ~ƒbƒNƒRƒ“ƒfƒ“ƒT,Æ 10µFˆÈ•ã,Ì“d‰ðƒRƒ“ƒfƒ“ƒT,ð VREFL/R pin,Æ AVSS ŠÔ,É•Ú‘±,µ,Ä‰º,³,¢•B“Á,ÉƒZƒ‰ƒ~ƒbƒNƒRƒ“ƒfƒ“ƒT,Íƒsƒ“,É,Å,«,é,¾,¯‹ß,Ã,¯,Ä•Ú‘±,µ,Ä‰º,³,¢•B,³,ç,ÉƒfƒBƒWƒ^ƒ‹•M•†•A“Á,ÉƒNƒ•ƒbƒN,Í•Ï’²Ší,Ö,ÌƒJƒbƒvƒŠƒ“ƒO,ð”ð,¯,é,½,ß,É VREFL/R pin,©,ç,Å,«,é,¾,¯—£,µ,Ä‰º,³,¢•B

VCOM,ÍƒAƒiƒ•ƒO•M•†,ÌƒRƒ,ƒ““dˆ³,Æ,µ,ÄŽg,í,ê,Ü,·•B,±,Ìƒsƒ“,É,Í•‚Žü”gƒmƒCƒY,ð•œ‹Ž,·,é,½,ß,É 0.22µF ’ö“x,ÌƒZƒ‰ƒ~ƒbƒNƒRƒ“ƒfƒ“ƒT,ð AVSS,Æ,ÌŠÔ,É•Ú‘±,µ,Ä‰º,³,¢•B“Á,É•AƒZƒ‰ƒ~ƒbƒNƒRƒ“ƒfƒ“ƒT,Íƒsƒ“,É,Å,«,é,¾,¯‹ß,Ã,¯,Ä•Ú‘±,µ,Ä‰º,³,¢•B VCOM pin,©,ç“d—¬,ðŽæ,Á,Ä,Í,¢,¯,Ü,¹,ñ•BƒfƒBƒWƒ^ƒ‹•M•†•A“Á,ÉƒNƒ•ƒbƒN,Í•Ï’²Ší,Ö,ÌƒJƒbƒvƒŠƒ“ƒO,ð”ð,¯,é,½,ß•A VCOM pin,©,ç,Å,«,é,¾,¯—£,µ,Ä‰º,³,¢•B

3. ƒAƒiƒ•ƒO“ü—Í

ƒAƒiƒ•ƒO“ü—Í•M•†,ÍŠeƒ`ƒƒƒlƒ‹,Å·“®“ü—Íƒsƒ“,©,ç•Ï’²Ší,É“ü—Í,³,ê,Ü,·•B“ü—Í“dˆ³,Í LIN+(RIN+),Æ LIN–(RIN–),Ì•·,Ì“dˆ³,É,È,è,Ü,·•B“ü—ÍƒŒƒ“ƒW,Í ±2.9Vpp (typ),Å,·•B AK5385A,Í AVSS,©,ç AVDD,Ü,Å,Ì“dˆ³,ð“ü—Í,·,é,±,Æ,ª,Å,«,Ü,·•B•o—ÍƒR•[ƒh,ÌƒtƒH•[ƒ}ƒbƒg,Í 2’sƒRƒ“ƒvƒŠƒ•ƒ“ƒg,Å,·•B DCƒIƒtƒZƒbƒg (ADCŽ©‘Ì,Ì DCƒIƒtƒZƒbƒg,àŠÜ,Þ),Í“à‘ ,Ì HPF,ÅƒLƒƒƒ“ƒZƒ‹,³,ê,Ü,·•B

AK5385A,Í 128fs (6.144MHz@fs=48kHz, Normal Speed Mode),ÅƒAƒiƒ•ƒO“ü—Í,ðƒTƒ“ƒvƒŠƒ“ƒO,µ,Ü,·•BƒfƒBƒWƒ^ƒ‹ƒtƒBƒ‹ƒ^,Í•A 128fs,Ì•®•”"{•t‹ß,Ì‘Ñˆæ,ð•œ,-‘jŽ~ˆæˆÈ•ã,ÌƒmƒCƒY,ð‘S,Ä•œ‹Ž,µ,Ü,·•B,Ù,Æ,ñ,Ç,ÌƒI•[ƒfƒBƒI•M•†,Å,Í 128fs•t‹ß,É‘å,«,ÈƒmƒCƒY,ðŽ•,Â,±,Æ,Í, ,è,Ü,¹,ñ,Ì,Å•A ŠÈ’P,È RCƒtƒBƒ‹ƒ^,Å 128fs•t‹ß,ÌƒmƒCƒY,ð•\•ª,ÉŒ¸•Š,³,¹,é,±,Æ,ª,Å,«,Ü,·•B

AK5385A,ÌƒAƒiƒ•ƒO“dŒ¹“dˆ³,Í +5V,É,È,Á,Ä,¨,è•AƒAƒiƒ•ƒO“ü—Íƒsƒ“ (LIN+/–, RIN+/–),É,Í•A AVDD+0.3VˆÈ•ã•A AVSS–0.3VˆÈ‰º,Ì“dˆ³,Æ 10mAˆÈ•ã,Ì“d—¬,ð“ü—Í,µ,Ä,Í,¢,¯,Ü,¹,ñ•B‰ß‘å“d—¬,Ì—¬“ü,Í“à•”,Ì•ÛŒì‰ñ˜H,Ì”j‰ó•A,³,ç,É,Íƒ‰ƒbƒ`ƒAƒbƒv,ðˆø,«‹N,±,µ•AIC,Ì”j‰ó,ÉŽŠ,è,Ü,·•B•],Á,Ä•AŽü•Ó,ÌƒAƒiƒ•ƒO‰ñ˜H,Ì“dŒ¹“dˆ³,ª•A ±15V“™,Ì•ê•‡,ÍƒAƒiƒ•ƒO“ü—Íƒsƒ“,ð•â‘Î•Å‘å’èŠiˆÈ•ã,Ì•M•†,©,ç•ÛŒì,·,é•K—v,ª, ,è,Ü,·•B

4. ŠO•”ƒAƒiƒ•ƒO“ü—Í‰ñ˜H—á

Figure 6,Í“ü—ÍƒofbftƒC@‰ñ˜H—á,Å,·•B”½“]•E”½“]‰ñ˜H,É,æ,éƒQƒCƒ“dB,Ì•·“®“ü—Í‰ñ˜H,Å,·LIN+/–(RIN+/–) ŠÔ,Ì10nF,Í•A•Ï²Ší,ÌƒNƒ•ƒbƒNftfB•[ƒhƒXƒ‹•[,ðŽæ,é,½,ß,ÌƒRƒ“fff“ƒT,Å,·•B,Ü,½•A22Ω ∅ ≠ ⊗3ϕ0kHz ,ÌƒJƒbƒgƒIft,ðŽ•,Â LPF,É,È,Á,Ä,¢,Ü,·•B‘O’iƒAƒ“ƒv,Í–ñ 370kHz,ÌƒJ ƒbƒgƒIft,ðŽ•,ÂLPF,É,È,Á,Ä,¢,Ü,·•B•Ú •×,Í•]‰¿ƒ{•[ƒh,ðŽQ•Æ,µ,Ä‰º,³,¢•B

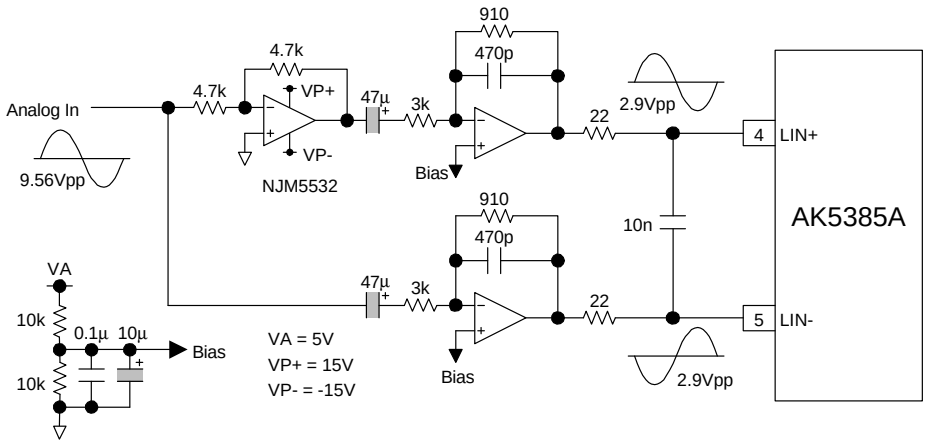


Figure 6.Input Buffer example

Figure 7,Í AK5385A,ÌƒAƒiƒ•ƒO“ü—Í‰ñ˜H2(1st order HPF: fc=0.66Hz, Table 6; 1st order LPF: fc=590kHz, gain=–14dB, Table 7),Å,·•BƒVƒ“ƒOƒ‹ƒGƒ“ƒh,Å“ü—Í,·,é•ê•‡,Í•·“®“ü—Í,·,é•ê•‡,Æ”äŠr,µ,Ä”½“]ƒofbftƒ@,ª^ê ,Â‘•,¦,Ü,·•BFigure 7,Å,ÍƒVƒ“ƒOƒ‹ƒGƒ“ƒh,Ì•ê•‡,ÍJP1, 2,ðƒVƒ‡•[ƒg•A•·“®,Ì•ê•‡,ÍJP1, 2,ðƒI•[ƒvƒ“,É,µ,Ü,·•B ,±,Ì‰ñ˜H,Ì“ü—ÍƒŒfxƒ‹,Í+/–14.7Vpp,Å,·•B

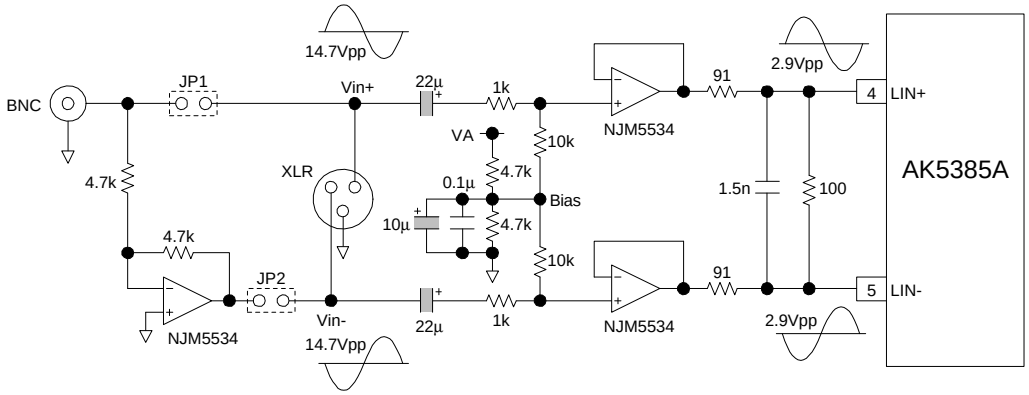


Figure 7.Input Buffer example

fin	1Hz	10Hz
Frequency Response	–1.56dB	–0.02dB

Table 6. Frequency Response of HPF

fin	20kHz	40kHz	6.144MHz
Frequency Response	–0.005dB	–0.02dB	–15.6dB

Table 7. Frequency Response of LPF

5. ‘ª’è—á

Figure 8,Í VREFL/R pin,É0.1µF,ÌƒRƒ“ƒfƒ“ƒT,Æ•À—ñ,É•Ú‘±,³,ê,éƒRƒ“ƒfƒ“ƒT,Ì—e—Ê,ªS/(N+D),ÌŠÖŒW,ðŽ¦,µ,½,à,Ì,Å,·•B‰¡Ž²,ªƒRƒ“ƒfƒ“ƒT,Ì—e—Ê•A•cŽ²,ª˜c“Á•«,Å,·•B

[‘ª’è•ðŒ¶]

- EAVDD = 5.0V, DVDD = 3.3V; AVSS = BVSS = DVSS = 0V
- Efs = 48kHz
- E‘ª’è‘Ñ ˆæ = 10Hz ~ 20kHz
- ETa = 25°C
- EAudio Precision System Two CascadeŽg—p

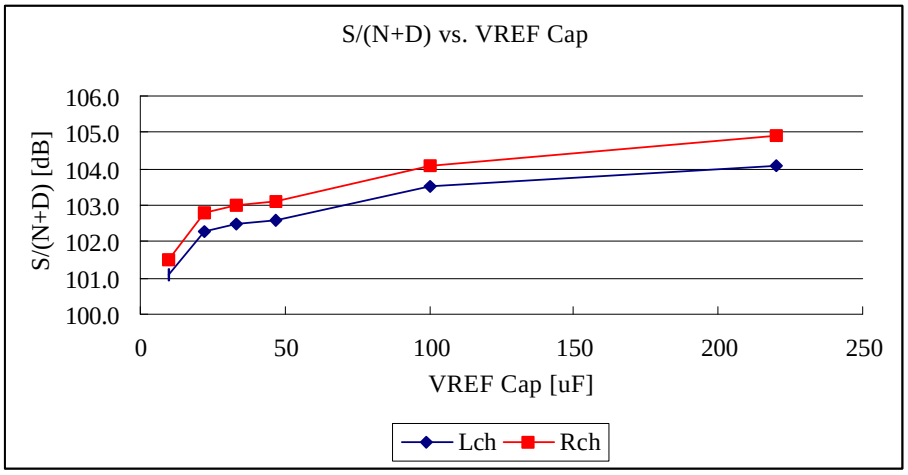


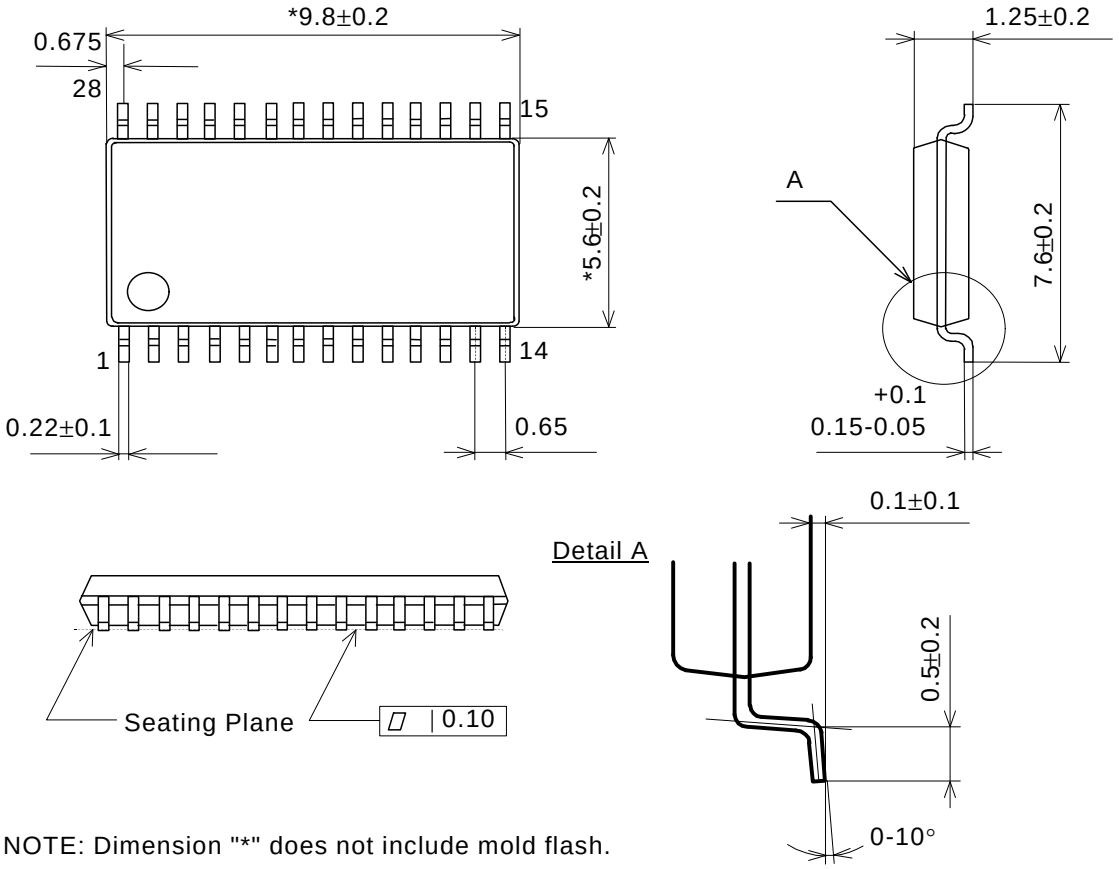
Figure 8. S/(N+D) vs. VREF Cap

6. •¡•”ƒfƒoƒCƒX,Ì“¯Šú

AK5385A,ðƒVƒXƒef€•ã,Å•¡•”ŒÂŽg,¢,·,é•ê•‡•AŠeƒfƒoƒCƒXŠÔ,Å“¯Žž,ÉƒTƒ“ƒvƒŠƒ“ƒO,·,é,½,ß,É,Í’•ˆÓ,ª•K—v,Å,·•B“¯ŠúƒTƒ“ƒvƒŠƒ“ƒO,·,é,½,ß,É,Í•AMCLK,ÆLRCK,ÍƒVƒXƒef€•ã,ÌAK5385A‘S,Ä,É‘Î,µ,Ä“¯,¶ƒ^ƒCƒ~ƒ“ƒO,Å, ,é•K—v,ª, ,è,Ü,·•BƒVƒXƒef€•ã,Ì‘S,Ä,Ì AK5385A,ð“¯,¶ƒNƒ•ƒbƒNƒGƒbƒW‚ÅD•ÏŠ·,³,¹,é,½,ß,É,Í•A AK5385A,Ö,ÌƒŠƒZƒbƒg•M•†,MCLK,ÌƒGƒbƒW,É•d,È,ç,È,¢,æ,¤,É,µ,Ä•A“¯Žž,ÉƒŠƒZƒbƒg,ð•s,Á,Ä‰º,³,¢•B

fpfbfP•[fW**(AK5385AVF)**

28pin VSOP (Unit: mm)



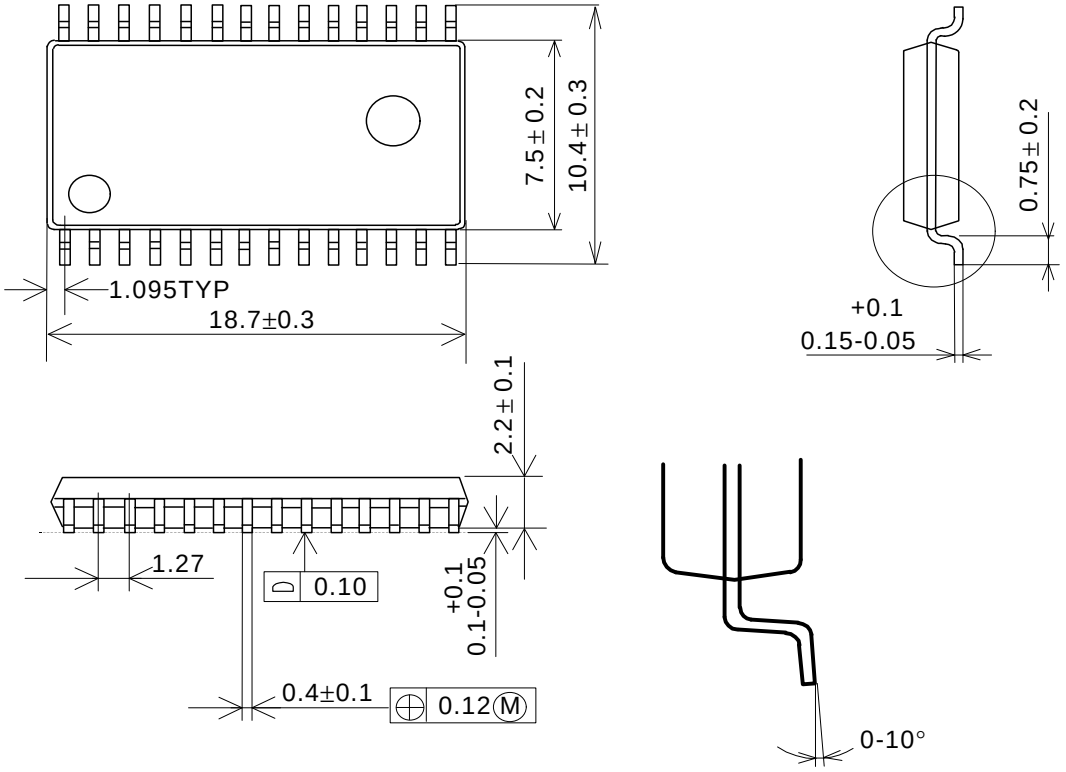
NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

fpfbfP•[fW**(AK5385AVS)**

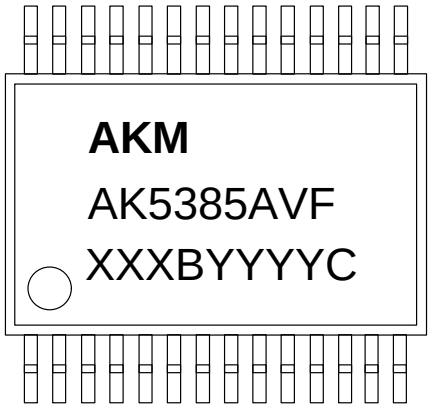
28pin SOP (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

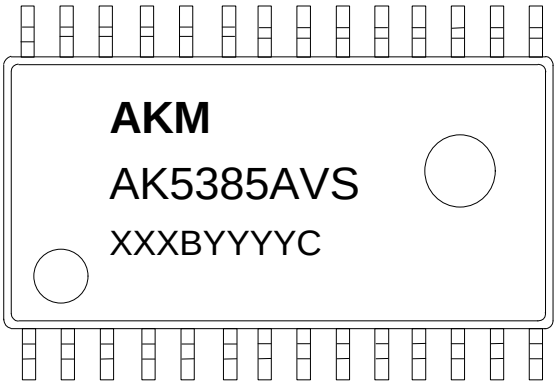
ƒ}•[ƒLƒ“ƒO **(AK5385AVF)**



XXXBYYYYC Date code identifier

XXXB :Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)

f}•[fLf“fO **(AK5385AVS)**



XXXBYYYYC Date code identifier

XXXB :Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)

•d—v,È’•^ÓŽ–•€

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