L4993

Low drop voltage regulator

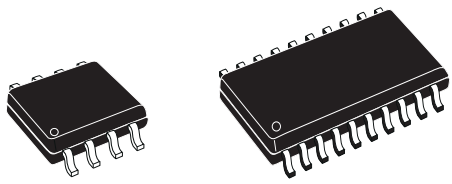
Preliminary Data

Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_0	+/-2%
Max dropout voltage	V_{dp}	400 mV
Output current	I_0	150 mA
Quiescent current	I_{qn}	79 µA(1)

1. Typical value with regulator disabled

- Operating DC supply voltage range 5.6V to 31V
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range (T_j = -40°C to 150°C)



SO-8 SO-20

Description

The L4993 is a monolithic integrated 5V Voltage regulator with a low drop voltage at currents up to 150mA.The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4993 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4993 is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
SO8	L4993D	L4993DTR
SO20 (16+2+2)	L4993MD	L4993MDTR

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1 Block diagram and pins description

Figure 1. Block diagram

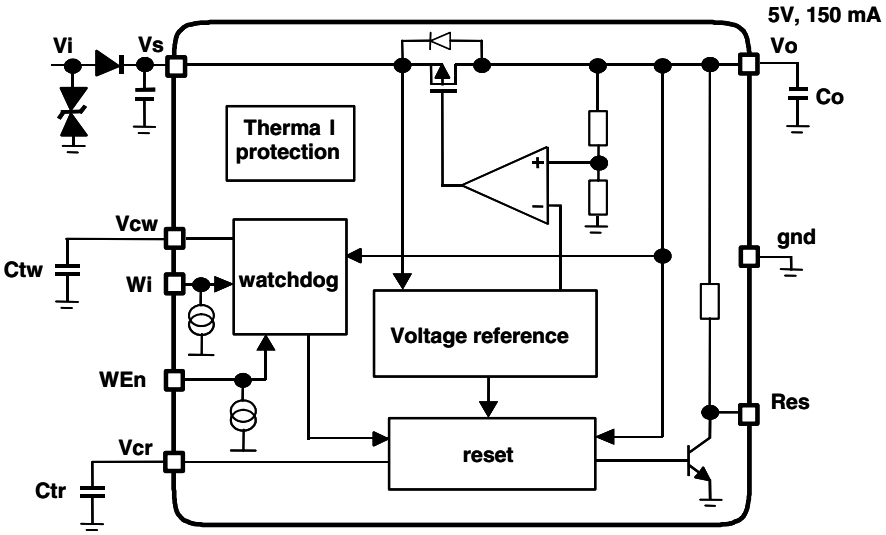
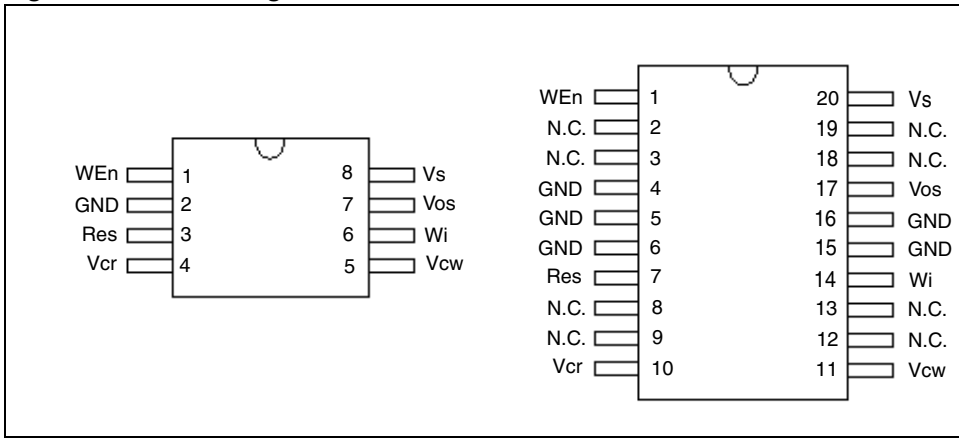


Table 2. Pins description

Pin name	SO8(D)	S020(MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
Vo_s	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2. Pins configuration



2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{Vsdc}	DC supply voltage	-0.3 to 40	V
I_{Vsdc}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to V_{Vo} + 0.3	V
V_{od}	Open drain output voltage	-0.3 to V_{Vo} + 0.3	V
I_{od}	Open drain output current	Internally limited	
V_{cr}	Reset delay voltage	-0.3 to V_{Vo} + 0.3	V
V_{cw}	Watchdog delay voltage	-0.3 to V_{Vo} + 0.3	V
V_{WEn}	Watchdog Enable input voltage	-0.3 to V_{Vo} +0.3	V
T_j	Junction temperature	-40 to 150	“C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	S08	S016+2+2	Unit
$R_{th\text{-}jamb}$	Thermal resistance Junction to Ambient (S08)	130(1)	51(2)	°C/W

1. See *Figure 7*
2. See *Figure 11*

2.3 Electrical characteristics

V_s =5.6V to 31V, T_j= -40°C to +150°C unless otherwise specified

Table 5. Electrical characteristics

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
5V Voltage regulator							
Vo	V_{o_ref}	Output voltage	Vs = 6 to 31V Io = 1 to 150mA	4.9	5.0	5.1	V
Vo	I_{short}	Short circuit current	Vs = 13.5V(1)	150	280	4000	mA
Vo	I_{lim}	Output current limitation	Vs = 13.5V(1)	150	320	500	mA
Vs, Vo	V_{line}	Line regulation voltage	Vs = 6 to 31V Io = 1 to 150mA			25	mV
Vo	V_{load}	Load regulation voltage	Io = 1 to 150mA			25	mV
Vs, Vo	V_{dp}	Drop voltage	Io = 150mA		200	400	mV
Vs, Vo	SVR	Ripple rejection	fr = 100 Hz(2)	55			dB
General							
Vs, Vo	I_q	Quiescent current	Vs=13.5V, Io=150mA, WEn = high		1.45	2	mA
Vs, Vo	I_q	Quiescent current	Vs=13.5V, Io= 50mA, WEn = high		538	1000	µA
Vs, Vo	I_q	Quiescent current	Vs=13.5V, Io< 1mA, WEn = high		120	180	µA
Vs, Vo	I_q	Quiescent current	Vs=13.5V, Io< 1mA, WEn = low		79	125	µA
	Tw	Thermal protection temperature		150		190	°C
	Tw_hy	Thermal protection temperature hysteresis			10		°C
Reset							
Res	Vres_l	Reset output low voltage	R_{ext} = 5kΩ to Vo, Vo > 1V			0.4	V
Res	I_{Res_h}	Reset output high leakage current	V_{Res} = 5V			1	µA
Res	R_p_u	Pull up internal resistance	with respect to Vo	12	25	50	kΩ
Res	Vo_th	Vo out of regulation threshold	Vs = 6 to 31V, Io = 1 to 150mA	6%	8%	10%	below V_{o_ref}

Table 5. Electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
Vcr	Vrlth	Reset timing low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset timing high threshold	Vs =13.5V	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	Vs = 13.5V	8	17.6	30	µA
Vcr	Idr	Discharge current	Vs = 13.5V	8	17.6	30	µA
Res	Trr_2	Reset reaction time(3)	Vo = V_{o_th} -100mV	100	275	1000	µs
Res	Trd	Reset delay time	Vs = 13.5V, Ctr = 1nF	65		150	ms
Watchdog							
Wi	Vih	Input high voltage	Vs = 13.5V	3.5			V
Wi	Vil	Input low voltage	Vs = 13.5V			1.5	V
Wi	Vih_hyst	Input hysteresis	Vs = 13.5V		500		mV
Wi	Ii	Pull down current	Vs = 13.5V		10	20	µA
Vcw	Vwhth	High threshold	Vs = 13.5V	2.20	2.35	2.50	V
Vcw	Vwlth	Low threshold	Vs = 13.5V	0.50	0.65	0.80	V
Vcw	Icwc	Charge current	Vs = 13.5V, Vcw = 0.1V	4	8	14	µA
Vcw	Icwd	Discharge current	Vs = 13.5V, Vcw = 2.5V	1.0	2.13	4.5	µA
Vcw	Twop	Watchdog period	Vs = 13.5V, Ctw = 47nF	25	50	90	ms
Res	twol	Watchdog output low time	Vs = 13.5V, Ctw = 47nF	6	10.5	22	ms
Watchdog Enable							
WEn	V_{En_l}	Enable input low voltage				1	V
WEn	V_{En_h}	Enable input high voltage		3			V
WEn	V_{En_hy}	Enable input hysteresis		500	800	1100	mV
WEn	I_leak	Pull down current	WEn = 5V	2	8	20	µA

1. See *Figure 3*
2. Guaranteed by design
3. When Vo becomes lower than 4V, the reset reaction time decreases down to 2µs assuring a faster reset condition in this particular case.

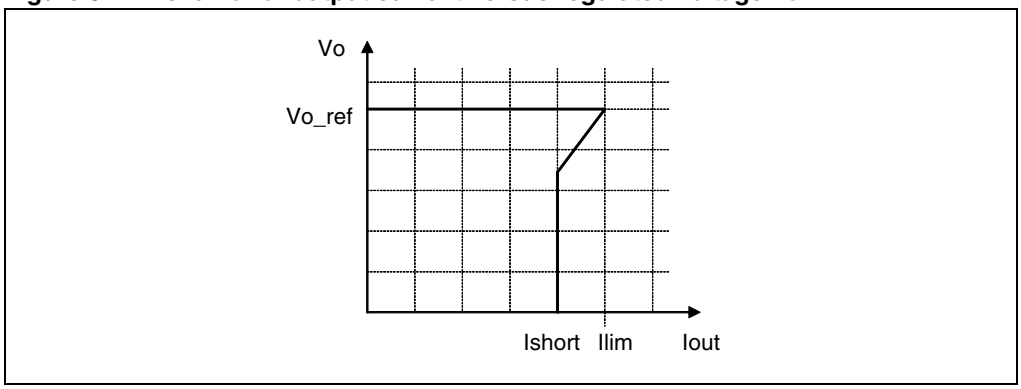
3 Application information

The input capacitor Cs > 200nF is necessary for the smoothing of line disturbances. The output capacitor C01 > 100nF is necessary for the stabilityy of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended put an additional electrolytic capacitor C02 > 10µF at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 150mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

Figure 3. Behavior of output current versus regulated voltage Vo



3.2 Reset

The reset circuit monitors the output voltage Vo. If the output voltage becomes lower than Vo_th then Res goes low with a delay time trr. If the output voltage becomes lower than 2.0 V (typ) than Res goes immediately low. The reset low signal is guaranteed for an output voltage Vo greater than 1V.

When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by 512 periods of oscillator. The oscillator period is given by :

$$Tosc = [(Vrhth-Vrlth) \times Ctr] / Icr + [(Vrhth-Vrlth) \times Ctr] / Idr$$

and reset pulse delay trd is given by:

$$trd = 512 \times Tosc$$

where:

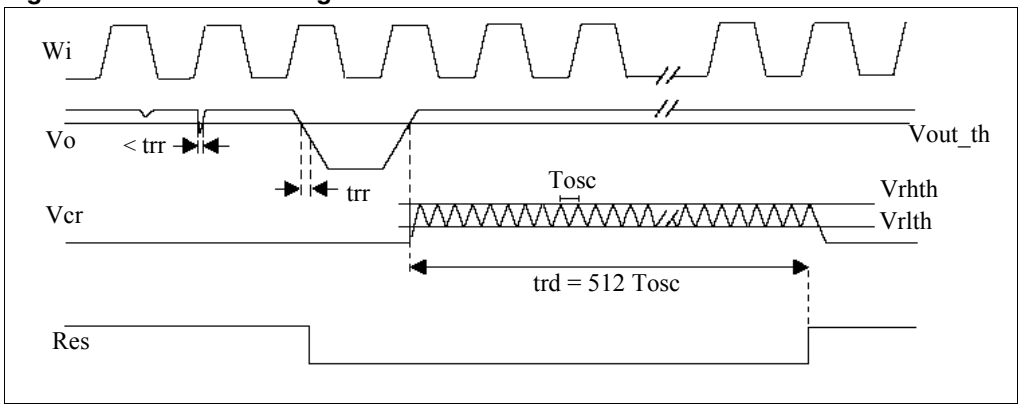
Icr = 17.6 µA is an internally generated charge current,

Idr = 17.6 µA is an internally generated discharge current,

Vrhth = 2.35 V (typ) and Vrlth =0.65 V (typ) are two voltage thresholds

Ctr is an external capacitance.

Figure 4. Reset time diagram



3.3 Watchdog

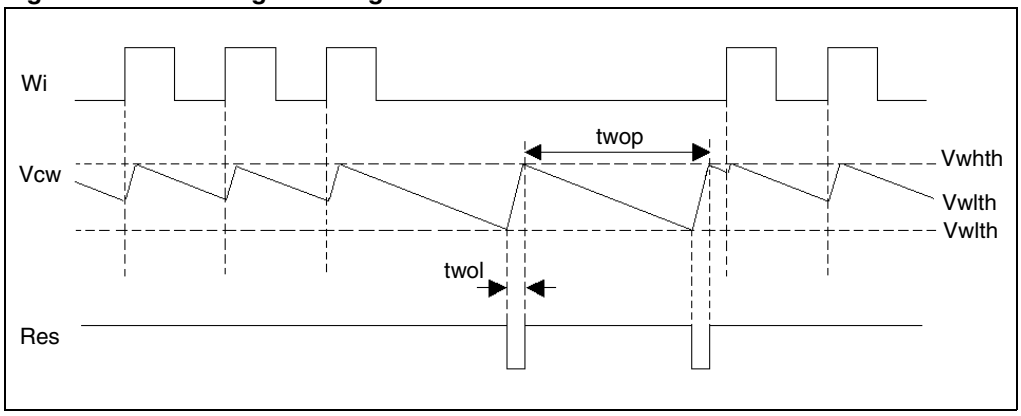
The watchdog input Wi monitors a connected microcontroller. If pulses are missing, the Reset output pin is set to low. This functionality can be disabled setting WEn input to a level low. The pulse sequence time can be ajusted within a wide range with the external capacitor Ctw. The watchdog circuit discharges the capacitor Ctw with a constant current Icwd. If the lower threshold Vwlth is reached, a watchdog reset is generated. To prevent this reset condition, the microcontroller must generate a positive edge during the discharge phase of the capacitor before the voltage reaches the threshold Vwlth.

In order to calculate the minimum time Tdis during which the microcontroller must provide the positive edge, the following equation can be used:

$$(Vwhth-Vwlth) \times Ctw = Icwd \times Tdis$$

Every Wi positive edge switches the current source from discharging to charging, the same happens when the lower threshold is reached. When the voltage reaches the upper threshold Vwhth the current switches from charging to discharging. The result is a sawtooth waveform at the watchdog timer capacitor Ctw.

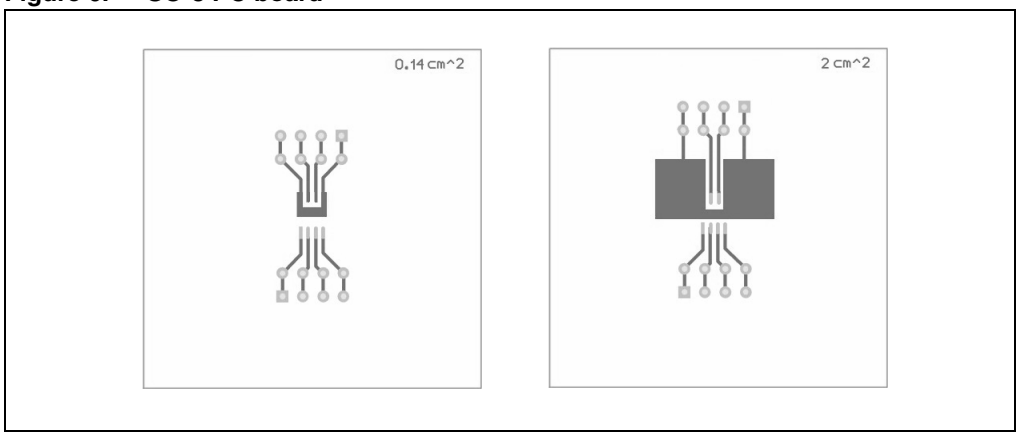
Figure 5. Watchdog time diagram



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 6. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm , Copper areas: from minimum pad lay-out to 8cm^2)

Figure 7. SO-8 $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

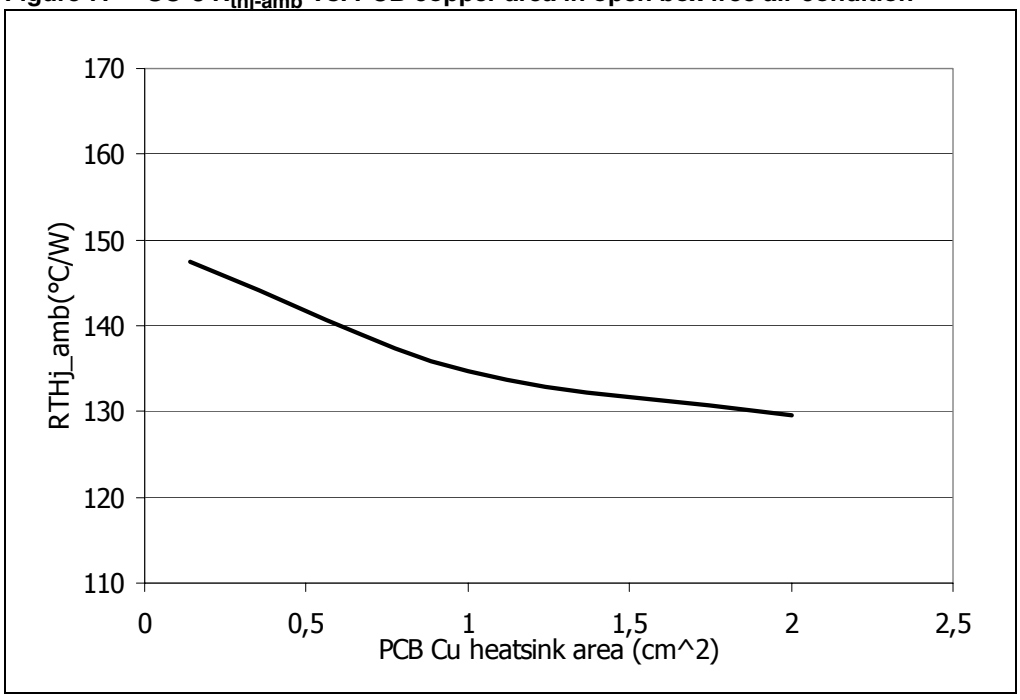
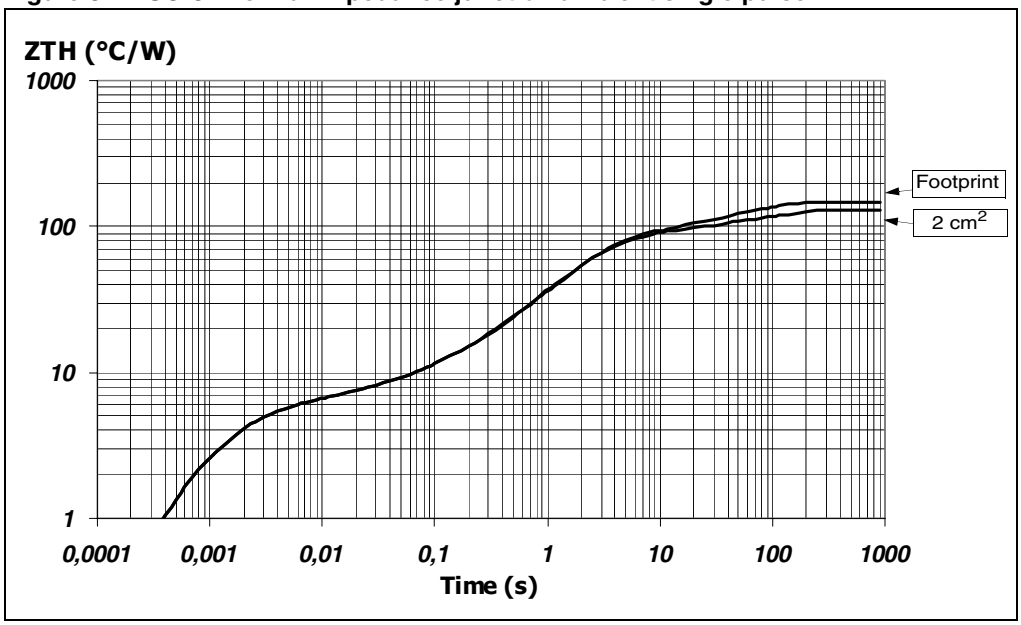


Figure 8. SO-8 Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 9. SO-8 Thermal fitting model of a single channel

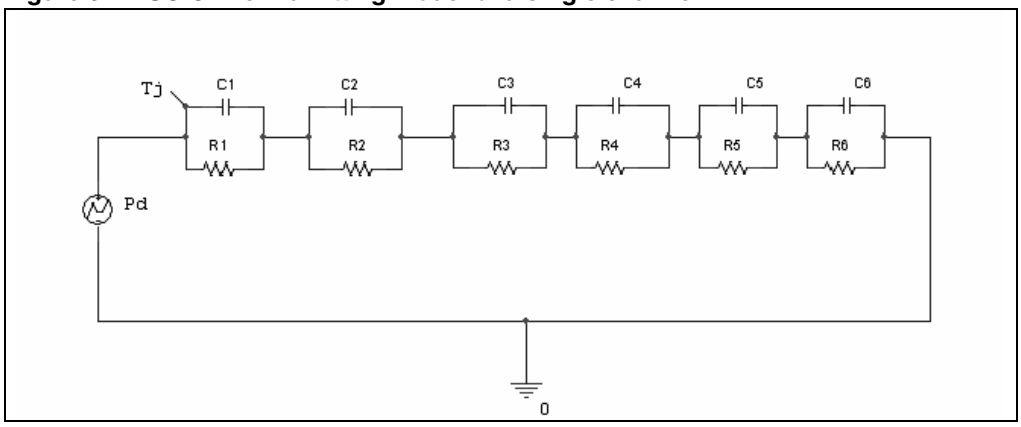
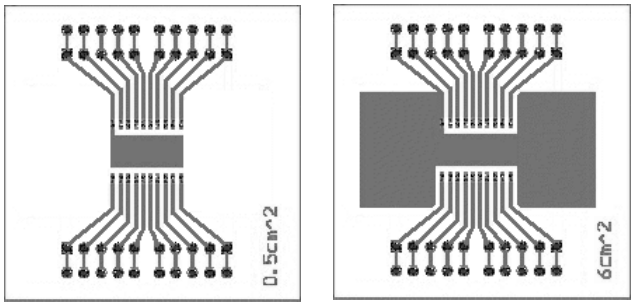


Table 6. SO-8 Thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

4.2 SO-20 thermal data

Figure 10. SO-20 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm,PCB thickness = 2mm, Cu thickness=35µm , Copper areas: from minimum pad lay-out to 8cm^2).

Figure 11. SO-20 $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

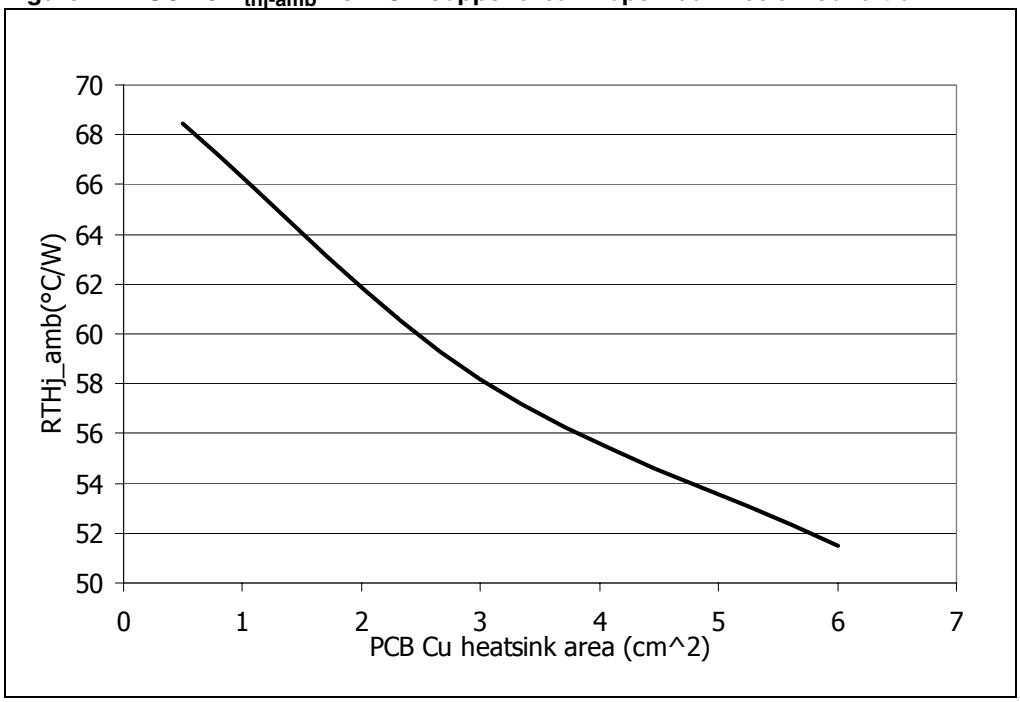
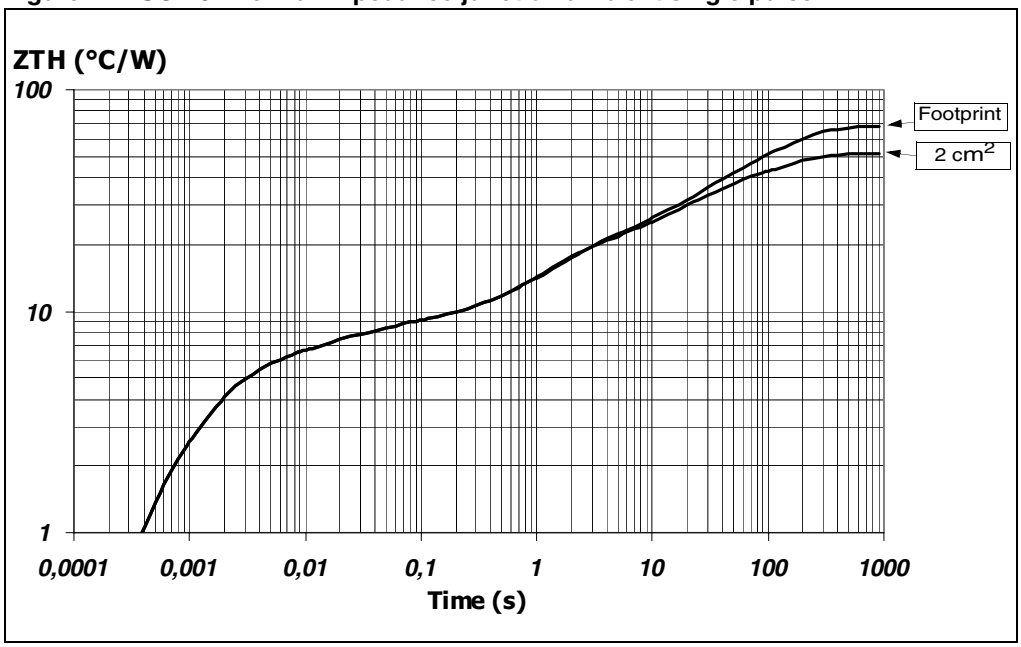


Figure 12. SO-20 Thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 13. SO-20 Thermal fitting model of a single channel

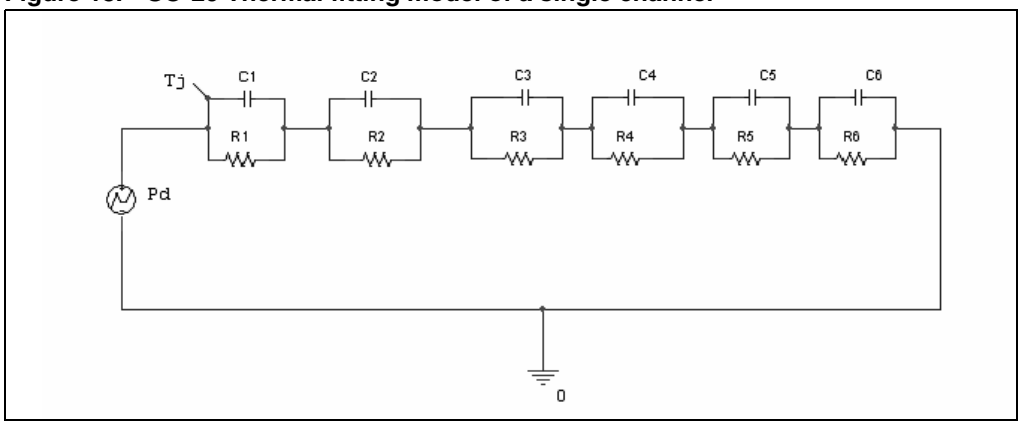


Table 7. SO-20 Thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

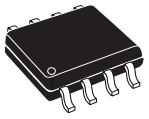
5.2 SO-8 Package mechanical data

Figure 14. SO-8 Package mechanical data & package outline

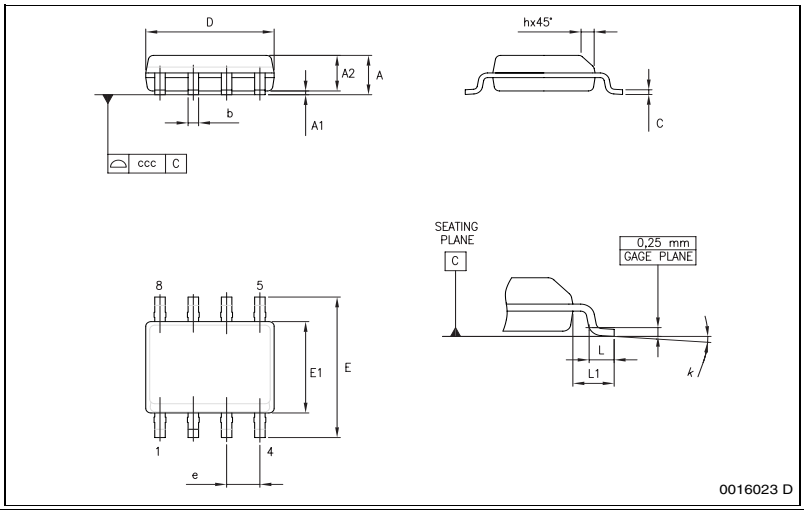
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D (1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.100			0.0039

Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

OUTLINE AND MECHANICAL DATA



SO-8



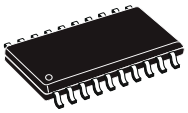
5.3 SO-20 Package mechanical data

Figure 15. SO-20 Package mechanical data & package outline

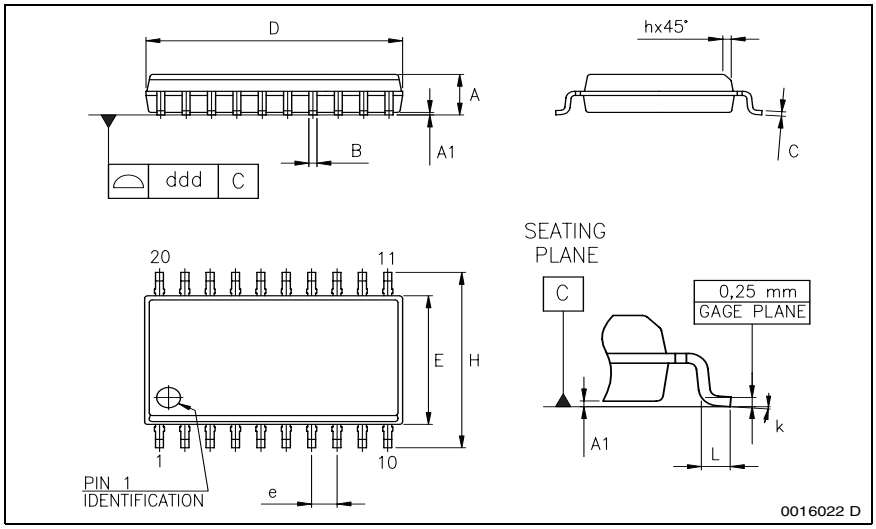
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

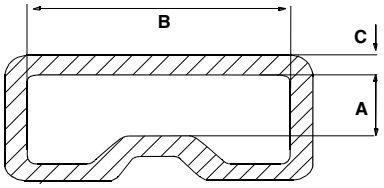


SO20



5.4 SO-8 Packing information

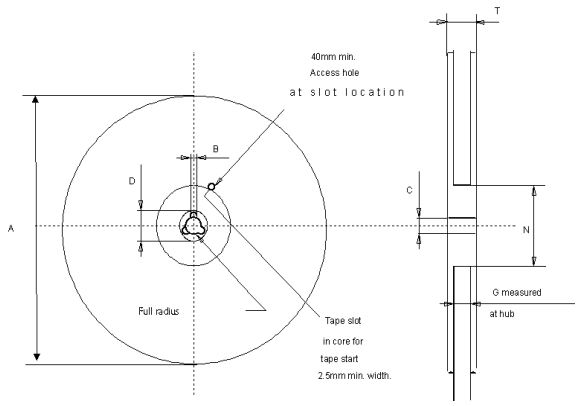
Figure 16. SO-8 Tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 17. SO-8 Tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

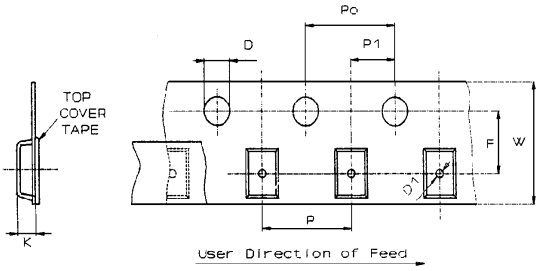
All dimensions are in mm.

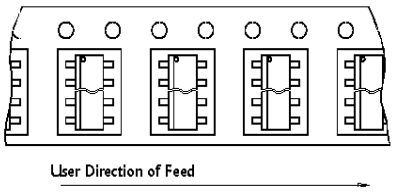
TAPE DIMENSIONS

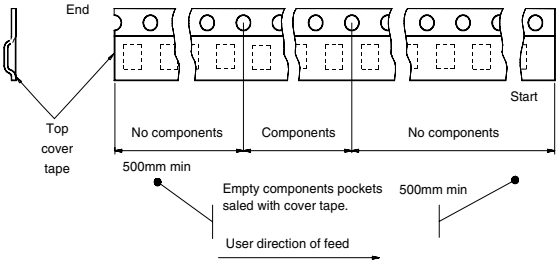
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

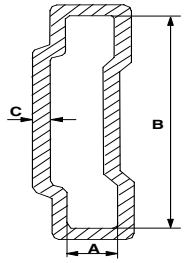






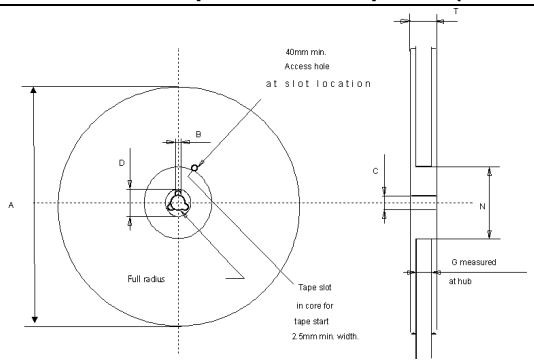
5.5 SO-20 Packing information

Figure 18. SO-20 Tube shipment (no suffix)



Base Q.ty	40
Bulk Q.ty	800
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

Figure 19. SO-20 Tape and reel shipment (suffix "TR")



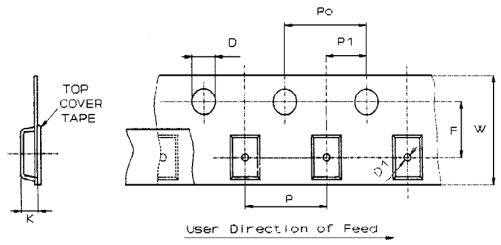
Reel dimensions

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
D	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

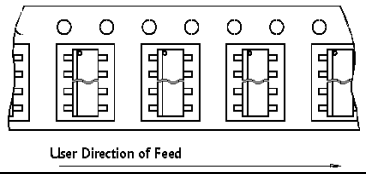
Tape dimensions

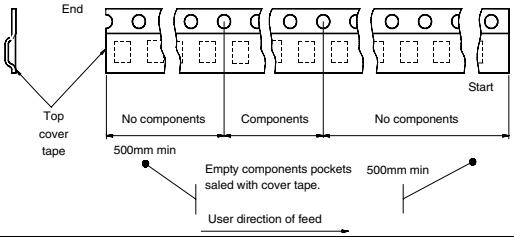
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2



All dimensions are in mm.





6 Revision history

Table 8. Document revision history

Date	Revision	Changes
June-2004	1	Initial release.
18-Jan-2007	2	Table 5, 6, 7 and 8 updated
01-Jun-2007	3	Document put in corporate technical literature template. Table 4 updated
22-Aug-2007	4	*Table 5: Electrical characteristics*: I_{short}, I_{lim}, I_q, T_{rr2}, V_{ih_hist} parameters updated
29-Aug-2007	5	List of tables and figures added. *Section 4: Package and PCB thermal data* added.

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