TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

Lead-Free

256Mbits Network FCRAM1
– 4,194,304-WORDS × 4 BANKS × 16-BITS
– 8,388,608-WORDS × 4 BANKS × 8-BITS

DESCRIPTION

Network FCRAM™ is Double Data Rate Fast Cycle Random Access Memory. TC59LM814/06CTG are Network FCRAM™ containing 268,435,456 memory cells. TC59LM814CTG is organized as 4,194,304-words × 4 banks s× 16 bits, TC59LM806CTG is organized as 8,388,608 words × 4 banks × 8 bits. TC59LM814/06CTG feature a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. TC59LM814/06CTG can operate fast core cycle using the FCRAM™ core architecture compared with regular DDR SDRAM.

TC59LM814/06CTG is suitable for Network, Server and other applications where large memory density and low power consumption are required. The Output Driver for Network FCRAM™ is capable of high quality fast data transfer under light loading condition.

FEATURES

PARAMETER			TC59LM814/06	
			-50	-60
t_{CK}	Clock Cycle Time (min)	CL = 3	5.5 ns	6.5 ns
		CL = 4	5 ns	6 ns
t_{RC}	Random Read/Write Cycle Time (min)		25 ns	30 ns
t_{RAC}	Random Access Time (max)		22 ns	26 ns
I_{DD1S}	Operating Current (single bank) (max)		190 mA	170 mA
I_{DD2P}	Power Down Current (max)		2 mA	2 mA
I_{DD6}	Self-Refresh Current (max)		3 mA	3 mA

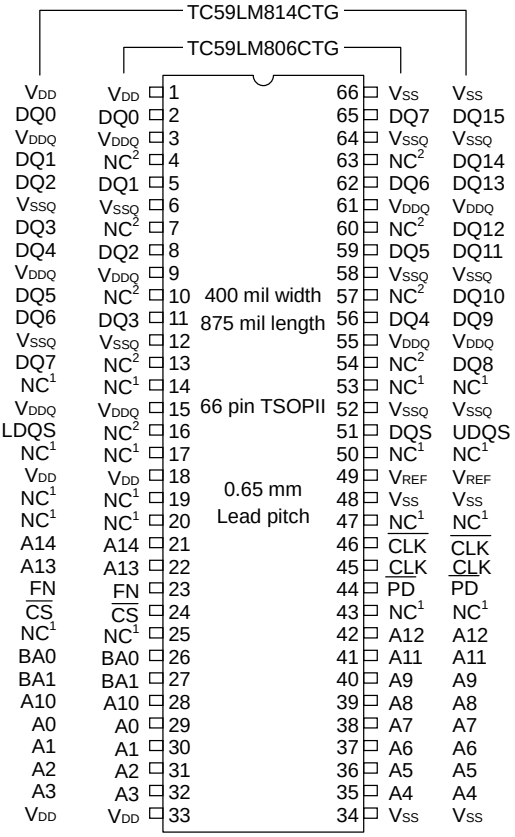
- Fully Synchronous Operation
  - Double Data Rate (DDR)
    Data input/output are synchronized with both edges of DQS.
  - Differential Clock (CLK and $\overline{\text{CLK}}$) inputs
    $\overline{\text{CS}}$, FN and all address input signals are sampled on the positive edge of CLK.
    Output data (DQs and DQS) is aligned to the crossings of CLK and $\overline{\text{CLK}}$.
- Fast clock cycle time of 5 ns minimum
  Clock: 200 MHz maximum
  Data: 400 Mbps/pin maximum
- Quad Independent Banks operation
- Fast cycle and Short Latency
- Bidirectional Data Strobe Signal
- Distributed Auto-Refresh cycle in 7.8 μs
- Self-Refresh
- Power Down Mode
- Variable Write Length Control
- Write Latency = $\overline{\text{CAS}}$ Latency-1
- Programable $\overline{\text{CAS}}$ Latency and Burst Length
  $\overline{\text{CAS}}$ Latency = 3, 4
  Burst Length = 2, 4
- Organization TC59LM814CTG: 4,194,304 words × 4 banks × 16 bits
  TC59LM806CTG: 8,388,608 words × 4 banks × 8 bits
- Power Supply Voltage V_{DD}: 2.5 V ± 0.15 V
  V_{DDQ}: 2.5 V ± 0.15 V
- 2.5 V CMOS I/O comply with SSTL_2 (half strength driver)
- Package: 400 × 875 mil, 66 pin TSOPII, 0.65 mm pin pitch (TSOPII66-P-400-0.65)
- Lead-Free

Notice: FCRAM is a trademark of Fujitsu Limited, Japan.

PIN NAMES

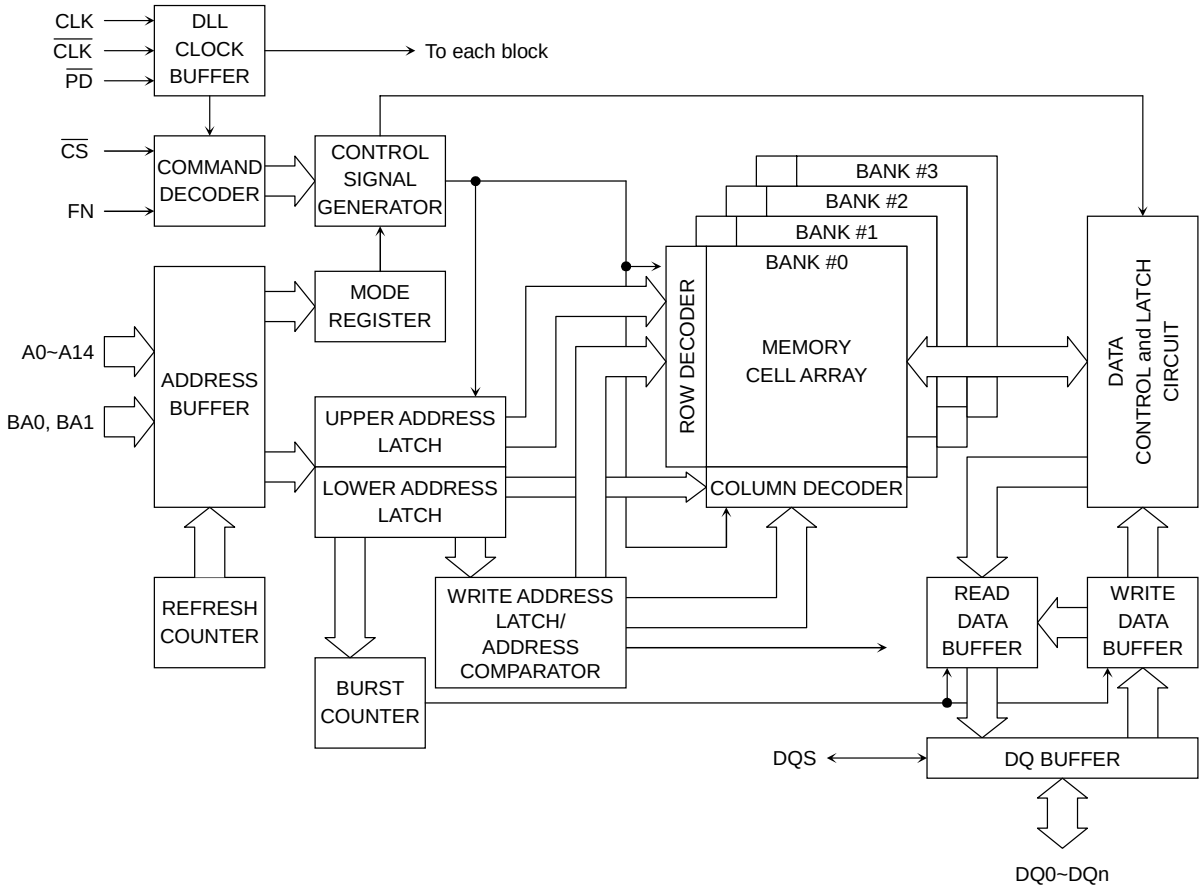
PIN	NAME
A0~A14	Address Input
BA0, BA1	Bank Address
DQ0~DQ7 (×8)	Data Input/Output
DQ0~DQ15 (×16)	
$\overline{CS}$	Chip Select
FN	Function Control
$\overline{PD}$	Power Down Control
CLK, $\overline{CLK}$	Clock Input
DQS (×8)	Write/Read Data Strobe
UDQS/LDQS (×16)	
V_{DD}	Power (+2.5 V)
V_{SS}	Ground
V_{DDQ}	Power (+2.5 V) (for I/O buffer)
V_{SSQ}	Ground (for I/O buffer)
V_{REF}	Reference Voltage
NC^1, NC^2	Not Connected

PIN ASSIGNMENT (TOP VIEW)



V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}
DQ0	DQ0	2	65	DQ7	DQ15
V_{DDQ}	V_{DDQ}	3	64	V_{SSQ}	V_{SSQ}
DQ1	NC^2	4	63	NC^2	DQ14
DQ2	DQ1	5	62	DQ6	DQ13
V_{SSQ}	V_{SSQ}	6	61	V_{DDQ}	V_{DDQ}
DQ3	NC^2	7	60	NC^2	DQ12
DQ4	DQ2	8	59	DQ5	DQ11
V_{DDQ}	V_{DDQ}	9	58	V_{SSQ}	V_{SSQ}
DQ5	NC^2	10	57	NC^2	DQ10
DQ6	DQ3	11	56	DQ4	DQ9
V_{SSQ}	V_{SSQ}	12	55	V_{DDQ}	V_{DDQ}
DQ7	NC^2	13	54	NC^2	DQ8
NC^1	NC^1	14	53	NC^1	NC^1
V_{DDQ}	V_{DDQ}	15	52	V_{SSQ}	V_{SSQ}
LDQS	NC^2	16	51	DQS	UDQS
NC^1	NC^1	17	50	NC^1	NC^1
V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}
NC^1	NC^1	19	48	V_{SS}	V_{SS}
NC^1	NC^1	20	47	NC^1	NC^1
A14	A14	21	46	$\overline{CLK}$	$\overline{CLK}$
A13	A13	22	45	CLK	CLK
FN	FN	23	44	$\overline{PD}$	$\overline{PD}$
$\overline{CS}$	$\overline{CS}$	24	43	NC^1	NC^1
NC^1	NC^1	25	42	A12	A12
BA0	BA0	26	41	A11	A11
BA1	BA1	27	40	A9	A9
A10	A10	28	39	A8	A8
A0	A0	29	38	A7	A7
A1	A1	30	37	A6	A6
A2	A2	31	36	A5	A5
A3	A3	32	35	A4	A4
V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}

BLOCK DIAGRAM



Note: The TC59LM806CTG configuration is 4Bank of 32768 × 256 × 8 of cell array with the DQ pins numbered DQ0~DQ7.
The TC59LM814CTG configuration is 4Bank of 32768 × 128 × 16 of cell array with the DQ pins numbered DQ0~DQ15.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT	NOTES
V_{DD}	Power Supply Voltage	−0.3~ 3.3	V	
V_{DDQ}	Power Supply Voltage (for I/O buffer)	−0.3~V_{DD}+ 0.3	V	
V_{IN}	Input Voltage	−0.3~V_{DD}+ 0.3	V	
V_{OUT}	DQ pin Voltage	−0.3~V_{DDQ} + 0.3	V	
V_{REF}	Input Reference Voltage	−0.3~3.3	V	
T_{opr}	Operating Temperature	0~70	°C	
T_{stg}	Storage Temperature	−55~150	°C	
T_{solder}	Soldering Temperature (10 s)	260	°C	
P_D	Power Dissipation	1	W	
I_{OUT}	Short Circuit Output Current	±50	mA	

Caution: Conditions outside the limits listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.
Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may affect device reliability.

RECOMMENDED DC, AC OPERATING CONDITIONS (Notes: 1)(Ta = 0°~70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.35	2.5	2.65	V	
V_{DDQ}	Power Supply Voltage (for I/O buffer)	2.35	V_{DD}	V_{DD}	V	
V_{REF}	Input Reference Voltage	$V_{DDQ}/2 \times 96\%$	$V_{DDQ}/2$	$V_{DDQ}/2 \times 104\%$	V	2
V_{IH} (DC)	Input DC High Voltage	V_{REF} + 0.2	—	V_{DDQ} + 0.2	V	5
V_{IL} (DC)	Input DC Low Voltage	−0.1	—	V_{REF} − 0.2	V	5
V_{ICK} (DC)	Differential Clock DC Input Voltage	−0.1	—	V_{DDQ} + 0.1	V	10
V_{ID} (DC)	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC)	0.4	—	V_{DDQ} + 0.2	V	7, 10
V_{IH} (AC)	Input AC High Voltage	V_{REF} + 0.35	—	V_{DDQ} + 0.2	V	3, 6
V_{IL} (AC)	Input AC Low Voltage	−0.1	—	V_{REF} − 0.35	V	4, 6
V_{ID} (AC)	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	0.7	—	V_{DDQ} + 0.2	V	7, 10
V_X (AC)	Differential AC Input Cross Point Voltage	$V_{DDQ}/2$ − 0.2	—	$V_{DDQ}/2$ + 0.2	V	8, 10
V_{ISO} (AC)	Differential Clock AC Middle Level	$V_{DDQ}/2$ − 0.2	—	$V_{DDQ}/2$ + 0.2	V	9, 10

NOTES:

(1) All voltages referenced to V_{SS}, V_{SSQ}.

(2) V_{REF} is expected to track variations in V_{DDQ} DC level of the transmitting device. Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).

(3) Overshoot limit: $V_{IH\ (max)} = V_{DDQ} + 0.9$ V with a pulse width ≤ 5 ns.

(4) Undershoot limit: $V_{IL\ (min)} = -0.9$ V with a pulse width ≤ 5 ns.

(5) V_{IH} (DC) and V_{IL} (DC) are levels to maintain the current logic state.

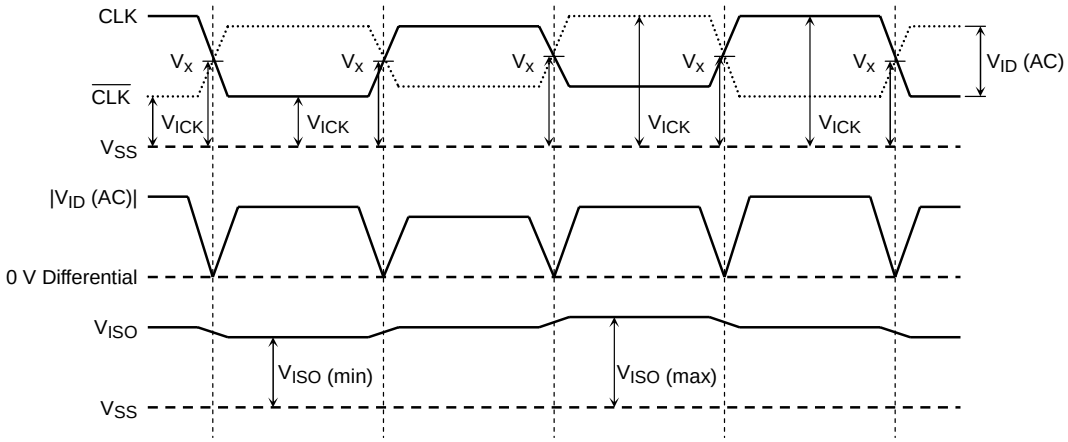
(6) V_{IH} (AC) and V_{IL} (AC) are levels to change to the new logic state.

(7) V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.

(8) The value of V_X (AC) is expected to equal $V_{DDQ}/2$ of the transmitting device.

(9) V_{ISO} means {V_{ICK} (CLK) + V_{ICK} ($\overline{CLK}$)} /2

(10) Refer to the figure below.



(11) In the case of external termination, VTT (termination voltage) should be gone in the range of V_{REF} (DC) ± 0.04 V.

CAPACITANCE (V_{DD}, V_{DDQ} = 2.5 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{IN}	Input pin Capacitance	2.5	4.0	pF
C_{INC}	Clock pin (CLK, $\overline{CLK}$) Capacitance	2.5	4.0	pF
$C_{I/O}$	I/O pin (DQ, DQS) Capacitance	4.0	6.0	pF
$C_{NC}{}^{1}$	NC^{1} pin Capacitance	—	1.5	pF
$C_{NC}{}^{2}$	NC^{2} pin Capacitance	4.0	6.0	pF

Note: These parameters are periodically sampled and not 100% tested.
The NC^{2} pins have additional capacitance for adjustment of the adjacent pin capacitance.
The NC^{2} pins have Power and Ground clamp.

RECOMMENDED DC OPERATING CONDITIONS (V_{DD},V_{DDQ}=2.5V ± 0.15V, Ta = 0°~70°C)

SYMBOL	PARAMETER	MAX		UNIT	NOTES
		-50	-60		
I_{DD1S}	Operating Current t_{CK} = min; I_{RC} = min, Read/Write command cycling, 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ}, 1 bank operation, Burst length = 4, Address change up to 2 times during minimum I_{RC}.	190	170	mA	1, 2
I_{DD2N}	Standby Current t_{CK} = min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IH}, 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ}, All banks: inactive state, Other input signals are changed one time during 4 × t_{CK}.	40	35		1, 2
I_{DD2P}	Standby (power down) Current t_{CK} = min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IL} (power down), 0 V ≤ V_{IN} ≤ V_{DDQ}, All banks: inactive state	2	2		1, 2
I_{DD5}	Auto-Refresh Current t_{CK} = min; I_{REFC} = min, t_{REFI} = min, Auto-Refresh command cycling, 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ}, Address change up to 2 times during minimum I_{REFC}.	65	60		1, 2
I_{DD6}	Self-Refresh Current Self-Refresh mode $\overline{PD}$ = 0.2 V, 0 V ≤ V_{IN} ≤ V_{DDQ}	3	3		2

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{LI}	Input Leakage Current (0 V ≤ V_{IN} ≤ V_{DDQ}, all other pins not under test = 0 V)		–5	5	µA	
I_{LO}	Output Leakage Current (Output disabled, 0 V ≤ V_{OUT} ≤ V_{DDQ})		–5	5	µA	
I_{REF}	V_{REF} Current		–5	5	µA	
I_{OH} (DC)	Normal Output Driver	Output Source DC Current V_{OH} = V_{DDQ} – 0.4 V	–10	—	mA	3
I_{OL} (DC)		Output Sink DC Current V_{OL} = 0.4 V	10	—		3
I_{OH} (DC)	Strong Output Driver	Output Source DC Current V_{OH} = V_{DDQ} – 0.4 V	–11	—		3
I_{OL} (DC)		Output Sink DC Current V_{OL} = 0.4 V	11	—		3
I_{OH} (DC)	Weaker Output Driver	Output Source DC Current V_{OH} = V_{DDQ} – 0.4 V	–8	—		3
I_{OL} (DC)		Output Sink DC Current V_{OL} = 0.4 V	8	—		3
I_{OH} (DC)	Weakest Output Driver	Output Source DC Current V_{OH} = V_{DDQ} – 0.4 V	–7	—		3
I_{OL} (DC)		Output Sink DC Current V_{OL} = 0.4 V	7	—		3

Notes: 1. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK}, t_{RC} and I_{RC}.
2. These parameters define the current between V_{DD} and V_{SS}.
3. Refer to output driver characteristics for the detail. Output Driver Strength is selected by Extended Mode Register.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 1, 2)

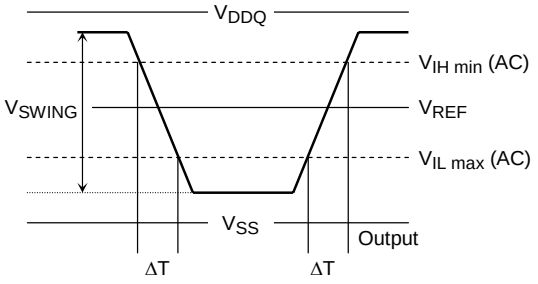
SYMBOL	PARAMETER		-50		-60		UNIT	NOTES
			MIN	MAX	MIN	MAX		
t_{RC}	Random Cycle Time		25	—	30	—	ns	3
t_{CK}	Clock Cycle Time	$C_L = 3$	5.5	12	6.5	12		3, 9
		$C_L = 4$	5	12	6	12		3, 9
t_{RAC}	Random Access Time		—	22	—	26		3
t_{CH}	Clock High Time		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—		3
t_{CL}	Clock Low Time		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—		3
t_{CKQS}	DQS Access Time from CLK		–0.65	0.65	–0.85	0.85		3, 8
t_{QSQ}	Data Output Skew from DQS		—	0.4	—	0.5		4
t_{AC}	Data Access Time from CLK		–0.65	0.65	–0.85	0.85		3, 8
t_{OH}	Data Output Hold Time from CLK		–0.65	0.65	–0.85	0.85		3, 8
t_{QSPRE}	DQS (read) Preamble Pulse Width		$0.9 \times t_{CK} - 0.2$	$1.1 \times t_{CK} + 0.2$	$0.9 \times t_{CK} - 0.2$	$1.1 \times t_{CK} + 0.2$		3, 8
t_{HP}	CLK half period (minimum of Actual t_{CH}, t_{CL})		$\min(t_{CH}, t_{CL})$	—	$\min(t_{CH}, t_{CL})$	—		3
t_{QSP}	DQS (read) Pulse Width		$t_{HP} - 0.55$	—	$t_{HP} - 0.65$	—		4, 8
t_{QSQV}	Data Output Valid Time from DQS		$t_{HP} - 0.55$	—	$t_{HP} - 0.65$	—		4, 8
t_{DQSS}	DQS (write) Low to High Setup Time		$0.75 \times t_{CK}$	$1.25 \times t_{CK}$	$0.75 \times t_{CK}$	$1.25 \times t_{CK}$		3
t_{DSPRE}	DQS (write) Preamble Pulse Width		$0.4 \times t_{CK}$	—	$0.4 \times t_{CK}$	—		4
t_{DSPRES}	DQS First Input Setup Time		0	—	0	—		3
t_{DSPREH}	DQS First Low Input Hold Time		$0.25 \times t_{CK}$	—	$0.25 \times t_{CK}$	—		3
t_{DSP}	DQS High or Low Input Pulse Width		$0.45 \times t_{CK}$	$0.55 \times t_{CK}$	$0.45 \times t_{CK}$	$0.55 \times t_{CK}$		4
t_{DSS}	DQS Input Falling Edge to Clock Setup Time	$C_L = 3$	1.3	—	1.5	—		3, 4
		$C_L = 4$	1.3	—	1.5	—		3, 4
t_{DSPST}	DQS (write) Postamble Pulse Width		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—		4
t_{DSPSTH}	DQS (write) Postamble Hold Time	$C_L = 3$	1.3	—	1.5	—		3, 4
		$C_L = 4$	1.3	—	1.5	—		3, 4
t_{DSSK}	UDQS - LDQS Skew (x16)		$-0.5 \times t_{CK}$	$0.5 \times t_{CK}$	$-0.5 \times t_{CK}$	$0.5 \times t_{CK}$		
t_{DS}	Data Input Setup Time from DQS		0.5	—	0.6	—		4
t_{DH}	Data Input Hold Time from DQS		0.5	—	0.6	—		4
t_{DIPW}	Data Input Pulse Width (for each device)		1.5	—	1.9	—		
t_{IS}	Command/Address Input Setup Time		0.9	—	1.0	—		3
t_{IH}	Command/Address Input Hold Time		0.9	—	1.0	—		3
t_{IPW}	Command/Address Input Pulse Width (for each device)		2.0	—	2.2	—		
t_{LZ}	Data-out Low Impedance Time from CLK		–0.65	—	–0.85	—		3,6,8
t_{HZ}	Data-out High Impedance Time from CLK		—	0.65	—	0.85		3,7,8

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 1, 2) (continued)

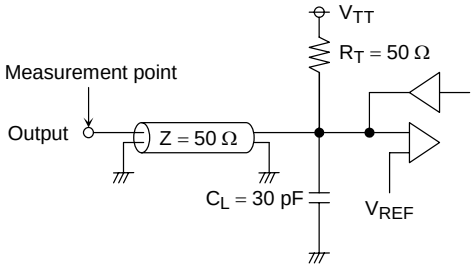
SYMBOL	PARAMETER		-50		-60		UNIT	NOTES
			MIN	MAX	MIN	MAX		
t_{QSLZ}	DQS-out Low Impedance Time from CLK		−0.65	—	−0.85	—	ns	3,6,8
t_{QSHZ}	DQS-out High Impedance Time from CLK		−0.65	0.65	−0.85	0.85		3,7,8
t_{QPDH}	Last output to $\overline{PD}$ High Hold Time		0	—	0	—		
t_{PDEX}	Power Down Exit Time		2	—	2	—		3
t_T	Input Transition Time		0.1	1	0.1	1		
t_{FPDL}	$\overline{PD}$ Low Input Window for Self-Refresh Entry		$-0.5 \times t_{CK}$	5	$-0.5 \times t_{CK}$	5		3
t_{REFI}	Auto-Refresh Average Interval		0.4	7.8	0.4	7.8	μs	5
t_{PAUSE}	Pause Time after Power-up		200	—	200	—		
I_{RC}	Random Read/Write Cycle Time (applicable to same bank)	$C_L = 3$	5	—	5	—	cycle	
		$C_L = 4$	5	—	5	—		
I_{RCD}	RDA/WRA to LAL Command Input Delay (applicable to same bank)		1	1	1	1		
I_{RAS}	LAL to RDA/WRA Command Input Delay (applicable to same bank)	$C_L = 3$	4	—	4	—		
		$C_L = 4$	4	—	4	—		
I_{RBD}	Random Bank Access Delay (applicable to other bank)		2	—	2	—		
I_{RWD}	LAL following RDA to WRA Delay (applicable to other bank)	$B_L = 2$	2	—	2	—		
		$B_L = 4$	3	—	3	—		
I_{WRD}	LAL following WRA to RDA Delay (applicable to other bank)		1	—	1	—		
I_{RSC}	Mode Register Set Cycle Time	$C_L = 3$	5	—	5	—		
		$C_L = 4$	5	—	5	—		
I_{PD}	$\overline{PD}$ Low to Inactive State of Input Buffer		—	1	—	1		
I_{PDA}	$\overline{PD}$ High to Active State of Input Buffer		—	1	—	1		
I_{PDV}	Power down mode valid from REF command	$C_L = 3$	15	—	15	—		
		$C_L = 4$	18	—	18	—		
I_{REFC}	Auto-Refresh Cycle Time	$C_L = 3$	15	—	15	—		
		$C_L = 4$	18	—	18	—		
I_{CKD}	REF Command to Clock Input Disable at Self-Refresh Entry		16	—	16	—		
I_{LOCK}	DLL Lock-on Time (applicable to RDA command)		200	—	200	—		

AC TEST CONDITIONS

SYMBOL	PARAMETER	VALUE	UNIT	NOTES
$V_{IH\ (min)}$	Input High Voltage (minimum)	V_{REF} + 0.35	V	
$V_{IL\ (max)}$	Input Low Voltage (maximum)	V_{REF} − 0.35	V	
V_{REF}	Input Reference Voltage	$V_{DDQ}/2$	V	
V_{TT}	Termination Voltage	V_{REF}	V	
V_{SWING}	Input Signal Peak to Peak Swing	1.0	V	
Vr	Differential Clock Input Reference Level	V_X (AC)	V	
V_{ID} (AC)	Input Differential Voltage	1.5	V	
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns	
V_{OTR}	Output Timing Measurement Reference Voltage	$V_{DDQ}/2$	V	



SLEW = ($V_{IH\ min}$ (AC) − $V_{IL\ max}$ (AC))/ΔT



AC Test Load

NOTES:

(1) Transition times are measured between $V_{IH\ min}$ (DC) and $V_{IL\ max}$ (DC).
Transition (rise and fall) of input signals have a fixed slope.

(2) If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., t_{DQSS} = 0.75 × t_{CK}, t_{CK} = 5 ns, 0.75 × 5 ns = 3.75 ns is rounded up to 3.8 ns.)

(3) There parameters are measured from the differential clock (CLK and $\overline{CLK}$) AC cross point.

(4) These parameters are measured from signal transition point of DQS crossing V_{REF} level.

(5) Te $t_{REFI\ (max)}$ applies to equally distributed refresh method.
The $t_{REFI\ (min)}$ applies to both burst refresh method and distribted refresh method.
In such case, the average interval of eight consecutive Auto-Refresh commands has to be more than 400 ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 μs (8 × 400 ns) is to 8 times in the maximum.

(6) Low Impedance State is specified at $V_{DDQ}/2$ ± 0.2 V from steady state.

(7) High Impedance State is specified where output buffer is no longer driven.

(8) These parameters depend on the clock jitter. These parameters are measured at stable clock.

(9) When t_{CK} is between 8.5ns and 12ns at "-50" product, all AC timing parameters refer to spec of "-60" speed version.

POWER UP SEQUENCE

(1) As for $\overline{PD}$, being maintained by the low state (≤ 0.2 V) is desirable before a power-supply injection.

(2) Apply V_{DD} before or at the same time as V_{DDQ}.

(3) Apply V_{DDQ} before or at the same time as V_{REF}.

(4) Start clock (CLK, $\overline{CLK}$) and maintain stable condition for 200 μs (min).

(5) After stable power and clock, apply DESL and take $\overline{PD}$ =H.

(6) Issue EMRS to enable DLL and to define driver strength. (Note: 1)

(7) Issue MRS for set $\overline{CAS}$ latency (CL), Burst Type (BT), and Burst Length (BL). (Note: 1)

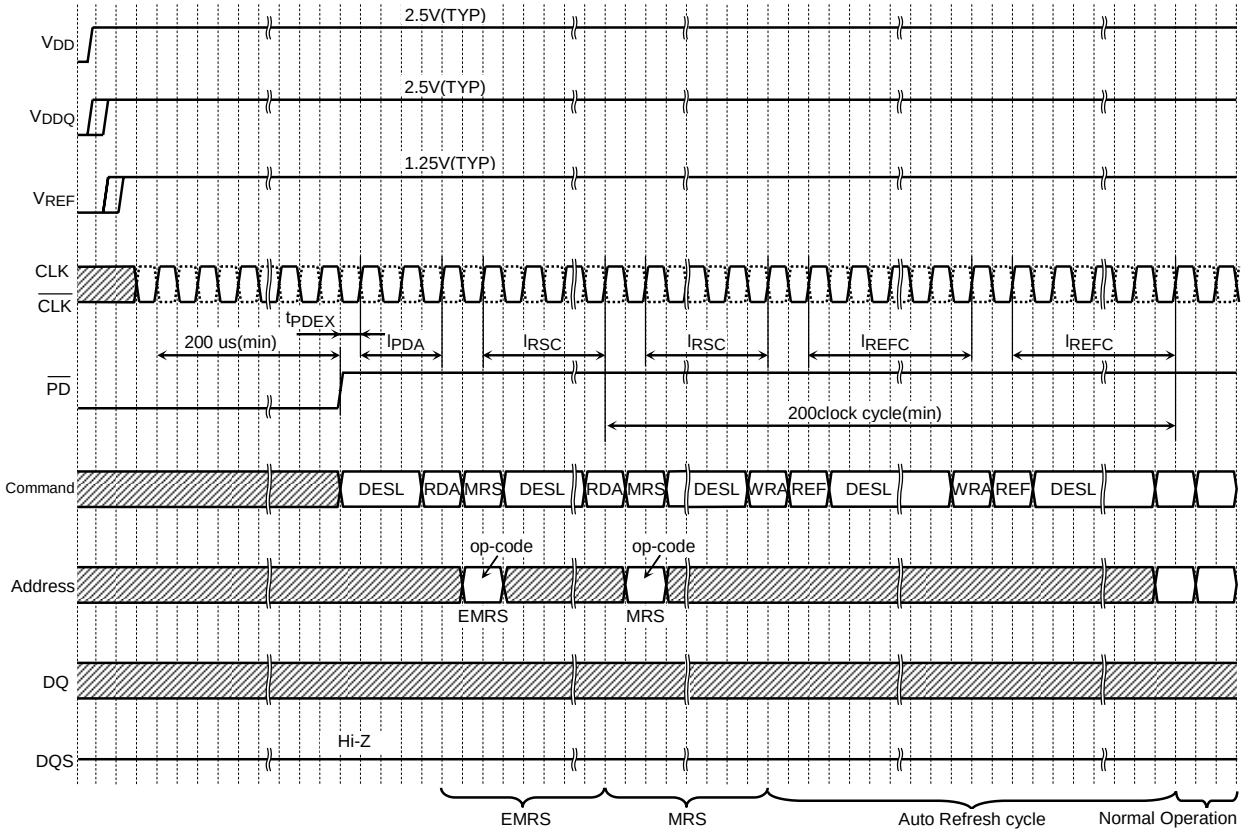
(8) Issue two or more Auto-Refresh commands (Note: 1).

(9) Ready for normal operation after 200 clocks from Extended Mode Register programming.

NOTES:

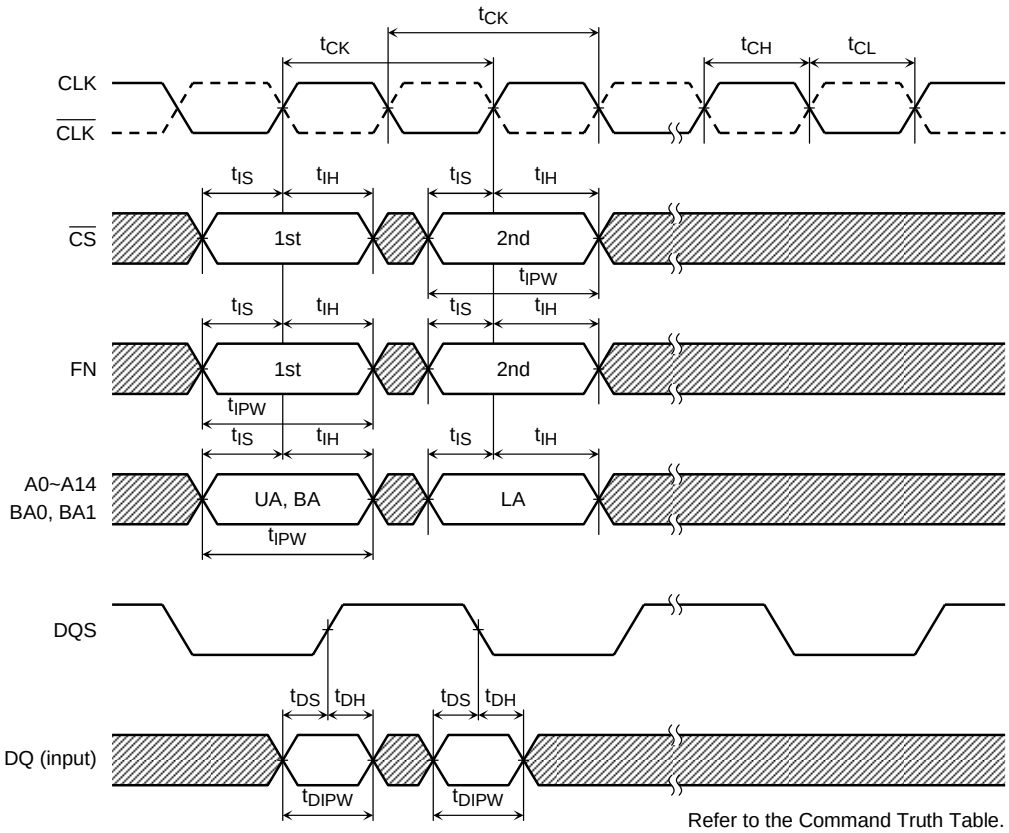
(1) Sequence 6, 7 and 8 can be issued in random order.

(2) L = Logic Low, H = Logic High

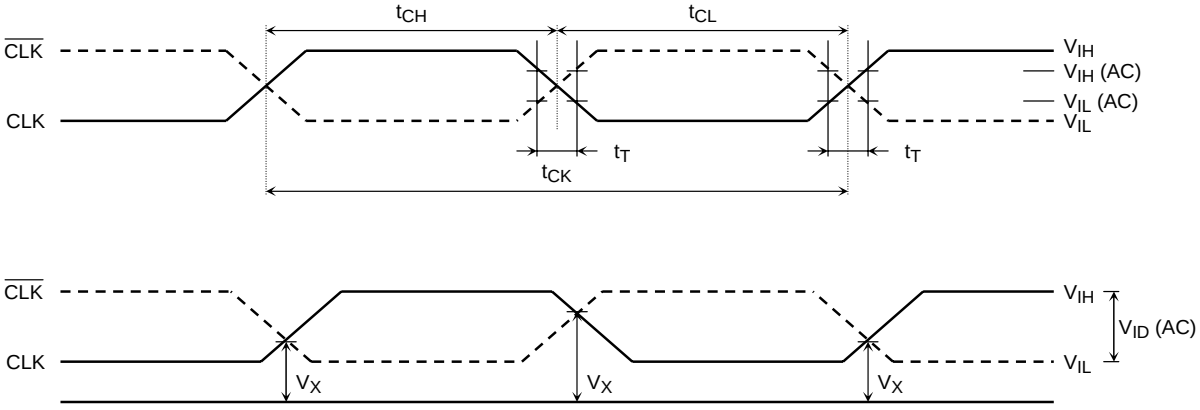


TIMING DIAGRAMS

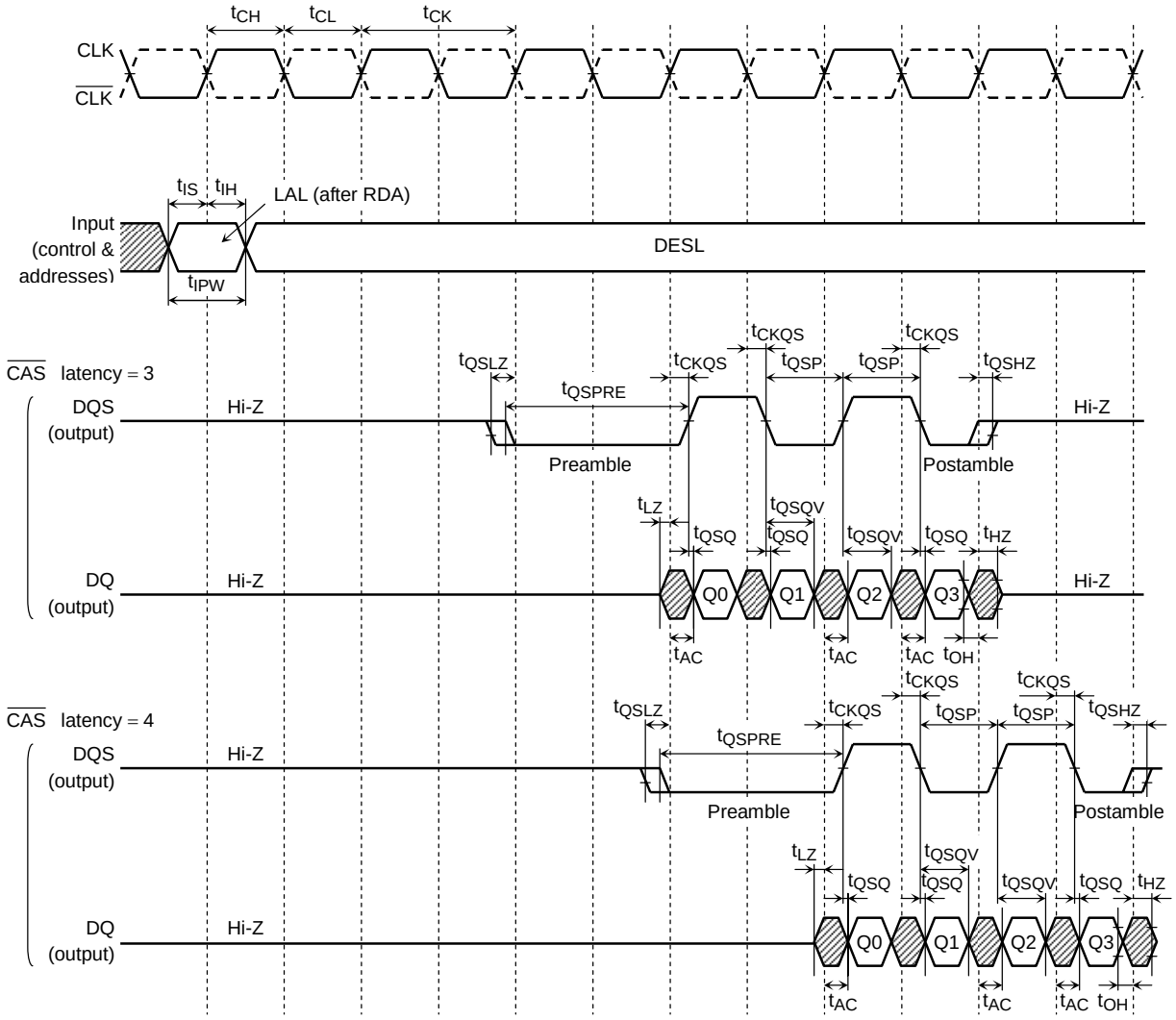
Input Timing



Timing of the CLK, $\overline{CLK}$



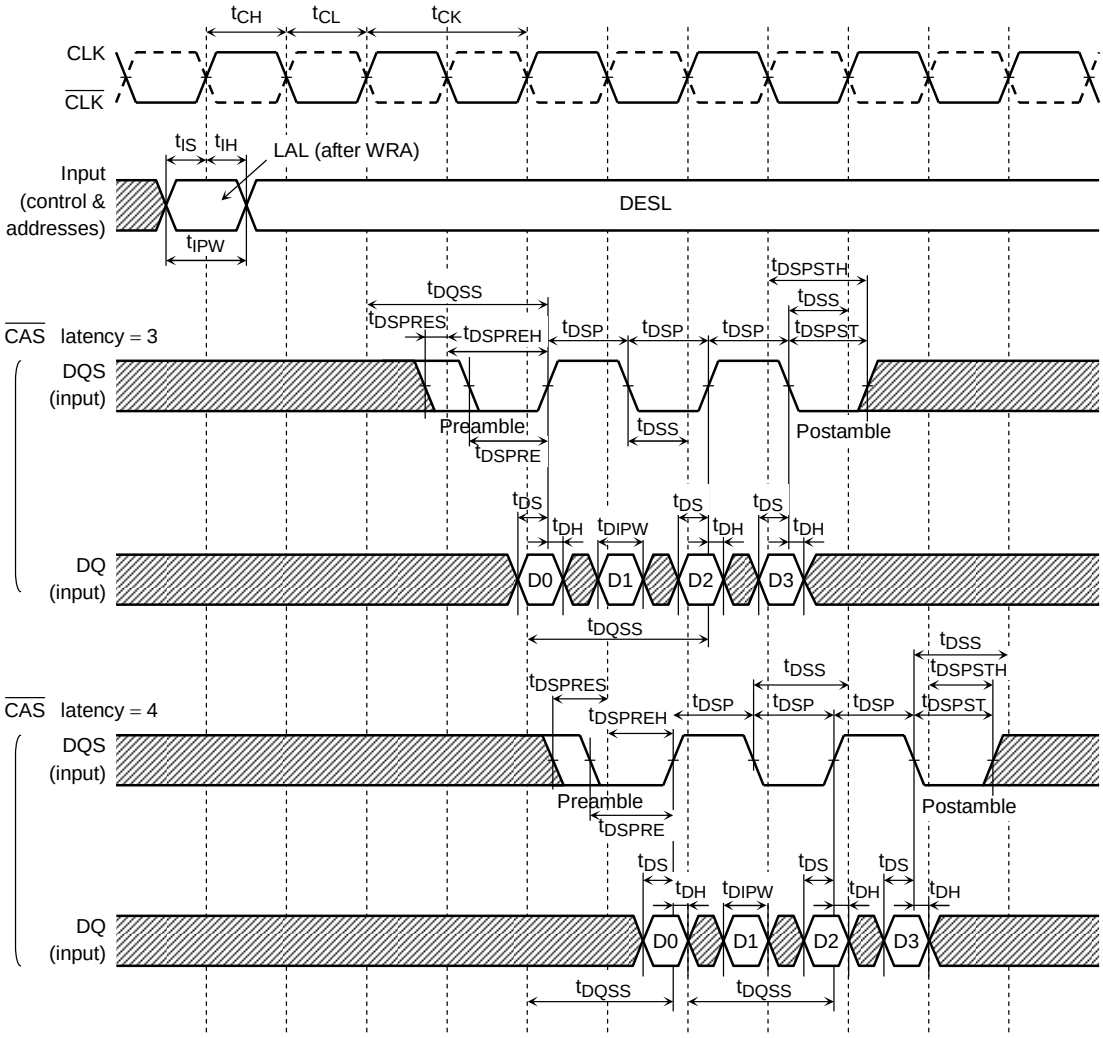
Read Timing (Burst Length = 4)



Note: The correspondence of LDQS, UDQS to DQ. (TC59LM814CTG)

LDQS	DQ0~DQ7
UDQS	DQ8~DQ15

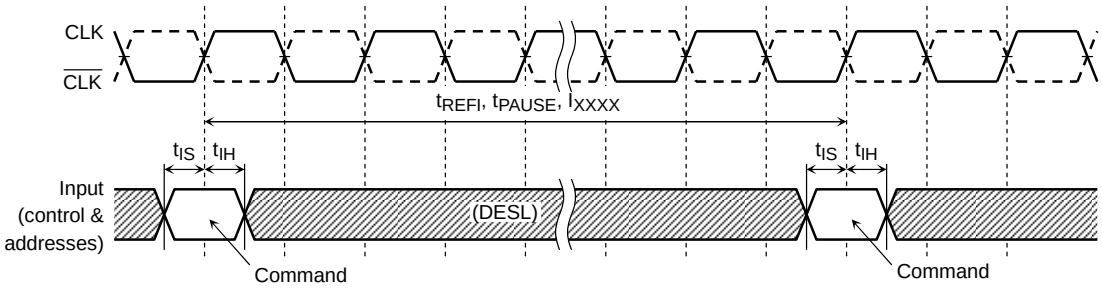
Write Timing (Burst Length = 4)



Note: the correspondence of LDQS, UDQS to DQ. (TC59LM814CTG)

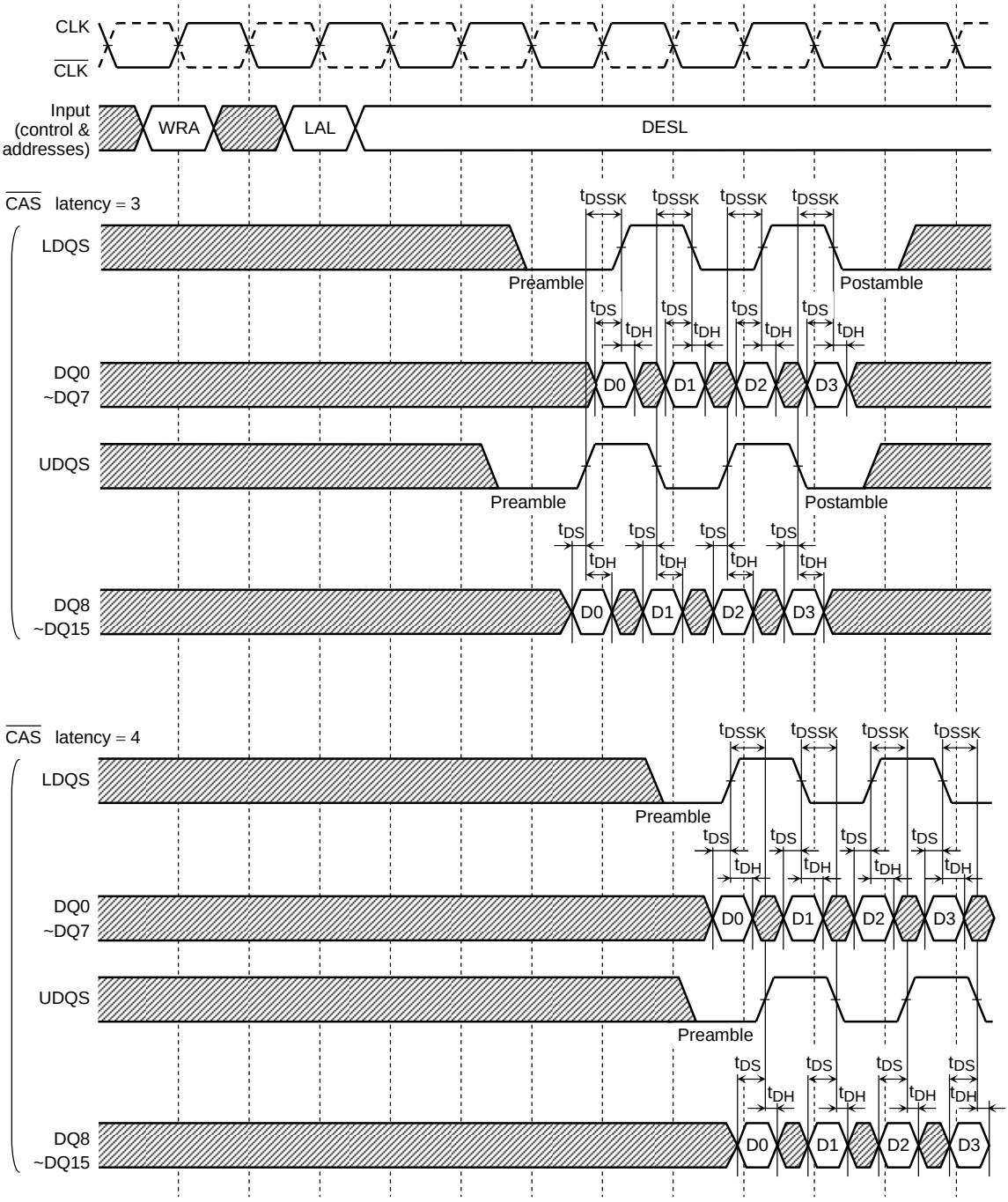
LDQS	DQ0~DQ7
UDQS	DQ8~DQ15

tREFI, tPAUSE, IXXXX Timing



Note: "I_{XXXX}" means "I_{RC}", "I_{RCD}", "I_{RAS}", etc.

Write Timing (x16 device) (Burst Length = 4)



FUNCTION TRUTH TABLE (Notes: 1, 2, 3)

Command Truth Table (Notes: 4)

• The First Command

SYMBOL	FUNCTION	$\overline{CS}$	FN	BA1~BA0	A14~A9	A8	A7	A6~A0
DESL	Device Deselect	H	×	×	×	×	×	×
RDA	Read with Auto-close	L	H	BA	UA	UA	UA	UA
WRA	Write with Auto-close	L	L	BA	UA	UA	UA	UA

• The Second Command (The next clock of RDA or WRA command)

SYMBOL	FUNCTION	$\overline{CS}$	FN	BA1~ BA0	A14~ A13	A12~ A11	A10~A9	A8	A7	A6~A0
LAL	Lower Address Latch (×16)	H	×	×	V	V	×	×	×	LA
LAL	Lower Address Latch (×8)	H	×	×	V	×	×	×	LA	LA
REF	Auto-Refresh	L	×	×	×	×	×	×	×	×
MRS	Mode Register Set	L	×	V	L	L	L	L	V	V

Notes: 1. L = Logic Low, H = Logic High, × = either L or H, V = Valid (specified value), BA = Bank Address, UA = Upper Address, LA = Lower Address
2. All commands are assumed to issue at a valid state.
3. All inputs for command (excluding SELFX and PDEX) are latched on the crossing point of differential clock input where CLK goes to High.
4. Operation mode is decided by the combination of 1st command and 2nd command. Refer to “STATE DIAGRAM” and the command table below.

Read Command Table

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA1~BA0	A14~A9	A8	A7	A6~A0	NOTES
RDA (1st)	L	H	BA	UA	UA	UA	UA	
LAL (2nd)	H	×	×	×	×	LA	LA	5

Notes: 5. For x16 device, A7 is "×" (either L or H).

Write Command Table

• TC59LM814CTG

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA1~ BA0	A14	A13	A12	A11	A10~ A9	A8	A7	A6~A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	×	×	LVW0	LVW1	UVW0	UVW1	×	×	×	LA

• TC59LM806CTG

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA1~ BA0	A14	A13	A12	A11	A10~ A9	A8	A7	A6~A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	×	×	VW0	VW1	×	×	×	×	LA	LA

Notes: 6. A14~ A11 are used for Variable Write Length (VW) control at Write Operation.

FUNCTION TRUTH TABLE (continued)

VW Truth Table

SYMBOL	Function	VW0	VW1
BL=2	Write All Words	L	×
	Write First One Word	H	×
BL=4	Reserved	L	L
	Write All Words	H	L
	Write First Two Words	L	H
	Write First One Word	H	H

Notes: 7. For x16 device, LVW0 and LVW1 control DQ0~DQ7.
UVW0 and UVW1 control DQ8~DQ15.

Mode Register Set Command Table

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA1~BA0	A14~A9	A8	A7	A6~A0	NOTES
RDA (1st)	L	H	×	×	×	×	×	
MRS (2nd)	L	×	V	L	L	V	V	8

Notes: 8. Refer to “MODE REGISTER TABLE”.

Auto-Refresh Command Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA1~BA0	A14~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Active	WRA (1st)	Standby	H	H	L	L	×	×	×	×	×	
Auto-Refresh	REF (2nd)	Active	H	H	L	×	×	×	×	×	×	

Self-Refresh Command Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA1~BA0	A14~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Active	WRA (1st)	Standby	H	H	L	L	×	×	×	×	×	
Self-Refresh Entry	REF (2nd)	Active	H	L	L	×	×	×	×	×	×	9, 10
Self-Refresh Continue	—	Self-Refresh	L	L	×	×	×	×	×	×	×	
Self-Refresh Exit	SELFX	Self-Refresh	L	H	H	×	×	×	×	×	×	11

Power Down Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA1~BA0	A14~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Power Down Entry	PDEN	Standby	H	L	H	×	×	×	×	×	×	10
Power Down Continue	—	Power Down	L	L	×	×	×	×	×	×	×	
Power Down Exit	PDEX	Power Down	L	H	H	×	×	×	×	×	×	11

Notes: 9. $\overline{PD}$ has to be brought to Low within t_{FPDL} from REF command.
10. $\overline{PD}$ should be brought to Low after DQ’s state turned high impedance.
11. When $\overline{PD}$ is brought to High from Low, this function is executed asynchronously.

FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	ADDRESS	COMMAND	ACTION	NOTES
	n – 1	n						
Idle	H	H	H	×	×	DESL	NOP	
	H	H	L	H	BA, UA	RDA	Row activate for Read	
	H	H	L	L	BA, UA	WRA	Row activate for Write	
	H	L	H	×	×	PDEN	Power Down Entry	12
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Refer to Power Down State	
Row Active for Read	H	H	H	×	LA	LAL	Begin Read	
	H	H	L	×	Op-code	MRS/EMRS	Access to Mode Register	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	MRS/EMRS	Illegal	
	L	×	×	×	×	—	Invalid	
Row Active for Write	H	H	H	×	LA	LAL	Begin Write	
	H	H	L	×	×	REF	Auto-Refresh	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	REF (self)	Self-Refresh Entry	
	L	×	×	×	×	—	Invalid	
Read	H	H	H	×	×	DESL	Continue Burst Read to End	
	H	H	L	H	BA, UA	RDA	Illegal	13
	H	H	L	L	BA, UA	WRA	Illegal	13
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Write	H	H	H	×	×	DESL	Data Write&Continue Burst Write to End	
	H	H	L	H	BA, UA	RDA	Illegal	13
	H	H	L	L	BA, UA	WRA	Illegal	13
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Auto-Refreshing	H	H	H	×	×	DESL	NOP → Idle after t_{REFC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	×	×	PDEN	Self-Refresh Entry	14
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Refer to Self-Refreshing State	
Mode Register Accessing	H	H	H	×	×	DESL	NOP → Idle after t_{RSC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Power Down	H	×	×	×	×	—	Invalid	
	L	L	×	×	×	—	Maintain Power Down Mode	
	L	H	H	×	×	PDEX	Exit Power Down Mode → Idle after t_{PDEX}	
	L	H	L	×	×	—	Illegal	
Self-Refreshing	H	×	×	×	×	—	Invalid	
	L	L	×	×	×	—	Maintain Self-Refresh	
	L	H	H	×	×	SELFX	Exit Self-Refresh → Idle after t_{REFC}	
	L	H	L	×	×	—	Illegal	

Notes: 12. Illegal if any bank is not idle.
13. Illegal to bank in specified states; Function may be legal in the bank inidicated by Bank Address (BA).
14. Illegal if t_{FPDL} is not satisfied.

MODE REGISTER TABLE

Regular Mode Register (Notes: 1)

ADDRESS	BA1 *1	BA0 *1	A14~A8	A7 *3	A6~A4	A3	A2~A0
Register	0	0	0	TE	CL	BT	BL

A7	TEST MODE (TE)
0	Regular (default)
1	Test Mode Entry

A3	BURST TYPE (BT)
0	Sequential
1	Interleave

A6	A5	A4	$\overline{CAS}$ LATENCY (CL)
0	0	×	Reserved *2
0	1	0	Reserved *2
0	1	1	3
1	0	0	4
1	0	1	Reserved *2
1	1	×	Reserved *2

A2	A1	A0	BURST LENGTH (BL)
0	0	0	Reserved *2
0	0	1	2
0	1	0	4
0	1	1	Reserved *2
1	×	×	

Extended Mode Register (Notes: 4)

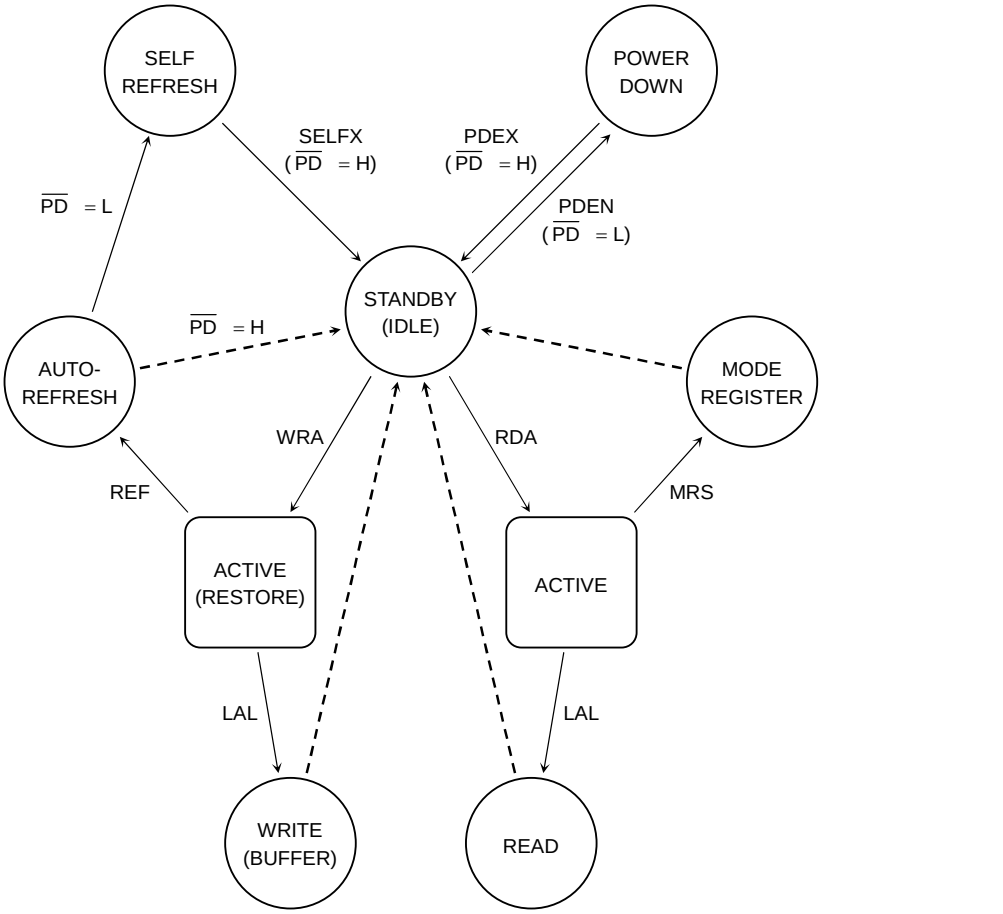
ADDRESS	BA1 *4	BA0 *4	A14~A7	A6	A5~A2	A1	A0 *5
Register	0	1	0	DIC	0	DIC	DS

A6	A1	OUTPUT DRIVE IMPEDANCE CONTROL (DIC)
0	0	Normal Output Driver
0	1	Strong Output Driver
1	0	Weaker Output Driver
1	1	Weakest Output Driver

A0	DLL SWITCH (DS)
0	DLL Enable
1	DLL Disable

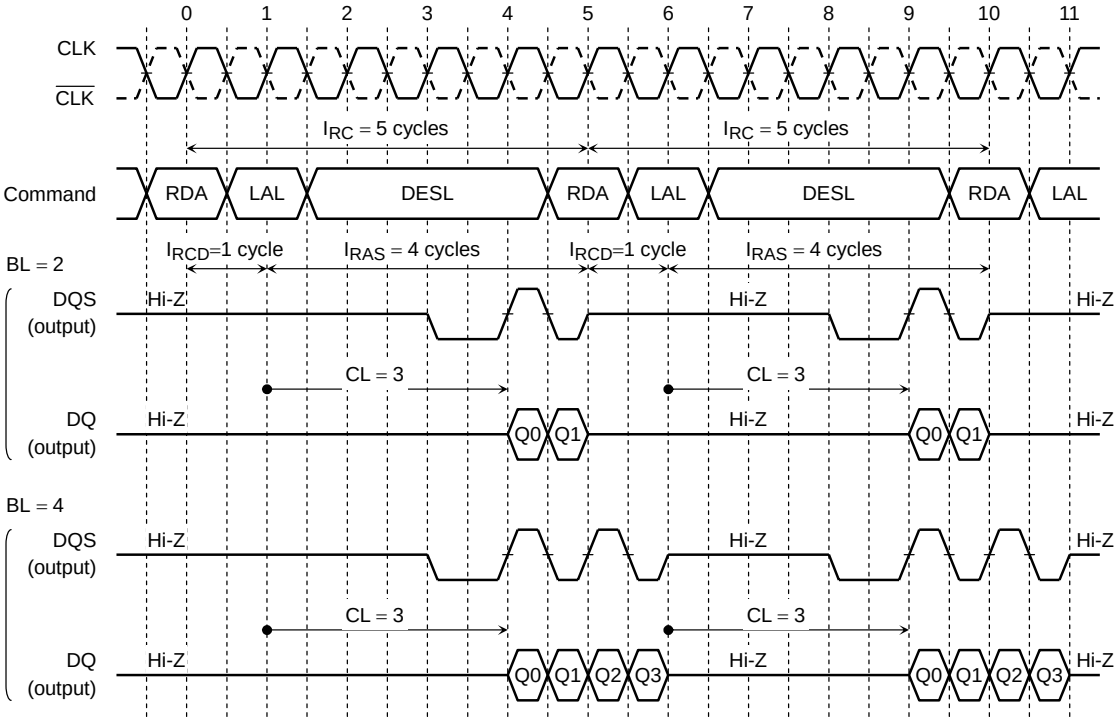
Notes: 1. Regular Mode Register is chosen using the combination of BA0 = 0 and BA1 = 0.
2. "Reserved" places in Regular Mode Register should not be set.
3. A7 in Regular Mode Register must be set to "0" (low state).
Because Test Mode is specific mode for supplier.
4. Extended Mode Register is chosen using the combination of BA0 = 1 and BA1 = 0.
5. A0 in Extended Mode Register must be set to "0" to enable DLL for normal operation.

STATE DIAGRAM

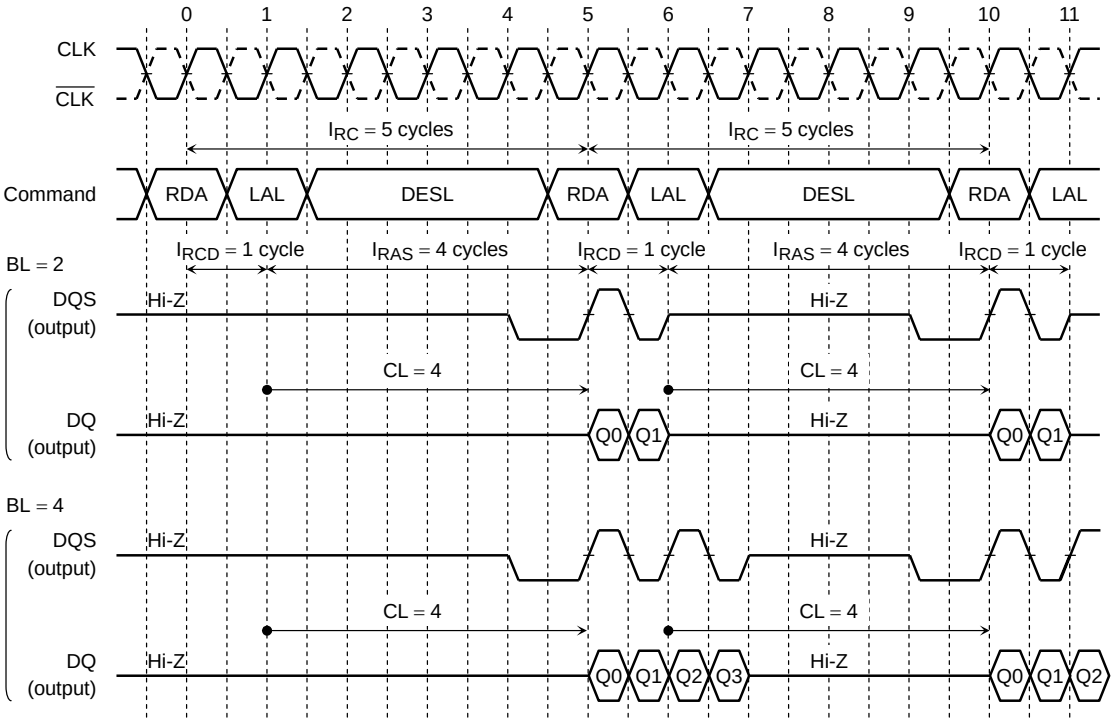


TIMING DIAGRAMS

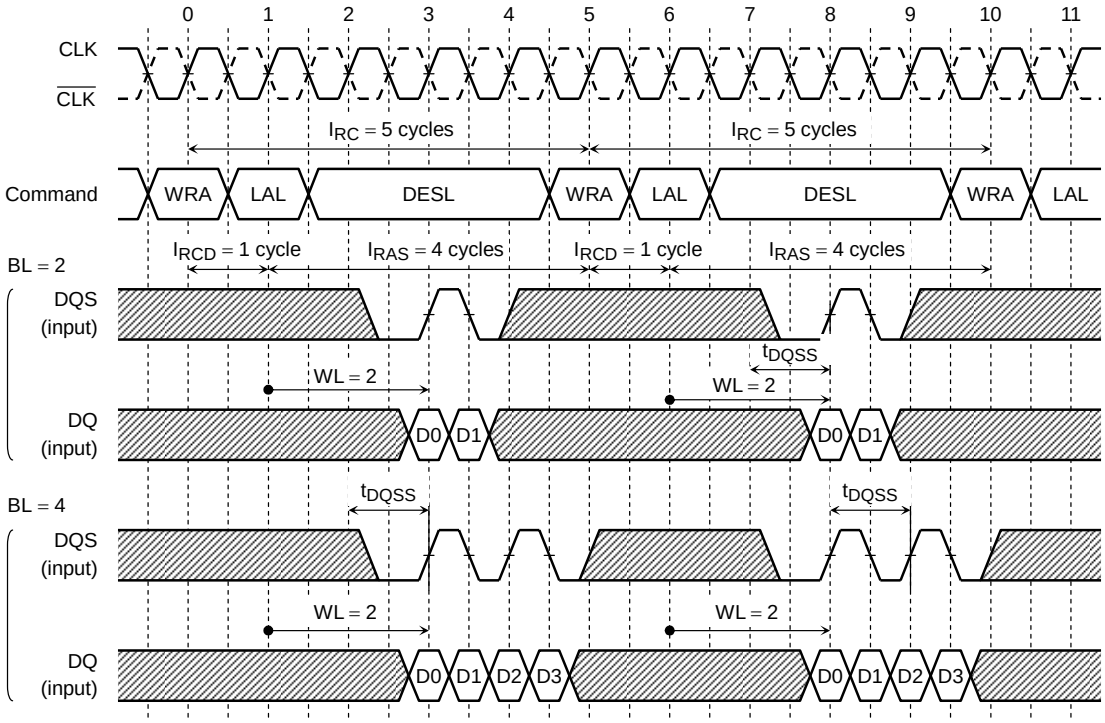
SINGLE BANK READ TIMING (CL = 3)



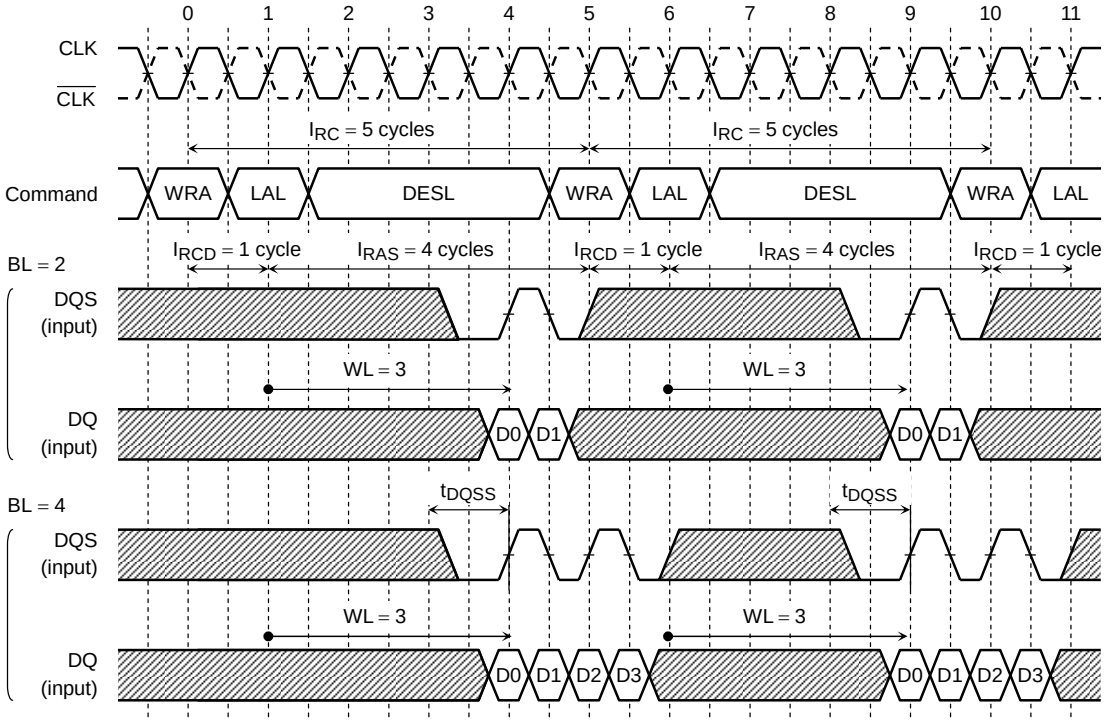
SINGLE BANK READ TIMING (CL = 4)



SINGLE BANK WRITE TIMING (CL = 3)

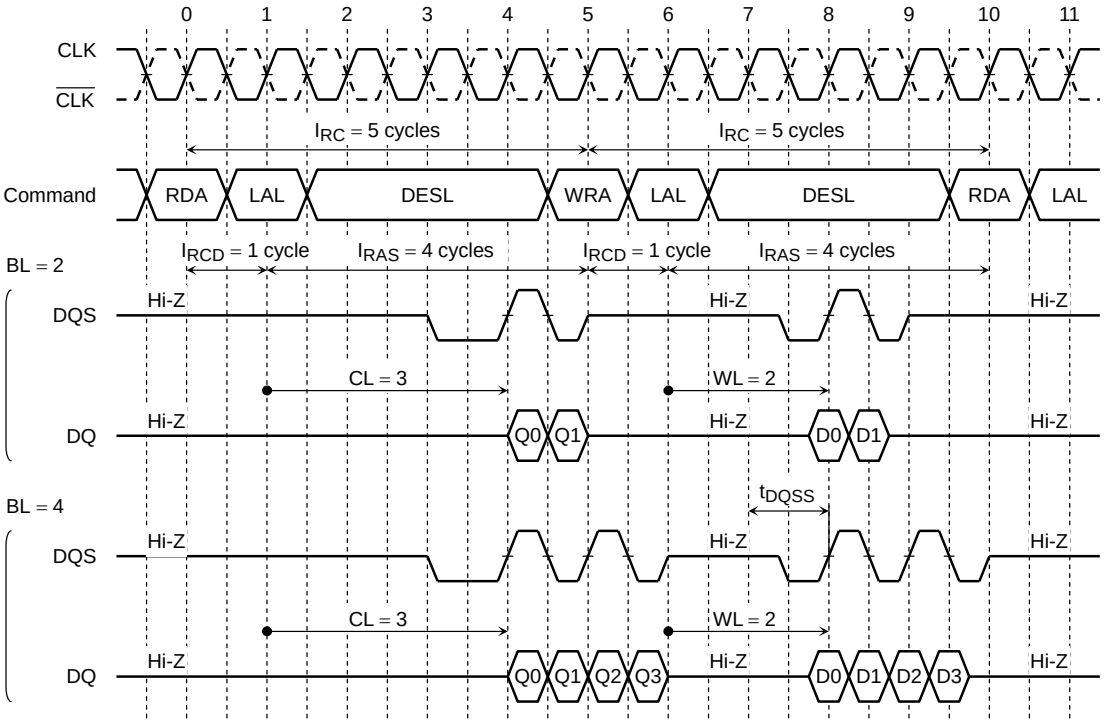


SINGLE BANK WRITE TIMING (CL = 4)

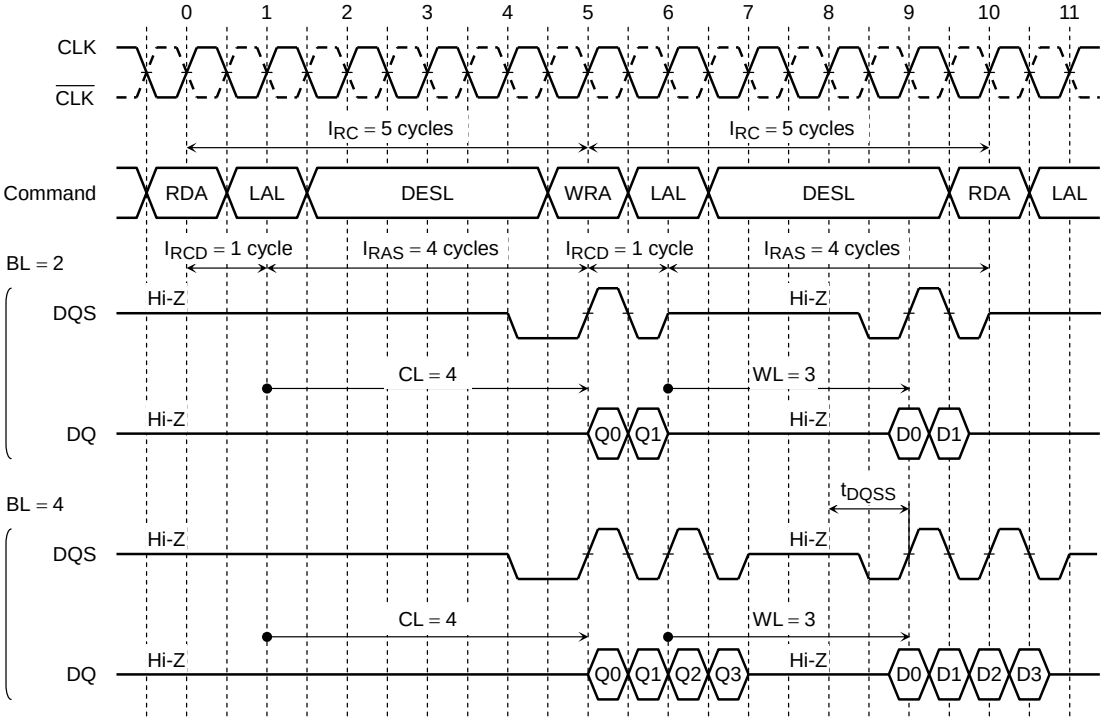


Note: ▨ means H or L

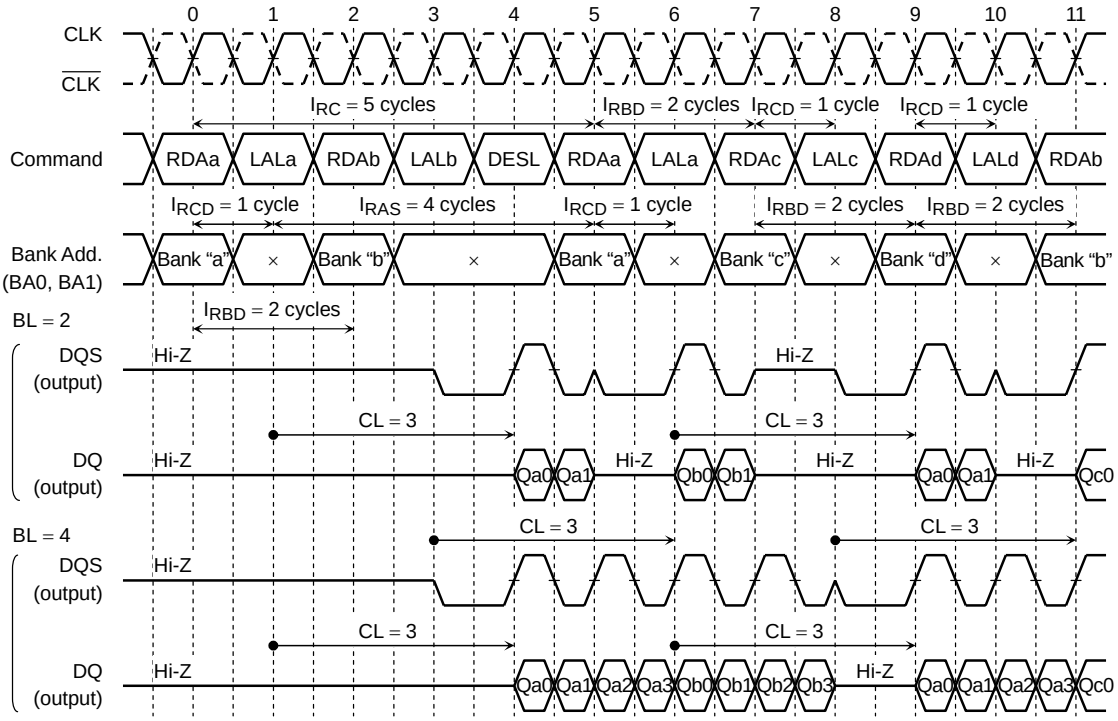
SINGLE BANK READ-WRITE TIMING (CL = 3)



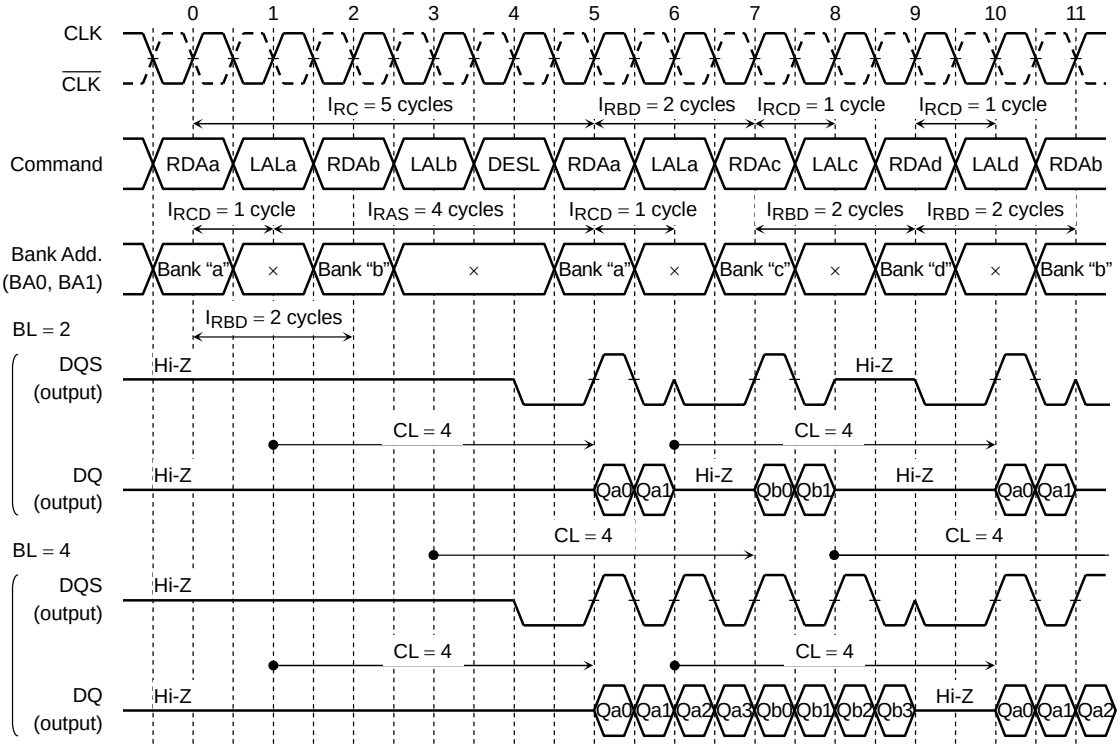
SINGLE BANK READ-WRITE TIMING (CL = 4)



MULTIPLE BANK READ TIMING (CL = 3)

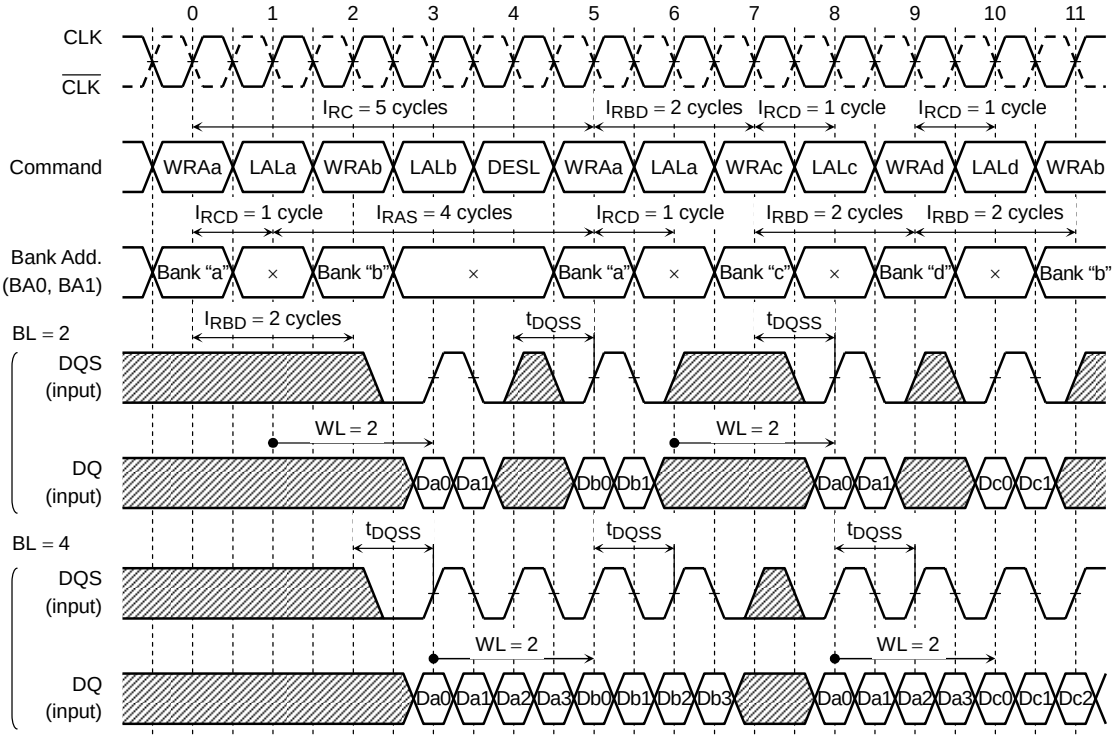


MULTIPLE BANK READ TIMING (CL = 4)

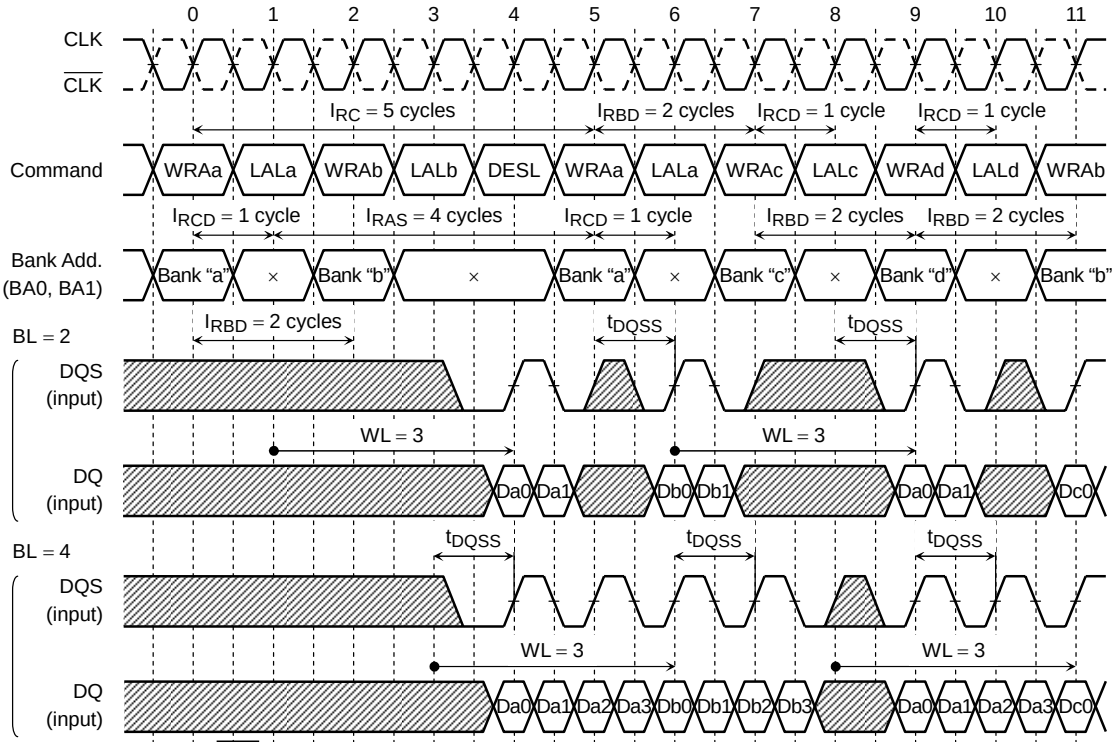


Note: "×" is don't care.
I_{RC} to the same bank must be satisfied.

MULTIPLE BANK WRITE TIMING (CL = 3)

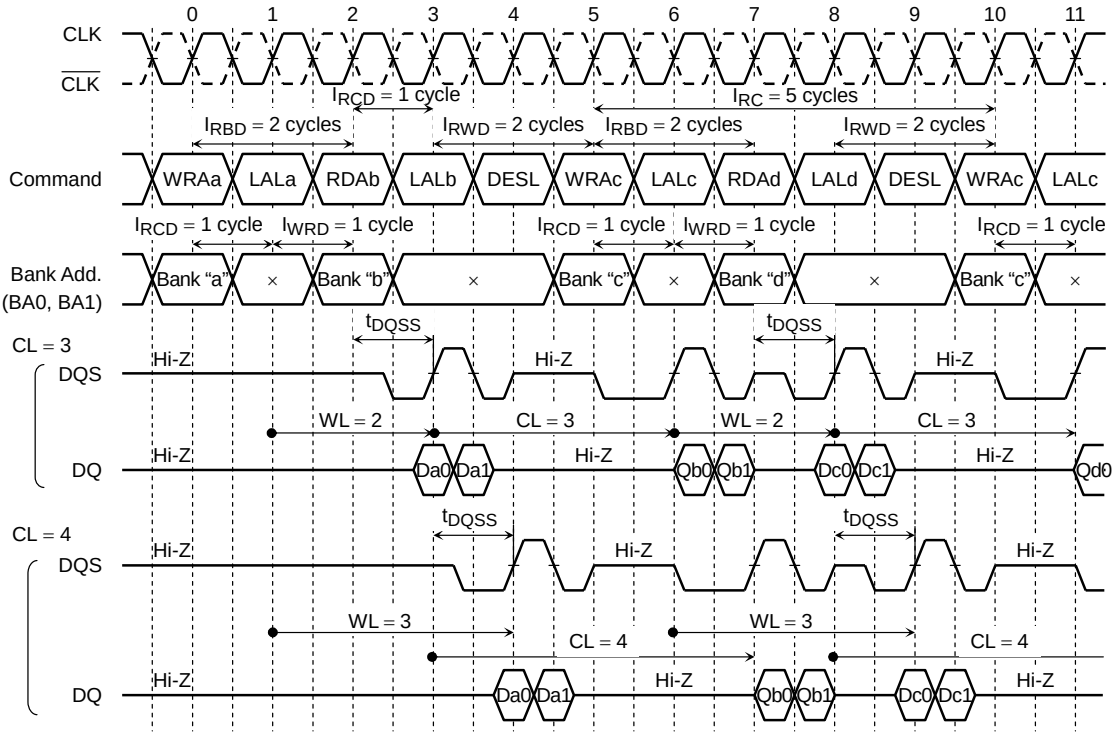


MULTIPLE BANK WRITE TIMING (CL = 4)

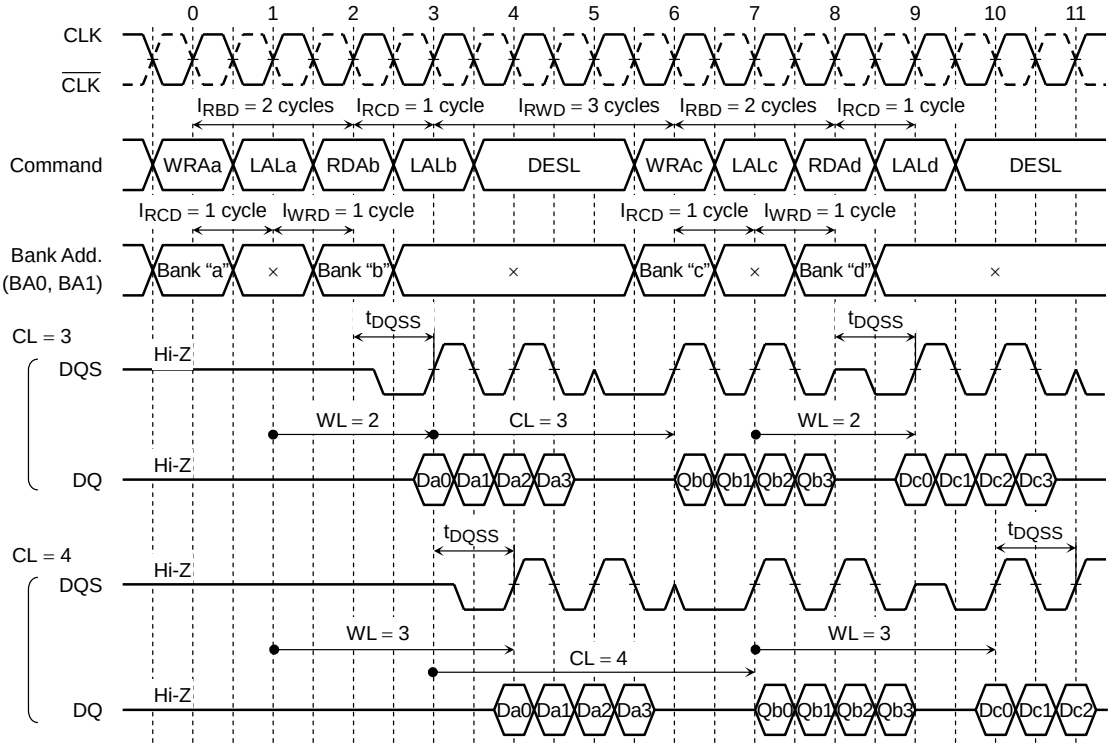


Note: ▨ means H or L.
"×" is don't care
I_{RC} to the same bank must be satisfied.

MULTIPLE BANK READ-WRITE TIMING (BL = 2)

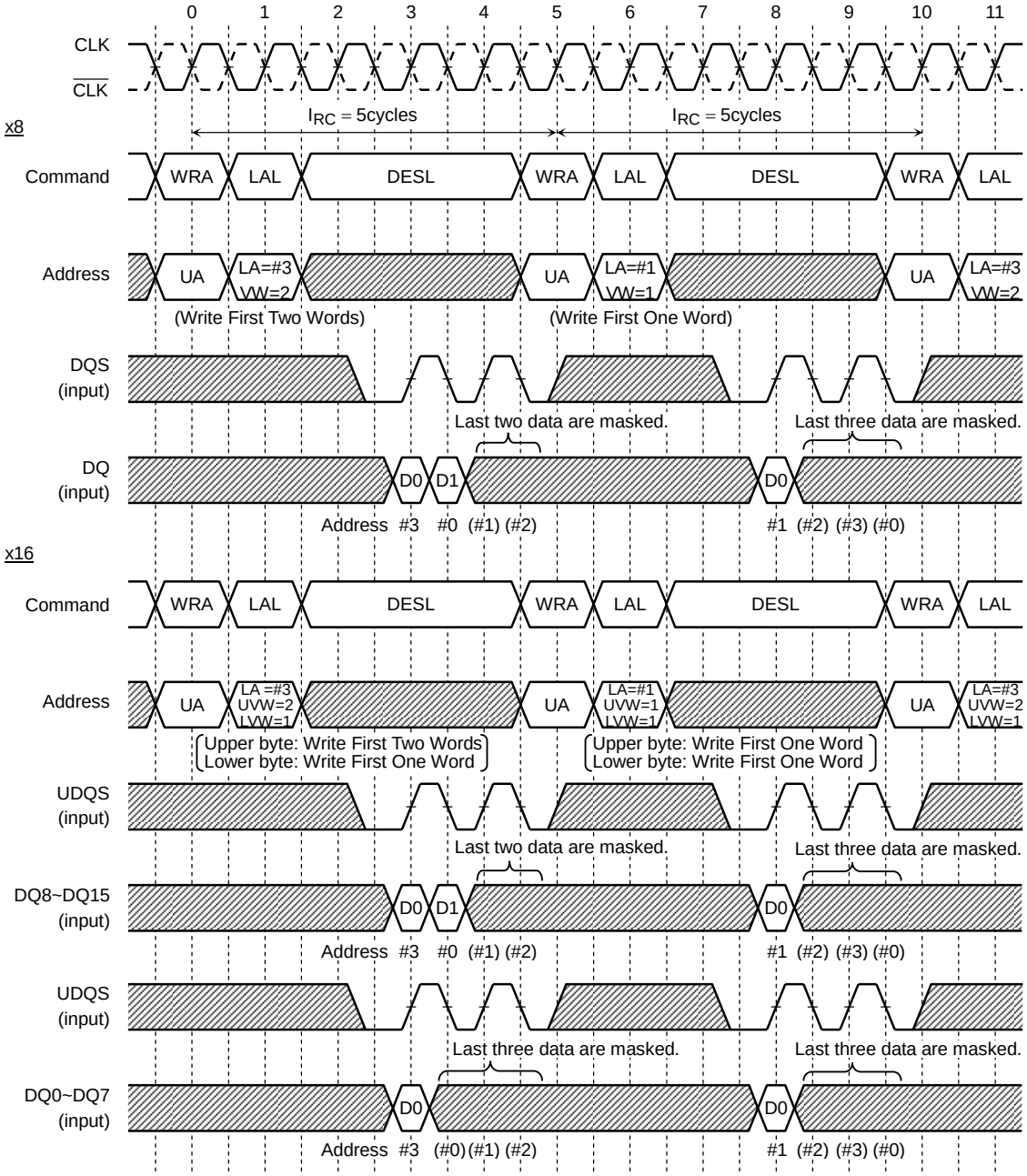


MULTIPLE BANK READ-WRITE TIMING (BL = 4)



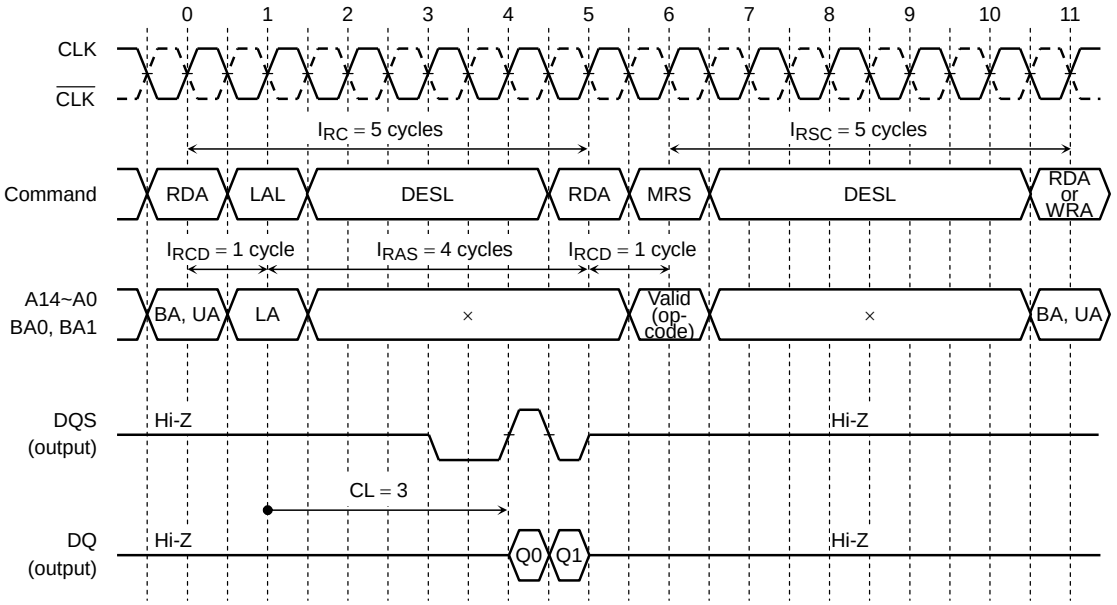
Note: "×" is don't care
I_{RC} to the same bank must be satisfied.

SINGLE BANK WRITE with VARIABLE WRITE LENGTH (VW) CONTROL
(CL = 3, BL = 4, Sequential mode)



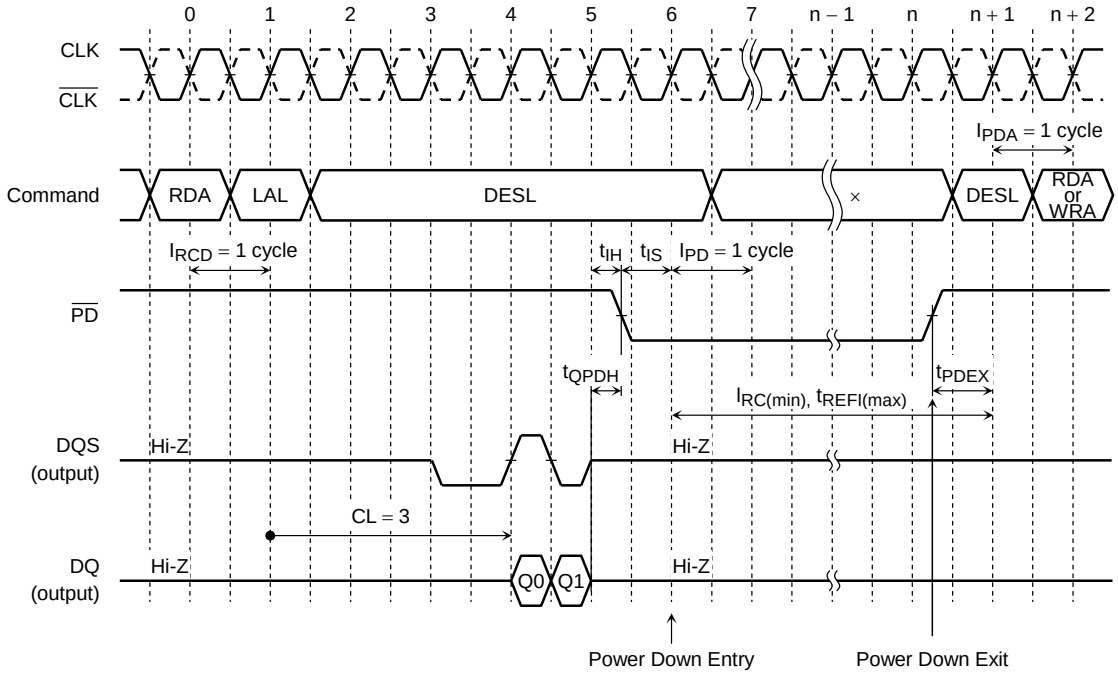
Note: DQS input must be continued till end of burst count even if some of laster data is masked.
Refer to "VW Truth Table".

MODE REGISTER SET TIMING (CL = 3, BL = 2)



POWER DOWN TIMING (CL = 3, BL = 2)

Read cycle to Power Down Mode



Note: "×" is don't care

t_{PD} is defined from the first clock rising edge after $\overline{PD}$ is brought to "Low".

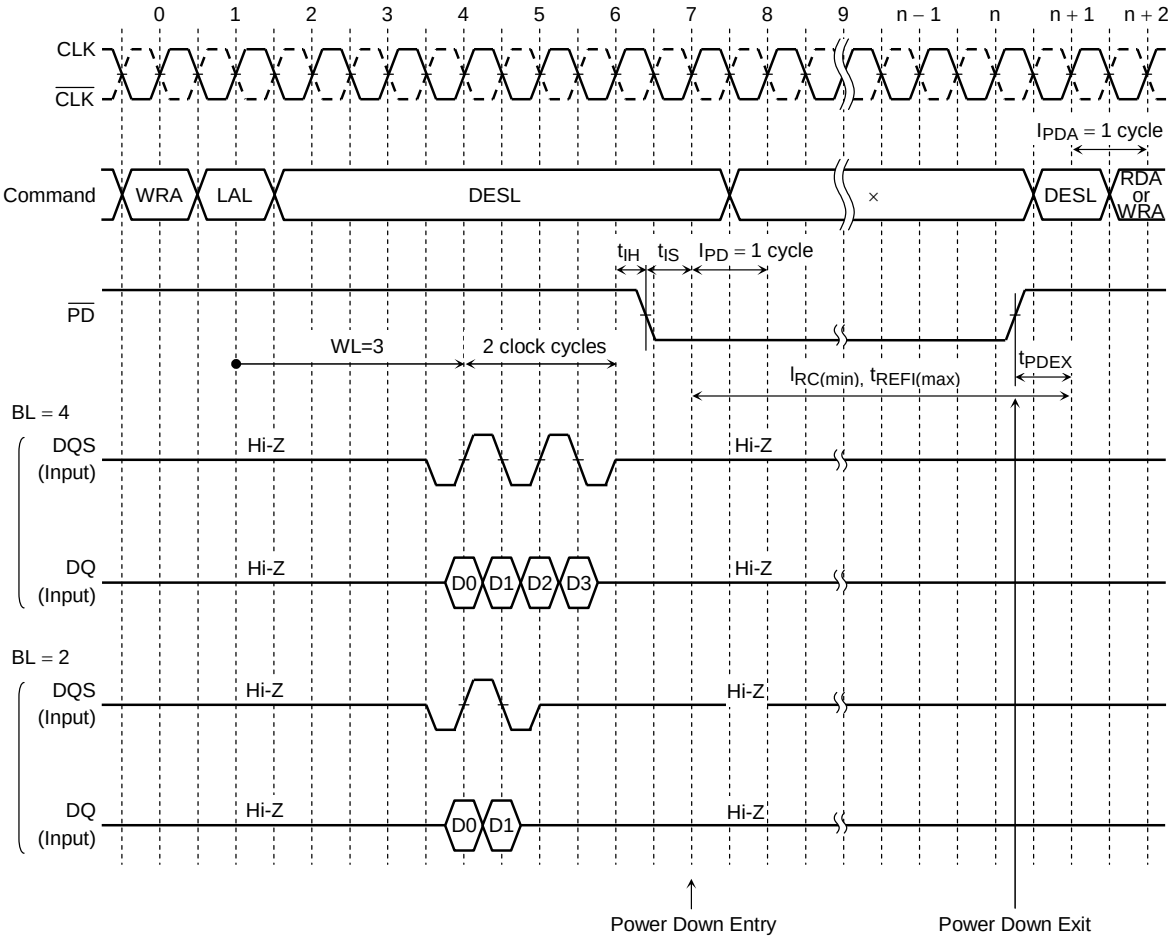
t_{PDA} is defined from the first clock rising edge after $\overline{PD}$ is brought to "High".

$\overline{PD}$ must be kept "High" level until end of Burst data output.

$\overline{PD}$ should be brought to high within $t_{REFI(max)}$ to maintain the data written into cell.

POWER DOWN TIMING (CL = 4)

Write cycle to Power Down Mode

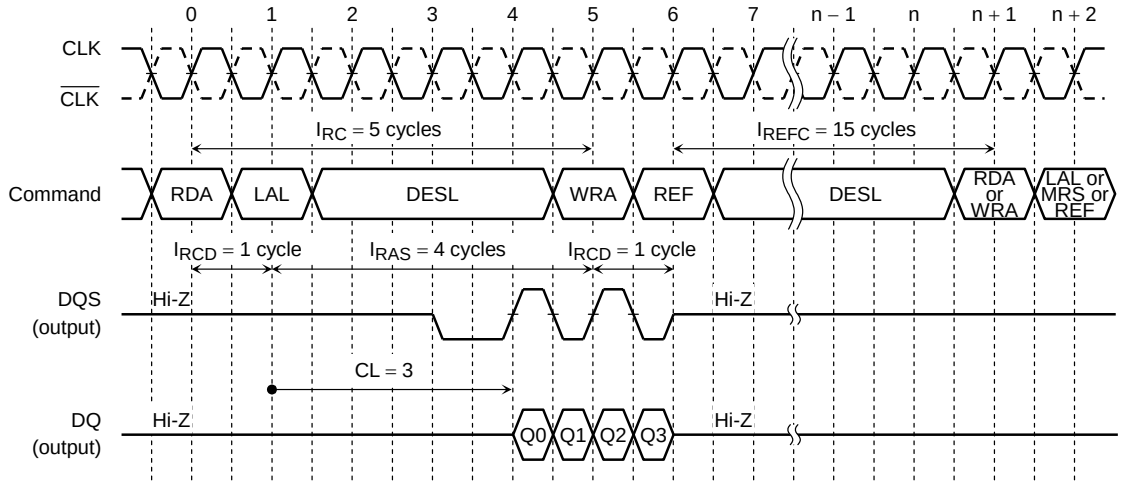


Note: "×" is care

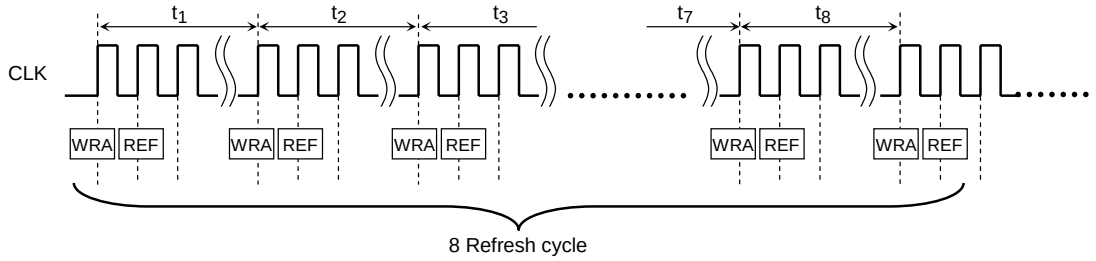
$\overline{PD}$ must be kept "High" level until WL+2 clock cycles from LAL command.

$\overline{PD}$ should be brought to high within $t_{REFI(max)}$ to maintain the data written into cell.

AUTO-REFRESH TIMING (CL = 3, BL = 4)



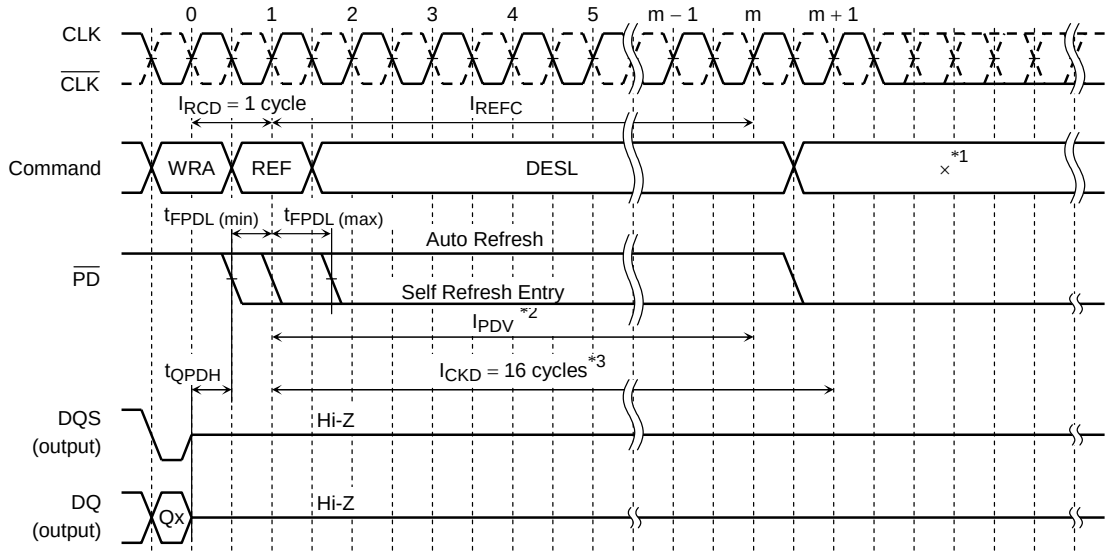
Note: In case of CL = 3, I_{REFC} must be meet 15 clock cycles.
When the Auto-Refresh operation is performed, the synthetic average interval of Auto-Refresh command specified by t_{REFI} must be satisfied.
t_{REFI} is average interval time in 8 Refresh cycles that is sampled randomly.



$$t_{REFI} = \frac{\text{Total time of 8 Refresh cycle}}{8} = \frac{t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8}{8}$$

t_{REFI} is specified to avoid partly concentrated current of Refresh operation that is activated larger area than Read / Write operation.

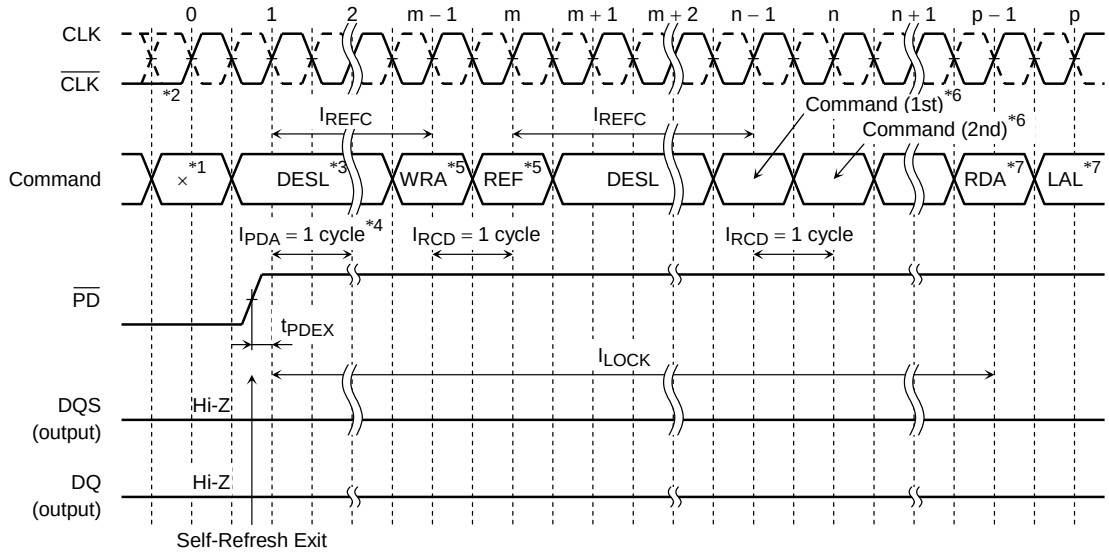
SELF-REFRESH ENTRY TIMING (CL = 3)



Notes: 1. "×" is don't care.

2. $\overline{PD}$ must be brought to "Low" within the timing between t_{FPDL}(min) and t_{FPDL}(max) to Self Refresh mode.When $\overline{PD}$ is brought to "Low" after t_{PDV}, FCRAM™ perform Auto Refresh and enter Power down mode.
3. It is necessary that clock input is continued at least 16 clock cycles from REF command even though $\overline{PD}$ is brought to "Low" for Self-Refresh Entry.

SELF-REFRESH EXIT TIMING



Notes: 1. "×" is don't care.

2. Clock should be stable prior to $\overline{PD}$ = "High" if clock input is suspended in Self-Refresh mode.
3. DESL command must be asserted during t_{REFC} after $\overline{PD}$ is brought to "High".
4. t_{PDA} is defined from the first clock rising edge after $\overline{PD}$ is brought to "High".
5. It is desirable that one Auto-Refresh command is issued just after Self-Refresh Exit before any other operation.
6. Any command (except Read command) can be issued after t_{REFC}.
7. Read command (RDA + LAL) can be issued after t_{LOCK}.

FUNCTIONAL DESCRIPTION

Network FCRAM™

The FCRAM™ is an acronym of Fast Cycle Random Access Memory. The Network FCRAM™ is competent to perform fast random core access, low latency, low consumption and high-speed data transfer.

PIN FUNCTIONS

CLOCK INPUTS: CLK & $\overline{CLK}$

The CLK and $\overline{CLK}$ inputs are used as the reference for synchronous operation. CLK is master clock input. The $\overline{CS}$, FN and all address input signals are sampled on the crossing of the positive edge of CLK and the negative edge of $\overline{CLK}$. The DQS and DQ output data are referenced to the crossing point of CLK and $\overline{CLK}$. The timing reference point for the differential clock is when the CLK and $\overline{CLK}$ signals cross during a transition.

POWER DOWN: $\overline{PD}$

The $\overline{PD}$ input controls the entry to the Power Down or Self-Refresh modes. The $\overline{PD}$ input does not have a Clock Suspend function like a CKE input of a standard SDRAMs, therefore it is illegal to bring $\overline{PD}$ pin into low state if any Read or Write operation is being performed.

CHIP SELECT & FUNCTION CONTROL: $\overline{CS}$ & FN

The $\overline{CS}$ and FN inputs are a control signal for forming the operation commands on FCRAM™. Each operation mode is decided by the combination of the two consecutive operation commands using the $\overline{CS}$ and FN inputs.

BANK ADDRESSES: BA0 & BA1

The BA0 and BA1 inputs are latched at the time of assertion of the RDA or WRA command and are selected the bank to be used for the operation.

	BA0	BA1
Bank #0	0	0
Bank #1	1	0
Bank #2	0	1
Bank #3	1	1

ADDRESS INPUTS: A0~A14

Address inputs are used to access the arbitrary address of the memory cell array within each bank. The Upper Addresses with Bank addresses are latched at the RDA or WRA command and the Lower Addresses are latched at the LAL command. The A0 to A14 inputs are also used for setting the data in the Regular or Extended Mode Register set cycle.

	UPPER ADDRESS	LOWER ADDRESS
TC59LM806CTG	A0~A14	A0~A7
TC59LM814CTG	A0~A14	A0~A6

DATA INPUT/OUTPUT: DQ0~DQ7 or DQ15

The input data of DQ0 to DQ15 are taken in synchronizing with the both edges of DQS input signal. The output data of DQ0 to DQ15 are outputted synchronizing with the both edges of DQS output signal.

DATA STROBE: DQS or LDQS, UDQS

The DQS is bi-directional signal. Both edges of DQS are used as the reference of data input or output. The LDQS is allotted for Lower Byte (DQ0 to DQ7) Data. The UDQS is allotted for Upper Byte (DQ8 to DQ15) Data. In write operation, the DQS used as an input signal is utilized for a latch of write data. In read operation, the DQS that is an output signal provides the read data strobe.

POWER SUPPLY: V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}

V_{DD} and V_{SS} are power supply pins for memory core and peripheral circuits.
V_{DDQ} and V_{SSQ} are power supply pins for the output buffer.

REFERENCE VOLTAGE: V_{REF}

V_{REF} is reference voltage for all input signals.

COMMAND FUNCTIONS and OPERATIONS

TC59LM814/06CTG are introduced the two consecutive command input method. Therefore, except for Power Down mode, each operation mode decided by the combination of the first command and the second command from stand-by states of the bank to be accessed.

Read Operation (1st command + 2nd command = RDA + LAL)

Issuing the RDA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a read mode. When the LAL command with Lower Addresses is issued at the next clock of the RDA command, the data is read out sequentially synchronizing with the both edges of DQS output signal (Burst Read Operation). The initial valid read data appears after $\overline{CAS}$ latency from the issuing of the LAL command. The valid data is outputted for a burst length. The $\overline{CAS}$ latency, the burst length of read data and the burst type must be set in the Mode Register beforehand. The read operated bank goes back automatically to the idle state after l_{RC}.

Write Operation (1st command + 2nd command = WRA + LAL)

Issuing the WRA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a write mode. When the LAL command with Lower Addresses is issued at the next clock of the WRA command, the input data is latched sequentially synchronizing with the both edges of DQS input signal (Burst Write Operation). The data and DQS inputs have to be asserted in keeping with clock input after $\overline{CAS}$ latency-1 from the issuing of the LAL command. The DQS have to be provided for a burst length. The $\overline{CAS}$ latency and the burst type must be set in the Mode Register beforehand. The write operated bank goes back automatically to the idle state after l_{RC}.

Auto-Refresh Operation (1st command + 2nd command = WRA + REF)

TC59LM814/06CTG are required to refresh like a standard SDRAM. The Auto-Refresh operation is begun with the REF command following to the WRA command. The Auto-Refresh mode can be effective only when all banks are in the idle state. In a point to notice, the write mode started with the WRA command is canceled by the REF command having gone into the next clock of the WRA command instead of the LAL command. The minimum period between the Auto-Refresh command and the next command is specified by l_{REFC}. However, about a synthetic average interval of Auto-Refresh command, it must be careful. In case of equally distributed refresh, Auto-Refresh command has to be issued within once for every 7.8 μs by the maximum. In case of burst refresh or random distributed refresh, the average interval of eight consecutive Auto-Refresh command has to be more than 400 ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 μs (8 × 400 ns) is to 8 times in the maximum.

Self-Refresh Operation (1st command + 2nd command = WRA + REF with $\overline{PD}$ = "L")

It is the function of Self-Refresh operation that refresh operation can be performed automatically by using an internal timer. When all banks are in the idle state and all outputs are in Hi-Z states, the TC59LM814/06CTG become Self-Refresh mode by issuing the Self-Refresh command. $\overline{PD}$ has to be brought to "Low" within t_{FPDL} from the REF command following to the WRA command for a Self-Refresh mode entry. In order to satisfy the refresh period, the Self-Refresh entry command should be asserted within 7.8 μs after the latest Auto-Refresh command. Once the device enters Self-Refresh mode, the DESL command must be continued for l_{REFC} period. In addition, it is necessary that clock input is kept in l_{CKD} period. The device is in Self-Refresh mode as long as $\overline{PD}$ held "Low". During Self-Refresh mode, all input and output buffers except for $\overline{PD}$ are disabled, therefore the power dissipation lowers. Regarding a Self-Refresh mode exit, $\overline{PD}$ has to be changed over from "Low" to "High" along with the DESL command, and the DESL command has to be continuously issued in the number of clocks specified by l_{REFC}. The Self-Refresh exit function is asynchronous operation. It is required that one Auto-Refresh command is issued to avoid the violation of the refresh period just after l_{REFC} from Self-Refresh exit.

Power Down Mode ($\overline{PD}$ = "L")

When all banks are in the idle state and all outputs are in Hi-Z states, the TC59LM814/06CTG become Power Down Mode by asserting $\overline{PD}$ is "Low". When the device enters the Power Down Mode, all input and output buffers except for $\overline{PD}$ are disabled after specified time. Therefore, the power dissipation lowers. To exit the Power Down Mode, $\overline{PD}$ has to be brought to "High" and the DESL command has to be issued at next CLK rising edge after $\overline{PD}$ goes high. The Power Down exit function is asynchronous operation.

Mode Register Set (1st command + 2nd command = RDA + MRS)

When all banks are in the idle state, issuing the MRS command following to the RDA command can program the Mode Register. In a point to notice, the read mode started with the RDA command is canceled by the MRS command having gone into the next clock of the RDA command instead of the LAL command. The data to be set in the Mode Register is transferred using A0 to A14, BA0 and BA1 address inputs. The TC59LM814/06CTG have two mode registers. These are Regular and Extended Mode Register. The Regular or Extended Mode Register is chosen by BA0 and BA1 in the MRS command. The Regular Mode Register designates the operation mode for a read or write cycle. The Regular Mode Register has four function fields.

The four fields are as follows:
(R-1) Burst Length field to set the length of burst data
(R-2) Burst Type field to designate the lower address access sequence in a burst cycle
(R-3) $\overline{\text{CAS}}$ Latency field to set the access time in clock cycle
(R-4) Test Mode field to use for supplier only.

The Extended Mode Register has two function fields.
The two fields are as follows:
(E-1) DLL Switch field to choose either DLL enable or DLL disable
(E-2) Output Driver Impedance Control field.

Once those fields in the Mode Register are set up, the register contents are maintained until the Mode Register is set up again by another MRS command or power supply is lost. The initial value of the Regular or Extended Mode Register after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

- Regular Mode Register/Extended Mode Register change bits (BA0, BA1)
  These bits are used to choose either Regular MRS or Extended MRS

BA1	BA0	Mode Register Set
0	0	Regular MRS
0	1	Extended MRS
1	×	Reserved

Regular Mode Register Fields

(R-1) Burst Length field (A2 to A0)
This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2 or 4 words.

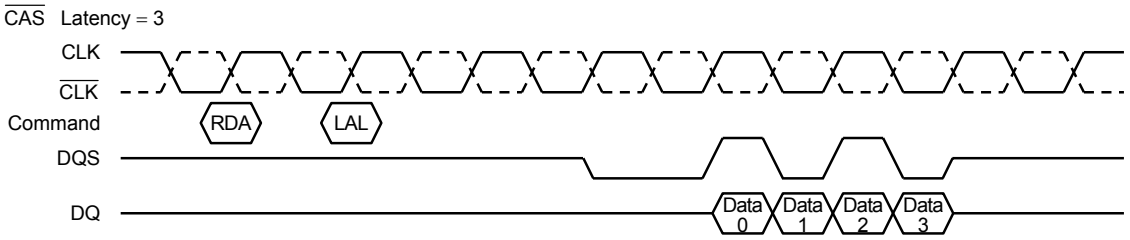
A2	A1	A0	BURST LENGTH
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	Reserved
1	×	×	Reserved

(R-2) Burst Type field (A3)
The Burst Type can be chosen Interleave mode or Sequential mode. When the A3 bit is “0”, Sequential mode is selected. When the A3 bit is “1”, Interleave mode is selected. Both burst types support burst length of 2 and 4 words.

A3	BURST TYPE
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode (A3)

A column access is started from the inputted lower address and is performed by incrementing the lower address input to the device. The address is varied by the Burst Length as the following.



Addressing sequence for Sequential mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is LA0) not carried from LA0~LA1
Data 1	n + 1	
Data 2	n + 2	4 words (address bits is LA1, LA0) not carried from LA1~LA2
Data 3	n + 3	

- Addressing sequence of Interleave mode

A column access is started from the inputted lower address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	···A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	···A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	

(R-3) $\overline{CAS}$ Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the LAL command following the RDA command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CLK. In a write mode, the place of clock which should input write data is $\overline{CAS}$ Latency cycles – 1.

A6	A5	A4	$\overline{CAS}$ LATENCY
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

(R-4) Test Mode field (A7)

This bit is used to enter Test Mode for supplier only and must be set to “0” for normal operation.

(R-5) Reserved field in the Regular Mode Register

- Reserved bits (A8 to A14)

These bits are reserved for future operations. They must be set to “0” for normal operation.

Extended Mode Register fields

(E-1) DLL Switch field (A0)

This bit is used to enable DLL. When the A0 bit is set “0”, DLL is enabled.

(E-2) Output Driver Impedance Control field (A1 / A6)

This bit is used to choose Output Driver Strength. Four types of Driver Strength are supported.

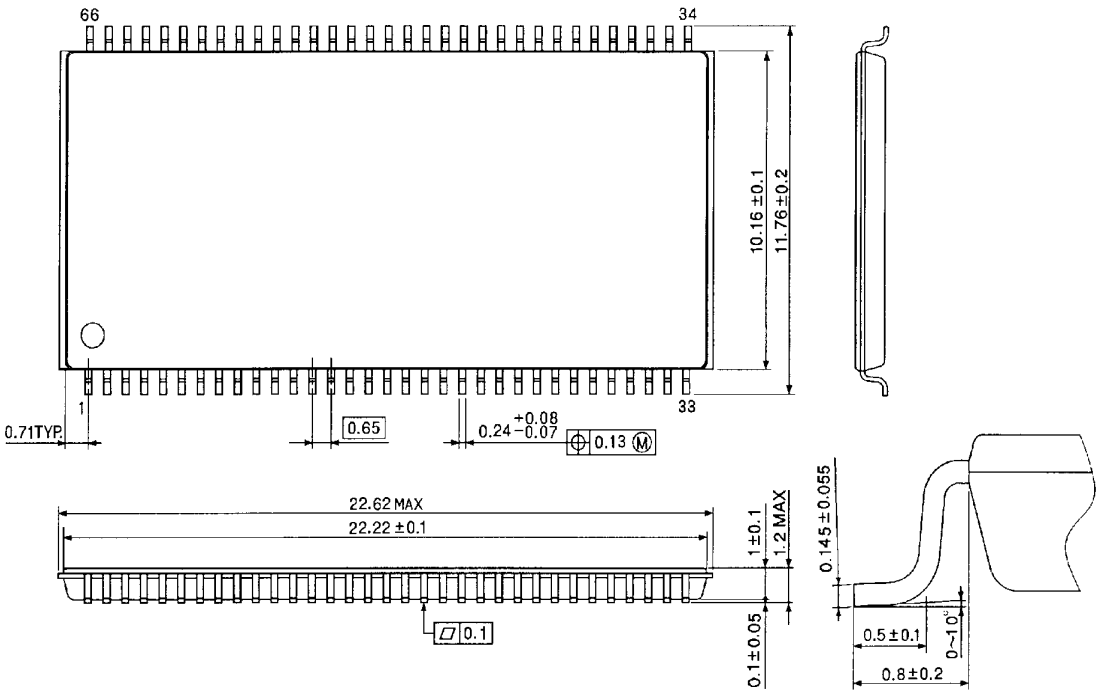
A6	A1	OUTPUT DRIVER IMPEDANCE CONTROL
0	0	Normal Output Driver
0	1	Strong Output Driver
1	0	Weaker Output Driver
1	1	Weakest Output Driver

(E-3) Reserved field (A2 to A5, A7 to A14)

These bits are reserved for future operations and must be set to “0” for normal operation.

PACKAGE DIMENSIONS

TSOP II 66-P-400-0.65 Unit : mm



Weight: 0.51 g (typ.)

REVISION HISTORY

– Rev.1.1 (Jan. 13 '2005)
Datasheet of Lead free released.

– Rev.1.2 (Jun. 21 '2005)
- "-55" speed bin dropped(it marged to "-50").
- Maximum clock cycle time(tCK,max) of "-50" changed from 8.5ns(117MHz) to 12ns(83MHz).
When t_{CK} is between 8.5ns and 12ns at "-50" product, all AC timing parameters refered to spec of "-60" speed version(page 7, 9)

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