NCP6602

Product Preview

Dual Channel Synchronous Rectified Buck MOSFET Driver

The NCP6602 is a two−channel dual MOSFET gate driver optimized to drive the gates of both the high and low−side Power MOSFETs in a MultiPhase Synchronous Buck converter. Each of the drivers is capable of driving a 3000 pF load with only a 12 nS transition time. Together with a wide 5−12 V MOSFET gate drive voltage range, adaptive shoot−through protection and reduced non−overlap time, the NCP6602 allows optimizing applications for the highest converter efficiency.

Internal bootstrapping on the upper gates utilizes only a single external capacitor to reduce parts cost and count, and allows the use of high−performance cost−effective N−Channel MOSFETs. Undervoltage Lockout circuitry ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection.

The NCP6602 is pin−to−pin compatible with the Intersil HIP6602B with the following advantages:

- Faster Rise and Fall Times with Higher Drive Capability
- Reduced Nonoverlap Times for Better Efficiency
- Thermal Shutdown for System Protection

Features

- Adaptive Shoot−Through Protection
- Three−State Input for Bridge Shutdown
- Undervoltage Lockout to Prevent Switching when the Input Voltage is Low
- LGATE to Phase Pull−Down Resistor Prevents HV Supply−Induced Turn On of High−Side MOSFET
- LGATE to PGND Pull−Down Resistor Prevents Transient Turn On of Low−Side MOSET
- Available in 14 Lead SOIC or 16 Lead QFN Thermally Enhanced Package

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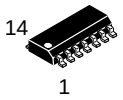
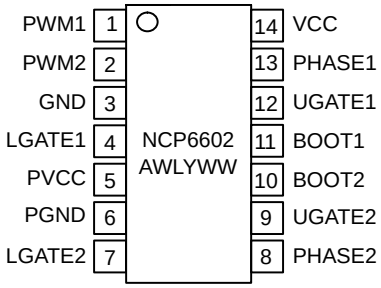


SO−14
D SUFFIX
CASE 751A

QFN−16
MN SUFFIX
CASE 485AC

PIN CONNECTIONS AND MARKING DIAGRAMS

SO−14



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP6602DR2	SO−14	2500 Tape & Reel
NCP6602MNR2	QFN−16	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

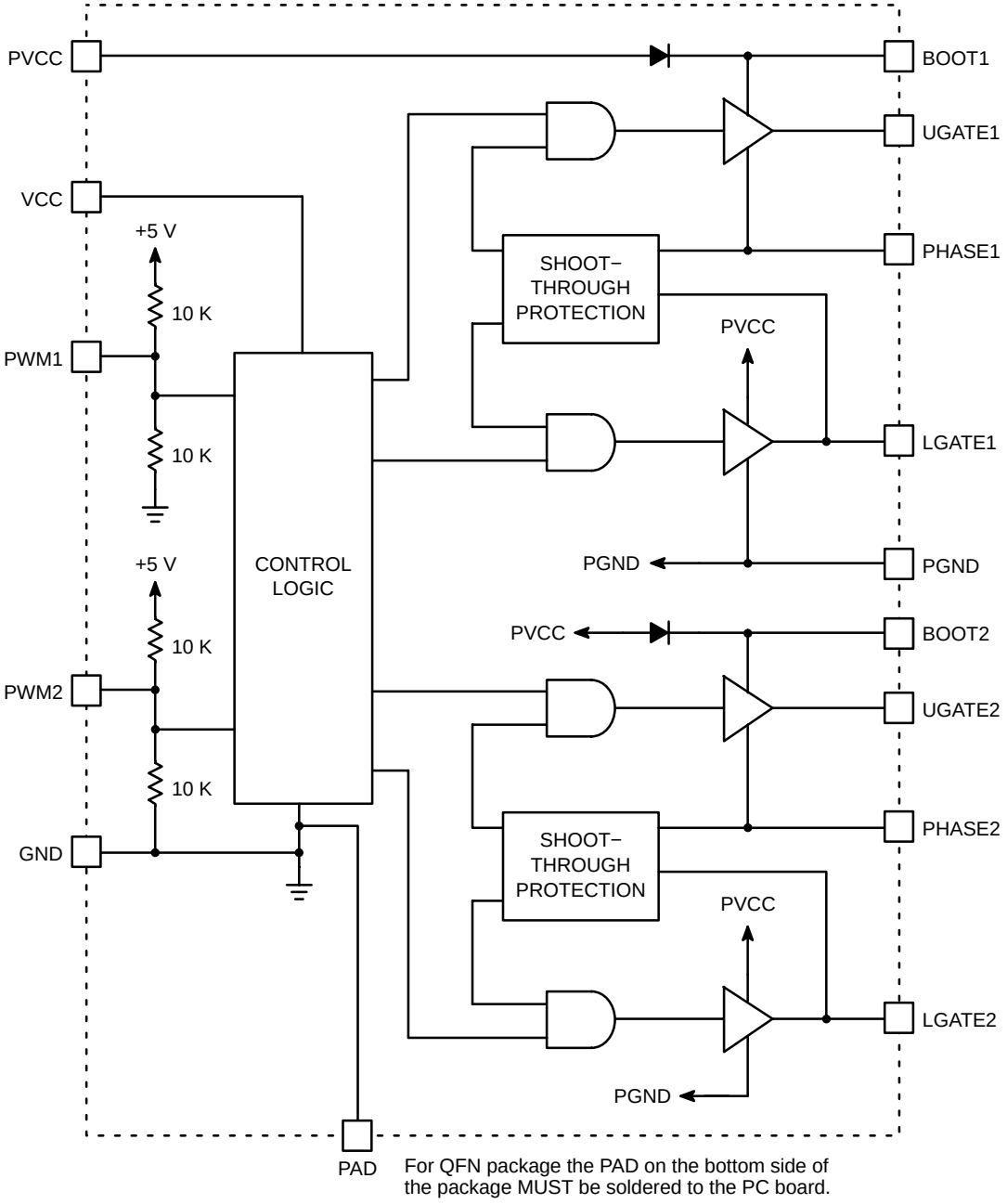


Figure 1.

PIN FUNCTION DESCRIPTION

Pin (QFN)	Pin (SOIC)	Pin Symbol	Description
11, 10	11, 10	BOOT1, BOOT2	Upper MOSFET floating Bootstrap Supply. A capacitor connected between BOOT and PHASE pins holds this bootstrap voltage for the high−side MOSFET as it is switched. The recommended capacitor value is between 100 nF and 1.0 μF.
15, 16	1, 2	PWM1, PWM2	This pin has primary control of the drive outputs from the controller.
1	3	GND	Ground. Ground for V_{CC}.
14	14	VCC	Input Supply. A 1.0 μF ceramic capacitor should be connected from this pin to GND.
12, 9	12, 9	UGATE1, UGATE2	Buck Drive. Output drive for the Upper MOSFET.
4	6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
13, 7	13, 8	Phase1, Phase2	Return path for the upper gate drive.
2, 6	4, 7	LGATE1, LGATE2	Synchronous Rectifier Drive. Output drive for the Lower MOSFET.
3	5	PVCC	Supplies the Upper & Lower Gate Drive Voltage. Connect from 5.0 V to 12 V. A 1.0 μF ceramic capacitor should be connected from this pin to PGND.
5, 8	−	NC	No Connect.

MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Operating Ambient Temperature	T_A	0−85	°C
Operating Junction Temperature	T_J	internally limited by thermal shutdown	
Package Thermal Resistance: Junction to Ambient (QFN) Junction to Ambient (SOIC)	 $R_{\theta JA}$ $R_{\theta JA}$	 36 68	°C/W
Storage Temperature Range	T_S	−65 to 150	°C
Lead Temperature Soldering (10 sec): Reflow: (SMD styles only) (Note 1)	−	300	°C
JEDEC Moisture Sensitivity (QFN) (SOIC)	 MSL MSL	 2 1	−

1. 60 seconds maximum above 183°C.

*The maximum package power dissipation must be observed.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC}	Supply Voltage	15 V	−0.3 V	NA	250 mA DC
P_{VCC}	Supply Voltage	V_{CC} + 0.3 V	−0.3 V	NA	2.0 A Peak (< 100 μs) 250 mA DC
BOOT1, BOOT2	Boot Voltage	30 V wrt/PGND 15 V wrt/Phase	−0.3 V wrt/Phase	NA	2.0 A Peak (< 100 μs) 250 mA DC
Phase1, Phase2	Switch Node	15 V DC 26 V (< 400 nS)	PGND – 5.0 V (< 400 nS) PGND – 0.3 V (> 400 nS)	2.0 A Peak (< 100 μs) 250 mA DC	NA
UGATE1, UGATE2	Upper Gate	V_{BOOT} + 0.3 V	V_{PHASE} –5.0 V (< 400 nS) V_{PHASE} – 0.3 V (> 400 nS)	2.0 A Peak (< 100 μs) 250 mA DC	2.0 A Peak (< 100 μs) 250 mA DC
LGATE1, LGATE2	Lower Gate	V_{PVCC} + 0.3 V	PGND – 5.0 V (< 400 nS) PGND – 0.3 V (> 400 nS)	2.0 A Peak (< 100 μs) 250 mA DC	2.0 A Peak (< 100 μs) 250 mA DC
PWM1, PWM2	Input	7.0 V	GND −0.3 V	1.0 mA	1.0 mA
PGND	Power Ground	0 V	0 V	2.0 A Peak (< 100 μs) 250 mA DC	NA
GND	Ground	PGND + 0.3 V	PGND – 0.3 V	–	–

NOTE: All voltages are with respect to PGND except where noted.

NCP6602−SPECIFICATIONS (Note 2) (V_{CC} = 12 V ± 10%, PVCC = 5.0 V to 12 V, T_A = 0°C to +85°C unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
V_{CC} SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	f_{PWM} = 500 kHz, V_{PVCC} = 12 V	−	3.7	5.0	mA
Power Supply Current	I_{PVCC}	f_{PWM} = 500 kHz, V_{PVCC} = 12 V	−	2.0	4.0	mA
POWER−ON RESET						
V_{CC} Rising Threshold	−	−	−	9.6	−	V
V_{CC} Falling Threshold	−	−	−	7.6	−	V
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 0 or 5.0 V	−	500	−	μA
PWM Rising Threshold	−	V_{PVCC} = 12 V	−	3.2	3.6	V
PWM Falling Threshold	−	V_{PVCC} = 12 V	1.4	1.6	−	V
Shutdown Window	−		1.4	−	3.6	V
Shutdown Holdoff Time	−		−	230	−	ns
UGATE Rise Time	TR_{UGATE}	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	16	−	ns
LGATE Rise Time	TR_{LGATE}	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	12	−	ns
UGATE Fall Time	TF_{UGATE}	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	15	−	ns
LGATE Fall Time	TF_{LGATE}	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	12	−	ns
UGATE Turn−Off Propagation Delay	$TPDL_{UGATE}$	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	25	−	ns
UGATE Non−Overlap Time	$TPDH_{UGATE}$	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	30	−	ns
LGATE Turn−Off Propagation Delay	$TPDL_{LGATE}$	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	25	−	ns
LGATE Non−Overlap Time	$TPDH_{LGATE}$	V_{PVCC} = V_{VCC} = 12 V, 3.0 nF Load	−	27	−	ns
UGATE Source Impedance	R_{UGATE}	V_{PVCC} = 5.0 V, V_{VCC} = 12 V V_{PVCC} = V_{VCC} = 12 V	− −	TBD 1.0	− −	Ω
UGATE Sink Impedance	R_{UGATE}	V_{PVCC} = 5.0 V, V_{VCC} = 12 V V_{PVCC} = V_{VCC} = 12 V	− −	TBD 1.0	− −	Ω
LGATE OUTPUT						
LGATE Source Current	I_{LGATE}	V_{PVCC} = 5.0 V, V_{VCC} = 12 V V_{PVCC} = V_{VCC} = 12 V	TBD TBD	TBD TBD	− −	mA
LGATE Source Impedance	R_{LGATE}	V_{PVCC} = 5.0 V, V_{VCC} = 12 V V_{PVCC} = V_{VCC} = 12 V	− −	TBD 1.1	− −	Ω
LGATE Sink Impedance	R_{LGATE}	V_{PVCC} = 5.0 V, V_{VCC} = 12 V V_{PVCC} = V_{VCC} = 12 V	− −	TBD 1.0	− −	Ω
THERMAL SHUTDOWN						
Over Temperature Protection (Note 2)			150	170	−	°C
Hysteresis (Note 2)			−	20	−	°C

2. All limits at temperature extremes are guaranteed via correlation using Standard Statistical Quality (SQC).
3. AC specifications are guaranteed by characterization, but not production tested.
4. For propagation delays, “tpdh’’ refers to the specified signal going high; “tpdl’’ refers to it going low.
Specifications subject to change without notice.

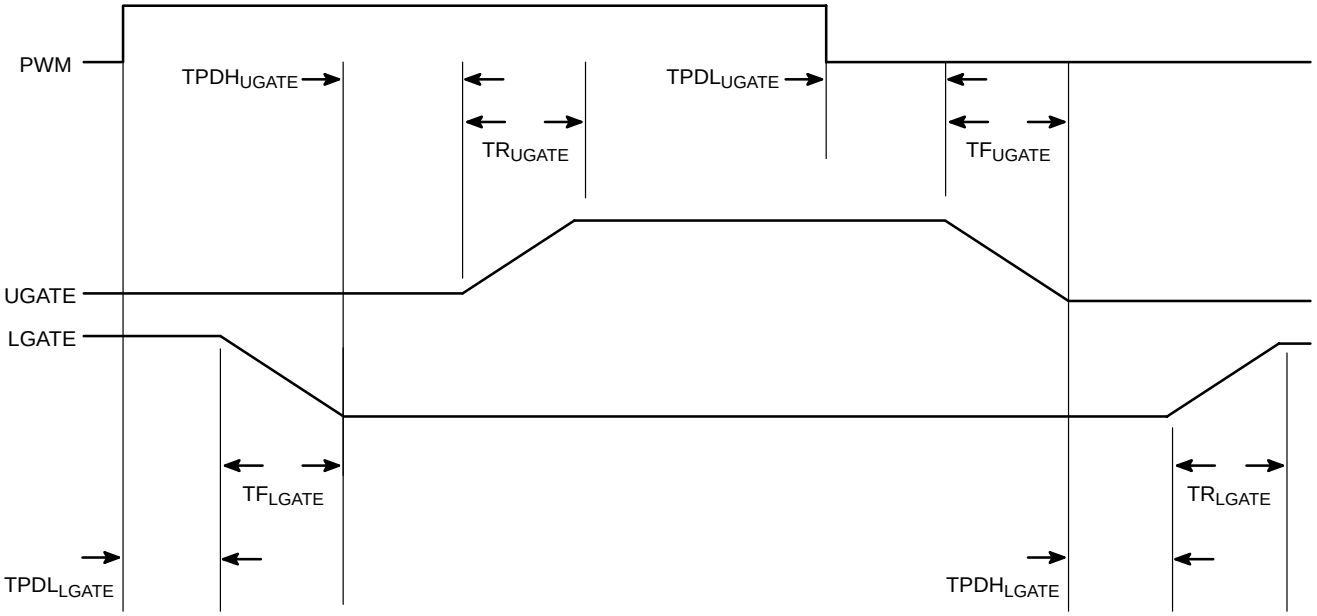


Figure 2. Timing Diagram

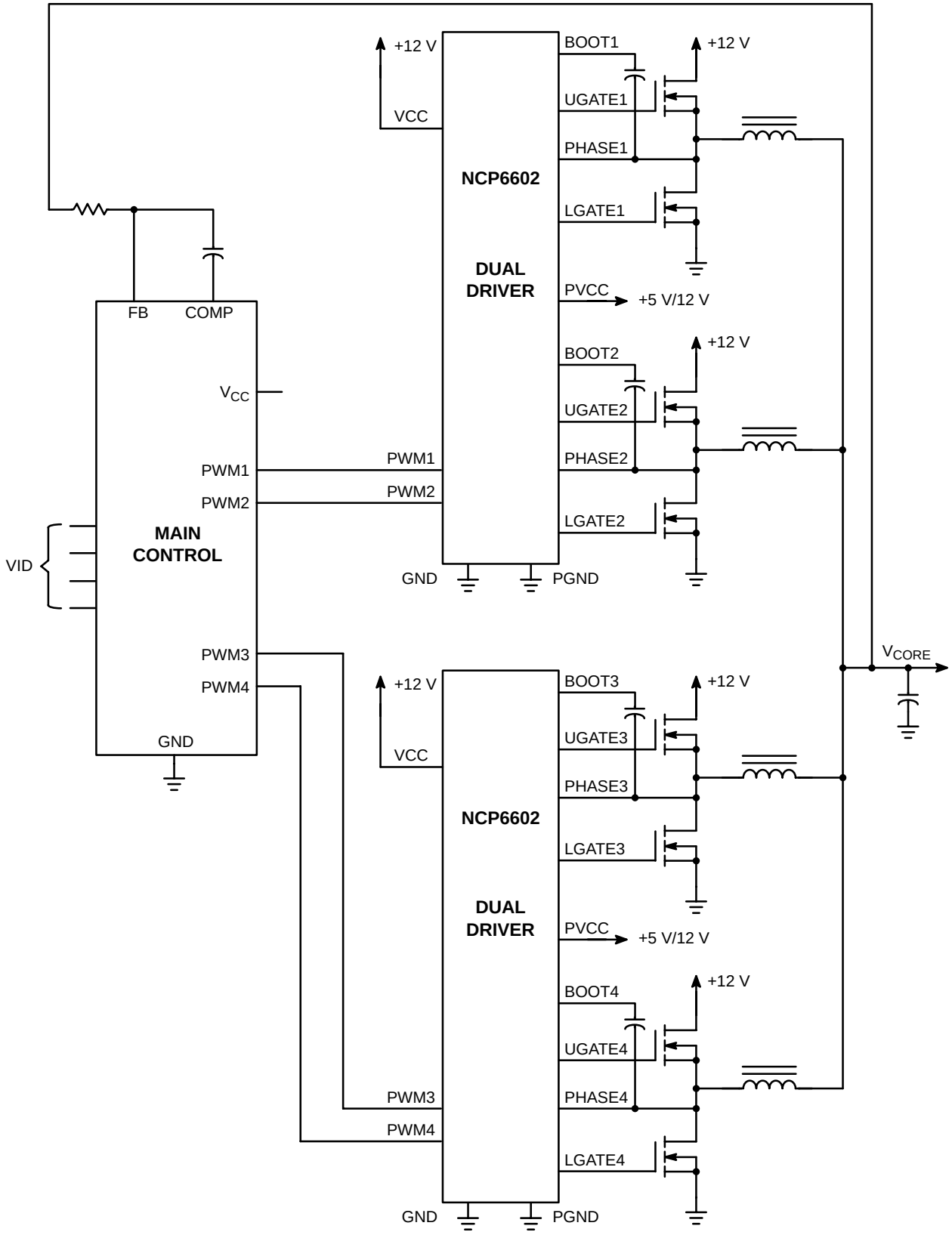
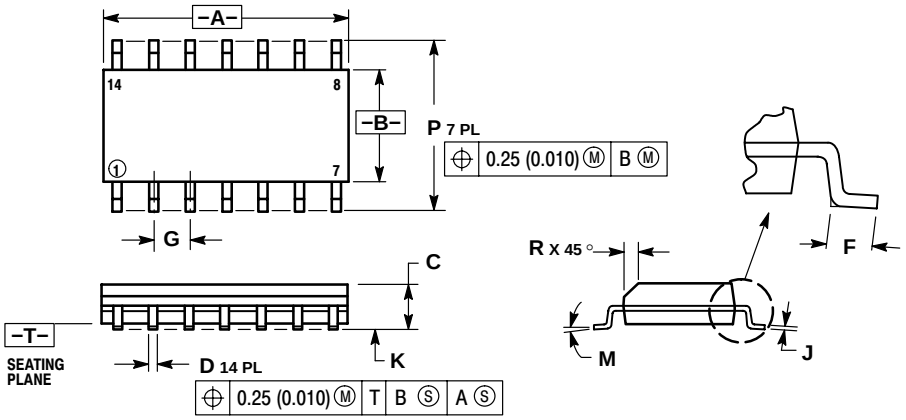


Figure 3. Four Phase Converter Using Two NCP6602 Gate Drivers

PACKAGE DIMENSIONS

SO−14
D SUFFIX
CASE 751A−03
ISSUE F

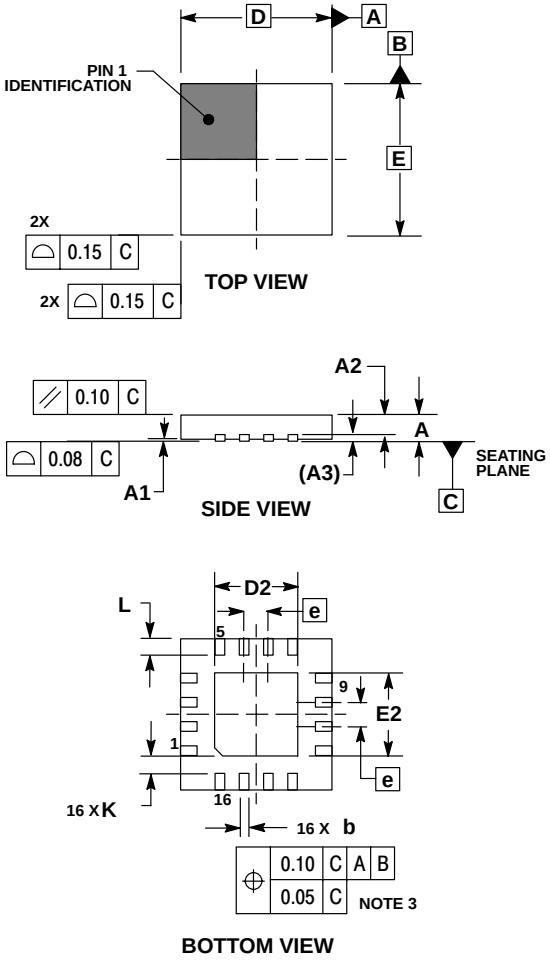


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

16 PIN QFN, 5X5, 0.8 MM
MN SUFFIX
CASE 485AC−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.25	0.35
D	5.00 BSC	
D2	2.55	2.85
E	5.00 BSC	
E2	2.55	2.85
e	0.80 BSC	
K	0.20	−−−
L	0.35	0.75

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