Integrated Circuit Systems, Inc.

ICS1531

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Chip Stage: Preliminary Product Preview

Triple 8-bit 100/140/165 MSPS ADC with Line-Locked Clock Generator

General Description

The ICS1531-100, -140 and -165 chips are each high-performance, cost-effective, 3-channel, 8-bit analog-to-digital converters with an integrated line-locked clock generator. They are part of a family of chips for high-resolution video applications that use analog inputs, such as LCD monitors, LCD projectors, plasma displays, and projection TVs. Using low-voltage CMOS mixed-signal technology, they are an effective data-capture solution for VGA to UXGA.

The ICS1531 chips offer analog-to-digital data conversion and synchronized pixel-clock generation up to 165 Mega samples per second, (MSPS) or 165 MHz. The Dynamic Phase Adjust (DPA) circuitry allows end-user control over the pixel clock phase, relative to the recovered sync signal and analog pixel data. Either the internal pixel clock can be used as a capture clock input to the analog-to-digital converters or an external clock input can be used. The ICS1531 provides either one or two 24-bit pixels per clock. An ADCSYNC output pin provides recovered HSYNC from the pixel clock phase-locked-loop (PLL) divider chain output, which can be used to synchronize display enable output.

A clamp signal can be generated internally or provided through the CLAMP pin. An adjustable-gain video amplifier fine tunes the analog signal. The PLL uses an internal programmable feedback divider. Two additional, independent programmable PLLs, each with spread-spectrum functionality, support memory and panel clock requirements.

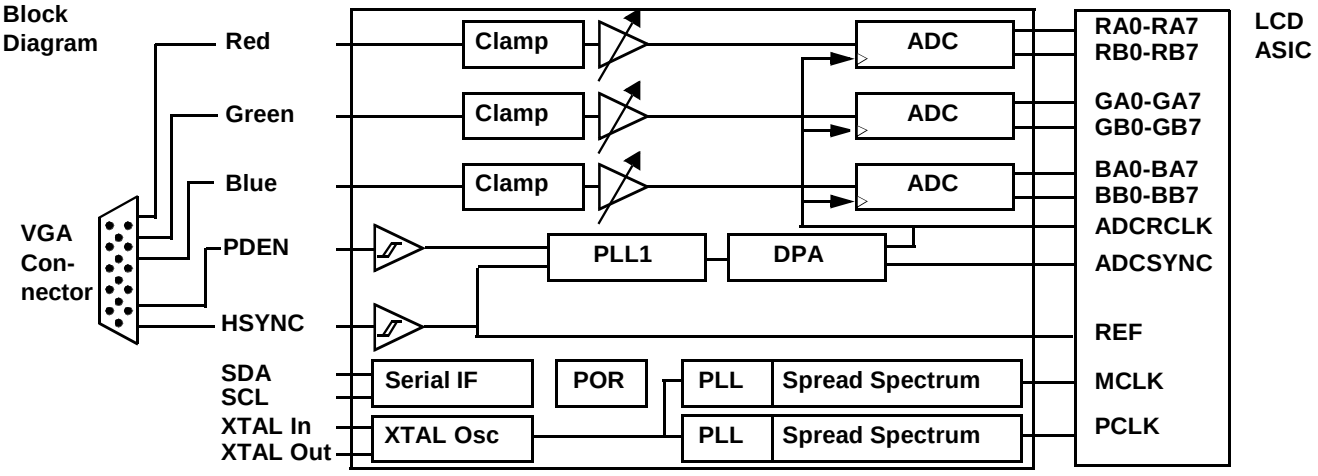
Features

- 3-channel 8-bit analog-to-digital conversion up to 165 MHz
- Uses 3.3 VDC. Digital inputs are 5-V tolerant, which saves design and manufacturing costs.
- Direct connection to analog input data (no external pre-amplification needed)
- Video amplifier: 500-MHz analog bandwidth, software-adjustable gain
- Dynamic Phase Adjust (DPA) for software-adjustable analog sample points
- Software selectable: One pixel per clock (for 24-bit pixels) or two pixels per clock (for a total of 48 bits)
- Internal clamp circuit.
- Very low jitter.
- Low-voltage TTL clock outputs, synchronized with digital pixel data outputs
- Two additional PLLs with spread spectrum for memory and panel clock
- Automatic Power-On Reset (POR) detection
- Industry-standard two-wire serial interface speeds: low (100 kHz), high (400 kHz), or ultra (800 kHz)
- Lock detection available in hardware and software
- 144-pin low-profile quad flat pack (LQFP) package

Applications

- LCD displays, LCD projectors, plasma displays, and projection TVs

Block Diagram



Overview

Summary

The ICS1531 addresses stringent display system line-locked applications by providing clock signals and digitized pixel data through internal high-performance analog-to-digital converters (ADCs). The ICS1531 is a complete solution for capturing analog red, green, and blue (RGB) signals from personal computers and workstations. It supports data capture for resolutions from VGA (640 × 480) to UXGA (1600 × 1200).

Clamp, Video Amplifier, and Analog-to-Digital Circuits (Condition RGB Inputs)

Clamp Circuits (Adjust RGB Inputs to ADC Range)

To properly digitize incoming RGB analog signals, the ICS1531 must adjust the signals to the range of the ADC. This adjustment is done by clamping the signal, which both (1) establishes a bottom voltage limit and (2) offsets the signal to align the black level of the incoming signal with the bottom voltage limit. Then the signal is amplified to adjust the top limit to the upper range of the ADC.

The ICS1531 incorporates an internal clamping circuit to generate a clamping signal. Optionally, the CLAMP pin can be used to input an externally generated clamp signal. In either case, the polarity of the signal to a clamp can be programmed. Typically, the clamp signal is generated by ADCSYNC (the recovered HSYNC timing pulse). The clamp signal is generated during a non-display region of time, when most PC display controllers output a black signal.

Video Amplifier Circuits (Amplify RGB Inputs)

The ICS1531's video amplifier circuit can directly accept analog RGB input signals from a PC display controller (that is, no external pre-amplifier is required). The video amplifier circuit has three independent 500-MHz video amplifiers for the RGB inputs. To adjust the top level of the signal, this video amplifier circuit can be programmed for a gain of 1.0, 1.2, 1.4, or 1.6. As a result, the video amplifier circuit can improve low-amplitude signals and adjust analog input signals for the optimum sampling range of the ADC circuit.

Analog-to-Digital Circuits (Digitize RGB Inputs)

The ICS1531 has high-performance analog-to-digital converters (ADCs) to digitize analog RGB data. Low-power CMOS technology is used to create 8-bit ADCs, which are calibrated to align the capture event between (1) the 3 analog input channels and (2) either 3 or 6 digital output channels. The ADC can provide one of the following:

- Two 24-bit pixels aligned to a half-rate pixel clock (two-pixels-per-clock mode), which can be used for 48-bit interface panels and image-scaling chips
- One 24-bit pixel aligned to a full-rate pixel clock (one-pixel-per-clock mode), which can be used for single-pixel-per-clock applications

In addition, programmable digital-to-analog converters for the R, G, and B inputs fine tune VRTR, VRTG, and VRTB, the individual R, G, and B maximum reference 'top' voltages.

Phase-Locked Loop (Generates Pixel Clock from Input HSYNC)

The ICS1531 uses a phase-locked loop (PLL) to generate its pixel clock output frequency. A PLL is a closed-loop feedback system that uses feedback to lock an output signal's phase and frequency to that of a reference input signal's phase and frequency. In the case of the ICS1531, when its PLL is locked it locks a pixel clock output to that of an HSYNC signal from input video.

- **Output Frequency.**

  The ICS1531 can use either an external loop filter or (more typically) an internal loop filter to filter the signal for the output frequency. The advantage of the internal loop filter is that it can be used for all Video Electronics Standards Association (VESA) timing modes, for ease in manufacturing.

- **Reference Input Frequency.**
  - **HSYNC.**

    Typically, the reference input frequency to the PLL block comes from the HSYNC of a PC display controller. This HSYNC signal can have a transition time of tens of nanoseconds. Furthermore, if the HSYNC signal is from a remote source, its pulses can degrade. To condition the HSYNC signal before it is input to the PLL's Phase/Frequency Detector, a high-performance Schmitt trigger sharpens HSYNC. The polarity of this input pulse can be programmed. The conditioning result is REF, a clean reference clock signal that compared to input HSYNC has a short transition time.
  - **Oscillator.**

    Alternatively, the input signal to the PLL block can be from an oscillator.

Analog-to-Digital Converter (Synchronizes Data Capture)

By using the internal 3-channel analog-to-digital converter (ADC), the ICS1531 internally uses the clock generated by the PLL. This clock then provides the pixel clock needed to synchronize data capture.

The pixel clock can be further processed by the Dynamic Phase Adjust. For the pixel clock to appear on the CLK pin, the pixel clock output must be enabled.

Additional PLLs, with Spread Spectrum (Drive Clocks for Memory and Panel Data)

Besides the pixel clock PLL, the ICS1531 has two other independent PLLs for use as needed. Typically, one of the PLLs is used to drive memory clocks and the other PLL is used to drive panel data clocks. Both of these additional PLLs are tailored for the required frequency ranges. Each supports software-controlled spread-spectrum clock dithering to reduce measured electro-magnetic interference (EMI).

Dynamic Phase Adjust (Positions the Pixel Clock)

So that analog pixel data inputs can be properly sampled and digitized, the ICS1531's pixel PLL tracks the input HSYNC signal and the line-to-line jitter. To provide a properly aligned sampling clock (ADCSYNC) to the ADC blocks, the ICS1531's Dynamic Phase Adjust (DPA) circuitry can add delays to the pixel clock position. The delay, which occurs in relation to the edge of ADCSYNC (the recovered HSYNC signal), is added in sub-pixel time increments.

The ICS1531 DPA can be programmed for a value representing incremental sub-pixel delay units. By choosing the proper value, pixel data to the ICS1531 can be sampled at the optimum time for proper digitization and the best-looking display. Typically, a system's microcontroller presets this value, based on either a table or proprietary algorithms. The end user can change the value through the system's on-screen display controls.

The following table lists the number of possible delay element units that can be used to program to add a delay of up to one pixel clock period, in increments of either 16, 32, or 64.

Increments for Delay Element Units

Number of Delay Element Units	Pixel Clock Range, MHz
16	55 – 260
32	27 – 130
64	14 – 64

Automatic Power-On Reset Detection (Automatically Resets ICS1531)

The ICS1531 automatically detects power-on resets. As a result, the ICS1531 resets itself if the supply voltage drops below threshold values. No external connection to a reset signal is required.

Industry-Standard 2-Wire Serial Interface (Accesses Registers)

To access all its registers, the ICS1531 uses an industry-standard 2-wire serial interface that operates at one of the following speeds:

- A low speed of 100 kHz
- A high speed of 400 kHz
- An ultra speed of 800 kHz

For use with the 2-wire serial interface, the ICS1531 has 5 V-tolerant inputs. The ICS1531 can use either of two unique, alternative sets of addresses.

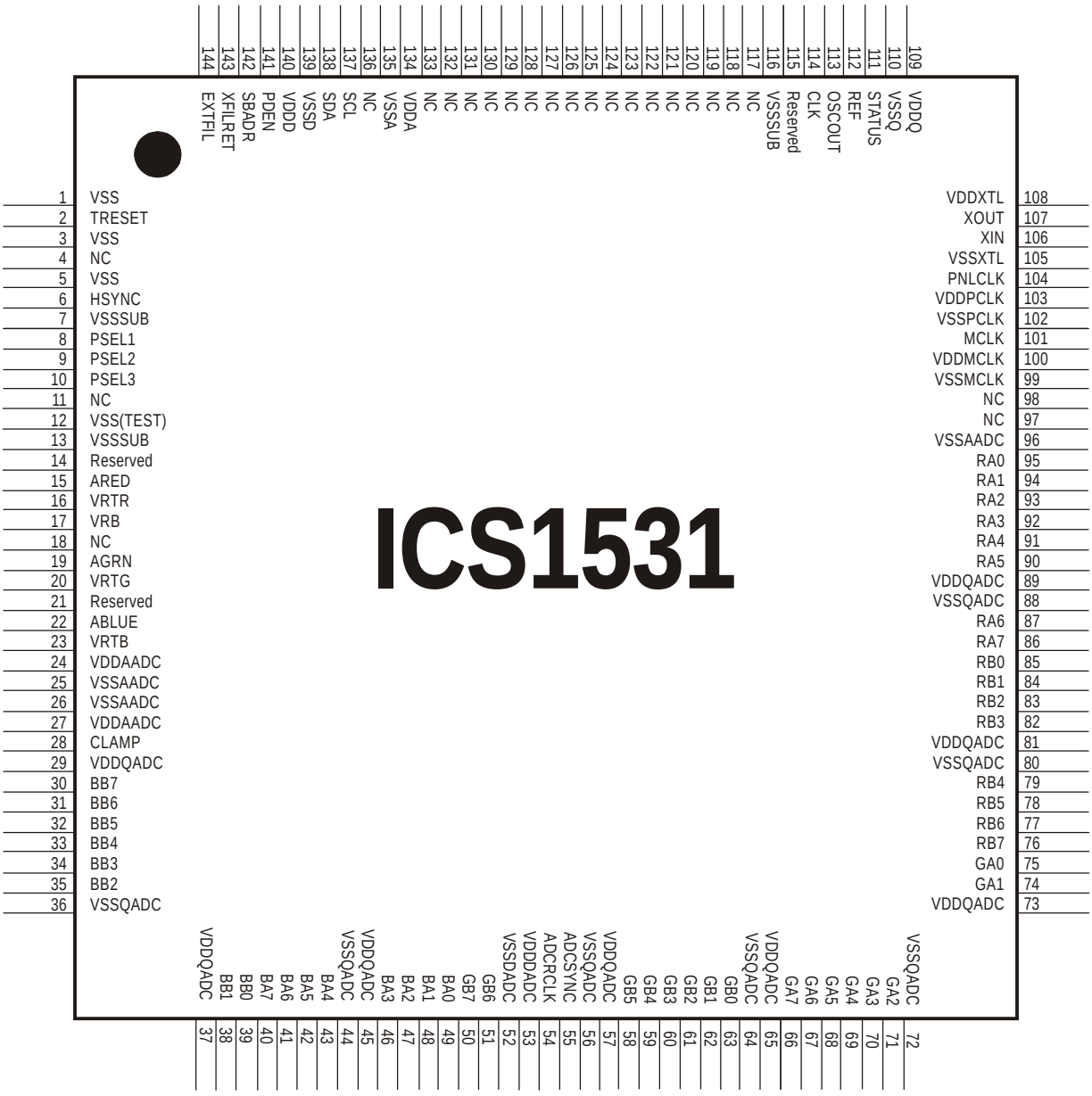
Programmable Outputs

For general-purpose outputs, the ICS1531 provides three programmable pins, PSEL3, PSEL2, PSEL1.

Board Manufacture and Layout

For information on how to manufacture and lay out a printed circuit board so the ICS1531 operates at peak performance, on the ICS website see the 1531LG Layout Guide.

Pin Diagram



Pin Listings, by Functional Grouping

Clock Pins

Table 1. Clock Pins

Pin Name	Pin Type	Pin Description
ADCRCLK	O	**Analog-to-Digital Converter Reference Clock:** Outputs a half-rate pixel clock for latching digital pixel data. Typically, it connects to an LCD panel controller/scaler.
ADCSYNC	O	**Analog-to-Digital Converter Sync:** Provides a recovered HSYNC signal (that is, an HSYNC signal conditioned by a Schmitt trigger) that aligns to an ADCRCLK.
CLK	O	**Clock:** Outputs full-rate pixel clock.
MCLK	O	**Memory Clock:** • This pin provides an independent user-programmable clock source. • Typically, this pin is used by LCD panel controller/scaler chips or microcontrollers.
OSCOUT	O	**Oscillator Output:** A crystal oscillator, the output frequency from which is one of the following: • The same frequency as the input frequency to the crystal oscillator • The frequency that results when the input frequency is divided by a programmable value
PNLCLK	O	**Panel Clock:** Used as a clock source for an LCD panel controller.
REF	O	**Reference:** Provides a reference line clock sync signal.
XIN	I	**Crystal Input:** Accepts input from a 14.31818-MHz crystal or external clock source.
XOUT	O	**Crystal Output:** For applications using the MCLK outputs, connect this pin to a 14.31818-MHz crystal.

Control Pins

Table 2. Control Pins

Pin Name	Pin Type	Pin Description
CLAMP	I	**Clamp:** Accepts an external signal provided as an alternative to the ICS1531's internally generated clamp signal.
PSEL1,2,3	O	**Programmable Select 1, 2, 3:** Used as general-purpose programmable output pins.
TRESET	I	**Test Reset.** When the ICS1531: • Is not in Test mode, this pin has no effect. • Is in Test mode, this pin acts as a reset that sets the ICS1531 to an initial known state.

Pixel Data Pins

Table 3. Pixel Data Pins

Pin Name	Pin Type	Pin Description
ABLUE, AGRN, ARED	I	**Analog Blue, Analog Green, Analog Red:** Accept analog data for ADC blue, green, and red channels, respectively (typically from a PC graphics controller).
BA0 – BA7, GA0 – GA7, RA0 – RA7	O	**Blue (Even Data) A0 – A7, Green (Even Data) A0 – A7, Red (Even Data) A0 – A7:** First blue, green, and red pixel data, respectively.
BB0 – BB7, GB0 – GB7, RB0 – RB7	O	**Blue (Odd Data) B0 – B7, Green (Odd Data) B0 – B7, Red (Odd Data) B0 – B7:** Second blue, green, and red pixel data, respectively.

Phase-Locked Loop Pins

Table 4. Phase-Locked Loop Pins

Pin Name	Pin Type	Pin Description
EXTFIL	I	**External Filter (for Pixel Phase-Locked Loop):** Works with XFILRET and other components as part of an optional external filter for the pixel phase-locked loop.
HSYNC	I	**Horizontal Sync:** The clock input for the pixel PLL. Typically it connects to the HSYNC from a PC display controller.
PDEN	I	**Phase-Detector Enable:** The input for the Phase/Frequency Detector enable that can suspend the charge pump activity. It is 5-V tolerant.
STATUS	O	**Status (formerly called 'Lock'):** The signal on this pin is: • Low when a lock condition occurs for one of the selectable PLLs • High when no lock condition occurs for one of the selectable PLLs
XFILRET	I	**External Filter Return (for Pixel PLL):** Works with EXTFIL and other components as part of an optional external filter for the pixel phase-locked loop.

Industry-Standard 2-Wire Serial Bus Pins

Table 5. Industry-Standard 2-Wire Serial Bus Pins

Pin Name	Pin Type	Pin Description
SBADR	I	**Serial Bus Address:** Determines the address for the ICS1531 industry-standard 2-wire serial bus.
SCL	I	**Serial Clock:** The clock for the interface to the industry-standard 2-wire serial bus. 5-V tolerant.
SDA	I/O	**Serial Data:** Connects to the data pin for an industry-standard 2-wire serial bus. 5-V tolerant.

Ground Pins

Table 6. Ground Pins

Pin Name	Pin Description
VSS	**Ground for (Analog Inputs for Digital Pixel PLL Circuitry):** • These pins ground digital portions of the pixel PLL circuitry that receive analog inputs. • The VSSD pin must also connect to these pins.
VSSA	**Ground for Analog (Pixel PLL Circuitry):** Grounds analog portions of the pixel PLL circuitry.
VSSAADC	**Ground for Analog ADC (Circuitry):** Grounds analog portions of the ADC.
VSSD	**Ground for Digital (Pixel PLL and Industry-Standard 2-Wire Serial Bus Circuitry):** Grounds digital portions of the pixel PLL circuitry and the industry-standard 2-wire serial bus circuitry.
VSSDADC	**Ground for Digital ADC (Circuitry):** Grounds digital portions of the ADC.
VSSMCLK	**Ground for Memory Clock (Circuitry):** Grounds circuitry for the memory clock PPL (that is, MCLK).
VSSPCLK	**Ground for Panel Clock (Circuitry):** Grounds circuitry for the panel clock PLL (that is, PNLCLK).
VSSQ	**Ground for Output Drivers:** Grounds output drivers for the pixel PLL circuitry.
VSSQADC	**Ground for Output Drivers for ADC:** Grounds pixel data output drivers for the analog-to-digital converter.
VSSSUB	**Ground for Substrate:** Provide ground for the chip substrate.
VSS(TEST)	**Ground or Test Mode:** Typically, connect this pin to ground (the normal mode).
VSSXTL	**Ground for Crystal Oscillator:** Used to ground the internal crystal oscillator circuitry.

Power Pins

Table 7. Power Pins

Pin Name	Pin Description
VDDA	**(3.3 V) Supply for Analog (Pixel PLL Circuitry):** Supplies 3.3 V to the analog portions of the pixel PLL circuitry.
VDDAADC	**(3.3 V) Supply for Analog ADC (Circuitry).** Supply 3.3 V to the analog portions of the ADC.
VDDD	**(3.3 V) Supply for Digital (Pixel PLL and Industry-Standard 2-Wire Serial Bus) Circuitry:** Supplies 3.3 V to the digital pixel PLL and circuitry for an industry-standard 2-wire serial bus interface.
VDDDADC	**(3.3 V) Supply for Digital ADC (Circuitry):** Supplies 3.3 V to digital portions of the ADC.
VDDMCLK	**(3.3 V) Supply for Memory Clock:** Supplies 3.3 V to the memory clock PLL circuitry.
VDDPCLK	**(3.3 V) Supply for Panel Clock.** Supplies 3.3 V to the panel clock PLL circuitry.
VDDQ	**(3.3 V) Supply for Output Drivers.** Supplies 3.3 V to the output driver circuitry for the pixel PLL.
VDDQADC	**(3.3 V) Supply for Output Drivers for Analog-to Digital Converter.** Supply 3.3 V to pixel data output drivers of the ADC.
VDDXTL	**(3.3V) Supply for Crystal Oscillator.** Supplies 3.3 V to the internal crystal oscillator circuitry.
VRB	**Voltage Reference Bottom.** This pin is a used by the ADC as a bottom reference. Typically, this pin is grounded.
VRTB, VRTG, VRTR	**Voltage Reference Top Blue, Green, Red** • The ADC uses these pins as an alternative to the blue, green, and red top reference voltages from the internal DACs. • Each of these pins must connect to its own separate bypass capacitor.

No-Connect and Reserved Pins

Table 8. No-Connect and Reserved Pins

Pin Name	Pin Description
NC	**No Connect.** Do not connect these pins. Connecting them can affect the performance and operation of the ICS1531 and future members of the ICS153X family.
Reserved	**Reserved:** For use by ICS. Reserved pins must not be connected. Connecting them can affect the performance and operation of the ICS1531and future members of the ICS153X family.