

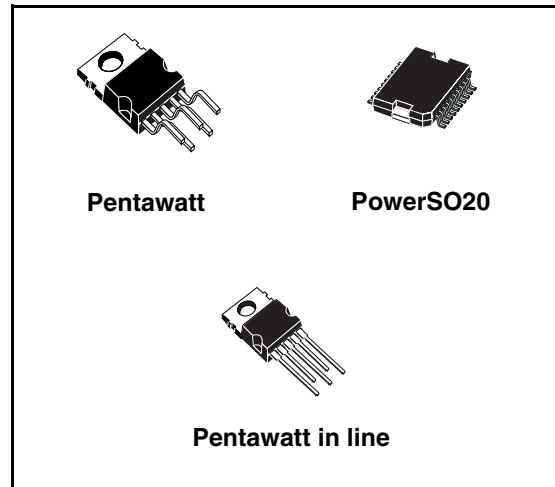
## Very Low Drop Voltage Regulator

### Features

- Operating DC supply voltage range 6V to 28V
- Transient supply voltage up to 40V
- Extremely low quiescent current
- High precision output voltage
- Output current capability up to 500mA
- Very low dropout voltage less than 0.6V
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Thermal shutdown and short circuit protections

### Description

The L4925 is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions such as power-on reset and programmable reset delay time.



It is designed for supplying microcomputer controlled systems especially in automotive applications.

### Order codes

Part number	Package	Packing
L4925	Pentawatt	Tube
L4925L	Pentawatt in Line	Tube
L4925PD	PowerSO20	Tube
L4925PD013TR	PowerSO20	Tape & Reel

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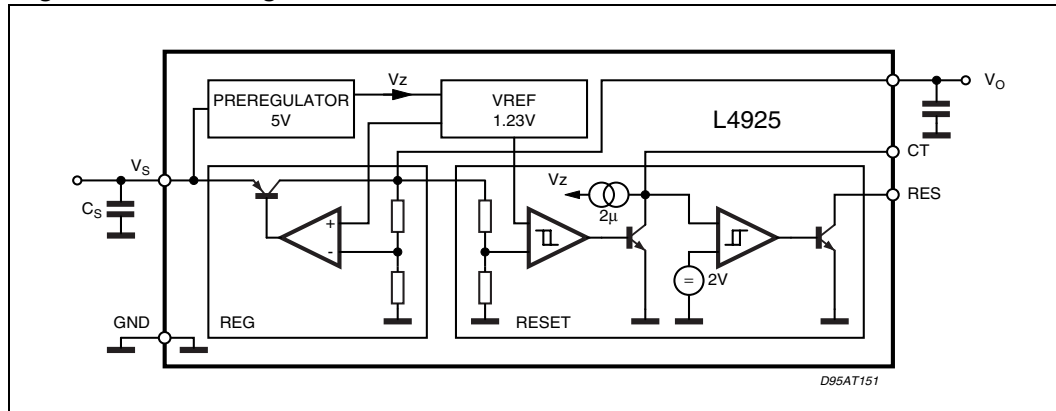
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# 1 Block and Pin Connections diagrams

## 1.1 Block diagram

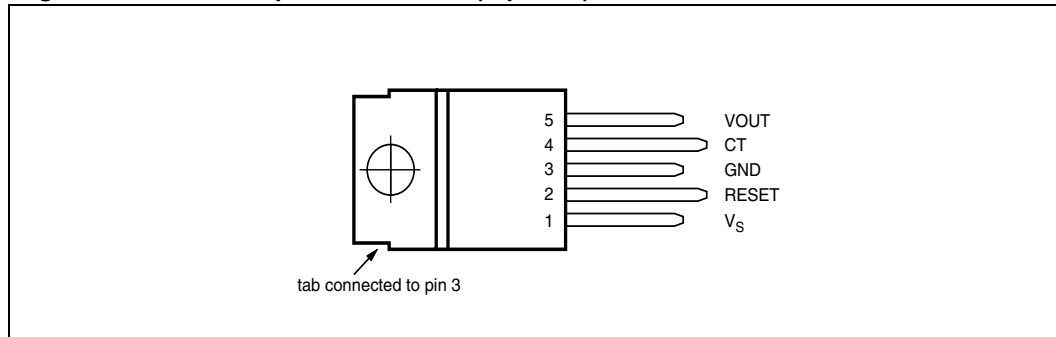
Figure 1. Block diagram



## 1.2 Pin Connections diagrams

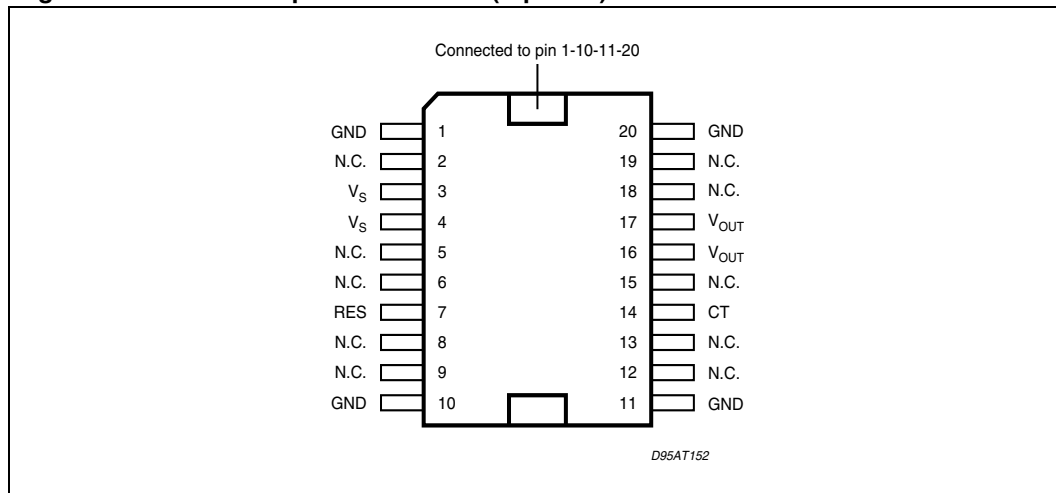
### 1.2.1 Pentawatt pin connections

Figure 2. Pentawatt pin connections (top view)



### 1.2.2 PowerSO20 pin connections

Figure 3. PowerSo20 pin connections (top view)



### 1.3 Thermal data

Table 1. Thermal data

Symbol	Parameter	Pentawatt	PSO20	Unit
$R_{th(j-amb)}$	Thermal Resistance Junction to ambient	20 to 60	15 to 60	°C/W
$R_{th(j-amb)}$	Thermal Resistance Junction to ambient max.	3.5	3.5	°C/W

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{SDC}$	DC Operating Supply Voltage	28	V
$V_{STR}$	Transient Supply Voltage ( $t < 1s$ )	40	V
$I_O$	Output Current	internally limited	
$V_O$	Output Voltage	20	V
$V_{RES}$	Output Voltage	20	V
$I_{RES}$	Output Current	5	mA
$T_{stg}$	Storage Temperature	-55 to 150	°C
$T_j$	Operating Junction Temperature	-40 to 150	°C
$T_{j-SD}$	Thermal Shutdown-Junction Temperature	165	°C

*Note:* The circuit is ESD protected according to MIL-STD-883C. According to ISO/DIS 7637 the transients must be clamped with external circuitry (see Application Circuit).

### 2.2 Electrical characteristics

**Table 3. Electrical characteristics**

( $V_S = 14V$ ;  $T_j = -40$  to  $125^\circ C$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$V_I = 6$ to $28V$ ; $I_O = 1$ to $500mA$	4.90	5	5.10	V
$V_O$	Output Voltage	$V_I = 35V$ ; $T < 1s$ ; $I_O = 1$ to $500mA$			5.50	V
$V_{DP}$	Dropout Voltage	$I_O = 100mA$		0.2	0.3	V
		$I_O = 500mA$		0.3	0.6	V
$V_{IO}$	Input to Output Voltage Difference in Undervoltage Condition	$V_I = 4V$ ; $I_O = 100mA$			0.5	V
$V_{OL}$	Line Regulation	$V_I = 6$ to $28V$ ; $I_O = 1$ to $1mA$			10	mV
$V_{OLO}$	Load Regulation	$I_O = 1$ to $500mA$			50	mV
$I_{LIM}$	Current Limit	$V_O = 4.5V$ ;	550	1000	1500	mA
		$V_O = 0$ ; Foldback characteristic		250		mA
$I_{QSE}$	Quiescent Current	$I_O = 0.3mA$		190	360	$\mu A$

**Table 3. Electrical characteristics** (continued)  
 ( $V_S = 14V$ ;  $T_j = -40$  to  $125^\circ C$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_Q$	Quiescent Current	$I_O = 500mA$			20	mA
<b>RESET</b>						
$V_{RT}$	Reset Threshold Voltage		4.2		4.8	V
$V_{RTH}$	Reset Threshold		50	100	200	mV
$t_{RD}$	Reset Pulse Delay	$C_T = 100nF$ ; $t_R \geq 100\mu s$	60	100	140	ms
$t_{RR}$	Reset Reaction Time	$C_T = 100nF$ ;		5	30	$\mu s$
$V_{RL}$	Reset Output LOW Voltage	$R_{RES} = 10K\Omega$ to $V_O$ ; $V_S = \geq 3V$			0.4	V
$I_{RH}$	Reset Output HIGH Leakage Current	$V_{RES} = 5V$			1	$\mu A$
$V_{CTth}$	Delay Comparator Threshold			2		V
$V_{CTth\ hy}$	Delay Comparator Threshold Hysteresis			200		mV

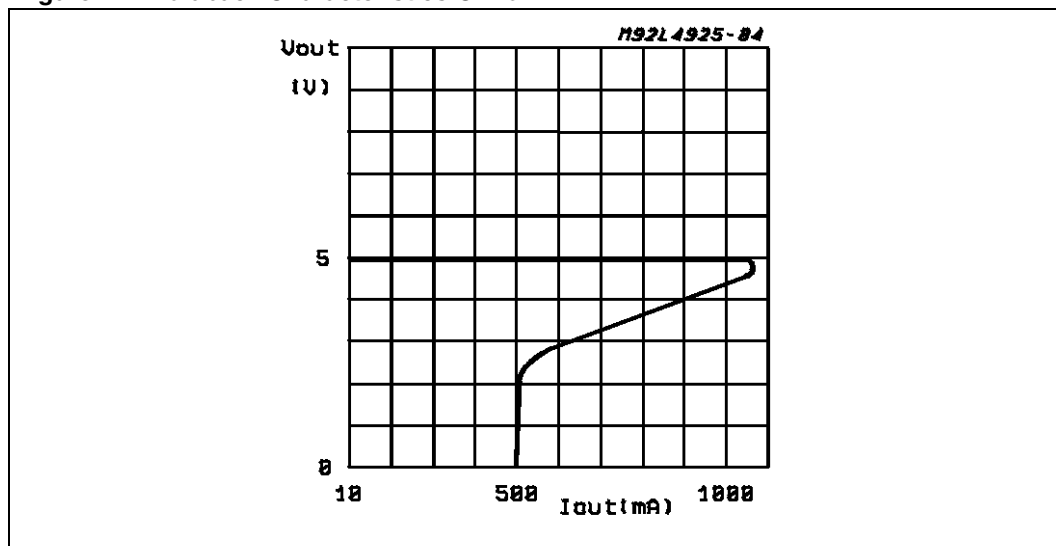
## 3 Functional description

The L4925 is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

### 3.1 Voltage regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. With this structure very low dropout voltage at currents up to 500mA is obtained.

**Figure 4. Foldback Characteristics Of  $V_o$**



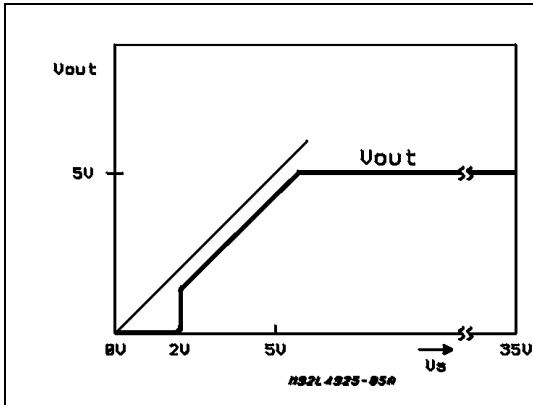
The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 35V. With this feature no functional interruption due to overvoltage pulses is generated.

The typical curve showing the standby output voltage as a function of the input supply voltage is shown in [Figure 5](#).

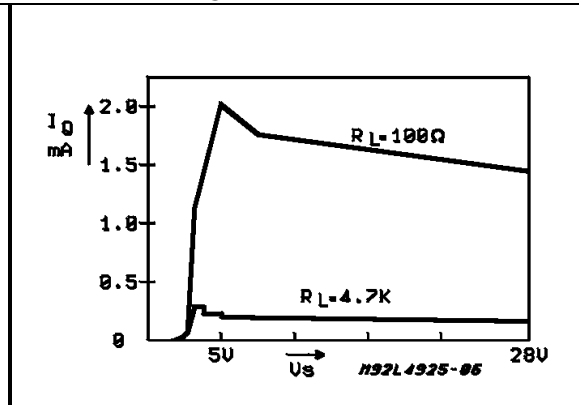
The current consumption of the device (quiescent current) is less than 250 $\mu$ A. To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled.

The quiescent current as a function of the supply input voltage is shown in [Figure 6](#).

**Figure 5. Output voltage vs. input voltage**



**Figure 6. Quiescent current vs. supply voltage**



### 3.2 Reset circuit

The block circuit diagram of the reset circuit is shown in [Figure 7](#). The reset circuit supervises the output voltage. The reset threshold of 4.5V is defined with the internal reference voltage and standby output divider. The reset pulse delay time  $t_{RD}$ , is defined with the charge time of an external capacitor  $C_T$ :

$$t_{RD} = \frac{C_T \cdot 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor  $C_T$  and it is proportional to the value of  $C_T$ . The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50ms. The typical reset output waveforms are shown in [Figure 8](#).

**Figure 7.**

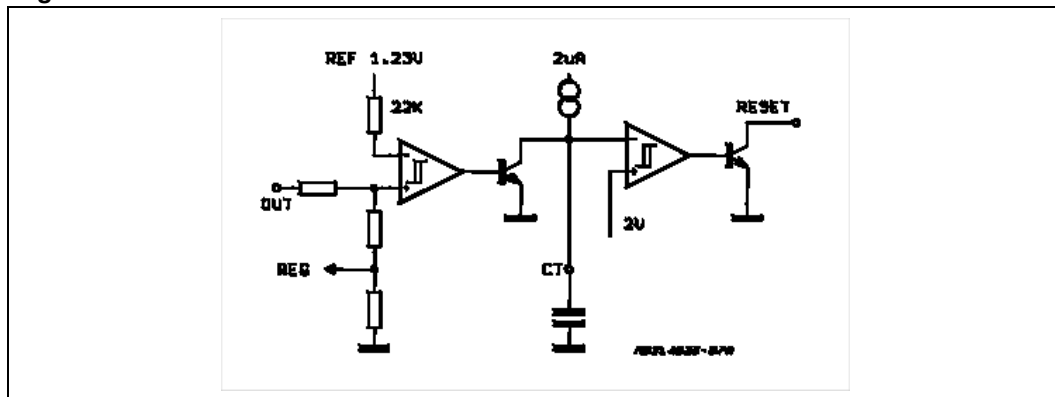
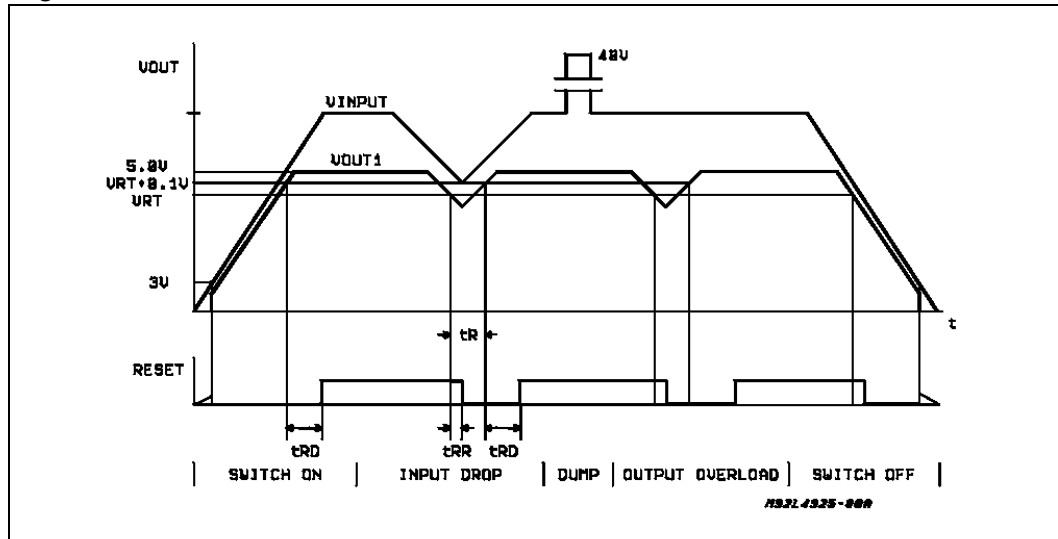




Figure 8.



## 4 Application information

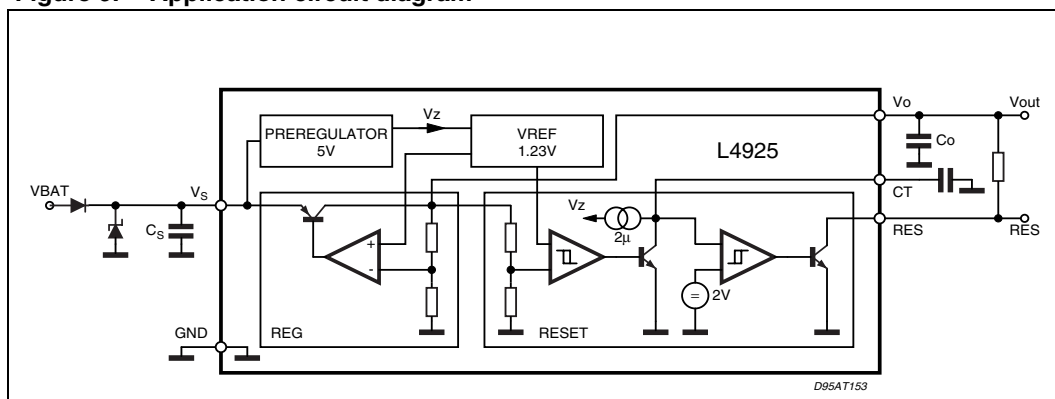
### 4.1 Supply voltage transients

High supply voltage transients can cause a reset output signal disturbance.

For supply voltage greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than 100V/ms. For supply voltage lower than 8V, supply transients of more than 0.4V/ms. can cause a reset signal disturbance.

### 4.2 Application circuit

Figure 9. Application circuit diagram



For stability:  $C_S \geq 1\mu\text{F}$ ;  $C_O \geq 10\mu\text{F}$ ;  $\text{ESR} \leq 2.5\Omega$  at 10 KHz

Recommended for application:  $C_S = C_O = 10\mu\text{F}$  to  $100\mu\text{F}$

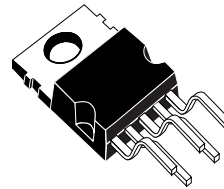
# 5 Package Informations

Figure 10. Pentawatt Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.80			0.188
C			1.37			0.054
D	2.40		2.80	0.094		0.11
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.76		1.19	0.030		0.047
F	0.80		1.05	0.031		0.041
F1	1.00		1.40	0.039		0.055
G	3.20	3.40	3.60	0.126	0.134	0.142
G1	6.60	6.80	7.00	0.260	0.267	0.275
H2			10.40			0.41
H3	10.05		10.40	0.395		0.409
L	17.55	17.85	18.15	0.691	0.703	0.715
L1	15.55	15.75	15.95	0.612	0.620	0.628
L2	21.2	21.4	21.6	0.831	0.843	0.850
L3	22.3	22.5	22.7	0.878	0.886	0.894
L4			1.29			0.051
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
L9	2.10		2.70	0.083		0.106
L10	4.30		4.80	0.170		0.189
M	4.23	4.5	4.75	0.167	0.178	0.187
M1	3.75	4.0	4.25	0.148	0.157	0.187
V4	40° (Typ.)					
V5	90° (Typ.)					
DIA	3.65		3.85	0.143		0.151

## OUTLINE AND MECHANICAL DATA

Weight: 2.00gr



## Pentawatt V

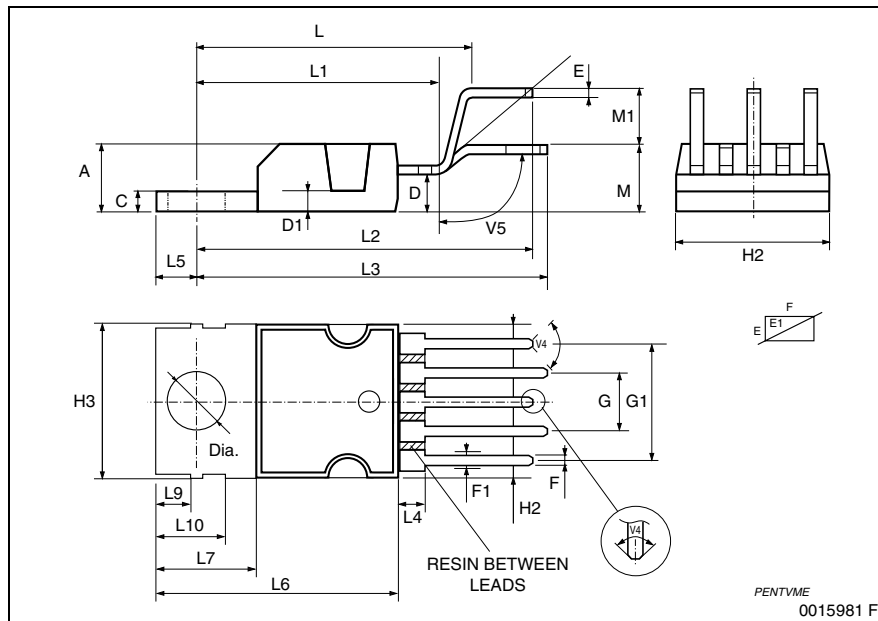


Figure 11. Pentawatt in Line Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.80			0.188
C			1.37			0.054
D	2.40		2.80	0.094		0.11
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.76		1.19	0.030		0.047
F	0.80		1.05	0.031		0.041
F1	1.00		1.40	0.039		0.055
G	3.20	3.40	3.60	0.126	0.134	0.142
G1	6.60	6.80	7.00	0.260	0.267	0.275
H2			10.40			0.41
H3	10.05		10.40	0.395		0.409
L2	23.05	23.40	23.80	0.9075	0.9213	0.9370
L3	25.30	25.65	26.10	0.9961	1.0098	1.0276
L4	0.90		2.90	0.0354		0.1142
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
L9	2.10		2.70	0.083		0.106
L10	4.30		4.80	0.170		0.189
DIA	3.65		3.85	0.143		0.151

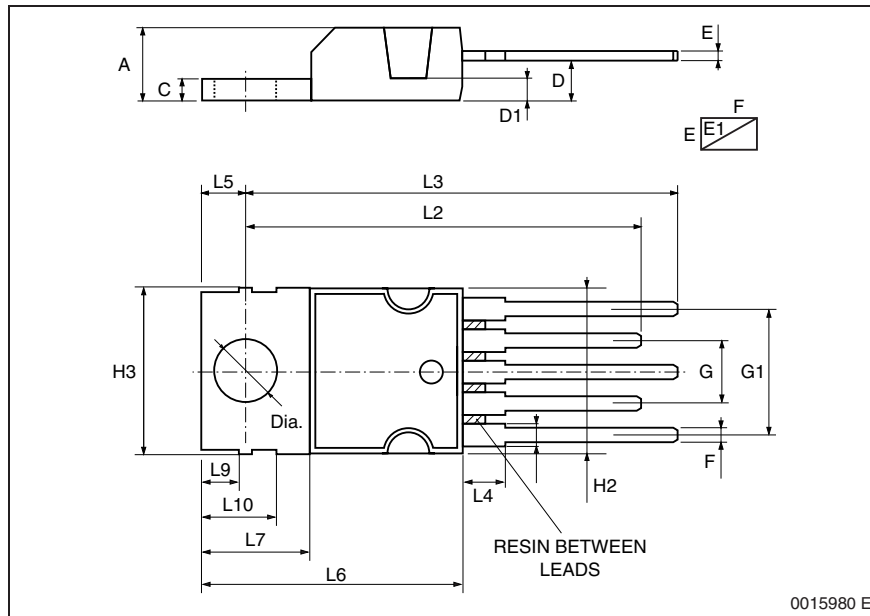
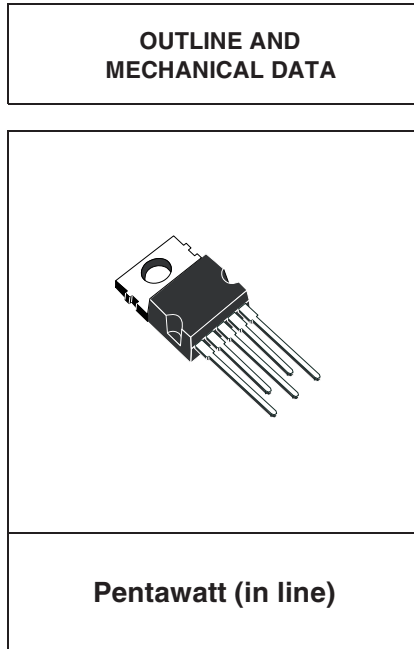


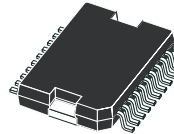
Figure 12. PowerSO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8' (typ.)					
S	8' (max. )					
T		10			0.394	

(1) "D and E1" do not include mold flash or protrusions.  
 - Mold flash or protrusions shall not exceed 0.15mm (0.006")  
 - Critical dimensions: "E", "G" and "a3".  
 (2) For subcontractors, the limit is the one quoted in jedec MO-166

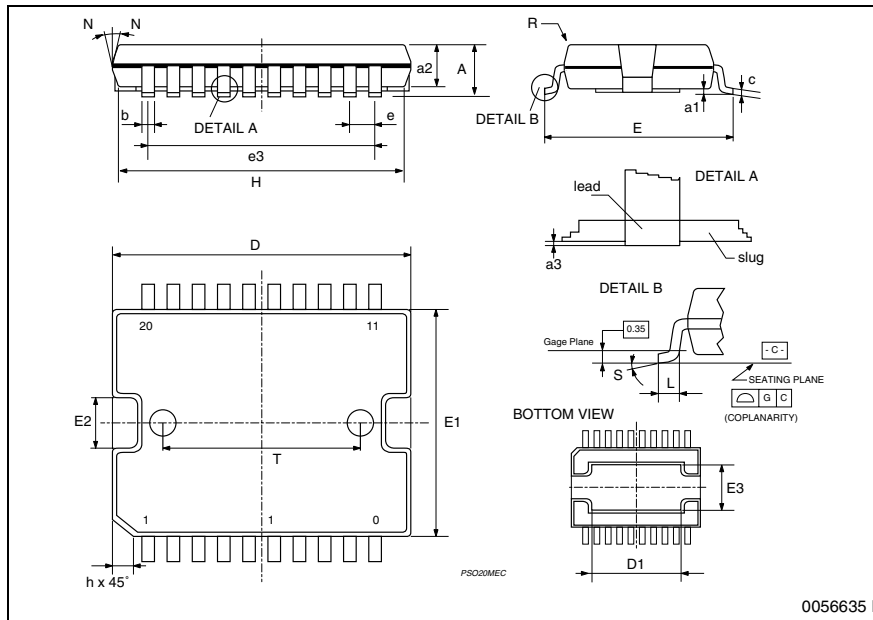
**OUTLINE AND MECHANICAL DATA**

Weight: 1.9gr



JEDEC MO-166

**PowerSO-20**



## 6 Revision history

Date	Revision	Changes
October 2003	4	First issue in EDOCD DMS
18-Nov-2005	5	Added GND pins to fig. 4 Added order code and changed the formatting style in compliance with the new template
03-Feb-2006	6	Reset Threshold Voltage changed from 4.5V / 5.2V (min/max) to 4.2V / 4.8V on <a href="#">Table 3</a> .

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