Features

- 12,441,600-bit Frame Memory
- 74.25MHz Max Data Rate
- May be Organized Into the Following Configurations:
  - 1,555,200 x 8-bit (single channel)
  - 1,244,160 x 10-bit (single channel)
  - 1,036,800 x 12-bit (single channel)
  - 777,600 x 16-bit (width expansion - dual channel)
  - 622,080 x 20-bit (width expansion - dual channel)
  - 518,400 x 24-bit (width expansion - dual channel)
  - 777,600 x 8-bit (each of two parallel channels)
  - 622,080 x 10-bit (each of two parallel channels)
  - 518,400 x 12-bit (each of two parallel channels)
- Operating Modes:
  - Random Access with External Address Port (Single-channel)
  - FIFO With Asynchronous I/O (Single-channel)
  - FIFO With Asynchronous I/O (Dual-channel)
  - Synchronous Shift Register (Single-channel)
  - Synchronous Shift Register (Dual-channel)
  - FIFO + shift register; Channel B Synchronized to Channel A
  - Shift register + FIFO; One channel Synchronized to the other
- Near-Full/Empty Flags With Programmable Thresholds
- Flexible Pointer Manipulation
  - Write and Read Pointers may be independently jumped to arbitrary address locations
  - Write or Read Pointers can be manipulated in real-time based on external 24bit address
- LF3312s may be Cascaded for depth and width, supporting HDTV, Multiframe SDTV, and other high resolution formats
  - Seamless address space is maintained with up to 16 cascaded devices
- Built-in ITU-R BT.656 TRS detection and Synchronization
- Set & Clear Read/Write Pointer Control Pins
- Choice of Control Interfaces:
  - Two-wire Serial Microprocessor Interface
  - Parallel Microprocessor Interface
- Input Enable Control (Write Mask) for freeze-frame applications
- Output Enable Control (Data Skipping)
- JTAG Boundary Scan - IEEE 1149.1
- 172 ball LBGA package
- 1.8V Internal Core Power Supply
- 3.3V I/O Supply

NOTE: This **Preliminary Datasheet** references **LF3312BGC** Engineering Samples with an **ES** marking under the part designation.

Applications

- DTV/HDTV Video Stream Buffer
- Frame Synchronization
- CCTV Security Camera Systems
- Time Base Correction (TBC)
- Freeze-Frame Buffer
- Regional Read/Write for Picture-in-Picture (PIP)
- Field-Based or Frame-Based Comb Filtering
- Video Capture & Editing Systems
- Deep Data Buffering
- Video Special Effects (Rotation, Zoom)
- Test Pattern Generation
- Motion Detection or Frame-to-Frame Correlation

LF3312 Overview

The LF3312 is a 12,441,600-bit memory device which can be configured by the user into either a two-data-port single-channel or a four-data-port dual-channel architecture. The input data ports may be clocked simultaneously or asynchronously with one another and with the output ports. Using the four 12-bit data ports provided, the user can operate the chip as one or two 8, 10, or 12-bit channels or as a single 16, 20, or 24-bit channel, without wasting any memory resources. Since reads are non-destructive, a given data value, once written into the memory core, may be read as many times as desired. A user requiring more storage can cascade up to sixteen LF3312s into a larger array.

A great deal of memory addressing flexibility is offered with the LF3312. In addition to simple clearing of the Write and Read pointers, either pointer may be set/jumped to any location within the entire address space. Real-time random-access Writing or Reading is also supported through an external address port.

The device is controlled by sixteen instruction words of eight bits each, which may be programmed or verified via a standard I²C 2-wire serial or parallel microprocessor interface.

The 3-bit OPMODE control selects one of the chip's operating modes, each of which has versatile submode options:

- One-Channel FIFO With Asynchronous I/O
- Two-Channel FIFO; Both Channels Sychronized to External Signals
- One-Channel Synchronous Shift Register (Single Clock; User-set Latency)
- Two-Channel Synchronous Shift Register (Single Clock; User-set Latencies)
- One-Channel Framestore With Random Access
- Two-Channel FIFO; Channel A Synchronized to Channel B
- Two-Channel FIFO; Channel B Synchronized to Channel A

LF3312 Functional Block Diagram

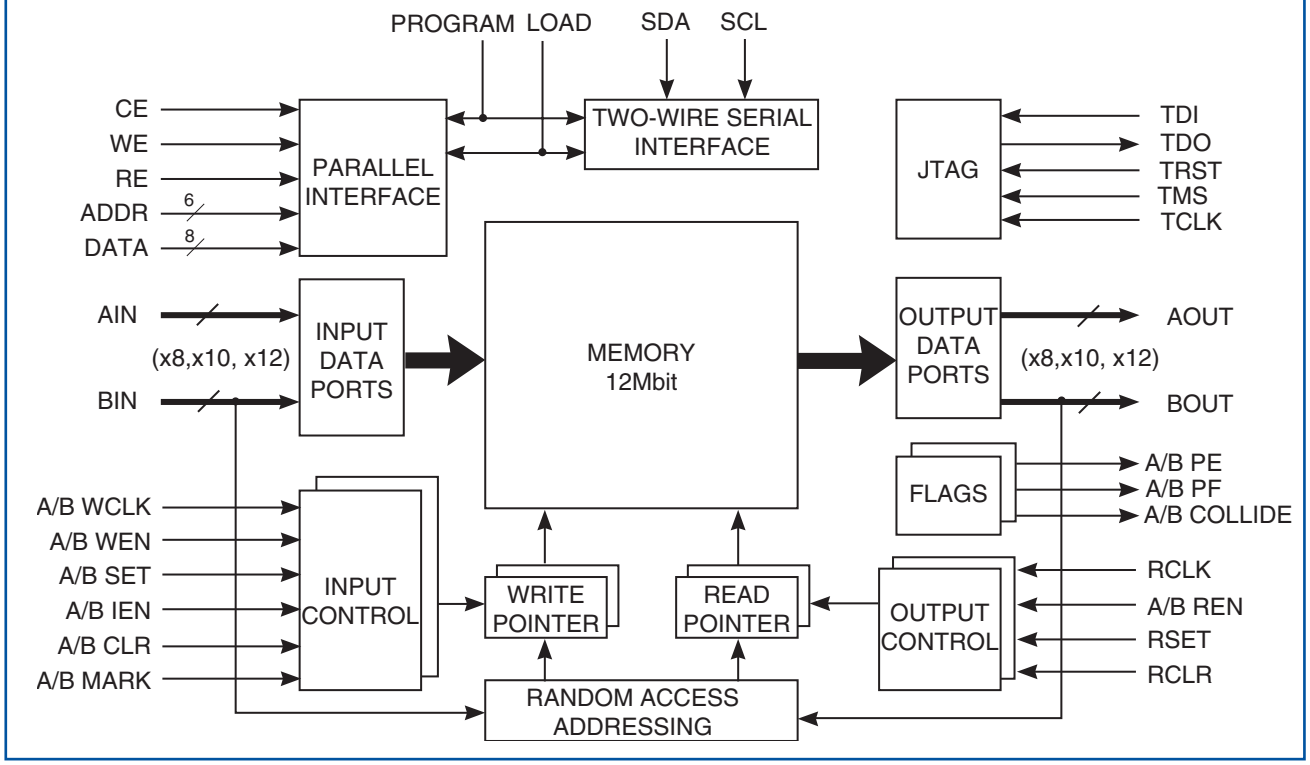


Figure 1. Dual Channel FIFO Mode Functional Block Diagram

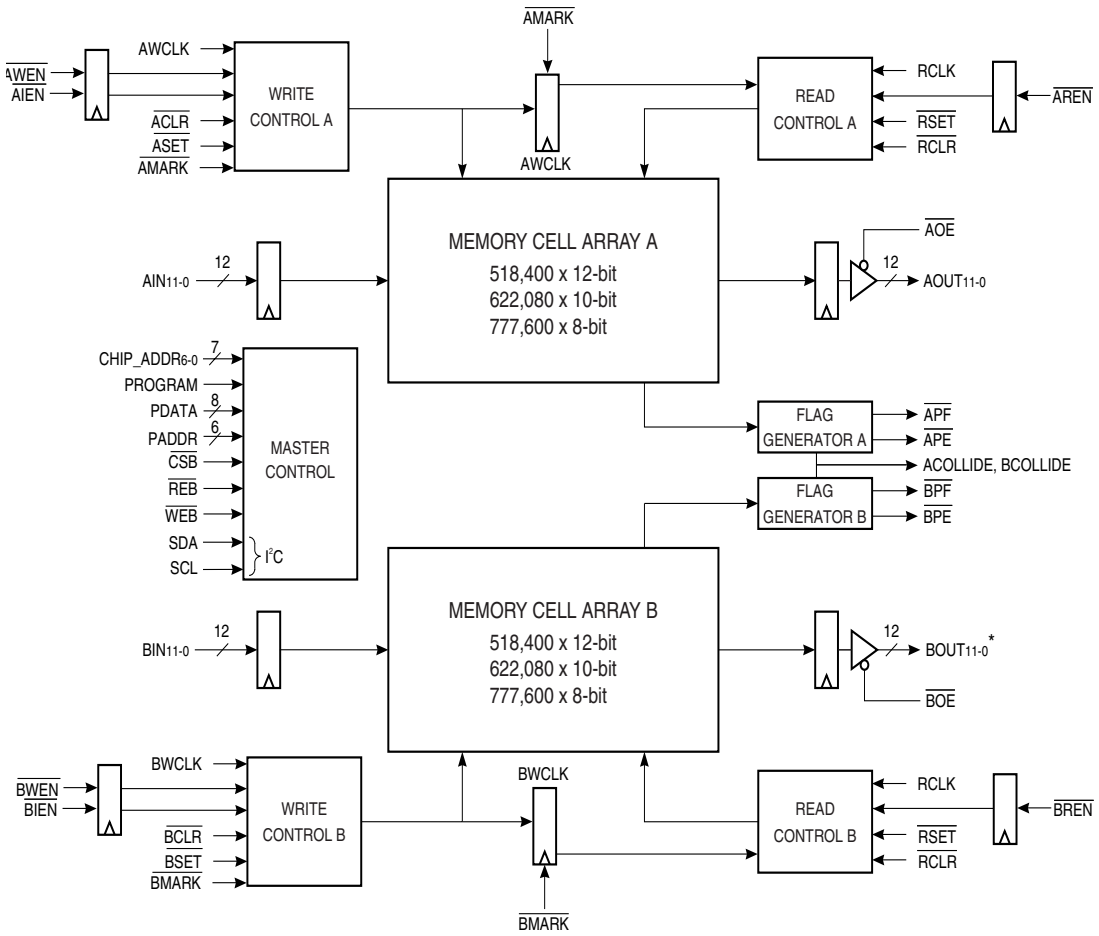


Figure 2. Single Channel FIFO Mode Functional Block Diagram

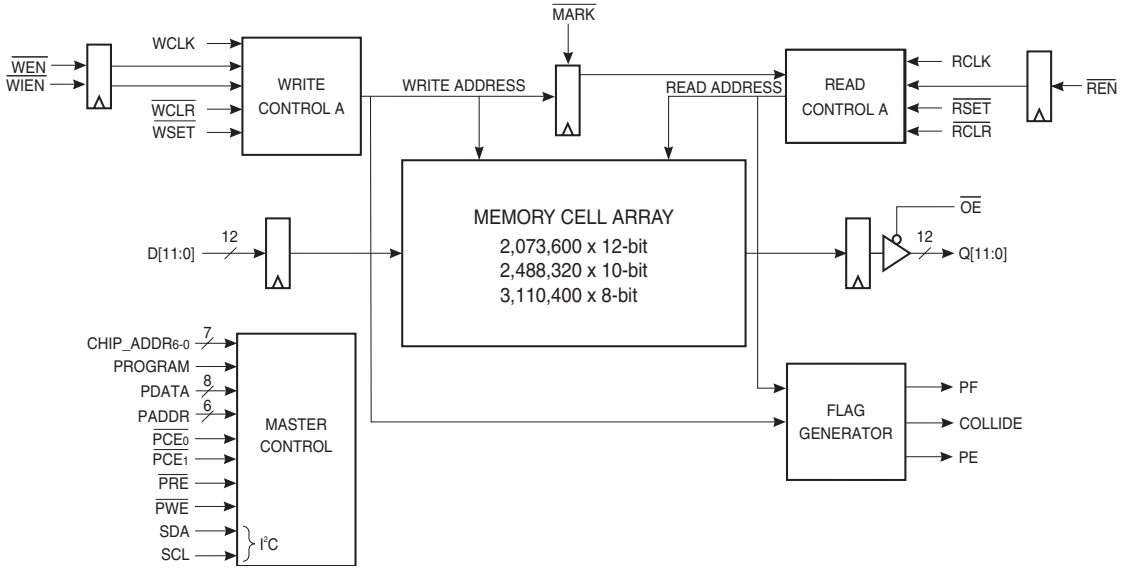
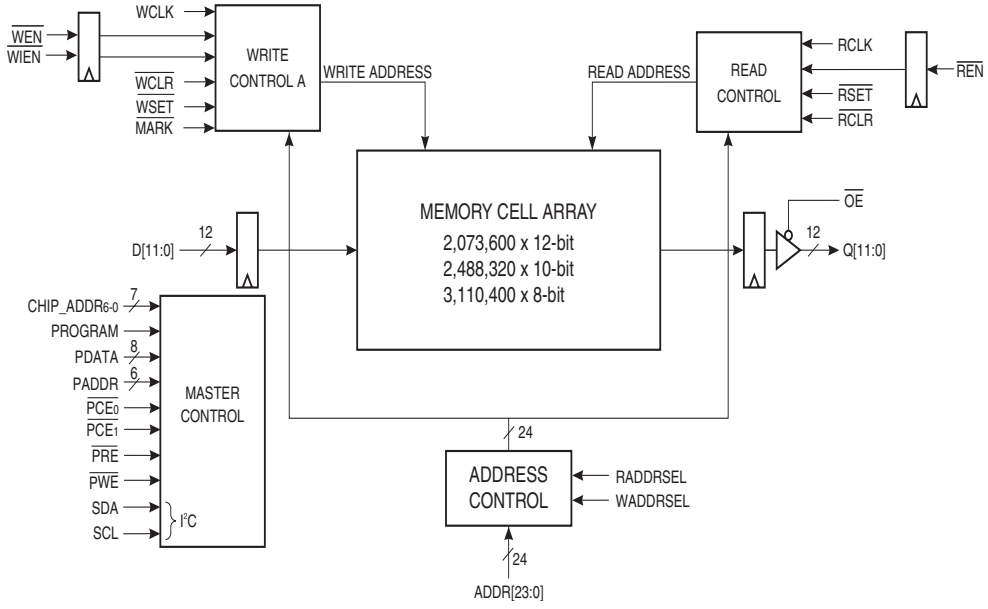


Figure 3. Random Access Mode Functional Block Diagram



Operating Modes

Asynchronous single-channel FIFO mode (OPMODE = 3)

In OPMODE 3, the LF3312 is configured as a single channel First-In-First-Out 12Mbit memory, with independent read and write clocks to allow for asynchronous operation. This mode is ideal for buffering or burst data applications. Arbitrary write/read pointer jumping is supported in all FIFO modes. In this mode the device can re-time a data stream according to a read sync signal ($\overline{\text{RSET}}$ or $\overline{\text{RCLR}}$) and either ITU-R656 Timing Reference Signals (TRS) embedded within the incoming (video) data or the falling edge of a write sync signal applied to $\overline{\text{ACLR}}$, $\overline{\text{ASET}}$, or $\overline{\text{AMARK}}$.

As a single channel FIFO, the LF3312 must have AWCLK and BWCLK tied together as must be $\overline{\text{AWEN}}$ with $\overline{\text{BWEN}}$, and $\overline{\text{AIEN}}$ with $\overline{\text{BIEN}}$. The input (write) and output (read) clocks need not be synchronous with one another, although the memory core will eventually fill or empty if they differ in average frequency. After it “fills,” the LF3312 continues writing and the oldest data gets written over. If the memory core “empties” (and neither the read nor write pointer have been set or cleared during run-time) the read pointer stops incrementing, and the device re-reads the last written sample until more data is written. In either case, when the read and write addresses reach equality, the ACOLLIDE flag will go high, to alert the host. The almost-full and almost-empty flags provide advance warning of these conditions whenever user-selected “fullness” or “emptiness” thresholds, expressed in approximate eightieths of the memory core size, are exceeded. For example, if the 1/80 and 79/80 thresholds are enabled, flag APE will go HIGH whenever the read pointer lags behind the write pointer by less than 1/80 of the memory space, and flag APF will go HIGH whenever the read pointer leads the write pointer by this amount. (Calculations are performed modulo the total address space.) The data input and output are sequential and the timing between write and read sync signals dynamically determines the effective delay (depth) of the FIFO.

The ‘stop reading when empty’ FIFO-mode behavior can be avoided by making sure LOAD is HIGH and issuing any write or read pointer SET or CLR command at any time. This effectively gets the device out of this ‘read-pointer-halting’ mode from that point onwards, but invalidates the flags. Random Access Mode allows free manipulation of the r/w pointers, and never halts the read pointer without being commanded to do so using AREN or BREN. Since Random Access mode naturally increments the r/w pointers sequentially, like in FIFO mode, it may be a better mode to use if pointer manipulation of a single-channel of memory is desired.

Dual-channel asynchronous FIFO mode (OPMODE = 7; power-on default)

OPMODE 7 operates identically to the single channel FIFO (OPMODE 3), with two independent chanels.

In dual-channel asynchronous FIFO mode, the device can accept two asynchronous data streams and automatically adjust the latency of each to bring it into alignment with an output sync signal applied to $\overline{\text{RSET}}$ or $\overline{\text{RCLR}}$. Again, the user may reference input synchronization either to $\overline{\text{ACLR}}$, $\overline{\text{ASET}}$, $\overline{\text{BCLR}}$, and $\overline{\text{BSET}}$, to $\overline{\text{AMARK}}$ and $\overline{\text{BMARK}}$, or to embedded TRS. The data read/output clock need not be synchronous with either of the two input clocks, which likewise need not be synchronous with one another. If memory core A or B “empties“ or “fills“ completely, ACOLLIDE and/or BCOLLIDE respectively, will be set accordingly if the write and read pointers collide.

The data Word that $\overline{\text{BMARK}}$ ‘marks’ (by going LOW during that xWCLK cycle) in the input data stream will be the first synchronized AOUT/BOUT data word. If N full frames of Channel A data have been loaded into AIN before the first Channel B data frame is loaded into BIN, the second frame of B channel data will be synchronized to the (N+1)th Channel A frame. (there will be N frames difference between Channel A and B).

Operating Modes

Single-channel synchronous shift register mode (OPMODE = 0)

In OPMODE 0, the LF3312 becomes a single channel shift register with programmable total latency up to 2^{24}-8 clock cycles. Writes and reads occur simultaneously, hence synchronous operation.

In OPMODE 0, the user provides a single clock for both the input and output clocks and specifies a desired input-to-output data path latency, (ALAT) via the control interface. AWCLK, BWCLK, and RCLK must be tied together, as should $\overline{\text{AWEN}}$, $\overline{\text{BWEN}}$, $\overline{\text{AREN}}$, and $\overline{\text{BREN}}$. When activated, ALAT will begin to countdown, and once expired, will allow the inputs to begin to appear on the outputs. In OPMODE 0, ALAT countdown can be activated in two ways. The first occurs when the first enable is brought LOW after the $\overline{\text{LOAD}}$ signal has been set HIGH after MPU programming. The second is by bringing $\overline{\text{LOAD}}$ HIGH once MPU programming complete, after the enables have been brought LOW.

Dual-channel synchronous shift register mode (OPMODE = 4)

The operation of dual-channel shift register mode is identical to single-channel operation, with the addition of a second independent channel. The latency for each channel is independent and set by the user.

The user must also supply a single clock to tie AWCLK, BWCLK, and RCLK together, and must load the respective desired constant latency for each channel, (ALAT, BLAT), via the microprocessor bus. ALAT and BLAT are activated in the same manner as in OPMODE 0, with the respective inputs being made available on the outputs once ALAT or BLAT expire. In this mode, $\overline{\text{AWEN}}$ and $\overline{\text{AREN}}$ must be tied together, as must be $\overline{\text{BWEN}}$ and $\overline{\text{BREN}}$.

Dual-channel master/slave mode (OPMODE = 5)

OPMODE 5 is one of two master/slave synchronizing modes where two data streams are written into the LF3312 at independent rates and with independent TRS timing information. In this mode, both channels are synchronized together based on the sync data supplied to channel A or by the embedded TRS data within the A channel.

When in OPMODE 5, channel A operates as a fully synchronous master shift register, to which the data in asynchronous FIFO channel B is re-timed. The user drives AWCLK and RCLK from the incoming AIN data stream's sample clock, and BWCLK from the BIN data stream's clock. The user also specifies whether sync timing will be derived from TRS words embedded within the incoming data streams or from signals applied to ACLR and ASET or to AMARK and BMARK. AWEN, AREN and BREN must be tied together to maintain constant reference latency through channel A and to synchronize the outputs. When a MARK occurs, the signal MARK_ACTIVE_RSET when set high, allows the read pointer to be set to the current value of the write pointer "ALAT" RCLK cycles later. If the user sets MARK_ACTIVE_RSET = 0, the LF3312 will ignore the internal read pointer set.

Dual-channel slave/master mode (OPMODE = 6)

OPMODE 6 is the reverse of OPMODE 5, with the difference being that the two streams are synchronized to the timing information applied to the B channel or embedded within the B channel as TRS data.

This OPMODE is identical to the previous, except that channel A is the slave FIFO and channel B is the master shift register, and RCLK needs to be tied to BWCLK, and BWEN needs to be tied to BREN and AREN. Similarly to mode 5, when a MARK occurs, the signal MARK_ACTIVE_RSET when set high, allows the read pointer to be set to the registered value of the write pointer BLAT number of RCLK cycles later. If the user sets MARK_ACTIVE_RSET = 0, the LF3312 will ignore the internal read pointer set.

Operating Modes

Random Access mode (OPMODE = 1)

Random Access mode is a single-channel FIFO mode, with the capability of either full-time write or read pointer Random Accessability. This mode also supports write and read pointer jumps to arbitrary locations throughout the address space. Unlike Asynchronous Single-Channel FIFO mode (OPMODE=3), Random Access mode does not disable memory reads when the read pointer catches up to the write pointer. Write pointer manipulation can be done through setting (jumping) the write pointer to the 24bit address via the BIN and BOUT ports or to the ALATENCY configuration register. Read pointer manipulation can be done through setting (jumping) the write pointer to the 24bit address via the BIN and BOUT ports or to the BLATENCY configuration register. Periodic write and read pointer jumping can be accomplished by supplying an address through either the BOUT/BIN address or the A or BLATENCY registers. Continuous random access can only be accomplished through the use of the BOUT/BIN ports. When the write/read pointers are not being set to an address, they increment sequentially.

In OPMODE 1, when $\overline{\text{BSET}}$ = 1 and $\overline{\text{BCLR}}$ = 0 the write pointer is set to the address supplied by the BOUT/BIN ports when $\overline{\text{ASET}}$ is brought LOW. AWCLK and BWCLK must be tied together as must $\overline{\text{AWEN}}$ and $\overline{\text{BWEN}}$. In other words, on each active write clock cycle (rising edge of AWCLK for which $\overline{\text{AWEN}}$ was LOW two rising edges of AWCLK previously), the user directs the write pointer to any desired memory location, using what are otherwise the second channel data input and output ports. **In this application, BOUT[11:0] denotes the vertical (row) component, and BIN[11:0], the horizontal (column) component, of a Cartesian set.** Setting the control register ROW_LENGTH to the frame's line (row) length internally defines the Cartesian coordinates. Or, if desired, the concatenation of BOUT[11:0] in front of BIN[11:0] represents a single 24-bit linear address. The user governs the mapping of (BOUT,BIN) to the internal memory space by setting the parameter ROW_LENGTH such that ADDRESS = BOUT * ROW_LENGTH + BIN. A ROW_LENGTH setting of 0 is interpreted as 4096, such that ADDRESS = a 24-bit concatenation of {BOUT,BIN} for this particular value. For a standard D1 video application with 1716 samples per line, the user would set ROW_LENGTH to 1716 decimal = 6B4 hex. Offset circuitry within the LF3312 permits the user to cascade several chips in parallel and to use them collectively as a single large memory with a seamless address space. Data are read out sequentially by rising edges of RCLK, under the control of $\overline{\text{AREN}}$ (read enable), $\overline{\text{RSET}}$ (read pointer force to constant), and $\overline{\text{RCLR}}$ (read pointer clear to 0). Holding $\overline{\text{ASET}}$ LOW keeps the device continuously in random access write mode. Releasing $\overline{\text{ASET}}$ to its HIGH state causes the chip to continue to write sequentially from the last-loaded address.

In OPMODE 1, when $\overline{\text{BCLR}}$ = 1, $\overline{\text{BSET}}$ = 0, MARK_SEL = 1, the read pointer is set to the address supplied by the BOUT/BIN ports when RSET is brought LOW. AWCLK and BWCLK must be tied together as well as $\overline{\text{AREN}}$ and $\overline{\text{BREN}}$. As mentioned above, BOUT[11:0] represents the upper bits or the vertical (row) address, whereas BIN[11:0] represents the lower bits or the horizontal (column) address. Releasing $\overline{\text{RSET}}$ HIGH causes the read address pointer to increment from its last assigned location to the next sequential address.

Cascading Devices for Depth Expansion

Multiple devices can be cascaded to deepen the address space. The usable 24bit address space is simply extended for every additional device that is cascaded.

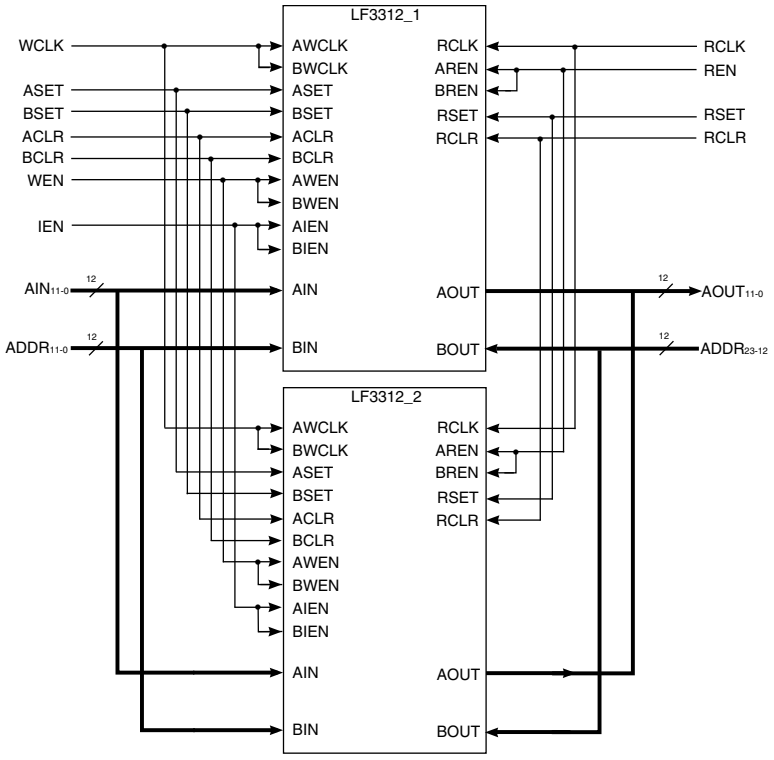
Internally, the LF3312 has a 24bit address space. When cascading LF3312s, each device's write and read pointers behave identically. The LF3312 was designed to be cascaded in parallel. That is, the inputs of each device are tied together. The input data word (the data word placed on the AIN input port) is to be common for all devices. Similarly, the outputs of all devices are tied together. Only one device drives the shared output bus at one time, controlled automatically through internal bus enables.

Each device in a cascade of N devices is responsible for 1/N of the address space. That is, each device writes and/or reads based on the common W/R pointer locations and where that particular device sits in the cascade. Configuration Register C[3:0] (BASE_ADDR) is used to define each device's place in the cascade.

When cascading LF3312s, only singe-channel modes are supported (OPMODES 0 to 3). All write enables AWEN/BWEN and AIEN/BIEN must be tied together, as must read enables AREN/BREN (see the device connection diagram below).

The configuration registers of each device must be programmed identically, depending on mode/function, except for Register C. Register C defines which region of the 24bit address space the particular device is responsible for. Within Register C, there is a 4bit BASE_ADDR and 4bit CASCADE word. BASE_ADDR determines the region of address space each device controls, and CASCADE defines how many devices are in cascade. Register C effectively is programmed as "Chip n of N".

Figure 4. 24Mbit FIFO Depth Expansion: Two Cascaded Devices



Device Configuration

Programming the LF3312

The LF3312 has two MPU interfaces. The first is a standard two wire serial interface following the I²C protocol. The second is a parallel interface allowing the user to write a byte of data at a time to the configuration registers. When the user wishes to use the serial interface, the PROGRAM pin must be set LOW, while a HIGH selects the parallel interface. To provide users with more flexibility, the control registers have been combined with a “working latch” . Ultimately, the register-latch combination allows users to update the configuration registers during chip operation, and then to transfer the register contents to all working latches simultaneously using the $\overline{\text{LOAD}}$ signal. When high, the $\overline{\text{LOAD}}$ signal allows the LF3312 to be pre-programmed during operation, and once brought low after programming updates the working latches allowing the new changes to take effect. $\overline{\text{LOAD}}$ can also be maintained low to allow changes to the configuration registers to be immediately reflected in the working latches.

Serial MPU Interface

When the PROGRAM pin is LOW, the serial interface is active. Up to 16 LF3312 devices can be connected to and programmed by the serial interface. The two wire interface is composed of an SCL clock pin and a bi-directional SDA data pin. When inactive, SDA and SCL are forced HIGH by external pull up resistors.

Data transmission is achieved over the SDA pin and must remain constant during the logical HIGH portion of the SCL clock pulse. The level of SDA, while SCL is HIGH, is interpreted as the appropriate bit value as will be shown later. Changing the data on SDA must only occur when SCL is low, because any changes to SDA while SCL is HIGH is interpreted as a start or stop request, which are shown in Figure 7 with an example data transfer in Figure 8.

The first operation to begin programming the LF3312 through the serial interface, is to send a start signal. When the interface is inactive, a HIGH to LOW transition must be sent on SDA while SCL is HIGH, notifying all connected devices (slaves) to expect a data transmission. When transferring data, the MSB of the eight bit sequence is the first bit to be transmitted to or from the master or slave. The first byte of data to be transmitted on SDA must consist of the 7-bit base address of the slave, along with an 8th READ/WRITE bit as the LSB, which describes the direction of the data transmission. The slave whose 7-bit CHIP_ADDR6-0, matches the 7-bit base address sent on SDA, will send an acknowledgement back to the master by bringing SDA LOW on the 9th SCL pulse.

During a write operation, if the slave does not send an acknowledgment back to the master device, SDA is left high which forces the master to generate a stop signal. In contrast, during a read operation, if there is no acknowledgement back from the master device, the LF3312 interprets this as if it were the end of the data transmission, and leaves SDA high, allowing the master to generate its stop signal.

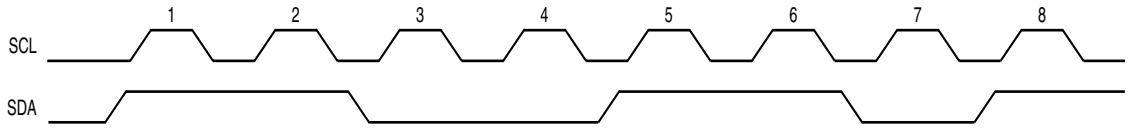
Figure 7 - I²C Start and Stop Signals

Device Configuration

There are four operations that can be performed between the master and the slave. They are: Write to consecutive registers, write to a single control register, read from consecutive registers and read from a single register. To write to consecutive control registers, a start signal and base address must be sent with the R/W bit as described above. After the acknowledgment back from the appropriate slave, the 8-bit address of the target control register must be written to the slave with the R/W bit LOW. The slave then acknowledges by setting SDA LOW. The data byte to be written into the register can now be transferred on SDA. The slave then acknowledges by pulling SDA LOW on the next positive going pulse of SCL. The first control register address loaded into the LF3312 is considered as the beginning address for consecutive writes, and automatically increments to the next higher address space. Therefore after the acknowledgement, the data byte to configure register (first address + 1) can now be transferred from master to slave. At any point a stop signal can be given to end the data transfer. To write to a single control register, the same technique can be applied adding a stop signal after the first data write.

To read from consecutive control registers, the master must again give the start signal followed by a base address with the R/W bit = 0, as if the master wants to write to the slave. The appropriate slave then acknowledges. The master will then transfer the target register address to the slave and wait for an acknowledge. The master will then give a repeated start signal to the slave, along with the base address and R/W bit this time HIGH signifying a read and wait for an acknowledge. The user must write to the LF3312 to select the appropriate initial target register. Otherwise the starting position of the read is uncertain. Once the LF3312 acknowledges, the next byte of data on SDA is the contents of the addressed register sent from the device. If the master acknowledges, the LF3312 will send the next higher register's contents on the following byte of data. To read from only one register is the same procedure as for consecutive reading with a stop signal following the transfer of the register's contents.

Figure 8 - I²C Example of transferring 11001101 on SDA



Parallel MPU Interface

The parallel MPU interface can be used to write instructions to the control registers or to read them back for verification. When the PROGRAM pin is HIGH, the parallel interface is selected. An external processor can write into an internal register by setting PADDR to the desired register address, selecting the chip using the $\overline{CSB}$ pin, setting PDATA to the desired value and then pulsing $\overline{WEB}$ LOW. The data will be written into the selected register when both $\overline{WEB}$ and $\overline{CSB}$ are LOW, and will be held when either signal goes HIGH. To read from a control register the processor must set PADDR to the desired address, select the chip with the $\overline{CSB}$ pin, and then set $\overline{REB}$ LOW. The chip will then drive PDATA with the contents of the selected register. After the processor has read the value from PDATA, $\overline{REB}$ and $\overline{CSB}$ should be set HIGH. The PDATA pins are turned off (High Impedance) whenever $\overline{CSB}$ or $\overline{REB}$ are HIGH or when $\overline{WEB}$ is LOW. The chip will only drive these pins when both $\overline{CSB}$ and $\overline{REB}$ are LOW and $\overline{WEB}$ is HIGH. One can also ground the $\overline{REB}$ pin and use the $\overline{WEB}$ pin as a read/write direction control and use the $\overline{CSB}$ pin as a control I/O strobe.

Device Configuration

Parallel Interface Cont'd

Figure 5 - Normal Reading and Writing From a Control Register

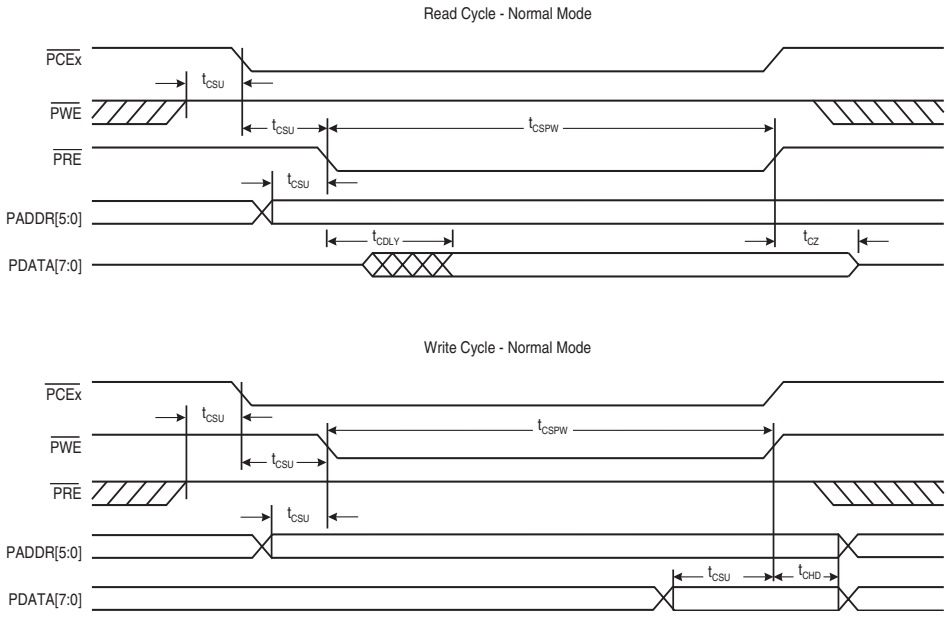
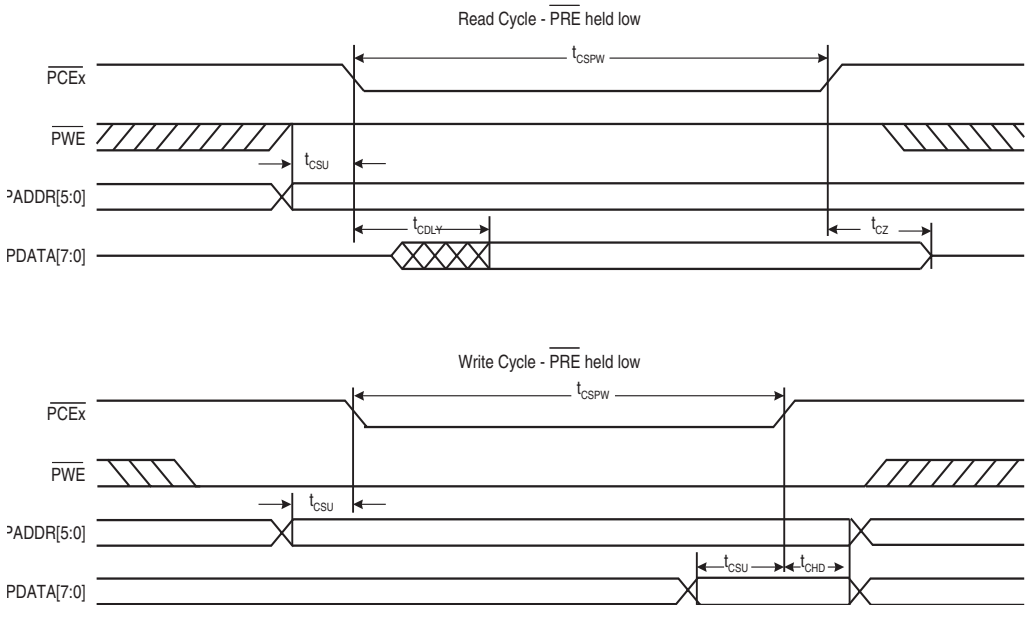


Figure 6 - Reading and Writing From a Control Register with REB Held Low



Detailed Signal Definitions

Power

***VCC_{INT}* - Internal Core Power Supply**
+1.8V power supply. All pins must be connected.

***VCC_O* - Output Driver Power Supply**
+3.3V power supply. All pins must be connected.

Clocks

AWCLK - Write Clock A
Data present on AIN11-0 is written into the LF3312 on the rising edge of AWCLK when $\overline{\text{AWEN}}$ was LOW for the previous rising edge of AWCLK.

BWCLK - Write Clock B
In two-channel modes($\overline{\text{OPMODES}}$ 4-7), data present on BIN11-0 is written into the LF3312 on the rising edge of BWCLK when $\overline{\text{BWEN}}$ is LOW. In one-channel modes(OPMODES 0-3), BWCLK must be tied to AWCLK.

RCLK - Read Clock
In single channel modes, data is read from the LF3312 and presented on the output port (AOUT11-0) after a rising edge of RCLK while $\overline{\text{AREN}}$ and $\overline{\text{AOE}}$ are LOW. In two-channel mode, data is also read from the LF3312 and presented on the output port (BOUT11-0) after a rising edge of RCLK while $\overline{\text{BREN}}$ and $\overline{\text{BOE}}$ are LOW.

Inputs

AIN11-0 - Data Input A
AIN11-0 is the 12-bit registered data input port. Bit 11 is the MSB in all modes. AIN1-0 are ignored in 10-bit mode and AIN3-0 are ignored in 8-bit mode. Any such unused inputs should either be tied to ground or driven to proper logic levels by external logic.

BIN11-0 - Data Input B
In dual-channel modes (OPMODES 4-7), BIN11-0 is the 12-bit registered data input port in all dual channel FIFO modes. Bit 11 is the MSB in all modes. BIN1-0 are ignored in 10-bit mode and BIN3-0 are ignored in 8-bit mode. Unused inputs should be tied off to ground or driven to proper logic levels by external logic. In single-channel modes (OPMODE 0-3), BIN11-0 can act as a 24bit external address port (ADDR).

CHIP_ADDR6-0 - Chip Address (CA6-0)
CHIP_ADDR6-0 determines the LF3312's address on the two-wire microprocessor bus. Each LF3312 chip's 7-bit two-wire serial microprocessor interface address is equal to its CHIP_ADDR6-0.

SCL - Serial Clock Input
SCL is a standard two-wire serial microprocessor interface clock pin. With this chip, it functions as a dedicated input, since this part cannot be the master on an two-wire serial microprocessor interface.

ADDR23-0 - External Random Access Read/Write Address Port
(OPMODE 0-3) ADDR23-0 is a virtual 24-bit memory address port, available in single channel modes. ADDR23-0 is a concatenation of the BIN and BOUT data ports. BIN11-0 specifies ADDR11-0 (X/Column-coordinate) and BOUT11-0 specifies ADDR23-12 (Y/Row-coordinate). The 24bit address is a purely linear address when the instruction register ROW_LENGTH is equal to 0(default). When ROW_LENGTH is a non-zero value, the memory is set to have a row (line) length of ROW_LENGTH.

PADDR5-0 - Parallel Microprocessor Interface Address Port
PADDR5-0 is the 6-bit address port for the parallel microprocessor interface. When inactive, it transitions to a high impedance state.

Detailed Signal Definition

Input/Output

PDATA7-0 - Parallel Microprocessor Interface Data Port
PDATA7-0 is the 8-bit data port for the parallel microprocessor interface. When inactive becomes high impedance.

SDA - Serial Data I/O
SDA is the standard bidirectional data pin of a two-wire serial microprocessor interface. External pullup is required on SDA.

BOUT11-0 - Data Output B
In two-channel modes(OPMODES 4-7), BOUT11-0 is the 12-bit registered data output port. BOUT[11] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{\text{BREN}}$ is LOW. In OPMODE 0-3 , BOUT11-0 can act as the upper word of the 24bit external address ADDR if ROW_LENGTH is equal to 0, or Y-coordinate address if ROW_LENGTH is some value other than zero. BOUT11-0 represents a portion of the read address port when executing an $\overline{\text{RSET}}$, if and only if $\overline{\text{AREN}}$=0, MARKSEL=1, $\overline{\text{BCLR}}$=1. BOUT11-0 represents a portion of the write address portwhen executing an $\overline{\text{ASET}}$, if and only if $\overline{\text{AWEN}}$=0, $\overline{\text{ACLR}}$=1, $\overline{\text{BSET}}$=1. For more details on $\overline{\text{RSET}}$ and $\overline{\text{ASET}}$, please refer to their signal definitions.

Controls

$\overline{\text{ACLR}}$ - Channel A Write Pointer Clear
When $\overline{\text{ACLR}}$ is brought LOW, the next rising edge of AWCLK will bring the current value on AIN[11:0] into memory Channel A, address 0. Whenever $\overline{\text{ACLR}}$ is HIGH, the destination for AIN[11:0] will be controlled by $\overline{\text{ASET}}$. The user may program ACLR such that either its falling edge or its LOW state is active. If its LOW state is active, holding this pin LOW will hold the write address in its zero position continuously. This control takes effect only when $\overline{\text{AWEN}}$ is LOW.

$\overline{\text{BCLR}}$ - Channel B Write Pointer Clear / Channel A Write Random Select
In dual-channel modes (OPMODE = 4-7), this pin clears the Channel B Write Pointer, in the same manner that $\overline{\text{ACLR}}$ clears the Channel A Write Pointer, and the user may program it to be falling edge or LOW state active. In single-channel modes (OPMODE = 0-3), this pin and control MARKSEL govern the action of $\overline{\text{RSET}}$. In OPMODES 4-7, this control takes effect only when $\overline{\text{BWEN}}$ is LOW.

$\overline{\text{ASET}}$ - Channel A Write Pointer Set
This control is active only when $\overline{\text{ACLR}}$ is HIGH. Bringing $\overline{\text{ASET}}$ LOW will cause the next rising edge of AWCLK to bring the current value on AIN[11:0] into memory A, at the address specified by ALAT, or if OPMODE = 0-3 and $\overline{\text{BSET}}$ = 1, at the address whose Cartesian coordinates are present on BOUT and BIN. Whenever $\overline{\text{ASET}}$ and $\overline{\text{ACLR}}$ are HIGH, the next rising edge of AWCLK will bring the current AIN[11:0] data value into the next-higher address in sequence. $\overline{\text{ASET}}$ may be programmed to be either edge-triggered, in which case it affects the write pointer for only one clock cycle following a falling edge, after which incrementing resumes, or level-triggered, in which case it affects the write pointer until it is brought HIGH. For continuous random access write operation, holding $\overline{\text{ASET}}$ LOW and programming it to be level-triggered will provide the needed continuous write pointer override. This control takes effect only when $\overline{\text{AWEN}}$ is LOW.

$\overline{\text{BSET}}$ - Channel B Write Pointer Set
In two-channel modes (OPMODE = 4-7), this pin's impact on the B write pointer is analogous to that of $\overline{\text{ASET}}$ on the A write pointer, and the user may program the pin's action to be either edge- or level-triggering. In one-channel modes, $\overline{\text{BSET}}$ determines whether $\overline{\text{ASET}}$ forces the write address pointer to ALAT ($\overline{\text{BSET}}$ = 0) or to BOUT,BIN ($\overline{\text{BSET}}$ = 1). In OPMODES 4-7, this control takes effect only when $\overline{\text{BWEN}}$ is LOW.

Detailed Signal Definitions

$\overline{\text{AMARK}}$ - Channel A Write Address Pointer Mark
In single-channel mode, bringing this bit LOW will cause an internal register to store a copy the current value of the write address pointer, for subsequent use in synchronizing the corresponding read address pointer to the same location. Unlike ACLR and ASET, this control does not affect the write pointer value itself. The system must use AMARK instead of ACLR if the entire memory core can be filled between sequential falling edges of the sync reference signal. In contrast, the system must use ACLR or ASET to establish a definite relationship between the internal address and the data stream, as in random access read mode.

$\overline{\text{BMARK}}$ - Channel B Write Address Pointer Mark
(active only in dual channel modes, OPMODE = 4-7) Bringing this bit LOW will cause an internal register to store a copy the current value of the Channel B write address pointer, for use in synchronizing the corresponding read address pointer to the same location. This signal does not affect the value of the memory B write address pointer itself.

$\overline{\text{RSET}}$ - Read Address Pointer Set
In dual-channel modes (OPMODE = 4-7), if AREN is LOW, bringing RSET LOW will force read address pointer A to ALAT (if MARK_SEL is HIGH) or to the value most recently captured from using AMARK (if MARK_SEL is LOW). If BREN is LOW, bringing RSET LOW will force read address pointer B to BLAT (if MARK_SEL is HIGH) or to the value most recently captured by BMARK (if MARKSEL is LOW). In single-channel modes (OPMODE = 0-3), if AREN is LOW, bringing RSET LOW will force the read address to the most recently marked value (MARK_SEL LOW), to BLAT (MARKSEL HIGH and BCLR LOW), or to BOUT,BIN (MARK_SEL is HIGH and BCLR is HIGH). This pin may be programmed to be either falling edge or level LOW active.

$\overline{\text{RCLR}}$ - Read Address Pointer Clear
Bringing RCLR LOW causes the next rising edge of RCLK to force the read address pointer (OPMODE 0-3) or pointers (OPMODE 4-7) to zero. This pin may be programmed to be active on its falling edge or in its LOW state. In single-channel mode, it can reset the read pointer only when AREN is LOW. In dual-channel mode, it can reset read pointer A only if AREN is LOW, and read pointer B only if BREN is LOW.

$\overline{\text{AWEN}}$ - Write Enable A
If AWEN is LOW, data on AIN11-0 is written to the device on the rising edge of AWCLK. When AWEN is HIGH, the device ignores data on AIN and holds the write pointer. The user must anticipate the use of AWEN by one cycle. Therefore when desiring not to write a sample, AWEN must be brought high the cycle before.

$\overline{\text{BWEN}}$ - Write Enable B
If BWEN is LOW, data on BIN11-0 is written to the device on the rising edge of BWCLK. When BWEN is HIGH, the device ignores data on BIN and holds the write pointer. The user must anticipate the use of BWEN by one cycle. Therefore when desiring not to write a sample, BWEN must be brought high the cycle before. In single channel modes (OPMODES 0-3), BWEN must be tied to AWEN.

$\overline{\text{AIEN}}$ - Memory Write Enable A (Write Masking)
AIEN is used to enable/disable writing into the memory core. A LOW on AIEN enables writing, while a HIGH on AIEN disables writing. The internal A write address pointer is incremented by AWEN regardless of the AIEN level. Unless writing into memory is to be disabled, tie AIEN LOW.

$\overline{\text{BIEN}}$ - Memory Write Enable B (Write Masking)
BIEN is used to enable/disable writing into the memory core. A LOW on BIEN enables writing, while a HIGH on BIEN disables writing. The internal B write address pointer is incremented by BWEN regardless of the BIEN level. Unless writing into memory is to be disabled, tie BIEN LOW

Detailed Signal Definitions

$\overline{\text{AREN}}$ - Read Enable A
If $\overline{\text{AREN}}$ is LOW and the output port is enabled, data from Channel A is read and presented on AOUT11-0 after tD has elapsed from the rising edge of RCLK. If $\overline{\text{AREN}}$ goes HIGH, the last value loaded into Channel A output register will remain unchanged and the read pointer will be held. The user must anticipate the use of $\overline{\text{AREN}}$ by one cycle. Therefore when desiring not to read a sample, $\overline{\text{AREN}}$ must be brought high the cycle before.

$\overline{\text{BREN}}$ - Read Enable B
If $\overline{\text{BREN}}$ is LOW and the output port is enabled, data from Channel B is read and presented on BOUT11-0 after tD has elapsed from the rising edge of RCLK. If $\overline{\text{BREN}}$ goes HIGH, the last value loaded into Channel B output register will remain unchanged and the read pointer will be held. The user must anticipate the use of $\overline{\text{BREN}}$ by one cycle. Therefore when desiring not to read a sample, $\overline{\text{BREN}}$ must be brought high the cycle before.

PROGRAM ***- Serial/Parallel Interface Selector***
When the user wishes to use the serial microprocessor to configure the LF3312, the PROGRAM pin must be set LOW, whereas if he or she wishes to use the parallel interface, PROGRAM must be set HIGH.

$\overline{\text{LOAD}}$ – Instruction Load
Bringing asynchronous control $\overline{\text{LOAD}}$ LOW updates the working instruction latches to match the current contents of the instruction preload latches. Holding it LOW causes the working latches to reflect all ongoing instruction preloads. Holding it HIGH permits the user to preset the instruction preload latches to any desired configuration without disturbing the work in progress. After any write to the configuration registers, $\overline{\text{LOAD}}$ must be brought high for one cycle, and can then be brought and left low if so desired.

$\overline{\text{RESET}}$ - Global Reset
Bringing synchronous control $\overline{\text{RESET}}$ LOW forces all state machines and read and write pointers to 0 and holds them there until it is released HIGH. It also forces the configuration registers to their default states, if and only if $\overline{\text{LOAD}}$ is also LOW. The user may then modify the control registers as necessary. Bringing $\overline{\text{RESET}}$ LOW while holding $\overline{\text{LOAD}}$ HIGH will reset the state machines and pointers, but will not change either the preload or the working latches.

$\overline{\text{AOE}}$ - Output Enable A
When $\overline{\text{AOE}}$ is LOW, AOUT11-0 is enabled for output. When $\overline{\text{AOE}}$ is HIGH, AOUT11-0 is placed in a high-impedance state. In 10-bit modes, AOUT1-0 are unconditionally tristated. In 8-bit modes, AOUT3-0 are tristated. The flag outputs are not affected by $\overline{\text{AOE}}$.

$\overline{\text{BOE}}$ - Output Enable B
In any dual-channel mode, when $\overline{\text{BOE}}$ is LOW, BOUT11-0 is enabled for output. When $\overline{\text{BOE}}$ is HIGH, or in any single-channel mode, BOUT11-0 is placed in a high-impedance state. In 10-bit modes, BOUT1-0 are tristated. In 8-bit modes, BOUT3-0 are tristated. The flag outputs are not affected by $\overline{\text{BOE}}$.

$\overline{\text{CSB}}$ - Chip Enable
When LOW, CSB enables writing to the LF3312 with the parallel micrprocessor interface.

$\overline{\text{WEB}}$ - Parallel Microprocessor Interface Write Enable
When LOW, WE enables writing to the LF3312's Instruction Registers with the parallel micrprocessor interface.

$\overline{\text{REB}}$ - Parallel Microprocessor Interface Read Enable
When LOW, RE enables reading from the LF3312's Instruction Registers with the parallel micrprocessor interface.

Detailed Signal Definitions

Data Outputs

AOUT11-0 - Data Output A
AOUT11-0 is the 12-bit registered data output port. AOUT[11] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{\text{AREN}}$ is LOW.

BOUT11-0 - Data Output B
In OPMODES 4-7, BOUT11-0 is the 12-bit registered data output port. BOUT[11] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{\text{BREN}}$ is LOW. In OPMODES 0-3 refer to the input description of BOUT11-0.

Flag Outputs

APF / BPF - Programmable Almost Full Flag A & B
APF / BPF goes HIGH (active) when the write pointer is more than (MAX_depth - (MAX_depth x TH)) locations ahead of the read pointer. TH is a threshold value stored in the Register 9 [2:0]. APF is updated on the rising edge of AWCLK. In Dual-Channel mode, BPF is updated on the rising edge of BWCLK. TRS bits from AIN or AOUT can be mapped to APF (Register B[3:0]). In Dual-Channel mode, TRS bits from BIN or BOUT can be mapped to BPF (Register B[7:4]).

APE / BPE - Programmable Almost Empty Flag A & B
APE / BPE goes HIGH (active) when the write pointer is less than or equal to (MAX_depth - (MAX_depth x TL)) locations ahead of the read pointer. TL is a threshold value stored in the Register 9 [2:0]. APE is updated on the rising edge of RCLK. In Dual-Channel mode, BPF is updated on the rising edge of RCLK. TRS bits from AIN or AOUT can be mapped to APE (Register B[3:0]). In Dual-Channel mode, TRS bits from BIN or BOUT can be mapped to BPE (Register B[7:4]).

ACOLLIDE - Memory Read/Write Pointer Collision Flag A
This flag goes high whenever the read and write addresses to the memory core (single-channel modes) or its “A” channel (dual-channel modes) coincide. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full). TRS bits from AIN or AOUT can be mapped to ACOLLIDE (Register B[3:0]).

BCOLLIDE - Memory Read/Write Pointer Collision Flag B
In dual-channel modes, this flag goes high whenever the read and write addresses to the Channel B memory core coincide. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full). TRS bits from BIN or BOUT can be mapped to BCOLLIDE (Register B[7:4]).

JTAG

TDI - JTAG input data
TDI is the input data pin when using JTAG.

TDO - JTAG output data
TDO is the output data pin when using JTAG.

TRSTB - JTAG reset
TRSTB is used to reset all the registers and state machine fount the the JTAG module.

TMS - JTAG Tap controller input
TMS controls the state of the tap controller.

TCK - JTAG clock
TCK is the used supplied clock of JTAG. It controls the flow of data and latches input data on the rising edge.

Configuration Register Map

The various 8-bit control registers may be pre-programmed with either the parallel microprocessor port (PROGRAM=1), or through the serial microprocessor interface bus(PROGRAM=0). Changes in pre-programming begin to affect the data path when $\overline{\text{LOAD}}$ is brought $\overline{\text{LOW}}$. In each instance, the value in parens () is the default state following assertion of $\overline{\text{RESET}}$ while $\overline{\text{LOAD}}$ = 0.

Instruction Register 0 (dflt = 00000000)

3:0 = ROW_LENGTH[11:8]	(0000: 24-bit linear map; see reg 7)

Instruction Register 1 (dflt = 00000000)

7:0 = ROW_LENGTH[7:0]	(00000000: 24-bit linear map; see reg 6)

Instruction Register 2 (dflt = 00000000)

7:0 = ALATENCY[23:16]	(00000000: default = 0; see reg 9, a)

Instruction Register 3 (dflt = 00000000)

7:0 = ALATENCY[15:8]	(00000000: default = 0; see reg 8, a)

Instruction Register 4 (dflt = 00000000)

7:0 = ALATENCY[7:0]	(00000000: default = 0; see reg 8, 9)

Instruction Register 5 (dflt = 00000000)

7:0 = BLATENCY[23:16]	(00000000)

Instruction Register 6 (dflt = 00000000)

7:0 = BLATENCY[15:8]	(00000000)

Instruction Register 7 (dflt = 00000000)

7:0 = BLATENCY[7:0]	(00000000)

Configuration Register Map

Instruction Register 8 (dflt = 10_00_0_111)

7:6 = WIDTH[1:0]	(10: 10 bits)
5:4 = Reserved	(Make equal to 00)
3 = MARK_ACTIVE_RESET	(Make equal to 0)
2:0 = OPMODE	(111: Two-Channel Asynchronous FIFO)

Instruction Register 9 (dflt = 00_000_000)

7:6 = TRS_SYNC[1:0]	(00: ignore embedded TRS)
5 = B_FLD	(0: frame sync - use falling F-bit from TRS)
4 = A_FLD	(0: frame sync - use falling F-bit from TRS)
3 = MARK_SEL	(0: use marked address - not user defined address)
2:0 = FLAG_SET	(000: trigger empty, full on 1/80, 79/80)

Instruction Register A (dflt = 00000000)

7 = BSET_catch	(0: setting B pointer does not MARK its new value)
6 = ASET_catch	(0: setting A pointer does not MARK its new value)
5 = RSET_b_sel	(0: $\overline{\text{RSET}}$ is falling edge triggered)
4 = RCLR_b_sel	(0: $\overline{\text{RCLR}}$ is falling edge triggered)
3 = BSET_b_sel	(0: $\overline{\text{BSET}}$ is falling edge triggered)
2 = BCLR_b_sel	(0: $\overline{\text{BCLR}}$ is falling edge triggered)
1 = ASET_b_sel	(0: $\overline{\text{ASET}}$ is falling edge triggered)
0 = ACLR_b_sel	(0: $\overline{\text{ACLR}}$ is falling edge triggered)

Instruction Register B (dflt = 00_00_00_00)

7:4 = BFLAG_CTL	(00: BPE, BPF are part-empty, -full)
3:0 = AFLAG_CTL	(00: APE, APF are part-empty, -full)

Instruction Register C (dflt = 0000_0000)

7:4 = BASE_ADDR	(0000: lowest-address chip in cascade sequence)
3:0 = CASCADE	(0000: single chip - no cascade of multiple chips)

Configuration Register Definitions

Register 0[3:0], Register 1[7:0] = ROW_LENGTH[11:0] - for Cartesian-to-linear address map in Single-channel modes

This control governs the remapping of Cartesian coordinates arriving on BIN (horizontal/column component) and BOUT (vertical/row component) into a linear address, for use by the chip's internal address generator. Setting ROW_LENGTH to 0 causes the incoming address to be interpreted directly as a linear address (or equivalently, a Cartesian address with 4095 pixels per line), with the 12 bits of BOUT concatenated with the lesser significant 12 bits of BIN.

Register 2[7:0], Register 3[7:0], Register 4[7:0] = ALATENCY[23:0] - Shift Register Latency (Channel A) or 24bit 'Jump' Address

In single-channel synchronous shift register mode (OPMODE = 0), ALATENCY determines the effective shift register depth, i.e., such that the chip's input-to-out latency = TBD + (ALATENCY clock cycles). In dual-channel shift register modes, this register sets the Channel A delay. For OPMODE = 0, 4 or 5, a falling edge on pin $\overline{\text{AMARK}}$ registers the current value of the write pointer and starts a countdown timer, which forces the read pointer to this registered value ALATENCY clock cycles later. The maximum delay that ALAT can be made equal to is 2^{24}-2 clock cycles.

In addition to this function, in all single-channel OPMODES, bringing $\overline{\text{ASET}}$ LOW forces/jumps the memory write pointer to the address defined by ALATENCY (when $\overline{\text{BSET}}$ is LOW). Thus, when ALATENCY is used to establish a time delay, it is interpreted as an ordinary unsigned binary number. In contrast, when it is used to override an address pointer, ALATENCY defines an address. When ROW_LENGTH is a non-zero value, ALATENCY[11:0] is equal to the 12-bit X-coordinate (Horizontal) and ALATENCY[23:12] is considered the Y-coordinate (Vertical) in a Cartesian Coordinate system. When ROW_LENGTH is 0, ALATENCY[23:0] is considered to be a linear address in the memory space. By changing the ROW_LENGTH, the X-coordinate can be from 0 to (ROW_LENGTH-1) to make up the Cartesian plane. For example, if ROW_LENGTH = 16, the X-coordinate or ALATENCY[11:0] can be from 0 to 15 in the Cartesian space.

Register 5[7:0], Register 6[7:0], Register 7[7:0] = BLATENCY[23:0] - shift register depth for (Channel B) or 24bit 'Jump' Address

In dual-channel synchronous shift register mode (OPMODE = 4), BLATENCY determines the effective Channel B shift register depth, i.e., such that the chip's input-to-out latency = TBD + (BLATENCY clock cycles).

in single-channel OPMODES, bringing $\overline{\text{RSET}}$ LOW forces/jumps the read pointer to the address defined by BLATENCY. In dual-channel modes, BLATENCY impacts channel B exactly as ALATENCY impacts channel A. Total Channel B data latency = TBD + (BLATENCY clock cycles).

Configuration Register Definitions

Register 8[7:6] = WIDTH[1:0] - data word size at input/output ports

0x	8 bits	[11:4]	xOUT[3:0] tristated
10	10 bits	[11:2] (dflt)	xOUT[1:0] tristated
11	12 bits	[11:0]	

Register 8[5:4] = Reserved

Register 8[3] = MARK_ACTIVE_RSET

0	ignores the internal RSET that occurs following the MARK
1	obeys the internal RSET according to the MARK

Register 8[2:0] = OPMODE[2:0] - operating mode

000	1 channel	Synchronous Shift Register
001	1 channel	Random Access
010	-------	RESERVED
011	1 channel	Asynchronous FIFO
100	2 channel	Synchronous Shift Register
101	2 channel	FIFO, B slaved to A
110	2 channel	FIFO, A slaved to B
111	2 channel	Asynchronous FIFO (default)

Configuration Register Definitions

Register 9[7:6] = TRS_SYNC[1:0] - response to embedded TRS EAV (a)

00	disable TRS sync detection (dflt)
01	F-bit of embedded TRS EAV marks current write pointer.
10	F-bit of embedded TRS EAV sets current write pointer to value set by BOUT/BIN or ALAT (1-chnl.modes) or ALAT & BLAT (2-chnl. modes, respectively).
11	F-bit of embedded TRS EAV clears current write pointer. - If B_FLD = 0 (frame-based sync), action is on each B-channel EAV with F = 0 for which the preceding EAV had F = 1. - If B_FLD = 1 (field-based sync), action is on each B-chan EAV whose F differs from that of the preceding EAV. A_FLD affects the tA-channel operation in the same fashion.

Register 9[5] = B_FLD frame/field sync select, chnl B

0	use only falling F-bit in EAV; ignore rising (dflt)
1	use both rising and falling F-bit in EAV

Register 9[4] = A_FLD frame/field sync select, chnl A

0	use only falling F-bit in EAV; ignore rising (dflt)
1	use both rising and falling F-bit in EAV

Register 9[3] MARK_SEL - This signal is used in combination with pin $\overline{BCLR}$ to determine to effect of bringing $\overline{RSET}$ low on the read pointer(s). When $\overline{RSET}$ goes to 0:

0	force read pointer(s) to marked address(es) (dflt)
1	force read pointer(s) as shown in following table:

OPMODE	*$\overline{BCLR}$*	*Read Pointer Equals:*
0-3	1	BIN/BOUT address
0-3	0	BLAT address
4-7	x	Ch. A=ALAT, Ch. B=BLAT

Configuration Register Definitions

Register 9[2:0] = FLAG_SET[2:0] - sets fractional "Fullness" and "Emptiness" Thresholds for Programmable Empty/Full Flags.

Full flag goes HIGH when the memory is more than "TH" full. Empty flag goes HIGH when the memory is less than or equal to "TL" full.

000	TH = 79/81 (dflt)	TL = 1/81 (dflt)
001	TH = 78/81	TL = 2/81
010	TH = 77/81	TL = 3/81
011	TH = 76/81	TL = 4/81
100	TH = 75/81	TL = 5/81
101	TH = 74/81	TL = 6/81
110	TH = 73/81	TL = 7/81
111	TH = 72/81	TL = 8/81

Register A[7] = BSET_catch - (OPMODES 4-7 only)

0:	setting write pointer B does not mark its new value (dflt)
1:	setting write pointer B automatically marks its new value

Register A[6] = ASET_catch - (all OPMODES) logic same as above for BSET_catch

Register A[5:0] Control action.

Rb[5]	RSET_b_sel
Rb[4]	RCLR_b_sel
Rb[3]	BSET_b_sel
Rb[2]	BCLR_b_sel
Rb[1]	ASET_b_sel
Rb[0]	ACLR_b_sel
if 0:	Each falling edge on the corresponding control pin overrides a memory address counter for exactly one clock cycle, after which normal memory address incrementing immediately resumes. (dflt)
if 1:	The corresponding pin continuously overrides the memory address counter as long as it is held LOW. Memory address incrementing resumes when the pin is returned HIGH.

Configuration Register Definitions

Register B[7:4] = BFLAG_CTL[3:0] for pins BPE and BPF * (See below for legend)

BFLAG_CTL	*BPE*	*BPF*	*BCOLLIDE*
0000	B empty (R)	B full (W)	BCOLLIDE (R)
0001	RB=MB (R)	RA=MA (R)	BCOLLIDE (R)
0010	BIN f (W)	BIN v (W)	BIN h (W)
0011	BOUT f (R)	BOUT v (R)	BOUT h (R)
0100	BIN f (W)	BIN v (W)	BCOLLIDE (R)
0101	BOUT f (R)	BOUT v (R)	BCOLLIDE (R)
0110	BIN f (W)	BIN h (W)	BCOLLIDE (R)
0111	BOUT f (R)	BOUT h (R)	BCOLLIDE (R)
1000	BIN v (W)	BIN h (W)	BCOLLIDE (R)
1001	BOUT v (R)	BOUT h (R)	BCOLLIDE (R)

**Each flag is updated on the rising edge of its associated clock: BWCLK (W) or RCLK (R)*

AIN f, v, h are the TRS bits embedded in the incoming A channel TRS signals.
AOUT f, v, h are the TRS bits embedded in the emerging A channel TRS signals.
BIN f, v, h and *BOUT f, v, h* are the analogous B channel values.
RA(RB) is the read address pointer value for channel A(B).
MA(MB) is the 'marked' address pointer value for channel A(B).

Register B[3:0] AFLAG_CTL[3:0] for pins APE and APF *

AFLAG_CTL	*APE*	*APF*	*ACOLLIDE*
0000	A empty (R)	A full (W)	ACOLLIDE (R)
0001	RB=MB (R)	RA=MA (R)	ACOLLIDE (R)
0010	AIN f (W)	AIN v (W)	AIN h (W)
0011	AOUT f (R)	AOUT v (R)	AOUT h (R)
0100	AIN f (W)	AIN v (W)	ACOLLIDE (R)
0101	AOUT f (R)	AOUT v (R)	ACOLLIDE (R)
0110	AIN f (W)	AIN h (W)	ACOLLIDE (R)
0111	AOUT f (R)	AOUT h (R)	ACOLLIDE (R)
1000	AIN v (W)	AIN h (W)	ACOLLIDE (R)
1001	AOUT v (R)	AOUT h (R)	ACOLLIDE (R)

**Each flag is updated on the rising edge of its associated clock: AWCLK (W) or RCLK (R)*

Configuration Register Definitions

Register C[7:4] = BASE_ADDR[3:0] - position of chip in cascade series; 0000 = lowest; BASE_ADDR[3:0] must not exceed CASCADE[3:0]

Register C[3:0] = CASCADE[3:0] - number of chips in a system with concatenated address spaces.

0000:	single chip operation; (dflt) sequential R, W addresses, modulo 103,680
0001:	two chip cascade; sequential R, W addresses, modulo 207,360
...	...
1111:	sixteen chip cascade; (a) sequential R, W addresses, modulo 1,658,880 (a) Note limits regarding the number of possible chips, related to WIDTH control: 8bit data: 10 or less LF3312s (WIDTH = 0x) 10bit data: 13 or less LF3312s (WIDTH = 10) 12bit data: 16 or less LF3312s (WIDTH = 11)

Configuration Registers For Testing

Addresses D hex and above are for test purposes only.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
VCC_{INT} , Internal supply voltage with respect to ground	–0.5V to + 2.0V
VCC_O, Output drivers supply voltage with respect to ground	–0.5V to + 4.0V
Signal applied to high impedance output	–0.5V to + 3.3V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Characteristic	Mode	Temperature Range	Supply Voltage
VCC_{INT}	Commerical	0°C to +70°C	1.71V ≤ Vcc ≤ 1.89V
VCC_O	Commerical	0°C to +70°C	3.00V ≤ Vcc ≤ 3.60V

Electrical Characteristics *Over Operating Conditions (Note 4)*

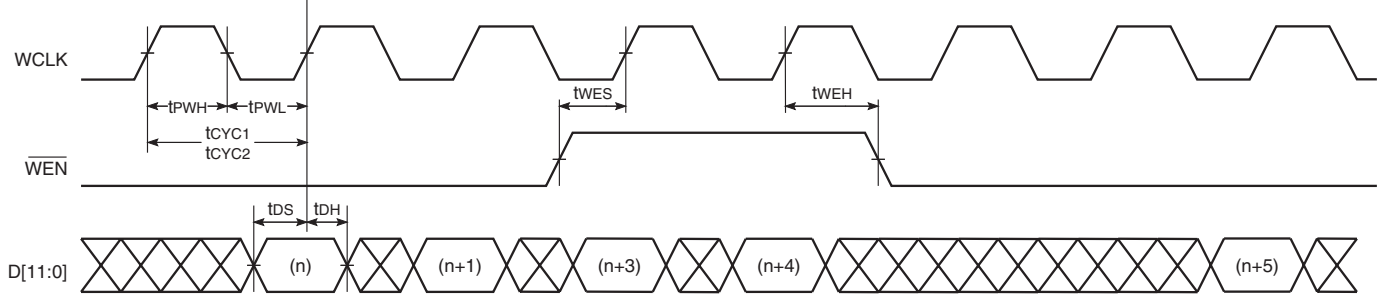
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., $I_{OH\ MAX}$ = -4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., $I_{OL\ MAX}$ = 4 mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{Ix}	Input Current	With Internal Pull-up - JTAG & I2C pins			+20	µA
I_{Ix}	Input Current	All other pins			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CCint} Current, Dynamic	f=55MHz, V_{CCint} =1.9V (Note 7)			48	mA
I_{CC2}	V_{CCint} Current, Quiescent	V_{CCint} =1.9V (Note 7)			550	µA
I_{CC3}	V_{CCo} Current, Dynamic	f=74MHz, V_{CCo} =3.6V (Note 6)			12	mA
I_{CC4}	V_{CCo} Current, Quiescent	V_{CCo} =3.6V			60	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			7	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			7	pF

Switching Characteristics

Commercial Operating Range (0°C to +70°C) Notes 9, 10 (ns)

		LF3312BGC			
		-			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**
t_{CYC1}	Cycle Time 1 (AWCLK,BWCLK,RCLK) - FIFO / Sh. Reg Modes	13.4			
t_{CYC2}	Cycle Time 2 (AWCLK,BWCLK,RCLK) - Full-time Random Access	18			
t_{PWH}	Clock Pulse Width High (AWCLK,BWCLK,RCLK)	5			
t_{PWL}	Clock Pulse Width Low (AWCLK,BWCLK,RCLK)	5			
t_{DS}	Setup Time, Data Inputs (AIN,BIN)	5			
t_{DH}	Hold Time, Data Inputs (AIN,BIN)	1			
t_{WES}	Write Enable Setup Time (AWEN,BWEN)	5			
t_{WEH}	Write Enable Hold Time (AWEN,BWEN)	1			
t_{RES}	Read Enable Setup Time (AREN,BREN)	5			
t_{REH}	Read Enable Hold Time (AREN,BREN)	1			
t_{LDS}	Load Setup Time	5			
t_{LDH}	Load Hold Time	1			
t_{RWS}	R/W Set/Clr Setup Time (ACLR,BCLR,ASET,BSET,RSET,RCLR)	5			
t_{RWH}	R/W Set/Clr Hold Time (ACLR,BCLR,ASET,BSET,RSET,RCLR)	1			
t_{D}	Access Time		7		
t_{F}	Write Clock to Programmable Flags (A/BPE,A/BPF,A/BOLLIDE)		7		
t_{DIS}	Tri-state Output Disable Delay		10		
t_{ENA}	Tri-state Output Enable Delay		10		
t_{CSU}	Parallel Interface Control Setup Time for Reads/Writes	5			
t_{CHD}	Parallel Interface Control Hold Time for Reads/Writes	1			
t_{CSPW}	Parallel Interface Control Strobe pulse width	20			
t_{CDLY}	Parallel Interface Control Output Delay		8		
t_{CZ}	Parallel Interface Control Tristate delay		10		

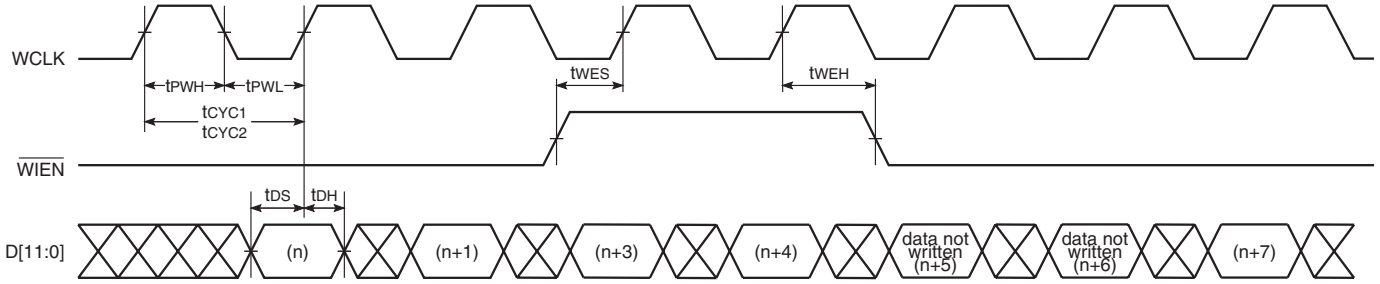
Write Cycle Timing - Write Enable



$\overline{IEN}$ = LOW

NOTE: WEN must be brought LOW 2 rising edges of WCLK prior to latching valid data on D

Write Cycle Timing - Write Masking

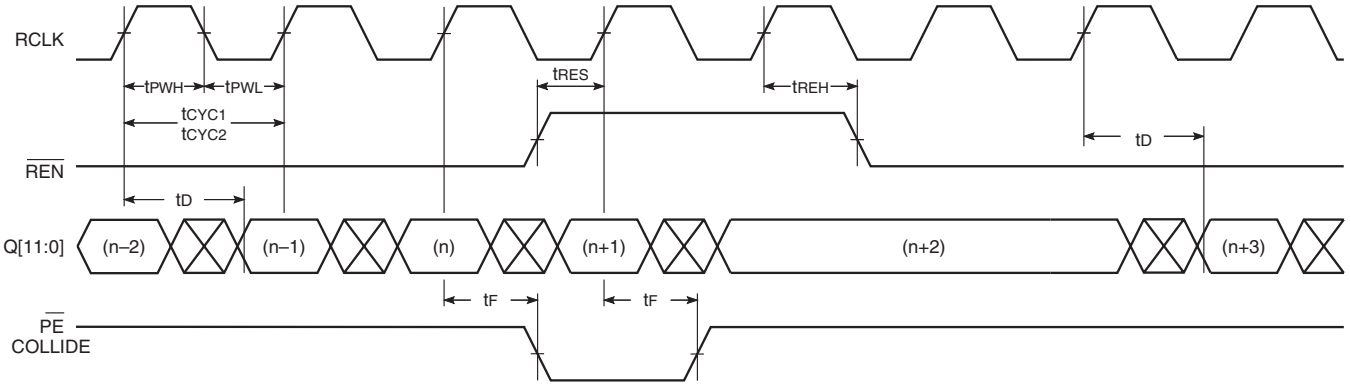


$\overline{WEN}$ = LOW

NOTE: Bringing WIEN HIGH disables data on D from being written into memory, yet it does not disable the Write pointer from incrementing

NOTE: WIEN must be brought HIGH 2 rising edges of WCLK prior to masking input data on D

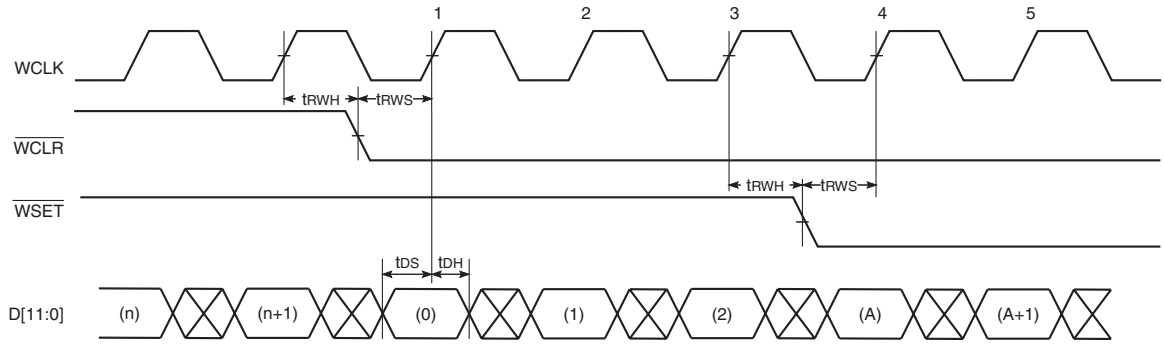
Read Cycle Timing



$\overline{OE}$ = LOW

NOTE: REN should be brought LOW 2 rising edges of RCLK prior to expecting valid data on Q

Write Reset Timing



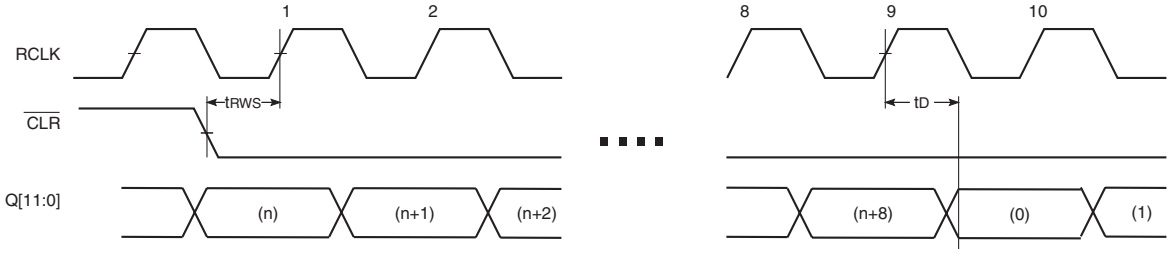
$\overline{WEN}$ = LOW

CLR and SET both programmed to be falling edge sensitive

* Rising Edge 1: Clears Write Pointer and latches data on D to be written in address 0

*Rising Edge 4: Sets Write Pointer to Address A (based on WADDR) and latches data on D to be written in Address A

Read Reset Timing

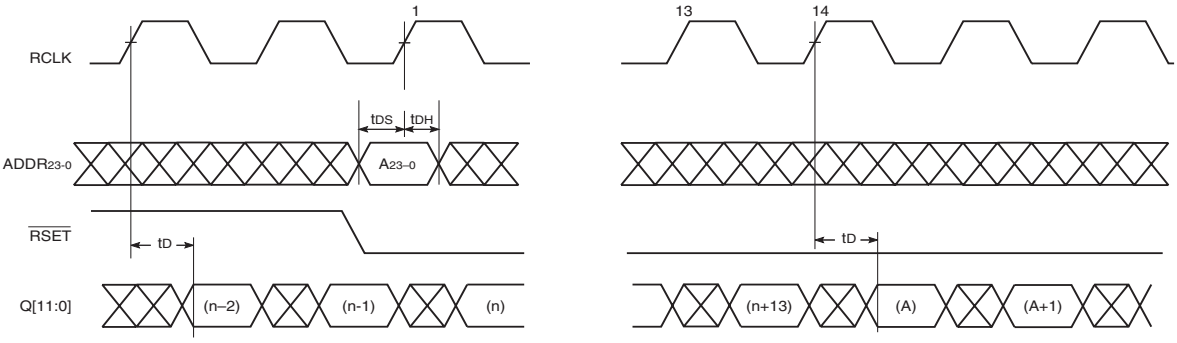


$\overline{REN}$ = LOW

NOTE: CLR programmed as being falling edge sensitive

It takes 9 REN-enabled rising edges of RCLK (including the edge that latches a LOW on CLR) to pass the contents of address 0 to the Q port.

Random Access Read Pointer 'Jump' Timing

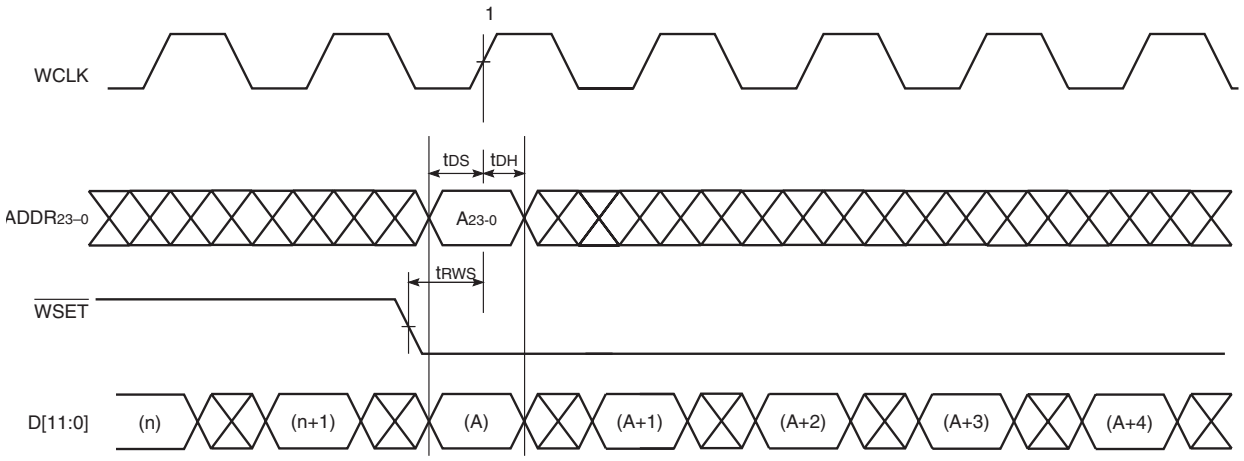


$\overline{OE}$ = LOW $\overline{REN}$ = LOW WADDRSEL= LOW RADDRSEL= HIGH OPMODE[2:0]=001 MARK_SEL (Register 9[3]) =1

NOTE: RSET programmed to be falling edge sensitive

NOTE: It takes 14 rising edges of RCLK upon setting/jumping the Read pointer
(to the 24bit Address "A" on ADDR) for the contents of location A to be dumped onto Q

Random Access Write Pointer 'Jump' Timing

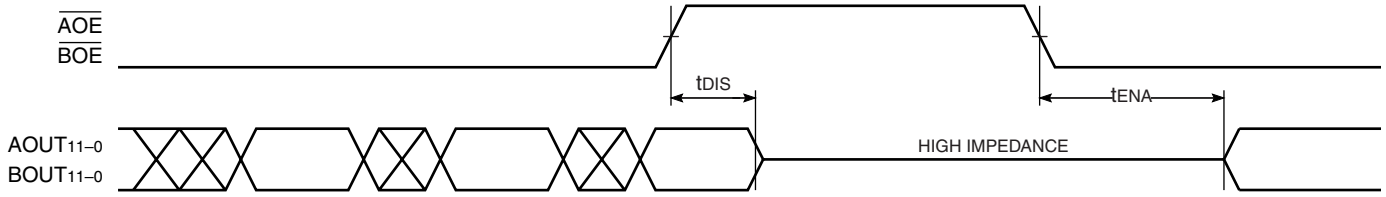


$\overline{WEN}$= LOW WADDRSEL= HIGH OPMODE[2:0]=001

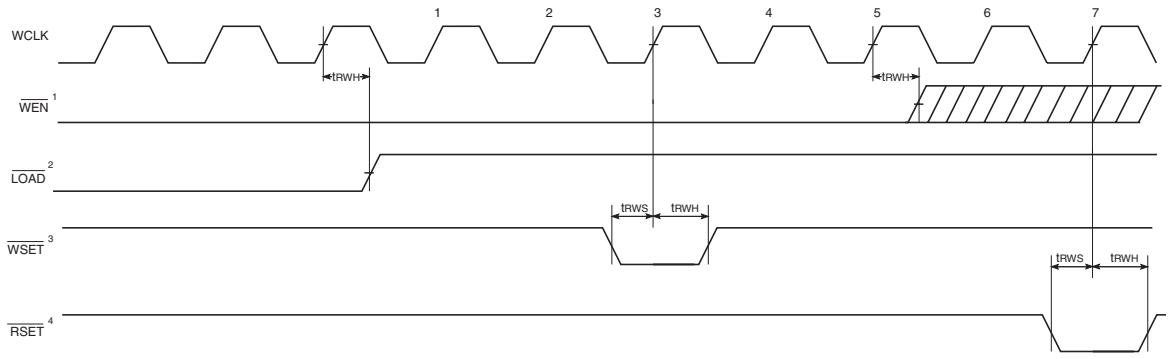
NOTE: SET programmed to be falling edge sensitive

NOTE: Rising edge of WCLK labeled "1" writes data on D to 24bit Address "A"

Output Enable and Disable



Jumping/Setting Pointers based on Configuration Register Address after Remapping Process



SET and RSET programmed to be level sensitive

[1] $\overline{WEN}$ is LOW for 3 rising edges of WCLK prior to LOAD transition. It stays LOW for the minimum required 5 rising edges after the LOAD transition.

[2] The configuration registers are programmed while LOAD is LOW. The LOAD transition triggers the address remap process.

[3] WSET can be brought LOW (edge "3") 3 rising edges of WCLK after the LOAD transition, jumping the write pointer to the address programmed into the WADR register.

[4] RSET can be brought LOW (edge "7") 7 rising edges of RCLK after the LOAD transition, jumping the read pointer to the address programmed into the RADDR register.

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6V. The device can withstand operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels may be in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. I/O Ring supply current for a given application can be approximated by:

where $\frac{NCV^2F}{2}$

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested in single-channel mode with 14 output pins driving 10pF loads, while toggling at an average of 30% of the 74MHz clock rate. The 10pF load is estimate of trace and downstream pin capacitance.

7. Operating condition assumed to be most demanding reading/writing memory scenario .

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{dis} test), and input levels of nominally 0 to 3.0V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current change pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the device as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the device leads.

Notes

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required input levels relative to the device ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the $\mathbf{t}_{ena}$ test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the $\mathbf{t}_{dis}$ test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{th}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case

Figure A. Output Loading Circuit

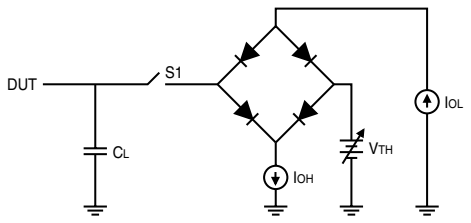
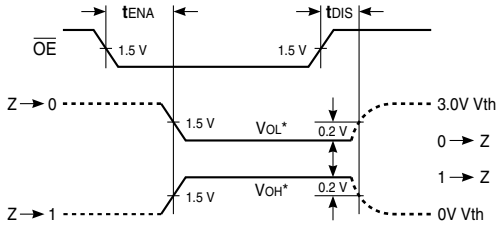
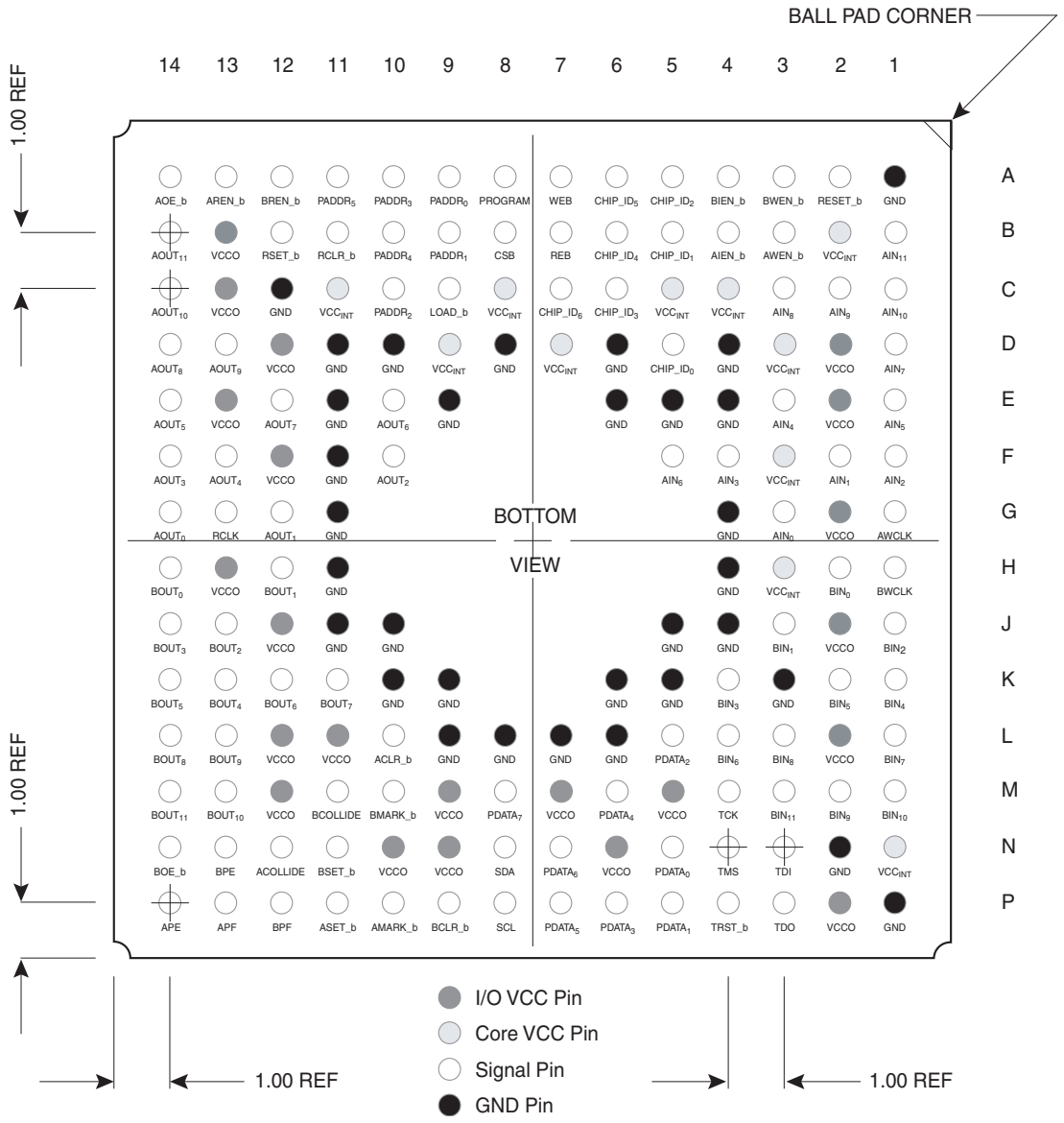


Figure B. Threshold Levels



VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

Package and Ordering Information



172 Ball - Low Profile Ball Grid Array (LBGA)

0°C to 70°C--Commercial Screening

Speed	
_	LF3312BGC

Document History Page

DOCUMENT TITLE: LF3312 12MBIT FRAME BUFFER / FIFO			
Rev.	ECN NO.	Issue Date	Description of Change
J		03/29/05	Cycle time changed to 13.5ns for fast FIFO modes
K		04/07/05	Fixed pg 17 PROGRAM pin reference. (PR=0 serial) (PR=1 parallel)
L		04/08/05	Cycle time changed to 13.4ns to better reflect HD 74.25MHz rate
M		08/18/05	Pg 24 VCC text, pg25 I2C descr, pg22 clarifications on Flag operation
N		09/14/05	General clarification of op-mode operation text
O		08/08/06	Fixed pg32 pin-out pin J1 (signal BIN2), Fixed cascaded device drawing