LF3324
24Mbit Frame Buffer / FIFO

Preliminary Datasheet

Features

- 24,883,200-bit Frame Memory
- 54 Mhz Max Data Rate
- May be Organized Into the Following Configurations:
  - 3,110,400 x 8-bit
  - 2,488,320 x 10-bit
  - 2,073,600 x 12-bit
- Operating Modes:
  - Random Access with Burst Control
  - FIFO
- Near-Full/Empty Flags With Programmable Thresholds
- Flexible Pointer Manipulation
  - Write and Read Pointers may be independently jumped to arbitrary address locations
  - Write or Read Pointers can be manipulated in real-time based on external 24bit address
- LF3324s may be Cascaded for depth and width, supporting HDTV, Multiframe SDTV, and other high resolution formats
  - Seamless address space is maintained with up to 8 cascaded devices
- Built-in ITU-R BT.656 TRS detection and Synchronization
- Set & Clear Read/Write Pointer Control Pins
- Choice of Control Interfaces:
  - Two-wire Serial Microprocessor Interface
  - Parallel Microprocessor Interface
- Input Enable Control (Write Mask) for freeze-frame applications
- Output Enable Control (Data Skipping)
- JTAG Boundary Scan - IEEE 1149.1
- 172 ball LBGA package
- 1.8V Internal Core Power Supply
- 3.3V I/O Supply

NOTE: This **Preliminary Datasheet** references **LF3324BGC** Engineering Samples with an **E** marking under the part designation.

Applications

- SD/HDTV Video Stream Buffer
- RGB Graphics Buffer
- Frame Synchronization
- CCTV Security Camera Systems
- Time Base Correction (TBC)
- Freeze-Frame Buffer
- Regional Read/Write for Picture-in-Picture (PIP)
- Field-Based or Frame-Based Comb Filtering
- Video Capture & Editing Systems
- Deep Data Buffering
- Video Special Effects (Rotation, Zoom)
- Test Pattern Generation
- Motion Detection or Frame-to-Frame Correlation

LF3324 Overview

The LF3324 is a 24 Mbit memory device that handles 8, 10, or 12bit data. The input data port may be clocked asynchronously to the output ports. Since reads are non-destructive, a given data value, once written into the memory core, may be read as many times as desired. A user requiring more storage can cascade up to eight LF3324s into a larger array.

A great deal of memory addressing flexibility is offered with the LF3324. Both Burst Mode and Random Access addressing is possible. In addition to simple clearing of the Write and Read pointers, either pointer may be set/jumped to any location within the entire address space. Real-time random-access Writing or Reading is also supported through an external address port.

The device is controlled by sixteen instruction words of eight bits each, which may be programmed or verified via standard I²C 2-wire serial or parallel microprocessor interfaces.

The OPMODE configuration register selects one of the chip's operating modes, each of which has versatile submode options:

- FIFO With Asynchronous I/O
- Synchronous Shift Register (Single Clock; User-set Latency)
- Random Access With Burst Address

Figure 1. LF3324 Functional Block Diagram

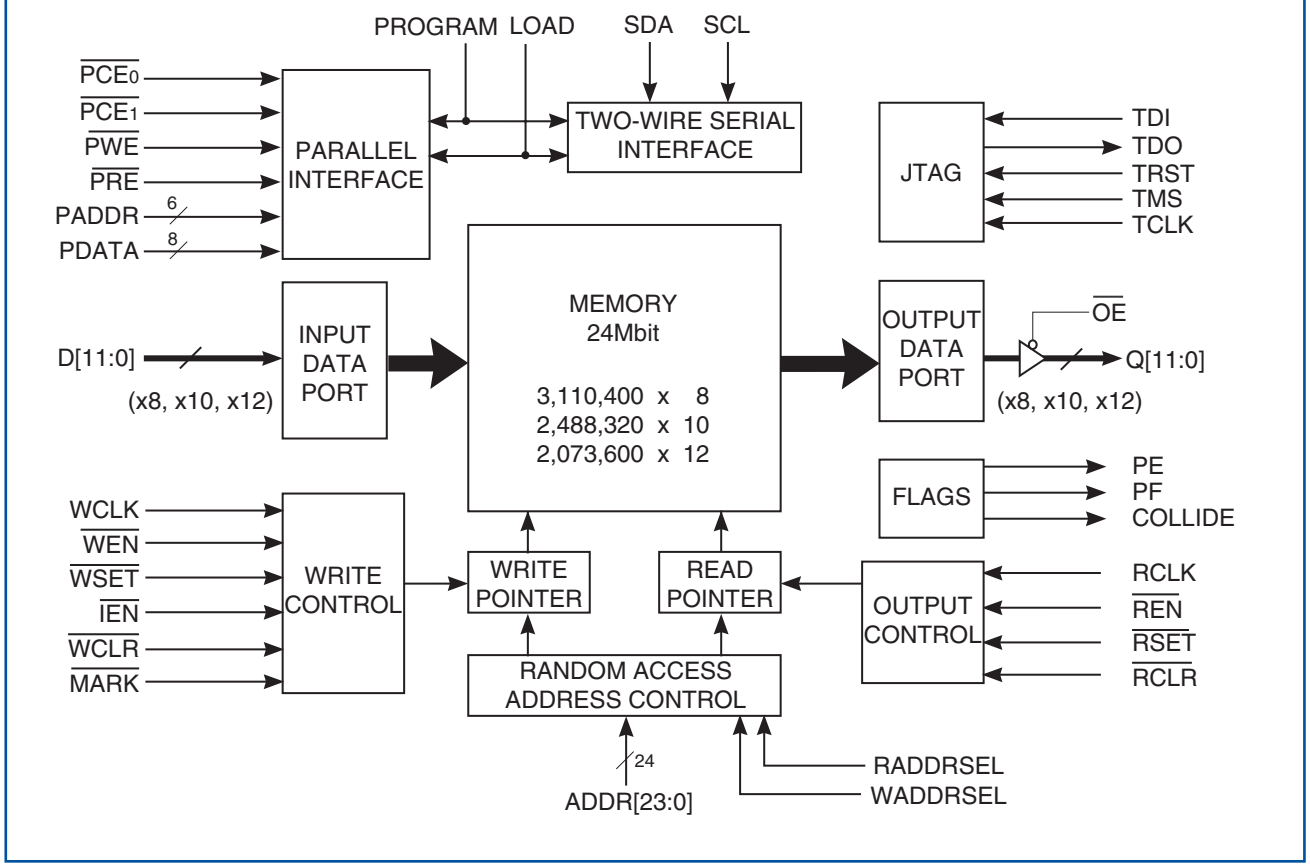


Figure 2. Single Channel FIFO Mode Functional Block Diagram

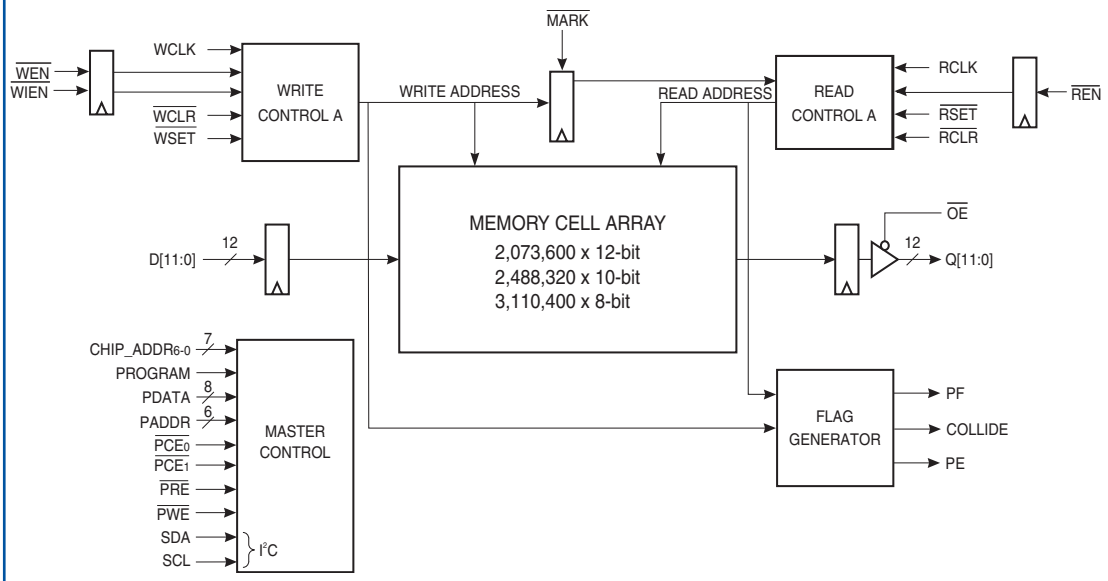
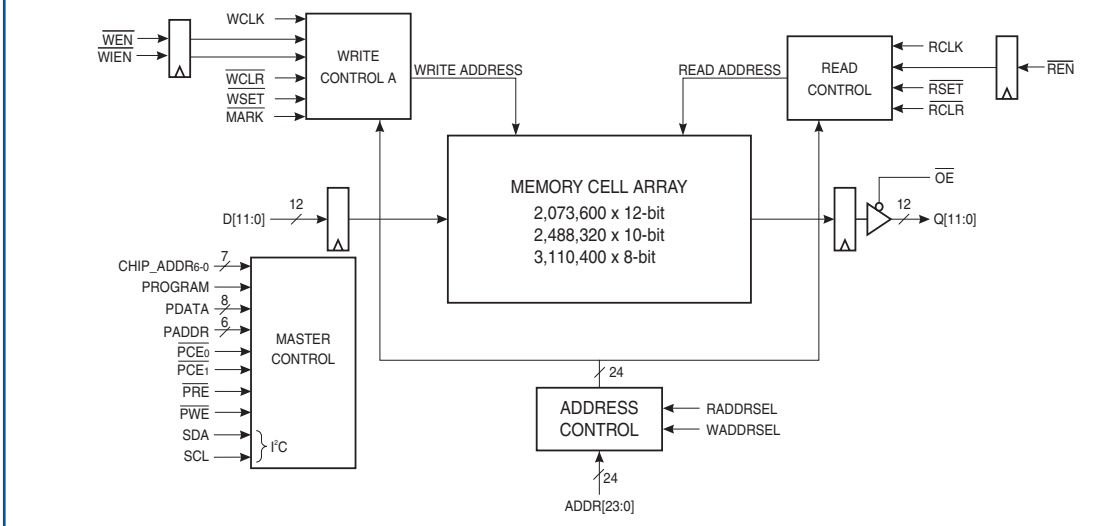


Figure 3. Random Access Mode Functional Block Diagram



Operating Modes

Asynchronous FIFO mode (OPMODE = 3)

In OPMODE 3, the LF3324 is configured as asynchronous First-In-First-Out 24Mbit memory, with independent read and write clocks to allow for asynchronous operation. This mode is ideal for buffering or burst data applications. Arbitrary write/read pointer jumping is supported in all FIFO modes. In this mode the device can re-time a data stream according to a read sync signal (RSET or RCLR) and either ITU-R656 Timing Reference Signals (TRS) embedded within the incoming (video) data or the falling edge of a write sync signal applied to WCLR, WSET, or MARK.

The input (write) and output (read) clocks need not be synchronous with one another, although the memory core may fill or empty if they differ in average frequency. After it "fills," the LF3324 continues writing and the oldest data gets written over. If the memory core "empties" (and neither the read nor write pointer have been set or cleared during run-time) the read pointer stops incrementing, and the device re-reads the last written sample until more data is written. In either case, when the read and write addresses are the same, the COLLIDE flag will go high, to alert the host. The almost-full (PF) and almost-empty (PE) flags provide advance warning of these conditions whenever user-selected "fullness" or "emptiness" thresholds, expressed in approximate eightieths of the memory core size, are exceeded. For example, if the 1/80 and 79/80 thresholds are enabled, flag PE will go HIGH whenever the read pointer lags behind the write pointer by less than 1/80 of the memory space, and flag PF will go HIGH whenever the read pointer leads the write pointer by this amount. (Calculations are performed modulo the total address space.) The data input and output are sequential and the timing between write and read sync signals dynamically determines the effective delay (depth) of the FIFO.

The "stop reading when empty" FIFO-mode behavior can be avoided by making sure LOAD is HIGH and issuing any write or read pointer SET or CLEAR command at any time. This effectively gets the device out of this "read-pointer-halting" mode from that point onwards, but invalidates the flags. Random Access Mode allows free manipulation of the r/w pointers, and never halts the read pointer without being commanded to do so using REN. Since Random Access mode naturally increments the r/w pointers sequentially, like in FIFO mode, it may be a better mode to use if complex pointer manipulation of a single-channel of memory is desired.

Synchronous shift register mode (OPMODE = 0)

In OPMODE 0, the LF3324 becomes a shift register with programmable total latency up to 2^{24}-8 clock cycles. Writes and reads occur simultaneously, hence synchronous operation.

In OPMODE 0, the user provides a single clock for both the input and output clocks and specifies a desired input-to-output data path latency, configuration register "WADDR" via the control interface. WCLK and RCLK must be tied together, as should WEN and REN. When activated, WADDR will begin to countdown, and once expired, will allow the inputs to begin to appear on the outputs. In OPMODE 0, WADDR countdown can be activated in two ways. The first occurs when the first enable is brought LOW after the LOAD signal has been set HIGH after MPU programming. The second is by bringing LOAD HIGH once MPU programming complete, after the enables have been brought LOW.

Random Access Mode (OPMODE = 1)

Random Access mode is a FIFO mode, with the capability of either full-time write or read pointer Random Accessability. This mode also supports write and read pointer jumps to arbitrary locations throughout the address space. Unlike Asynchronous FIFO mode, Random Access mode does not disable memory reads when the read pointer catches up to the write pointer. Write pointer manipulation can be done

Operating Modes

through setting (jumping) the write pointer to the 24bit address via the ADDR[23:0] port or to the WADDR configuration register. Read pointer manipulation can be done through setting (jumping) the write pointer to the 24bit address via the ADDR[23:0] port or to the RADDR configuration register. Periodic write and read pointer jumping can be accomplished by supplying an address through either the ADDR[23:0] external address or the WADDR/RADDR instruction registers. Continuous random access can only be accomplished through the use of the ADDR[23:0] ports. When the write/read pointers are not being set to an address, they increment sequentially in burst mode.

In Random Access Mode, when WADRSEL = 1 and RADRSEL = 0 the write pointer is set to the address supplied by the ADDR[23:0] ports when $\overline{\text{WSET}}$ is brought LOW. In other words, on each active write clock cycle (rising edge of WCLK for which $\overline{\text{WEN}}$ was LOW two rising edges of WCLK previously), the user directs the write pointer to any desired memory location, using what are otherwise the second channel data input and output ports. **In this application, ADDR[23:12] denotes the vertical (row) component, and ADDR[11:0], the horizontal (column) component, of a Cartesian set.** Setting the configuration register ROW_LENGTH to the frame's line (row) length internally defines the Cartesian coordinates. Also, ADDR[23:0] can also represent a single 24-bit linear address. The user governs the mapping of (ADDR) to the internal memory space by setting the parameter ROW_LENGTH such that the internal ADDRESS = ADDR[23-12] * ROW_LENGTH + ADDR[11-0]. A ROW_LENGTH setting of 0 is interpreted as 4096, such that ADDRESS = a 24-bit concatenation of {ADDR} for this particular value. For a standard D1 video application with 1716 samples per line, the user would set ROW_LENGTH to 1716 decimal = 6B4 hex. Offset circuitry within the LF3324 permits the user to cascade several chips in parallel and to use them collectively as a single large memory with a seamless address space. Data are read out sequentially by rising edges of RCLK, under the control of $\overline{\text{REN}}$ (read enable), $\overline{\text{RSET}}$ (read pointer force to constant), and $\overline{\text{RCLR}}$ (read pointer clear to 0). Holding WSET LOW keeps the device continuously in random access write mode. Releasing WSET to its HIGH state causes the chip to continue to write sequentially from the last-loaded address.

In Random Access Mode, when RADRSEL = 1, WADRSEL = 0, MARK_SEL = 1, the read pointer is set to the address supplied by the ADDR[23:0] ports when $\overline{\text{RSET}}$ is brought LOW. As mentioned above, ADDR[23:12] represents the upper bits or the vertical (row) address, whereas ADDR[11:0] represents the lower bits or the horizontal (column) address. Releasing $\overline{\text{RSET}}$ HIGH causes the read address pointer to increment from its last assigned location to the next sequential address.

It is important to note that $\overline{\text{WSET}}$ and $\overline{\text{RSET}}$ can be programmed to be level or negative-edge triggered. An edge sensitive "SET" command is useful for using SYNC signals to reset FIFO pointers. Level sensitive "SET" commands allow full-time Random Access capability.

Depth Expansion

Cascading Devices

Multiple devices can be cascaded to deepen the address space. For every device cascaded more of the 24bit address space is used.

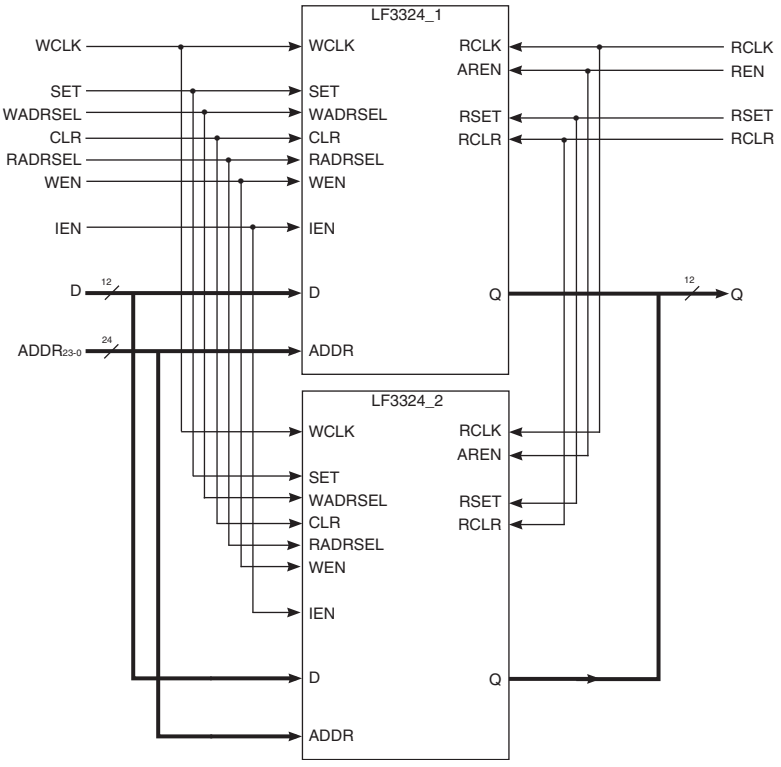
Internally, the LF3324 has a 24bit address space. The LF3324 was designed to be cascaded in parallel. That is, the inputs of each device are tied together. The input data word (the data word placed on the D input port) is to be common for all devices. Similarly, the outputs of all devices are tied together. Each device's write and read pointers behave identically. Only one device drives the shared output bus at one time, controlled automatically through internal bus enables.

Each device in a cascade of N devices is responsible for 1/N of the address space. That is, each device writes and/or reads based on the common W/R pointer locations and where that particular device sits in the cascade. Configuration Register C[3:0] (BASE_ADDR) is used to define each device's place in the cascade.

When cascading LF3324s, all write enables $\overline{WEN}$ and $\overline{WIEN}$ must be tied together, as must read enables $\overline{REN}$ (see the device connection diagram below).

The configuration registers of each device must be programmed identically, depending on mode/function, except for Register C. Register C defines which region of the 24bit address space the particular device is responsible for. Within Register C, there is a 4bit BASE_ADDR and 4bit CASCADE word. BASE_ADDR determines the region of address space each device controls, and CASCADE defines how many devices are in cascade. Register C effectively is programmed as "Chip n of N".

Figure 4. Depth Expansion Example: 48Mbit Memory



Device Configuration

Programming the LF3324

The LF3324 has two MPU interfaces. The first is a standard two wire serial interface following the I²C protocol. The second is a parallel interface allowing the user to write a byte of data at a time to the configuration registers. When the user wishes to use the serial interface, the PROGRAM pin must be set LOW, while a HIGH selects the parallel interface. To provide users with more flexibility, the control registers have been combined with a “working latch” . Ultimately, the register-latch combination allows users to update the configuration registers during chip operation, and then to transfer the register contents to all working latches simultaneously using the $\overline{\text{LOAD}}$ signal. When high, the $\overline{\text{LOAD}}$ signal allows the LF3324 to be pre-programmed during operation, and once brought low after programming updates the working latches allowing the new changes to take effect. $\overline{\text{LOAD}}$ can also be maintained low to allow changes to the configuration registers to be immediately reflected in the working latches.

Serial MPU Interface

When the PROGRAM pin is LOW, the serial interface is active. Up to 8 LF3324 devices can be connected to and programmed by the serial interface. The two wire interface is composed of an SCL clock pin and a bi-directional SDA data pin. When inactive, SDA and SCL are forced HIGH by external pull up resistors.

Data transmission is achieved over the SDA pin and must remain constant during the logical HIGH portion of the SCL clock pulse. The level of SDA, while SCL is HIGH, is interpreted as the appropriate bit value as will be shown later. Changing the data on SDA must only occur when SCL is low, because any changes to SDA while SCL is HIGH is interpreted as a start or stop request, which are shown in Figure 7 with an example data transfer in Figure 8.

The first operation to begin programming the LF3324 through the serial interface, is to send a start signal. When the interface is inactive, a HIGH to LOW transition must be sent on SDA while SCL is HIGH, notifying all connected devices (slaves) to expect a data transmission. When transferring data, the MSB of the eight bit sequence is the first bit to be transmitted to or from the master or slave. The first byte of data to be transmitted on SDA must consist of the 7-bit base address of the slave, along with an 8th READ/WRITE bit as the LSB, which describes the direction of the data transmission. The slave whose 7-bit CHIP_ADDR6-0, matches the 7-bit base address sent on SDA, will send an acknowledgement back to the master by bringing SDA LOW on the 9th SCL pulse. NOTE: In order to differentiate the two internal die, die 0’s CHIP_ADDR(0) is tied LOW and die 1’s CHIP_ADDR(0) is tied HIGH.

During a write operation, if the slave does not send an acknowledgment back to the master device, SDA is left high which forces the master to generate a stop signal. In contrast, during a read operation, if there is no acknowledgement back from the master device, the LF3324 interprets this as if it were the end of the data transmission, and leaves SDA high, allowing the master to generate its stop signal.

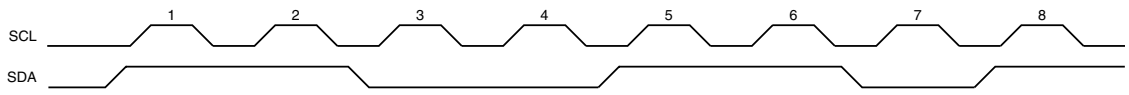
Figure 5. I²C Start and Stop Signals

Device Configuration

There are four operations that can be performed between the master and the slave. They are: Write to consecutive registers, write to a single configuration register, read from consecutive registers and read from a single register. To write to consecutive control registers, a start signal and base address must be sent with the R/W bit as described above. After the acknowledgment back from the appropriate slave, the 8-bit address of the target configuration register must be written to the slave with the R/W bit LOW. The slave then acknowledges by setting SDA LOW. The data byte to be written into the register can now be transferred on SDA. The slave then acknowledges by pulling SDA LOW on the next positive going pulse of SCL. The first configuration register address loaded into the LF3324 is considered as the beginning address for consecutive writes, and automatically increments to the next higher address space. Therefore after the acknowledgement, the data byte to configure register (first address + 1) can now be transferred from master to slave. At any point a stop signal can be given to end the data transfer. To write to a single configuration register, the same technique can be applied adding a stop signal after the first data write.

To read from consecutive control registers, the master must again give the start signal followed by a base address with the R/W bit = 0, as if the master wants to write to the slave. The appropriate slave then acknowledges. The master will then transfer the target register address to the slave and wait for an acknowledge. The master will then give a repeated start signal to the slave, along with the base address and R/W bit this time HIGH signifying a read and wait for an acknowledge. The user must write to the LF3324 to select the appropriate initial target register. Otherwise the starting position of the read is uncertain. Once the LF3324 acknowledges, the next byte of data on SDA is the contents of the addressed register sent from the device. If the master acknowledges, the LF3324 will send the next higher register's contents on the following byte of data. To read from only one register is the same procedure as for consecutive reading with a stop signal following the transfer of the register's contents.

Figure 6. I^2C Example of transferring 11001101 on SDA



Parallel MPU Interface

The parallel MPU interface can be used to write instructions to the control registers or to read them back for verification. When the PROGRAM pin is HIGH, the parallel interface is selected. An external processor can write into an internal register by setting PADDR to the desired register address, selecting the chip using the $\overline{PCE}$x pin, setting PDATA to the desired value and then pulsing $\overline{PWE}$ LOW. The data will be written into the selected register when both $\overline{PWE}$ and $\overline{PCE}$x are LOW, and will be held when either signal goes HIGH. To read from a configuration register the processor must set PADDR to the desired address, select the chip with the $\overline{PCE}$x pin, and then set $\overline{PRE}$ LOW. The chip will then drive PDATA with the contents of the selected register. After the processor has read the value from PDATA, $\overline{PRE}$ and $\overline{PCE}$x should be set HIGH. The PDATA pins are turned off (High Impedance) whenever $\overline{PCE}$x or $\overline{PRE}$ are HIGH or when $\overline{PWE}$ is LOW. The chip will only drive these pins when both $\overline{PCE}$x and $\overline{PRE}$ are LOW and $\overline{PWE}$ is HIGH. One can also ground the $\overline{PRE}$ pin and use the $\overline{PWE}$ pin as a read/write direction control and use the $\overline{PCE}$x pin as a control I/O strobe. NOTE: $\overline{PCE}$0 addresses die 0, while $\overline{PCE}$1 addresses die 1.

Device Configuration

Parallel Interface Cont'd

Figure 7. Normal Reading and Writing From a Configuration Register

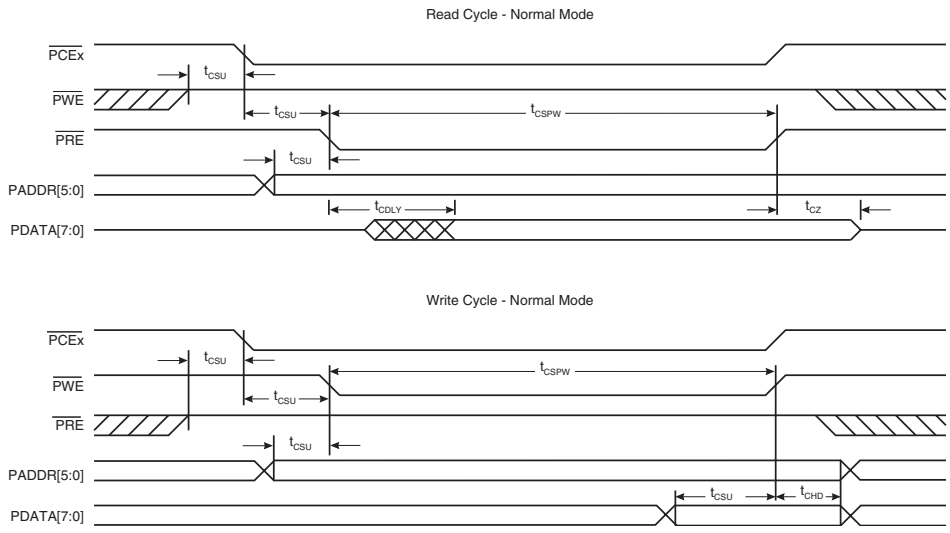
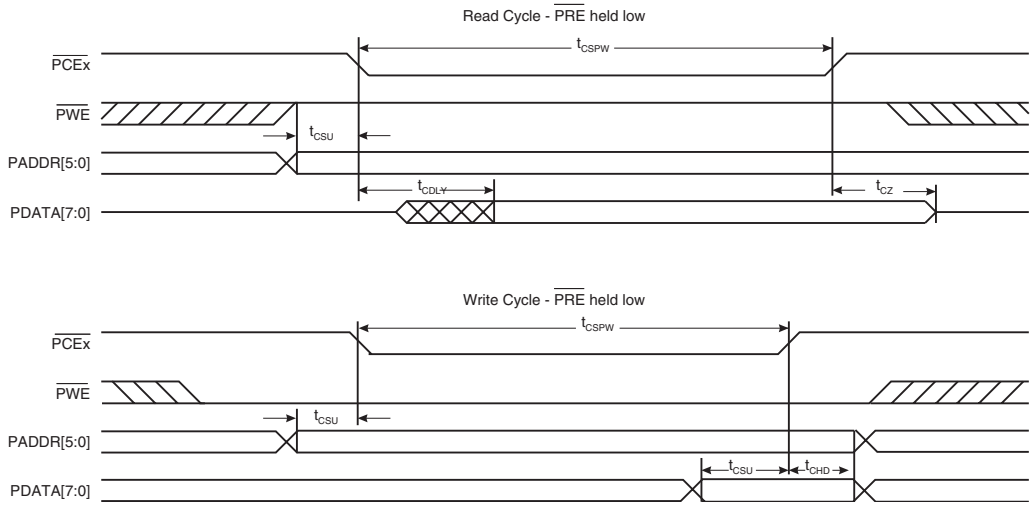


Figure 8. Reading and Writing From a Configuration Register with PRE Held Low



Detailed Signal Definitions

Power

***VCC_{INT}* - Internal Core Power Supply**
+1.8V power supply. All pins must be connected.

***VCC_O* - Output Driver Power Supply**
+3.3V power supply. All pins must be connected.

Clocks

WCLK - Write Clock
Data present on D11-0 is written into the LF3324 on the rising edge of WCLK when $\overline{WEN}$ was LOW for the previous rising edge of WCLK.

RCLK - Read Clock
In data is read from the LF3324 and presented on the output port (Q11-0) after a rising edge of RCLK while $\overline{REN}$ and $\overline{OE}$ are LOW. When using the ADDR[23:0] external address port for read-address setting, ADDR[23:0] is latched on the rising edge or RCLK.

Inputs

D_{11-0} - Data Input
D11-0 is the 12-bit registered data input port. Bit 11 is the MSB in all modes. D1-0 are ignored in 10-bit mode and D3-0 are ignored in 8-bit mode. Any such unused inputs should either be tied to ground or driven to proper logic levels by external logic.

$ADDR_{23-0}$ - Random Access Address Port
ADDR[23:0] is the 24-bit external address port. The 24bit address is a purely linear address when the configuration register ROW_LENGTH is equal to 0(default). When ROW_LENGTH is a non-zero value, the memory is set to have a row (line) length of ROW_LENGTH. ADDR11-0 specifies the X/Column-coordinate and ADDR23-12 specifies the Y/Row-coordinate.

$CHIP\_ADDR_{6-1}$ - Serial Interface Chip Address
CHIP_ADDR6- determines the LF3324's address on the two-wire microprocessor bus. Each LF3324 chip's 7-bit two-wire serial microprocessor interface address is equal to its CHIP_ADDR6-0. NOTE: CHIP_ADDR0 is internally tied LOW on die 0 and HIGH on die 1.

SCL - Serial Clock Input
SCL is a standard two-wire serial microprocessor interface clock pin. With this chip, it functions as a dedicated input, since this part cannot be the master on an two-wire serial microprocessor interface.

$PADDR_{5-0}$ - Parallel Microprocessor Interface Address Port
PADDR5-0 is the 6-bit address port for the parallel microprocessor interface.

Input/Output

$PDATA_{7-0}$ - Parallel Microprocessor Interface Data Port
PDATA7-0 is the 8-bit data port for the parallel microprocessor interface. When inactive becomes high impedance.

SDA - Serial Data I/O
SDA is the standard bidirectional data pin of a two-wire serial microprocessor interface. External pullup is required on SDA.

Controls

$\overline{WCLR}$ - Write Pointer Clear
When $\overline{WCLR}$ is brought LOW, the next rising edge of WCLK will bring the current value on D[11:0] into memory address 0. Whenever $\overline{WCLR}$ is HIGH, the destination for D[11:0] will be controlled by $\overline{WSET}$. The user may program $\overline{WCLR}$ such that either its falling edge or its LOW state is active. If its LOW state

Detailed Signal Definitions

is active, holding this pin LOW will hold the write address in its zero position continuously. This control takes effect only when WEN is LOW.

RADDRSEL - Read Address Select
RADDRSEL selects the source of the read address. This pin and control MARKSEL select whether RSET forces the read address to the RADDR configuration register (RADDRSEL = 0) or to ADDR[23:0] (RADDRSEL = 1). This control takes effect only when REN is LOW.

WSET - Write Pointer Set
This control is active only when WCLR is HIGH. Bringing WSET LOW will cause the next rising edge of WCLK to bring the current value on D[11:0] into memory at the address specified by WADDR, or at the address present on ADDR[23:0]. Whenever WSET and WCLR are HIGH, the next rising edge of WCLK will bring the current D[11:0] data value into the next-higher address in sequence. WSET may be programmed to be either edge-triggered, in which case it affects the write pointer for only one clock cycle following a falling edge, after which incrementing resumes, or level-triggered, in which case it affects the write pointer until it is brought HIGH. For continuous random access write operation, holding WSET LOW and programming it to be level-triggered will provide the needed continuous write pointer override. This control takes effect only when WEN is LOW.

WADDRSEL - Write Pointer Set
WADDRSEL selects the source of the write address. WADDRSEL determines whether WSET forces the write address pointer to the WADDR configuration register (WADDRSEL = 0) or to ADDR[23:0] (WADDRSEL = 1). This control takes effect only when WEN is LOW.

MARK - Write Address Pointer Mark
Bringing this bit LOW will cause an internal register to store a copy the current value of the write address pointer, for subsequent use in synchronizing the corresponding read address pointer to the same location. Unlike WCLR and WSET, this control does not affect the write pointer value itself. The system must use MARK instead of WCLR if the entire memory core can be filled between sequential falling edges of the sync reference signal. In contrast, the system must use WCLR or WSET to establish a definite relationship between the internal address and the data stream, as in random access read mode.

RSET - Read Address Pointer Set
If REN is LOW, bringing RSET LOW will force the read address to the most recently marked value (MARK_SEL LOW), to RADDR (MARKSEL HIGH and RADRSEL LOW), or to ADDR[23:0] (MARK_SEL is HIGH and RADRSEL is HIGH). This pin may be programmed to be either falling edge or level sensitive active.

RCLR - Read Address Pointer Clear
Bringing RCLR LOW causes the next rising edge of RCLK to force the read address pointer to zero. This pin may be programmed to be active on its falling edge or in its LOW state. It can reset the read pointer only when REN is LOW.

WEN - Write Enable
If WEN is LOW, data on D11-0 is written to the device on the rising edge of WCLK. When WEN is HIGH, the device ignores data on D and holds the write pointer. The user must anticipate the use of WEN by one cycle. Therefore when desiring not to write a sample, WEN must be brought high the cycle before.

WIEN - Memory Write Enable (Write Masking)
WIEN is used to enable/disable writing into the memory core. A LOW on WIEN enables writing, while a HIGH on WIEN disables writing. The internal write address pointer is incremented by WEN regardless of the WIEN level. If disabling of WIEN is never desired, tie WIEN LOW.

Detailed Signal Definitions

REN - Read Enable
If REN is LOW and the output port is enabled, data is read and presented on Q[11:0] after t_D has elapsed from the rising edge of RCLK. If REN goes HIGH, the last value loaded into output register will remain unchanged and the read pointer will be held. The user must anticipate the use of REN by one cycle. Therefore when desiring not to read a sample, REN must be brought high the cycle before.

PROGRAM - ***Serial/Parallel Interface Selector***
When the user wishes to use the serial microprocessor to configure the LF3324, the PROGRAM pin must be set LOW. If the user wishes to use the parallel interface, PROGRAM must be set HIGH.

LOAD – Instruction Load
Bringing asynchronous control LOAD LOW updates the working instruction latches to match the current contents of the instruction preload latches. Holding it LOW causes the working latches to reflect all ongoing instruction preloads. Holding it HIGH permits the user to preset the instruction preload latches to any desired configuration without disturbing the work in progress. After any write to the configuration registers, LOAD must be brought high for one cycle, and can then be brought and left low if so desired.

RESET - Global Reset
Bringing synchronous control RESET LOW forces all state machines and read and write pointers to 0 and holds them there until it is released HIGH. It also forces the configuration registers to their default states, if and only if LOAD is also LOW. The user may then modify the control registers as necessary. Bringing RESET LOW while holding LOAD HIGH will reset the state machines and pointers, but will not change either the preload or the working latches.

OE - Output Enable
When OE is LOW, Q[11:0] is enabled for output. When OE is HIGH, Q[11:0] is placed in a high-impedance state. In 10-bit modes, Q1-0 are unconditionally tristated. In 8-bit modes, Q3-0 are tristated. The flag outputs are not affected by OE.

PCE_0/PCE_1 - Parallel Interface Chip Enable
When LOW, PCE_0 enables writing to die 0 with the parallel micrprocessor interface. When LOW, PCE_1 enables writing to die 1 with the parallel micrprocessor interface.

PWE - Parallel Interface Write Enable
When LOW, PWE enables writing to the LF3324's Instruction Registers with the parallel micrprocessor interface.

PRE - Parallel Interface Read Enable
When LOW, PRE enables reading from the LF3324's Instruction Registers with the parallel micrprocessor interface.

Data Outputs

Q_{11-0} - Data Output
Q[11:0] is the 12-bit registered data output port. Q[11:0] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when REN is LOW.

Detailed Signal Definitions

Flag Outputs

PF - Programmable Almost Full
PF goes HIGH (active) when the write pointer is more than (MAX_depth - (MAX_depth x TH)) locations ahead of the read pointer. TH is a threshold value stored in Register 9 [2:0]. PF is updated on the rising edge of WCLK. TRS bits either entering of emerging to/from the device can be mapped to PF (Register B[3:0]).

PE - Programmable Almost Empty Flag
PE goes HIGH (active) when the write pointer is less than or equal to (MAX_depth - (MAX_depth x TL)) locations ahead of the read pointer. TL is a threshold value stored in Register 9 [2:0]. PE is updated on the rising edge of RCLK. TRS bits either entering of emerging to/from the device can be mapped to PE (Register B[7:4]).

COLLIDE - Memory Read/Write Pointer Collision Flag
This flag goes high whenever the read and write addresses to the memory core coincide. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full). TRS bits from D and Q can be mapped to COLLIDE (Register B[3:0]).

JTAG

TDI - JTAG input data
TDI is the input data pin when using JTAG.

TDO - JTAG output data
TDO is the output data pin when using JTAG.

TRSTB - JTAG reset
TRSTB is used to reset all the registers and state machine fount the the JTAG module.

Detailed Signal Definitions

TMS - JTAG Tap controller input
TMS controls the state of the tap controller.

TCK - JTAG clock
TCK is the used supplied clock of JTAG. It controls the flow of data and latches input data on the rising edge.

Configuration Register Map

The various 8-bit control registers may be pre-programmed with either the parallel microprocessor port (PROGRAM=1), or through the serial microprocessor interface bus(PROGRAM=0). Changes in pre-programming begin to affect the data path when $\overline{\text{LOAD}}$ is brought $\overline{\text{LOW}}$. In each instance, the value in parens () is the default state following assertion of $\overline{\text{RESET}}$ while $\overline{\text{LOAD}}$ = 0.

Configuration Register 0 (default = 00000000)

3:0 = ROW_LENGTH[11:8]	(0000: 24-bit linear map; see reg 7)

Configuration Register 1 (default = 00000000)

7:0 = ROW_LENGTH[7:0]	(00000000: 24-bit linear map; see reg 6)

Configuration Register 2 (default = 00000000)

7:0 = WADDR[23:16]	(00000000: default = 0; see reg 9, a)

Configuration Register 3 (default = 00000000)

7:0 = WADDR[15:8]	(00000000: default = 0; see reg 8, a)

Configuration Register 4 (default = 00000000)

7:0 = WADDR[7:0]	(00000000: default = 0; see reg 8, 9)

Configuration Register 5 (default = 00000000)

7:0 = RADDR[23:16]	(00000000)

Configuration Register 6 (default = 00000000)

7:0 = RADDR[15:8]	(00000000)

Configuration Register 7 (default = 00000000)

7:0 = RADDR[7:0]	(00000000)

Configuration Register Map

Configuration Register 8 (default = 10_00_0_111)

7:6 = WIDTH[1:0]	(10: 10 bits)
5:4 = Reserved	(Make equal to 00)
3 = MARK_ACTIVE_RSET	(Make equal to 0)
2:0 = OPMODE	(111)

Configuration Register 9 (default = 00_000_000)

7:6 = TRS_SYNC[1:0]	(00: ignore embedded TRS)
5 = -------	Reserved - set to 0
4 = A_FLD	(0: frame sync - use falling F-bit from TRS)
3 = MARK_SEL	(0: use marked address - not user defined address)
2:0 = FLAG_SET	(000: trigger empty, full on 1/80, 79/80)

Configuration Register A (default = 00000000)

7 = -------	Reserved - set to 0
6 = WSET_catch	(0: setting pointer does not MARK its new value)
5 = RSET_b_sel	(0: $\overline{\text{RSET}}$ is falling edge triggered)
4 = RCLR_b_sel	(0: $\overline{\text{RCLR}}$ is falling edge triggered)
3 = -------	Reserved - set to 0
2 = -------	Reserved - set to 0
1 = WSET_b_sel	(0: $\overline{\text{WSET}}$ is falling edge triggered)
0 = WCLR_b_sel	(0: $\overline{\text{WCLR}}$ is falling edge triggered)

Configuration Register B (default = 00_00_00_00)

7:4 = -------	RESERVED
3:0 = FLAG_CTL	(00: PE, PF are part-empty, -full)

Configuration Register C (default = 0000_0000)

7:4 = BASE_ADDR	(0000: lowest-address chip in cascade sequence)
3:0 = CASCADE	(0000: single chip - no cascade of multiple chips)

Configuration Register Definitions

Register 0[3:0], Register 1[7:0] = ROW_LENGTH[11:0] - for Cartesian-to-linear address map

This control governs the remapping of Cartesian coordinates arriving on ADDR[11-0] (horizontal/column component) and ADDR[23-12] (vertical/row component) into a linear address, for use by the chip's internal address generator. Setting ROW_LENGTH to 0 causes the incoming address to be interpreted directly as a linear address, with the 24bits ADDR[23:0] address.

Register 2[7:0], Register 3[7:0], Register 4[7:0] = WADDR[23:0] - 24bit 'Jump' Address

Configuration register WADDR defines a static 24bit address (image pixel or memory location) that the Write pointer can be 'jumped' to. Bringing WSET LOW forces/jumps the memory write pointer to the address defined by WADDR (when WADRSEL is LOW). When used in this way, WADDR is an override address. For 2-D applications, where ROW_LENGTH defines a frame's Horizontal dimension, , WADDR[11:0] is equal to the 12-bit X-coordinate (Horizontal) and WADDR[23:12] is considered the Y-coordinate (Vertical) in a Cartesian Coordinate system. When ROW_LENGTH is 0, WADDR[23:0] is considered to be a linear address ~~in the~~ memory space. By changing the ROW_LENGTH, the X-coordinate can be from 0 to (ROW_LENGTH-1) to make up the Cartesian plane. For example, if ROW_LENGTH = 16, the X-coordinate or WADDR[11:0] can be from 0 to 15 in the Cartesian space.

Register 5[7:0], Register 6[7:0], Register 7[7:0] = RADDR[23:0] - 24bit 'Jump' Address

Bringing RSET LOW forces/jumps the read pointer to the address defined by RADDR.

Register 8[7:6] = WIDTH[1:0] - data word size at input/output ports

		Input Port	Output Port
0x	8 bits	D[11:4]	Q[11:4] (Q[3:0] tristated)
10	10 bits	D[11:2] (default)	Q[11:2] (Q[1:0] tristated)
11	12 bits	D[11:0]	Q[11:0]

Register 8[5:4] = Reserved

Register 8[3] = MARK_ACTIVE_RSET

0	ignores the internal RSET that occurs following the MARK
1	obeys the internal RSET according to the MARK

Configuration Register Definitions

Register 8[2:0] = OPMODE[2:0] - operating mode

000	RESERVED
001	Random Access
010	RESERVED
011	FIFO
1XX	RESERVED

Register 9[7:6] = TRS_SYNC[1:0] - response to embedded TRS EAV

00	disable TRS sync detection (default)
01	F-bit of embedded TRS EAV marks current write pointer.
10	F-bit of embedded TRS EAV sets current write pointer to value set by ADDR[23:0] or WADDR
11	RESERVED

Register 9[4] = FLD frame/field sync select

0	use only falling F-bit in EAV (frame-based sync); ignore rising F-bit (default)
1	use both rising and falling F-bit in EAV (field-based sync)

Register 9[3] MARK_SEL - This signal is used in combination with pin RADRSEL to determine to effect of bringing RSET low on the read pointer(s). When RSET goes to 0:

0	force read pointer(s) to marked address(es) (default)
1	force read pointer(s) as shown in following table:

RADRSEL	*Read Pointer Equals:*
1	ADDR[23:0] address
0	RADDR address

Configuration Register Definitions

Register 9[2:0] = FLAG_SET[2:0] - sets fractional "fullness" and "emptiness" thresholds in memory core.

Partially Full flag goes HIGH when the memory is more than "TH" full. Partially Empty flag goes HIGH when the memory is less than or equal to "TL" full.

000	TH = 79/81 (default)	TL = 1/81 (default)
001	TH = 78/81	TL = 2/81
010	TH = 77/81	TL = 3/81
011	TH = 76/81	TL = 4/81
100	TH = 75/81	TL = 5/81
101	TH = 74/81	TL = 6/81
110	TH = 73/81	TL = 7/81
111	TH = 72/81	TL = 8/81

Register A[6] = WSET_catch

0	Setting Write Pointer does not "MARK" its new value (default)
1	Setting Write Pointer auto-MARKS its new value

Register A[5:0] Control action.

Rb[5]	RSET_b_sel
Rb[4]	RCLR_b_sel
Rb[3]	WADDRSEL_b_sel
Rb[2]	RADDRSEL_b_sel
Rb[1]	WSET_b_sel
Rb[0]	WCLR_b_sel
if 0:	Each falling edge on the corresponding control pin overrides a memory address counter for exactly one clock cycle, after which normal memory address incrementing immediately resumes. (default)
if 1:	The corresponding pin continuously overrides the memory address counter as long as it is held LOW. Memory address incrementing resumes when the pin is returned HIGH.

Register B[7:4]=

-------	Reserved

Configuration Register Definitions

Register B[3:0] FLAG_CTL[3:0] for pins PE and PF *

FLAG_CTL	*PE*	*PF*	*COLLIDE*
0000	Empty (Emerging)	Full (Incoming)	COLLIDE (Emerging)
0001	------	RA=MA (Emerging)	COLLIDE (Emerging)
0010	D f (Incoming)	D v (Incoming)	D h (Incoming)
0011	Q f (Emerging)	Q v (Emerging)	Q h (Emerging)
0100	D f (Incoming)	D v (Incoming)	COLLIDE (Emerging)
0101	Q f (Emerging)	Q v (Emerging)	COLLIDE (Emerging)
0110	D f (Incoming)	D h (Incoming)	COLLIDE (Emerging)
0111	Q f (Emerging)	Q h (Emerging)	COLLIDE (Emerging)
1000	D v (Incoming)	D h (Incoming)	COLLIDE (Emerging)
1001	Q v (Emerging)	Q h (Emerging)	COLLIDE (Emerging)

**Each flag is updated on the rising edge of its associated clock: WCLK (Incoming) or RCLK (Emerging)*

D f, v, h are the TRS bits embedded in the incoming TRS signals.
Q f, v, h are the TRS bits embedded in the emerging TRS signals.
RA is the read address pointer value.
MA is the 'marked' address pointer value.

Register C[7:4] = BASE_ADDR[3:0] - position of chip in cascade series; 0000 = lowest; BASE_ADDR[3:0] must not exceed CASCADE[3:0]**

0000:	chip one of N (N is number of chips in system)
0001:	chip two of N (N is number of chips in system)
....	....
0111:	chip eight of N (N is number of chips in system)

** Note: There are two cascaded die per LF3324. Die 0 is chip 1 of 2, die 2 is chip 2 of 2.

Register C[3:0] = CASCADE[3:0] - number of chips in a system with concatenated address spaces*.

0001:	single chip operation (two die)
0011:	two chip cascade (four die)
....	....
1111:	eight chip cascade (sixteen die)

* Note limits regarding the number of possible chips, related to WIDTH control:
8bit data: 5 or less LF3324s (WIDTH = 0x)
10bit data: 6 or less LF3324s (WIDTH = 10)
12bit data: 8 or less LF3324s (WIDTH = 11)

Reserved Configuration Registers

Instruction registers D hex and above are reserved for test purposes only.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
VCC_{INT} , Internal supply voltage with respect to ground	–0.5V to + 2.0V
VCC_O, Output drivers supply voltage with respect to ground	–0.5V to + 4.0V
Signal applied to high impedance output	–0.5V to + 3.3V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Characteristic	Mode	Temperature Range	Supply Voltage
VCC_{INT}	Commerical	0°C to +70°C	1.71V ≤ Vcc ≤ 1.89V
VCC_O	Commerical	0°C to +70°C	3.00V ≤ Vcc ≤ 3.60V

Electrical Characteristics *Over Operating Conditions (Note 4)*

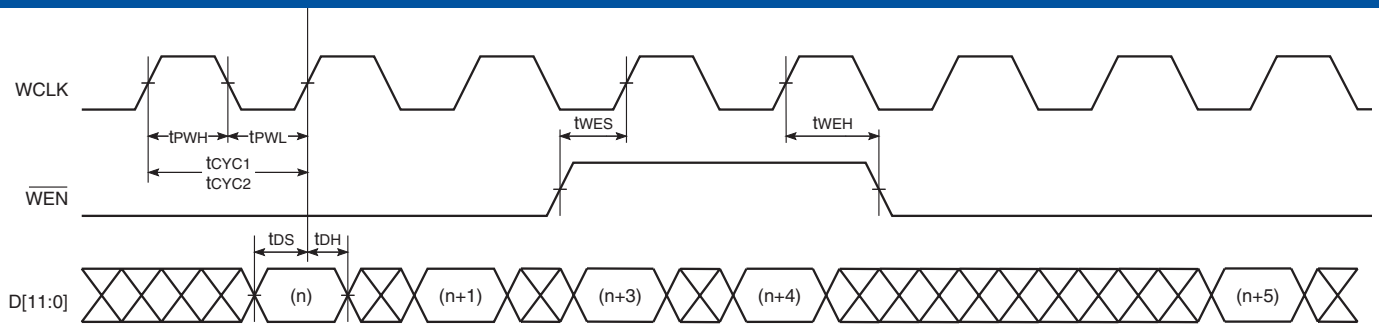
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., $I_{OH\ MAX}$ = -4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., $I_{OL\ MAX}$ = 4 mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{Ix}	Input Current	With Internal Pull-up - JTAG			+20	µA
I_{Ix}	Input Current	All other pins			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Note 5,6)			400	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			10	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			7	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			7	pF

Switching Characteristics

Commercial Operating Range (0°C to +70°C) Notes 9, 10 (ns)

		LF3324BGC			
		-			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**
t_{CYC1}	Cycle Time 1 (WCLK, RCLK) - FIFO Mode	18			
t_{CYC2}	Cycle Time 2 (WCLK, RCLK) - Full-time Random Access	18			
t_{PWH}	Clock Pulse Width High (WCLK, RCLK)	5			
t_{PWL}	Clock Pulse Width Low (WCLK, RCLK)	5			
t_{DS}	Setup Time, Data Inputs (D)	5			
t_{DH}	Hold Time, Data Inputs (D)	1			
t_{WES}	Write Enable Setup Time (WEN)	5			
t_{WEH}	Write Enable Hold Time (WEN)	1			
t_{RES}	Read Enable Setup Time (REN)	5			
t_{REH}	Read Enable Hold Time (REN)	1			
t_{LDS}	Load Setup Time	5			
t_{LDH}	Load Hold Time	1			
t_{RWS}	R/W Set/Clr Setup Time	5			
t_{RWH}	(WCLR,RADDRSEL,WSET,WADDRSEL,RSET,RCLR)	1			
t_{D}	R/W Set/Clr Hold Time		7		
t_{F}	(WCLR,RADDRSEL,WSET,WADDRSEL,RSET,RCLR)		7		
t_{DIS}	Access Time		10		
t_{ENA}	Write Clock to Programmable Flags (PE, PF, COLLIDE)		10		
t_{CSU}	Tri-state Output Disable Delay	5			
t_{CHD}	Tri-state Output Enable Delay	1			
t_{CSPW}	Parallel Interface Control Setup Time for Reads/Writes	20			
t_{CDLY}	Parallel Interface Control Hold Time for Reads/Writes		8		
t_{CZ}	Parallel Interface Control Strobe Pulse Width		10		
	Parallel Interface Control Output Delay				
	Parallel Interface Control Tristate Delay				

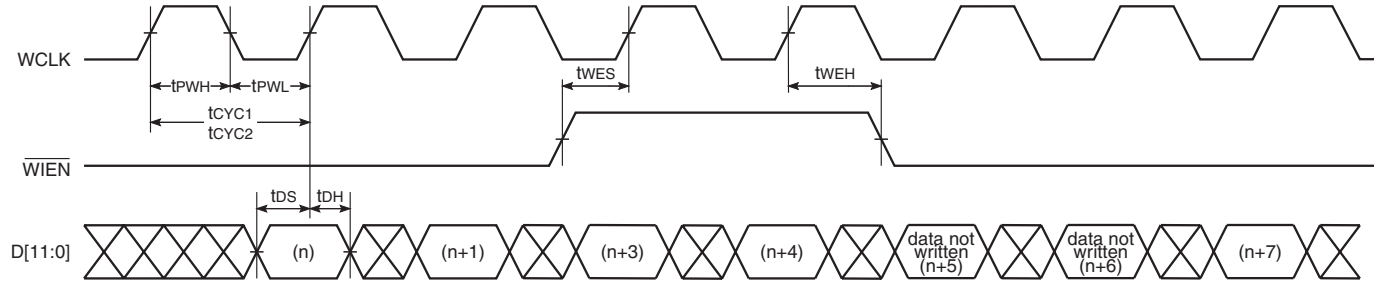
Write Cycle Timing - Write Enable



$\overline{IEN}$ = LOW

NOTE: WEN must be brought LOW 2 rising edges of WCLK prior to latching valid data on D

Write Cycle Timing - Write Masking

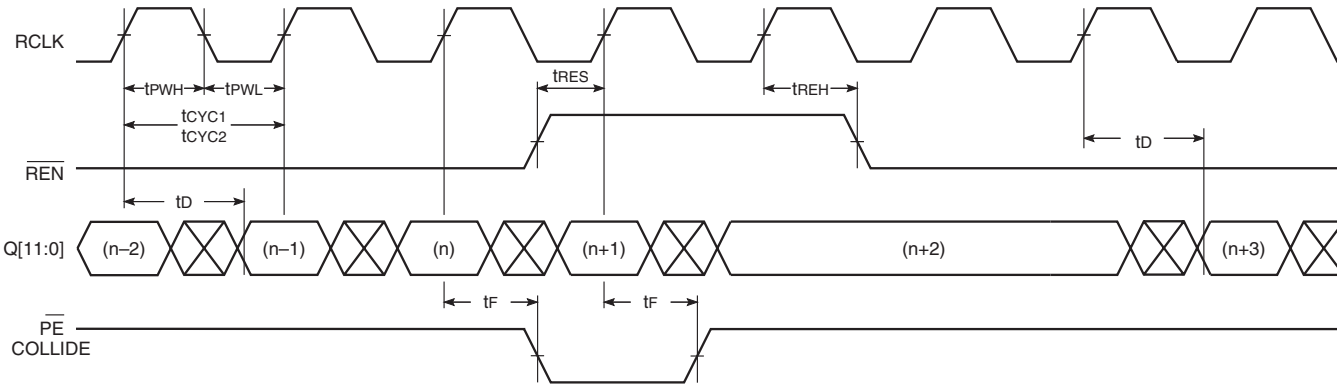


$\overline{WEN}$ = LOW

NOTE: Bringing WIEN HIGH disables data on D from being written into memory, yet it does not disable the Write pointer from incrementing

NOTE: WIEN must be brought HIGH 2 rising edges of WCLK prior to masking input data on D

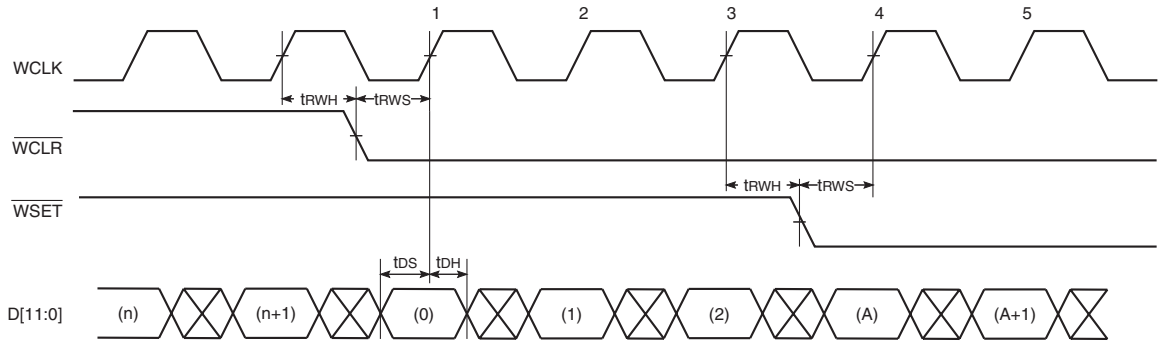
Read Cycle Timing



$\overline{OE}$ = LOW

NOTE: REN should be brought LOW 2 rising edges of RCLK prior to expecting valid data on Q

Write Reset Timing



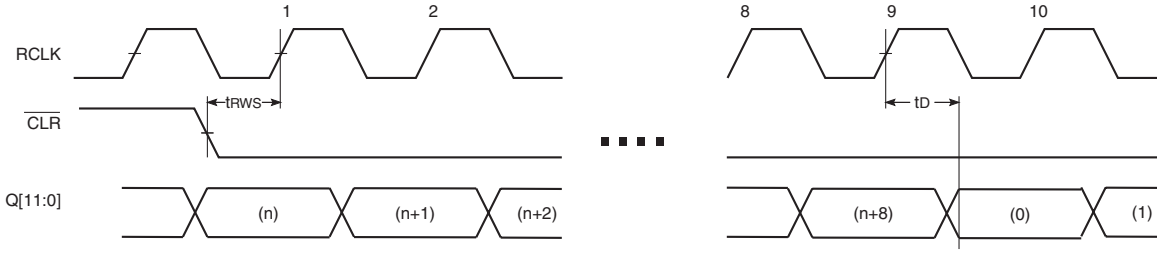
$\overline{WEN}$ = LOW

CLR and SET both programmed to be falling edge sensitive

* Rising Edge 1: Clears Write Pointer and latches data on D to be written in address 0

* Rising Edge 4: Sets Write Pointer to Address A (based on WADDR) and latches data on D to be written in Address A

Read Reset Timing

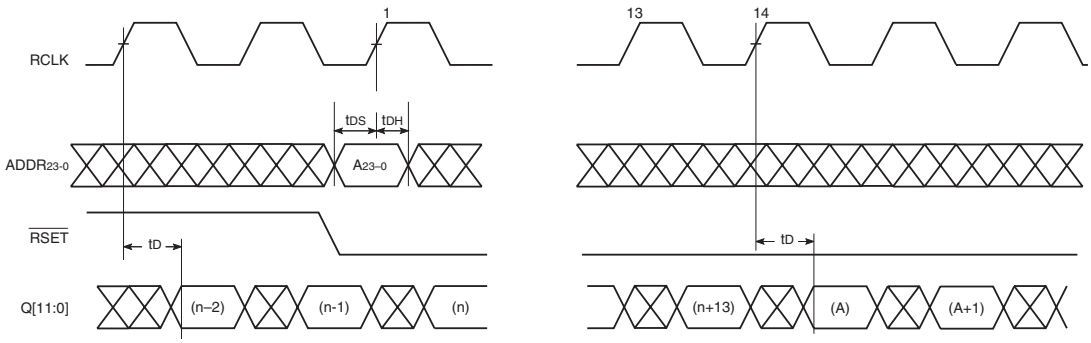


$\overline{REN}$ = LOW

NOTE: CLR programmed as being falling edge sensitive

It takes 9 REN-enabled rising edges of RCLK (including the edge that latches a LOW on CLR) to pass the contents of address 0 to the Q port.

Random Access Read Pointer 'Jump' Timing

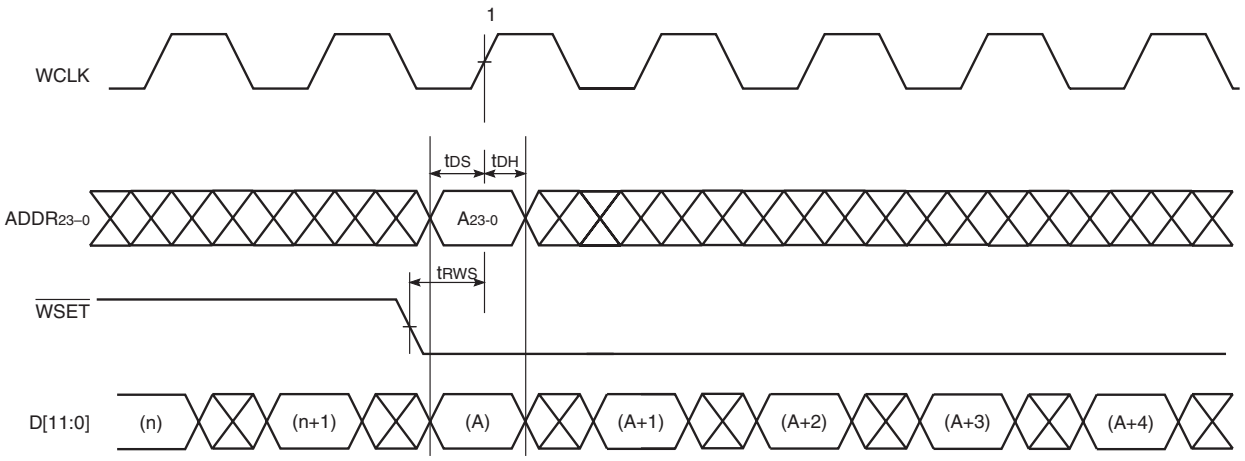


$\overline{OE}$ = LOW $\overline{REN}$ = LOW WADDRSEL= LOW RADDRSEL= HIGH OPMODE[2:0]=001 MARK_SEL (Register 9[3]) =1

NOTE: RSET programmed to be falling edge sensitive

NOTE: It takes 14 rising edges of RCLK upon setting/jumping the Read pointer
(to the 24bit Address "A" on ADDR) for the contents of location A to be dumped onto Q

Random Access Write Pointer 'Jump' Timing

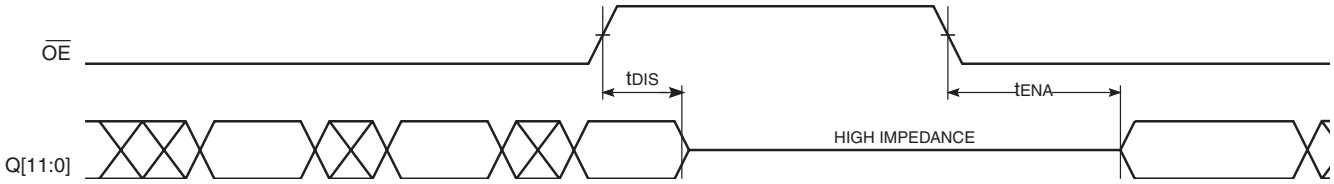


$\overline{WEN}$= LOW WADDRSEL= HIGH OPMODE[2:0]=001

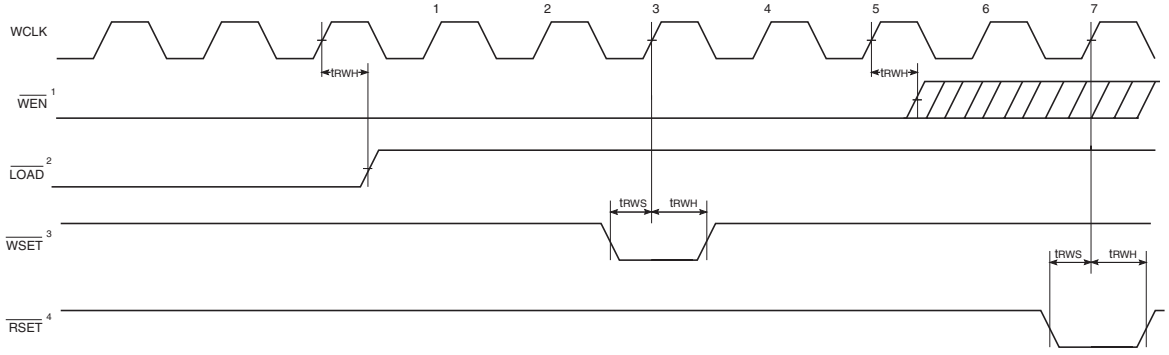
NOTE: SET programmed to be falling edge sensitive

NOTE: Rising edge of WCLK labeled "1" writes data on D to 24bit Address "A"

Output Enable and Disable



Jumping/Setting Pointers based on Configuration Register Address after Remapping Process



SET and RSET programmed to be level sensitive

[1] $\overline{WEN}$ is LOW for 3 rising edges of WCLK prior to LOAD transition. It stays LOW for the minimum required 5 rising edges after the LOAD transition.

[2] The configuration registers are programmed while LOAD is LOW. The LOAD transition triggers the address remap process.

[3] WSET can be brought LOW (edge "3") 3 rising edges of WCLK after the LOAD transition, jumping the write pointer to the address programmed into the WADR register.

[4] RSET can be brought LOW (edge "7") 7 rising edges of RCLK after the LOAD transition, jumping the read pointer to the address programmed into the RADDR register.

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6V. The device can withstand operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels may be in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be approximated by:

where $\frac{NCV^2F}{2}$

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 50 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, and no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{dis} test), and input levels of nominally 0 to 3.0V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current change pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the device as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the device leads.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required input levels relative to the device ground pin.

Notes

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ena} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{dis} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{th}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

Figure A. Output Loading Circuit

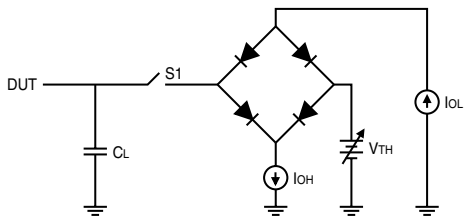
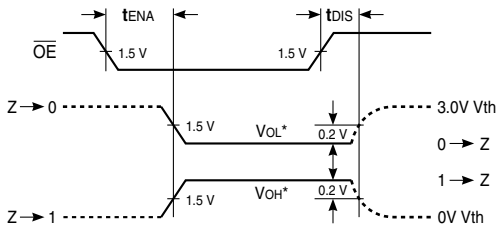
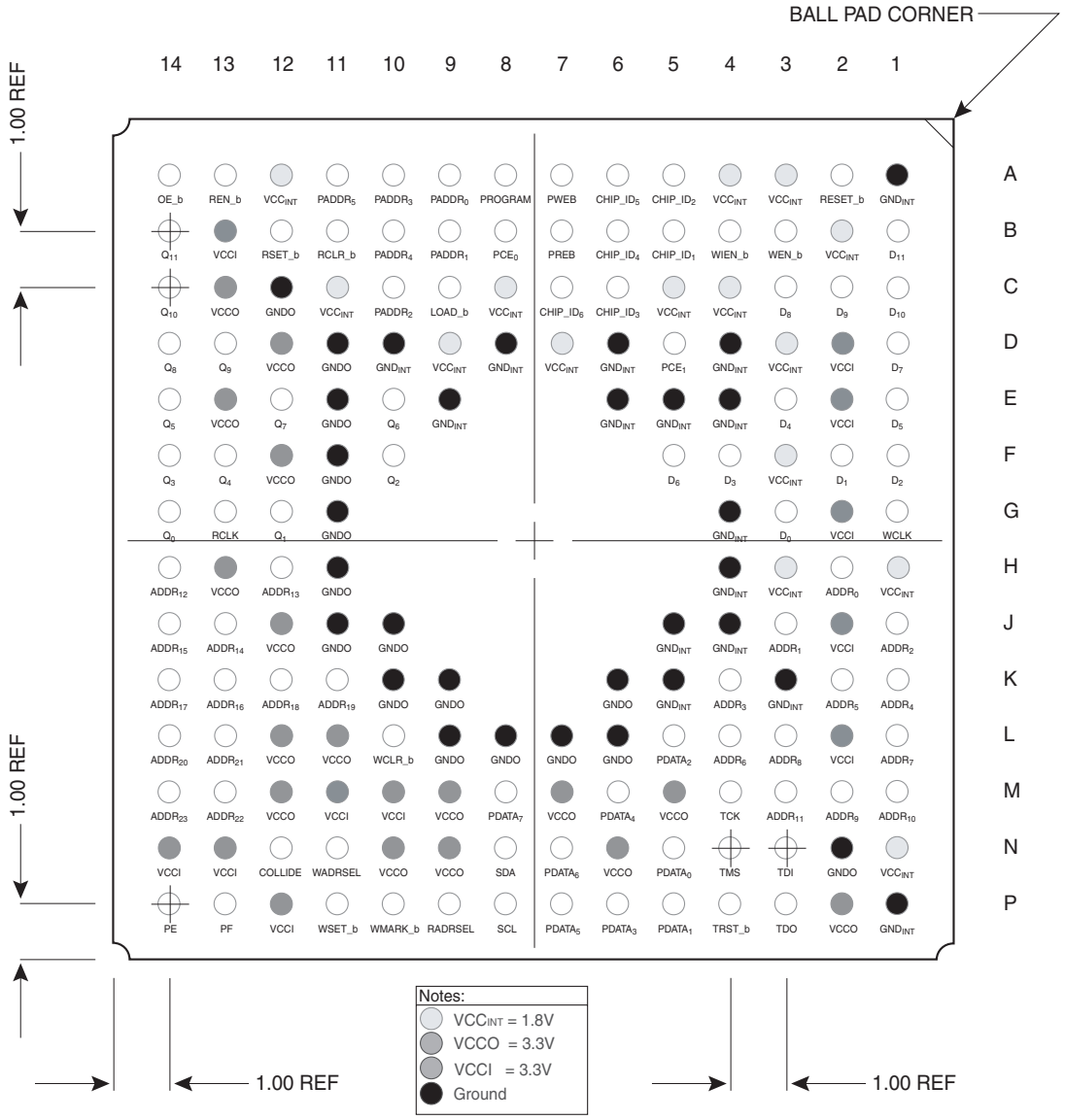


Figure B. Threshold Levels



VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

Package and Ordering Information



172 Ball - Low Profile Ball Grid Array (LBGA)

0°C to 70°C--Commercial Screening

Speed	
_	LF3324BGC

Document History Page

DOCUMENT TITLE: LF3324 24MBIT FRAME BUFFER / FIFO			
Rev.	ECN NO.	Issue Date	Description of Change
A		03/08/05	Initiate
B		03/28/05	Downgraded part speed from 12ns to 13.5ns
C		04/07/05	Upgraded Speed from 13.5ns to 13.4ns Fixed incorrect description of the program pin on page 14 Added data rate
D		08/18/05	Clarified Programmable FLAG operation text
E		09/14/05	Clarified FIFO operation text
F		07/7/06	Downgraded speed in full-time Random Access to 54MHz
G		06/08/07	Downgraded speed in FIFO Mode to 54MHz