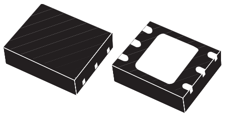
LD39050xx

500 mA low quiescent current
low noise voltage regulator

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low dropout voltage (200 mV typ. at 500 mA load)
- Very low quiescent current (20 µA typ. at no load, 100 µA typ. at 500 mA load, 1 µA max in off mode)
- Very low noise without bypass capacitor
- Output voltage tolerance: ± 2.0 % @ 25 °C
- 500 mA guaranteed output current
- Wide range of output voltages available on request: 0.8 V to 4.5 V with 100 mV step and ADJ from 0.8 V
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor $C_{OUT} = 1$ µF
- Internal current and thermal limit
- Package DFN6 (3 x 3 mm)
- Temperature range: -40 °C to 125 °C



DFN6 (3 x 3 mm)

Description

The LD39050 provides 500 mA maximum current from an input voltage ranging from 1.5 V to 5.5 V with a typical dropout voltage of 200 mV. Stability is provided using ceramic capacitors. The ultra low drop-voltage, low quiescent current and low noise features make it suitable for low power battery-powered applications. Power supply rejection is 65 dB at low frequencies and starts to roll off at 10 kHz. An Enable logic control function puts the LD39050 in shut-down mode allowing a total current consumption lower than 1 µA. The device also includes short-circuit constant current limiting and thermal protection. Typical applications are mobile phones, personal digital assistants (PDAs), cordless phones and similar battery-powered systems.

Table 1. Device summary

Part numbers	Order codes	Output voltages
LD39050XX	LD39050PUR	ADJ from 0.8 V
LD39050XX10	LD39050PU10R	1.0 V
LD39050XX12	LD39050PU12R	1.2 V
LD39050XX25	LD39050PU25R	2.5 V
LD39050XX33	LD39050PU33R	3.3 V

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1 Diagrams

Figure 1. Schematic diagram for the LD39050PU

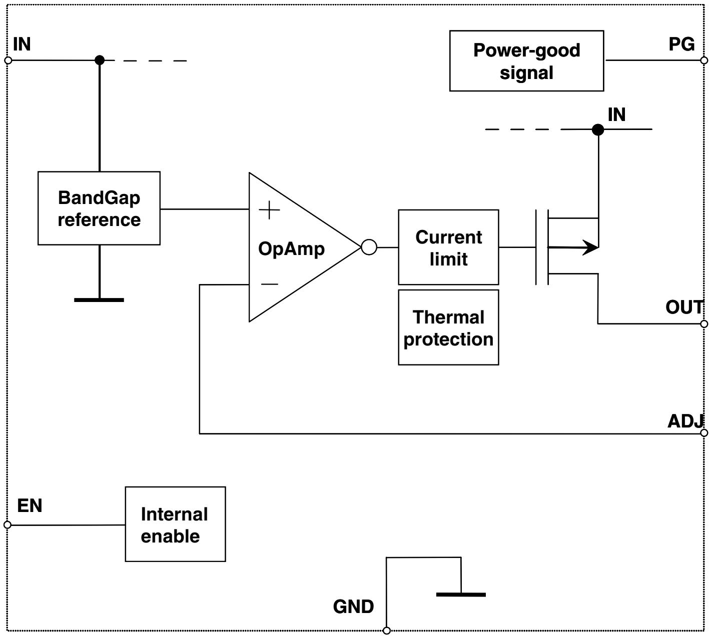
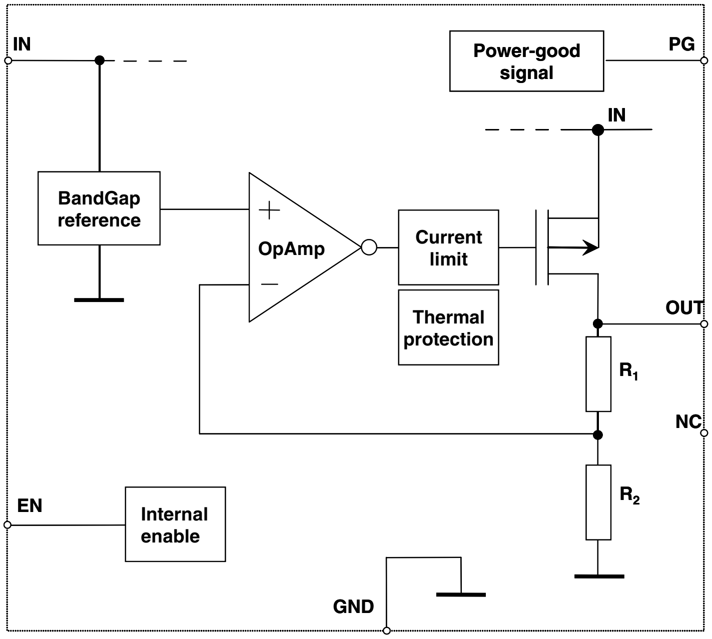
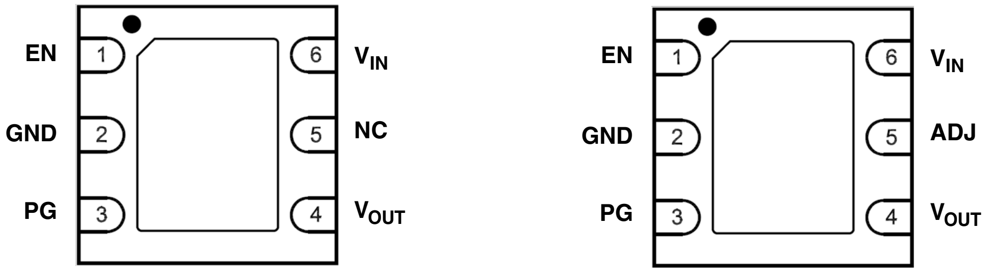

IN
Power-good signal
PG
IN
BandGap reference
+
OpAmp
–
Current limit
Thermal protection
OUT
ADJ
EN
Internal enable
GND

Figure 2. Schematic diagram for the LD39050PUxx


IN
Power-good signal
PG
IN
BandGap reference
+
OpAmp
–
Current limit
Thermal protection
OUT
R_1
NC
R_2
EN
Internal enable
GND

2 Pin configuration

Figure 3. Pin connection (top view)


EN
GND
PG
1
2
3
6
5
4
V_{IN}
NC
V_{OUT}
EN
GND
PG
1
2
3
6
5
4
V_{IN}
ADJ
V_{OUT}

LD39050PUxx LD39050PU

Table 2. Pin description

Symbol	Pin n°		Function
	LD39050PU	LD39050PUxx	
EN	1	1	Enable pin logic input: Low=shutdown, High=active
GND	2	2	Common ground
PG	3	3	Power Good
V_{OUT}	4	4	Output voltage
ADJ	5	-	Adjust pin
V_{IN}	6	6	Input voltage of the LDO
NC	-	5	Not connected
GND	EXP pad		Exposed pad must be connected to GND

3 Maximum ratings

Table 3. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	-0.3 to 7	V
V_{OUT}	DC output voltage	-0.3 to V_I + 0.3 (7 V max)	V
EN	Enable pin	-0.3 to V_I + 0.3 (7 V max)	V
PG	Power Good pin	-0.3 to 7	V
ADJ	Adjust pin	4	V
I_{OUT}	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. **Thermal data**

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W
R_{thJC}	Thermal resistance junction-case	10	°C/W

Table 5. **ESD performance**

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		MM	0.3	kV

4 Electrical characteristics

T_J = 25 °C, V_{IN} = 1.8 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 10 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 6. Electrical characteristics for the LD39050PU

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{ADJ}	V_{ADJ} accuracy	I_{OUT} =10 mA, T_J = 25°C	784	800	816	mV
		I_{OUT} = 10 mA, -40°C<T_J<125°C	776	800	824	
I_{ADJ}	Adjust pin current				1	µA
ΔV_{OUT}	Static line regulation	V_{OUT} +1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (1)	ΔV_{IN}=500 mV, I_{OUT}=10 mA, t_R=5 µs		10		mVpp
		ΔV_{IN}=500 mV, I_{OUT}=10 mA, t_F=5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 500 mA		0.002		%/mA
ΔV_{OUT}	Transient load regulation (1)	I_{OUT} = 10 mA to 500 mA, t_R=5µs		40		mVpp
		I_{OUT} = 10 mA to 500 mA, t_F=5µs		40		
V_{DROP}	Dropout voltage (2)	I_O = 500mA, V_{OUT} fixed to 1.5V 40°C<T_J<125°C		200	400	mV
e_N	Output noise voltage	10Hz to 100kHz, I_{OUT} = 100 mA, V_{OUT} = 0.8 V		30		μV_{RMS}
SVR	Supply voltage rejection V_{OUT} = 0.8V	V_{IN} = 1.8V+/-V_{RIPPLE} V_{RIPPLE} = 0.25V, freq. = 1kHz I_{OUT} = 10 mA		65		dB
		V_{IN} = 1.8V+/-V_{RIPPLE} V_{RIPPLE} = 0.25V, freq.=10 kHz I_{OUT} = 100 mA		62		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT}= 0 mA, -40°C<T_J<125°C			50	
		I_{OUT} = 0 to 500mA		100		
		I_{OUT}=0 to 500mA, -40°C<T_J<125°C			200	
		V_{IN} input current in off mode: V_{EN} = GND(3)		0.001	1	
PG	Power Good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power Good output voltage low	Isink=6mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L=0	600	800		mA

Table 6. Electrical characteristics for the LD39050PU (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{EN}	Enable input logic low	V_{IN}=1.5 V to 5.5 V, 40°C<T_J<125°C			0.4	V
	Enable input logic high	V_{IN}=1.5 V to 5.5 V, 40°C<T_J<125°C	0.9			V
I_{EN}	Enable pin input current	V_{EN}= V_{IN}		0.1	100	nA
t_{ON}	Turn on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see typical performance characteristics for stability)	1		22	µF

1. All transient values are guaranteed by design, not production tested
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V
3. PG pin floating
4. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 10 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 7. Electrical characteristics for the LD39050PUxx

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	V_{OUT} >1.5V, I_{OUT} =10 mA, T_J = 25°C	-2.0		2.0	%
		V_{OUT} >1.5 V, I_{OUT} = 10 mA, -40°C<T_J<125°C	-3.0		3.0	
		$V_{OUT} \leq$ 1.5 V, I_{OUT} = 10 mA		±20		mV
		$V_{OUT} \leq$ 1.5 V, I_{OUT} =10 mA, -40°C<T_J<125°C		±30		
ΔV_{OUT}	Static line regulation	V_{OUT} +1 V $\leq V_{IN} \leq$ 5.5 V, I_{OUT} = 1 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (1)	ΔV_{IN}=500 mV, I_{OUT}=10 mA, t_R=5 µs		10		mVpp
		ΔV_{IN}=500 mV, I_{OUT}=10 mA, t_F=5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 500 mA		0.002		%/mA
ΔV_{OUT}	Transient load regulation (1)	I_{OUT} = 10 mA to 500 mA, t_R=5µs		40		mVpp
		I_{OUT} = 10 mA to 500 mA, t_F=5µs		40		
V_{DROP}	Dropout voltage (2)	I_{OUT} = 500mA, V_{OUT} > 1.5 V -40°C<T_J<125°C		200	400	mV
e_N	Output noise voltage	10Hz to 100kHz, I_O = 100 mA,		30		μV_{RMS}
SVR	Supply voltage rejection V_{OUT} = 1.5V	V_{IN} = $V_{OUT(NOM)}$+0.5V+/-V_{RIPPLE} V_{RIPPLE} = 0.1V, freq. = 1kHz I_{OUT} = 10 mA		65		dB
		V_{IN} = $V_{OUT(NOM)}$+0.5V+/-V_{RIPPLE} V_{RIPPLE} = 0.1V, freq.=10 kHz I_{OUT} = 100 mA		62		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA, -40°C<T_J<125°C			50	
		I_{OUT} = 0 to 500mA		100		
		I_{OUT} = 0 to 500mA -40°C<T_J<125°C			200	
		V_{IN} input current in off mode: V_{EN} = GND (3)		0.001	1	
PG	Power Good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power Good output voltage low	Isink=6mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L=0	600	800		mA

Table 7. Electrical characteristics for the LD39050PUxx (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{EN}	Enable input logic low	V_{IN}=1.5 V to 5.5 V, -40°C<T_J<125°C			0.4	V
	Enable input logic high	V_{IN}=1.5 V to 5.5 V, -40°C<T_J<125°C	0.9			V
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$		0.1	100	nA
t_{ON}	Turn on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see typical performance characteristics for stability)	1		22	µF

1. All transient values are guaranteed by design, not production tested
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V
3. PG pin floating
4. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95 % of its nominal value

5 Typical performance characteristics

Figure 4. V_{ADJ} accuracy

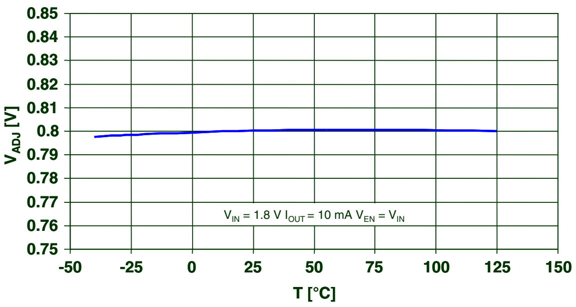


Figure 5. V_{OUT} accuracy

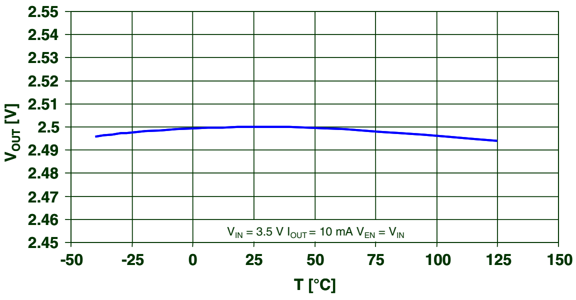


Figure 6. Dropout voltage vs. temperature

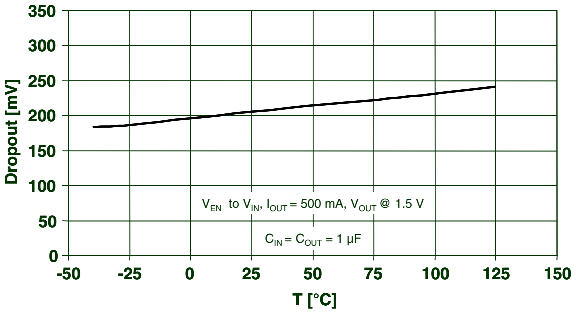


Figure 7. Dropout voltage vs. temperature

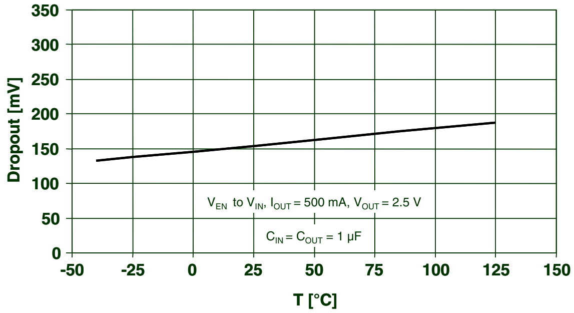


Figure 8. Dropout voltage vs. output current

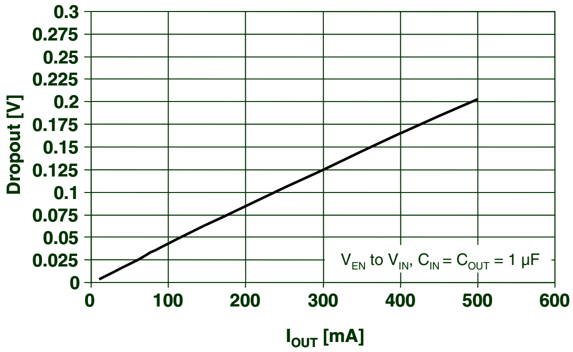


Figure 9. Short-circuit current vs. dropout voltage

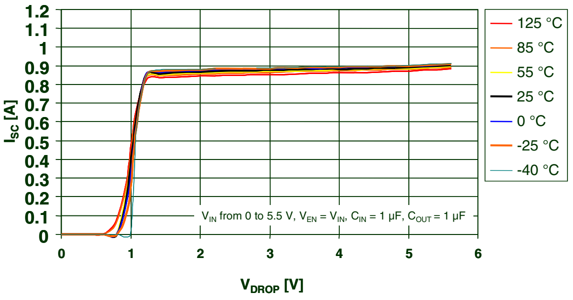


Figure 10. Output voltage vs. input voltage

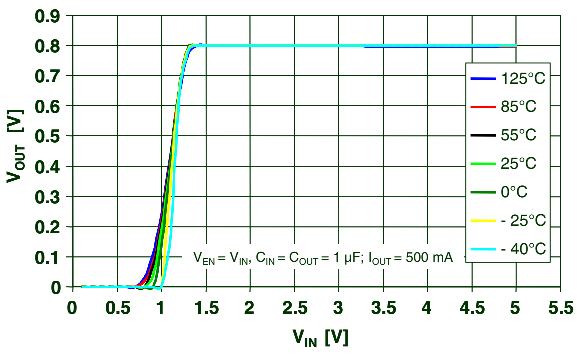


Figure 11. Quiescent current vs. temperature

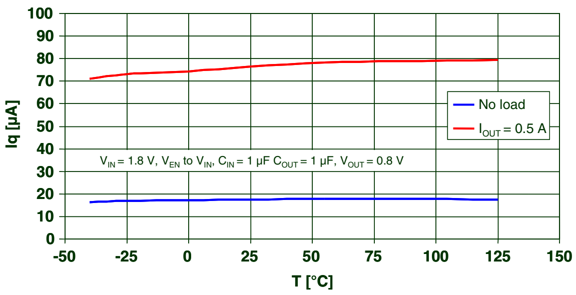


Figure 12. Quiescent current vs. temperature

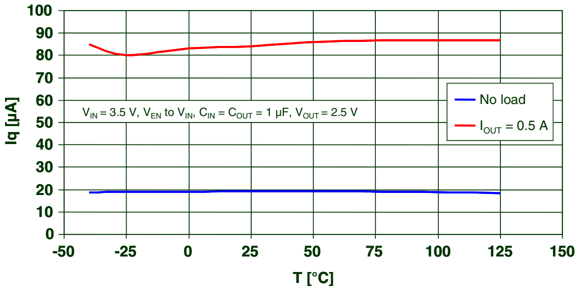


Figure 13. Quiescent current in off mode vs. temperature

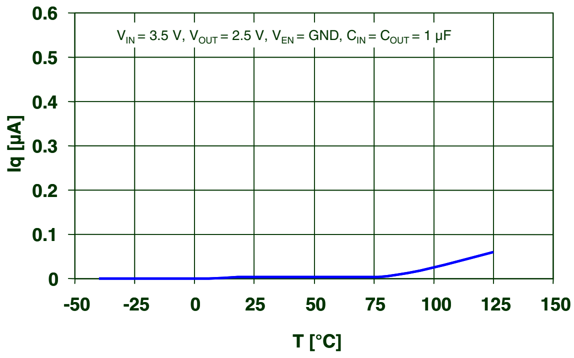


Figure 14. Load regulation

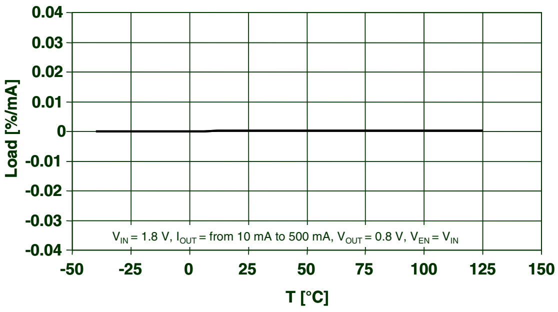


Figure 15. Line regulation

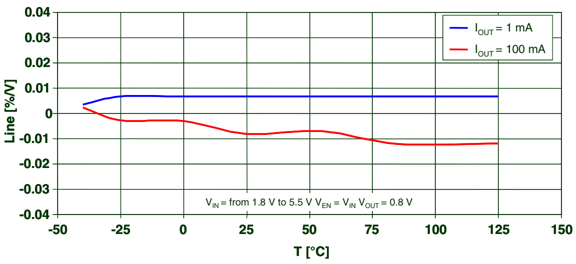


Figure 16. Line regulation

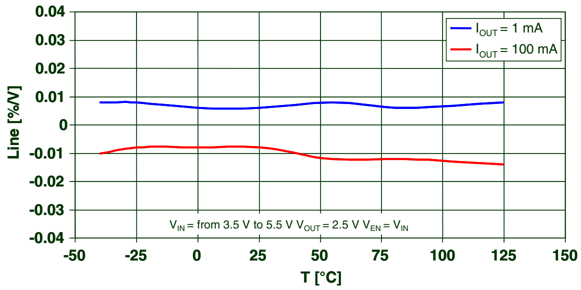


Figure 17. Supply voltage rejection vs. temperature

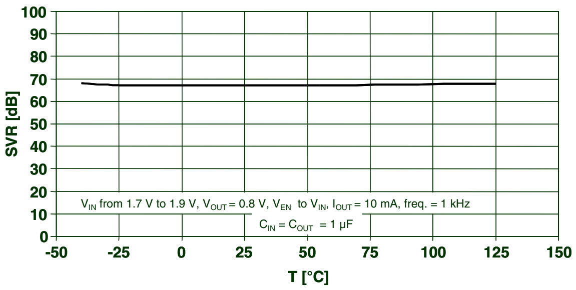


Figure 18. Supply voltage rejection vs. temperature

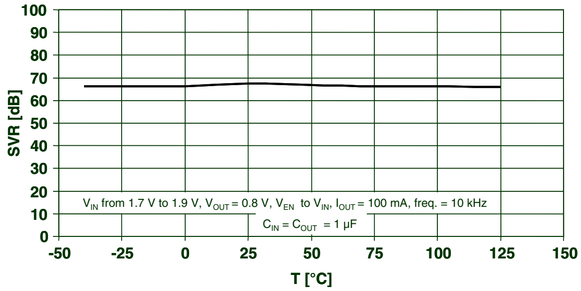


Figure 19. Supply voltage rejection vs. temperature

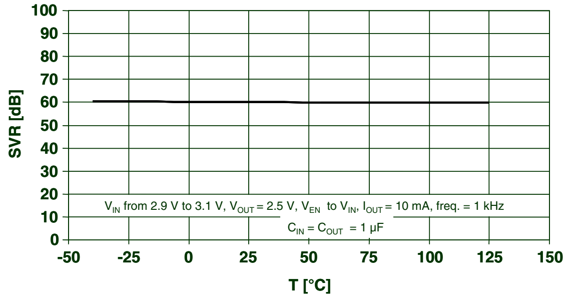


Figure 20. Supply voltage rejection vs. temperature

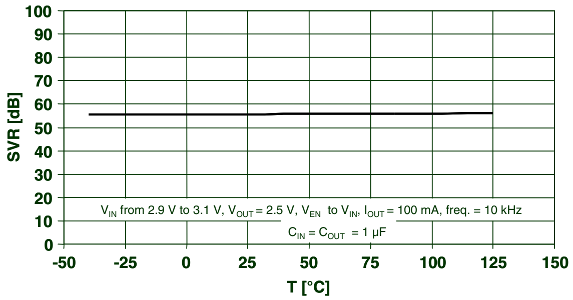


Figure 21. Supply voltage rejection vs. frequency

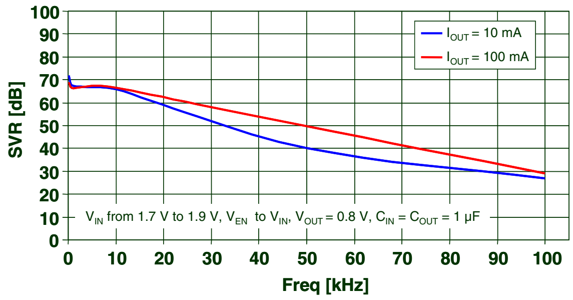


Figure 22. Supply voltage rejection vs. frequency

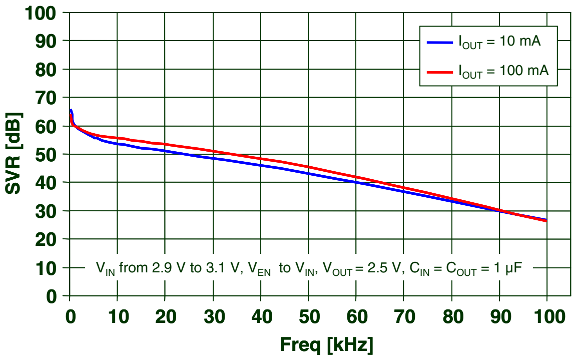
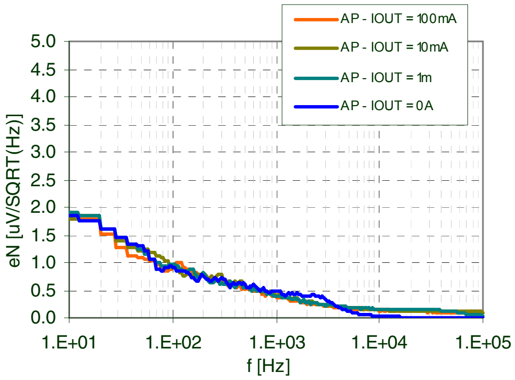


Figure 23. Noise output voltage vs. frequency



V_{IN} = 1.8 V, V_{OUT} = 0.8 V, V_{EN} = 1 V, C_{IN} = C_{OUT} = 1 µF, T_A = 25 °C

Figure 24. Enable voltage vs. temperature

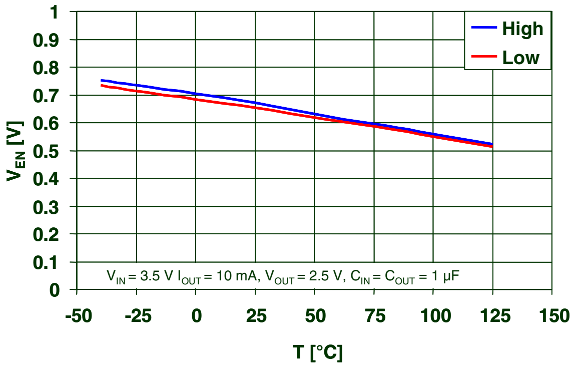


Figure 25. Enable voltage vs. temperature

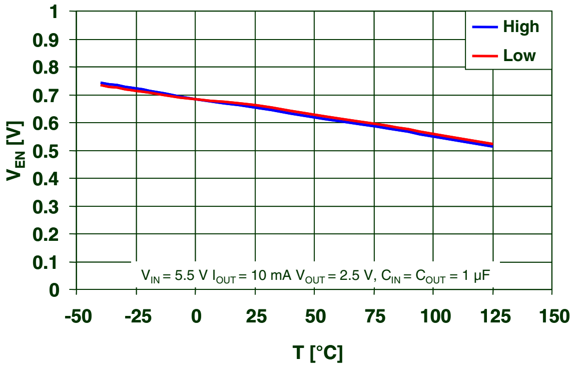
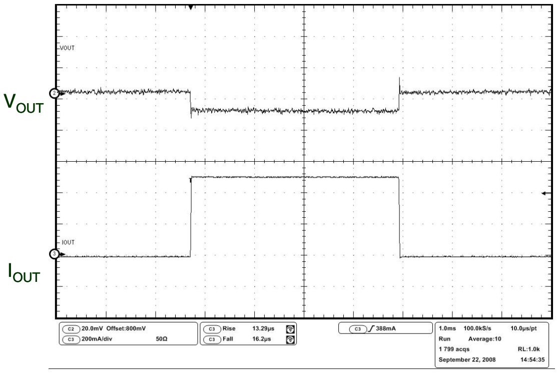
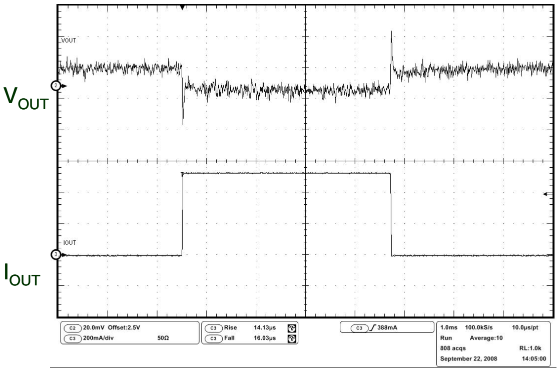


Figure 26. Load transient



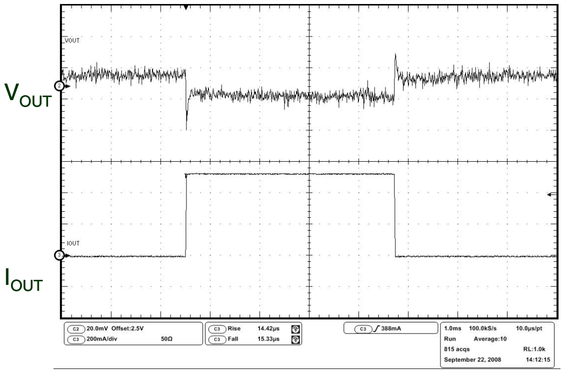
V_{EN} = V_{IN}=1.8 V, I_{OUT} = from10 mA to 0.5 A, C_{IN} = C_{OUT} = 1 µF, V_{OUT} = 0.8 V

Figure 27. Load transient



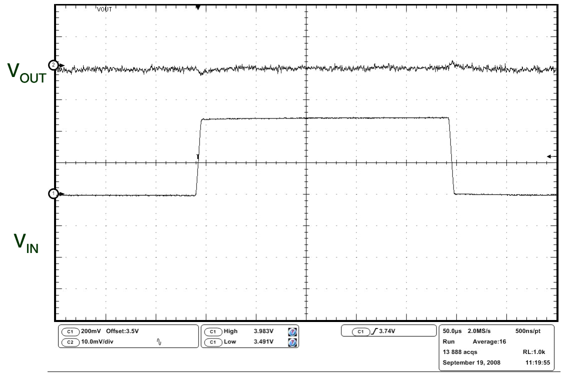
V_{EN} = V_{IN} = 3.5V, I_{OUT} from 10 mA to 0.5 A, V_{OUT} = 2.5 V, C_{IN} = C_{OUT} = 1 µF

Figure 28. Load transient



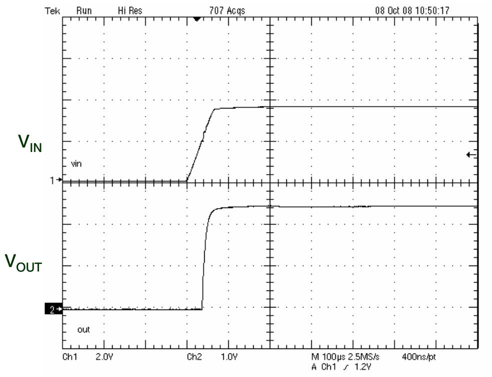
$V_{EN} = V_{IN} = 3.5$ V, I_{OUT} from 100 mA to 0.5 A, $V_{OUT} = 2.5$ V, $C_{IN} = C_{OUT} = 1$ µF

Figure 29. Line transient



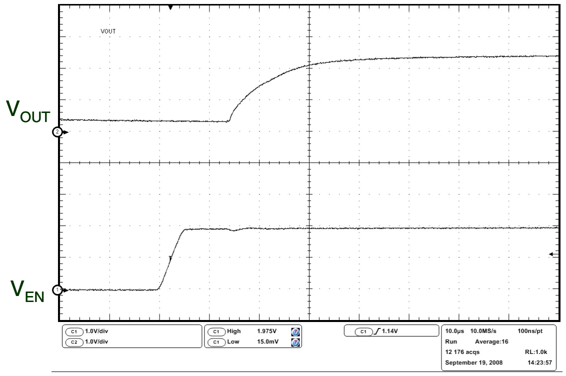
$V_{EN} = V_{IN}$ from 4.3 V to 4.8 V, $I_{OUT} = 10$ mA, $C_{OUT} = 1$ µF, C_{IN} = NO

Figure 30. Startup transient



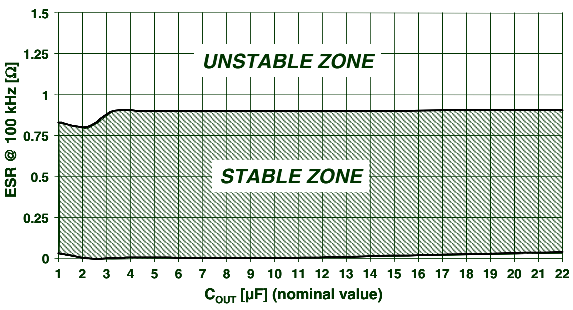
$V_{EN} = V_{IN}$ = from 0 V to 5.5 V, I_{OUT}=10 mA, $C_{IN} = C_{OUT} = 1$ µF, $V_{OUT} = 2.5$ V

Figure 31. Enable transient



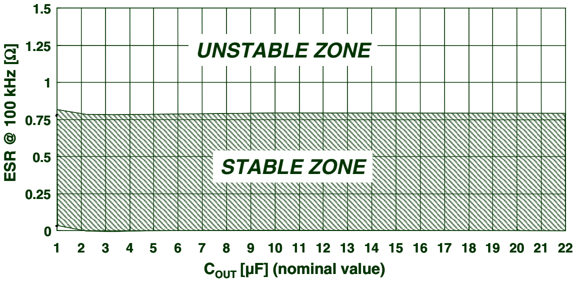
V_{EN} from 0 V to 2 V, $V_{IN} = 3.5$ V, $V_{OUT} = 2.5$ V, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 1$µF

Figure 32. ESR required for stability with ceramic capacitors



$V_{IN} = V_{EN}$ = from 1.8 V to 5.5 V, I_{OUT} = from 1 mA to 500 mA, $V_{OUT} = 0.8$ V, $C_{IN} = 1$ µF

Figure 33. ESR required for stability with ceramic capacitors



$V_{IN} = V_{EN}$ = from 3.5 V to 5.5 V, I_{OUT} = from 1 mA to 500 mA, $V_{OUT} = 2.5$ V, $C_{IN} = 1$ µF

6 Application information

The LD39050 is an ultra low dropout linear regulator. It provides up to 500 mA with a low 200 mV dropout. The input voltage range is from 1.5 V to 5.5 V. The device is available in fixed and adjustable output versions.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

The regulator is designed to be stable with ceramic capacitors on the input and the output. The expected values of the input and output ceramic capacitors are from 1 µF to 22 µF with 1 µF typical. The input capacitor must be connected within 0.5 inches of the V_{IN} terminal. The output capacitor must also be connected within 0.5 inches of output pin. There is no upper limit to the value of the input capacitor.

Figure 34 and *Figure 35* illustrate the typical application schematics:

Figure 34. Application schematic for fixed version

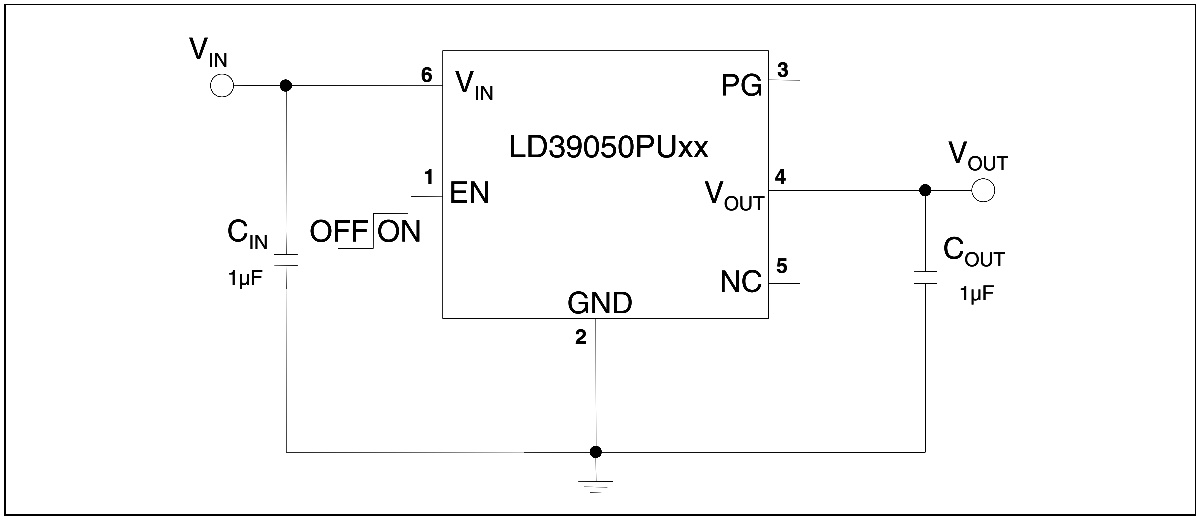
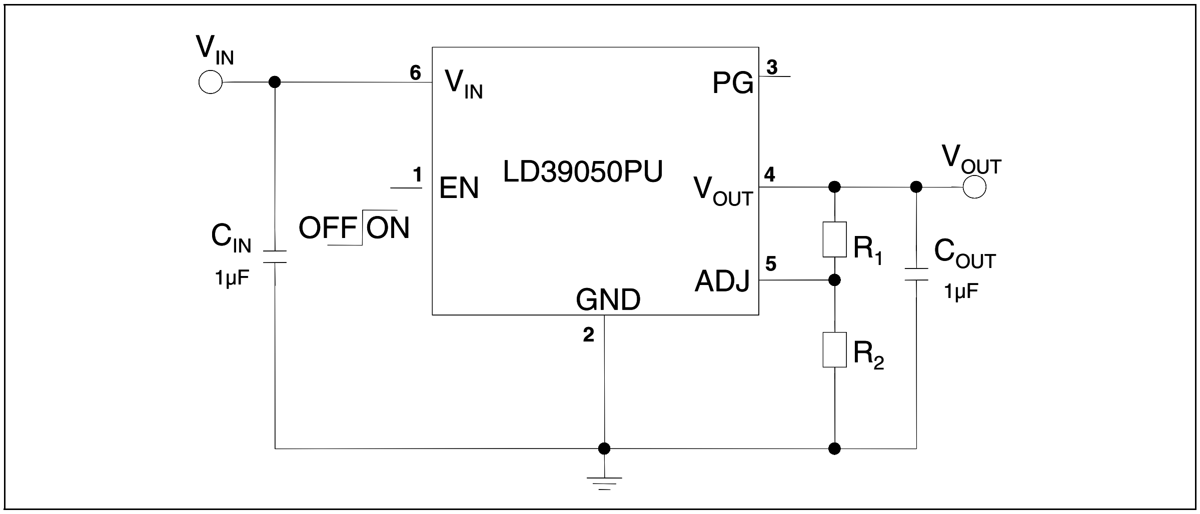

VIN
6
VIN
PG
3
LD39050PUxx
VOUT
1
EN
4
VOUT
CIN
1µF
OFF ON
COUT
1µF
5
NC
GND
2

Figure 35. Application schematic for adjustable version


VIN
6
VIN
PG
3
LD39050PU
1
EN
VOUT
4
VOUT
CIN
1µF
OFF ON
R1
COUT
1µF
5
ADJ
GND
2
R2

For the adjustable version, the output voltage can be adjusted from 0.8 V up to the input voltage minus the voltage drop across the PMOS (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider should be selected using the following equation:

$V_{OUT} = V_{ADJ} (1 + R_1 / R_2)$ with $V_{ADJ} = 0.8$ V (typ.)

It is recommended to use resistors with values in the range of 10 kΩ to 50 kΩ. Lower values can also be suitable, but will increase current consumption.

6.1 Power dissipation

An internal thermal feedback loop disables the output voltage if the die temperature rises to approximately 160 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device.

It is very important to use a good PC board layout to maximize power dissipation. The thermal path for the heat generated by the device is from the die to the copper lead frame through the package leads and exposed pad to the PC board copper. The PC board copper acts as a heat sink. The footprint copper pads should be as wide as possible to spread and dissipate the heat to the surrounding ambient. Feed-through vias to inner or backside copper layers are also useful in improving the overall thermal performance of the device.

The power dissipation of the device depends on the input voltage, output voltage and output current, and is given by:

$P_D = (V_{IN} - V_{OUT}) I_{OUT}$

The junction temperature of the device is:

$T_{J\_MAX} = T_A + R_{thJA} \times P_D$

where:

T_{J_MAX} is the maximum junction of the die,125 °C;

T_A is the ambient temperature;

R_{thJA} is the thermal resistance junction-to-ambient.

6.2 Enable function

The LD39050 features an enable function. When the EN voltage is higher than 2 V the device is ON, and if it is lower than 0.8 V the device is OFF. In shutdown mode, consumption is lower than 1 µA.

The EN pin does not have an internal pull-up, which means that it cannot be left floating if it is not used.

6.3 Power Good function

Most applications require a flag showing that the output voltage is in the correct range.

The Power Good threshold depends on the adjust voltage. When the adjust is higher than 0.92^*V_{ADJ}, the Power Good (PG) pin goes to high impedance. If the adjust is below

$0.80*V_{ADJ}$ the PG pin goes to low impedance. If the device is functioning well, the Power Good pin is at high impedance. If the output voltage is fixed using an external or internal resistor divider, the Power Good threshold is $0.92*V_{OUT}$.

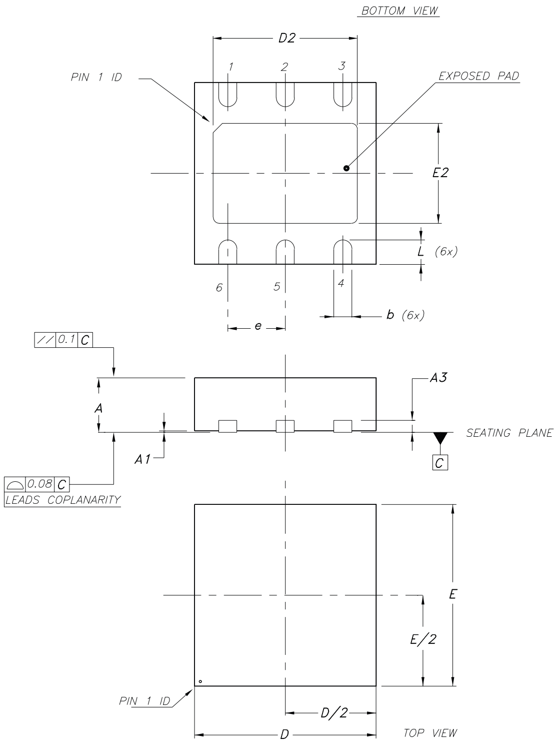
The use of the Power Good function requires an external pull-up resistor, which must be connected between the PG pin and V_{IN} or V_{OUT}. The typical current capability of the PG pin is up to 6 mA. The use of a pull-up resistor for PG in the range of 100 kΩ to 1 MΩ is recommended. If the Power Good function is not used, the PG pin must remain floating.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

DFN6 (3x3 mm) mechanical data

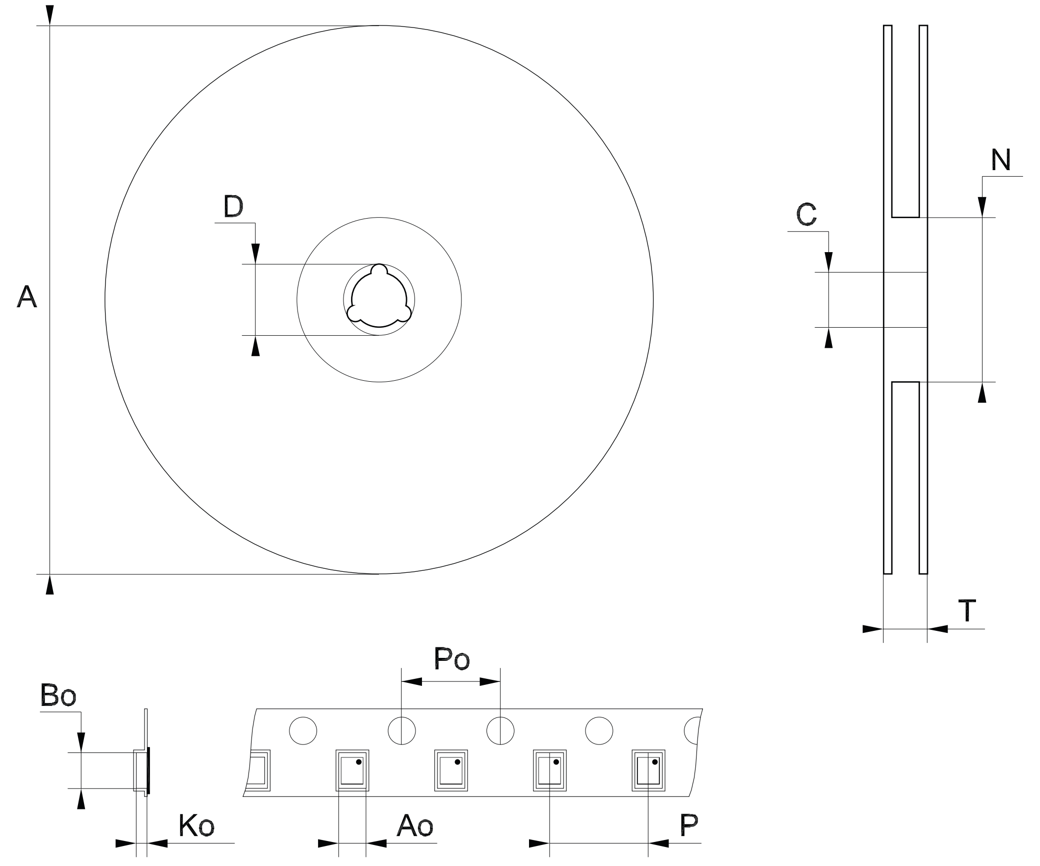
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23	0.30	0.38	0.009	0.012	0.015
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23	2.38	2.48	0.088	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50	1.65	1.75	0.059	0.065	0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020


BOTTOM VIEW
D2
1
2
3
PIN 1 ID
EXPOSED PAD
E2
L (6x)
6
5
4
b (6x)
e
0.1 C
A3
A
SEATING PLANE
C
A1
0.08 C
LEADS COPLANARITY
E
E/2
PIN 1 ID
D/2
D
TOP VIEW

7946637A

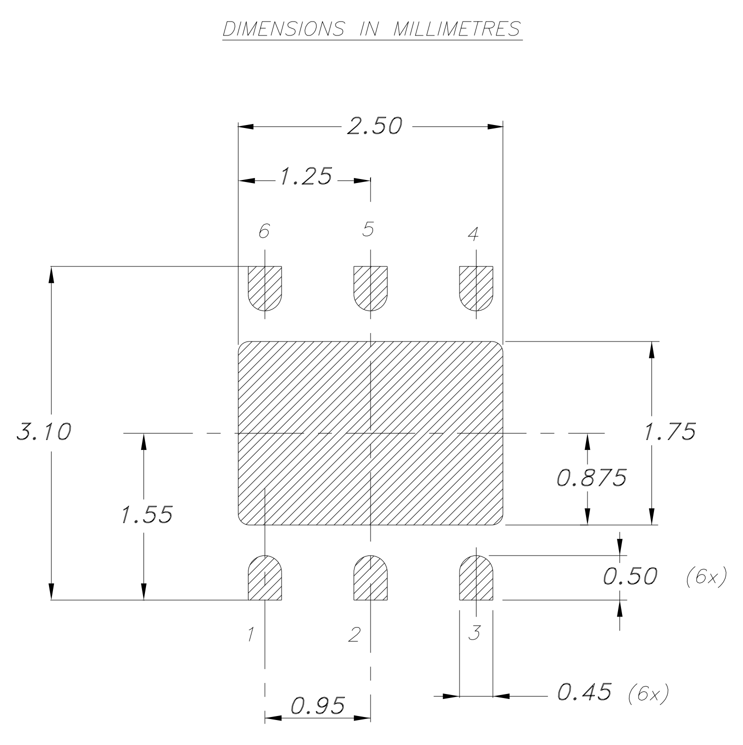
Tape & reel QFNxx/DFNxx (3x3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 36. DFN6 (3x3) footprint recommended data


DIMENSIONS IN MILLIMETRES
2.50
1.25
6
5
4
3.10
1.75
0.875
1.55
0.50 (6x)
1
2
3
0.95
0.45 (6x)

8 Different output voltage versions of the LD39050xx available on request

Table 8. Options available on request

Order codes	Output voltages
LD39050PU105R	1.05 V
LD39050PU15R	1.5 V
LD39050PU18R	1.8 V

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Mar-2009	1	Initial release.

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