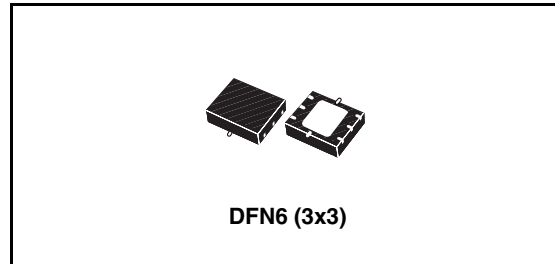


Feature summary

- Input voltage from 1.7 to 3.6V
- Ultra low dropout voltage (130mV typ. at 300mA load)
- Very low quiescent current (110µA typ. at no load, 130µA max. at 300mA load; max 0.5µA in OFF MODE)
- Output voltage tolerance: +/- 1.0% @ 25°C, +/- 2.0% full temperature range
- Guaranteed output current up to 300mA
- Wide range of output voltage: 0.8V to 3.0V
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor $C_O = 1\mu\text{F}$
- Internal current and thermal limit
- Temperature range: -40°C to 85°C

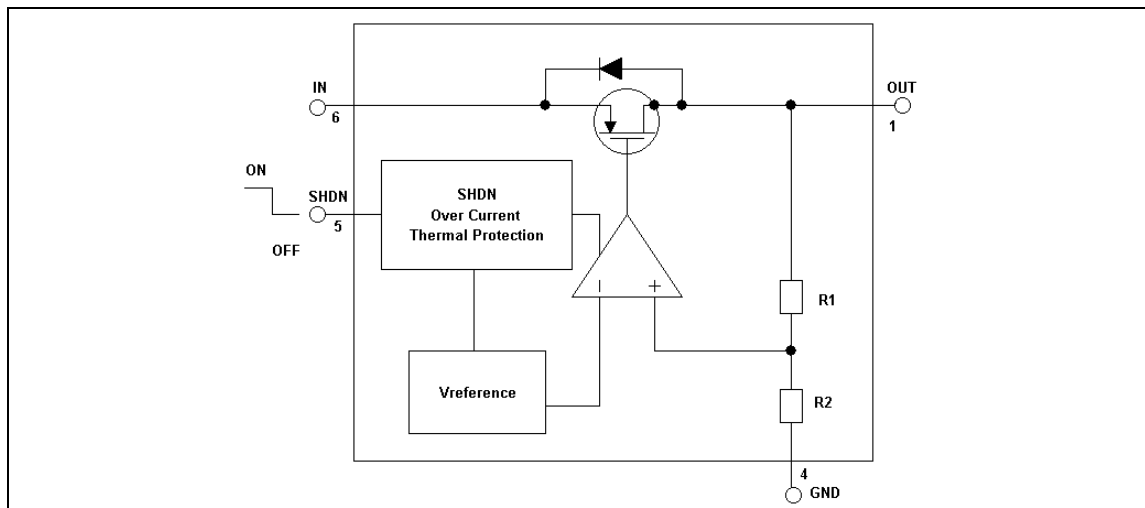


ultra low drop-voltage, low quiescent current and low noise makes it suitable for low power applications and in battery powered systems. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits. Shutdown Logic Control function is available this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The device also includes a constant current limiting and thermal overload protection. Typical applications are in mobile phone, personal digital assistant (PDAs), cordless phone and similar battery powered wireless systems, portable information appliances..

Description

The LD3980 provides up to 300mA, from 1.7V to 3.6V input voltage. It can deliver a guaranteed 300mA continuous load current with a low 100mV dropout. It is stable with ceramic capacitor. The

Block diagram



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1 Pin configuration

Figure 1. Pin connections

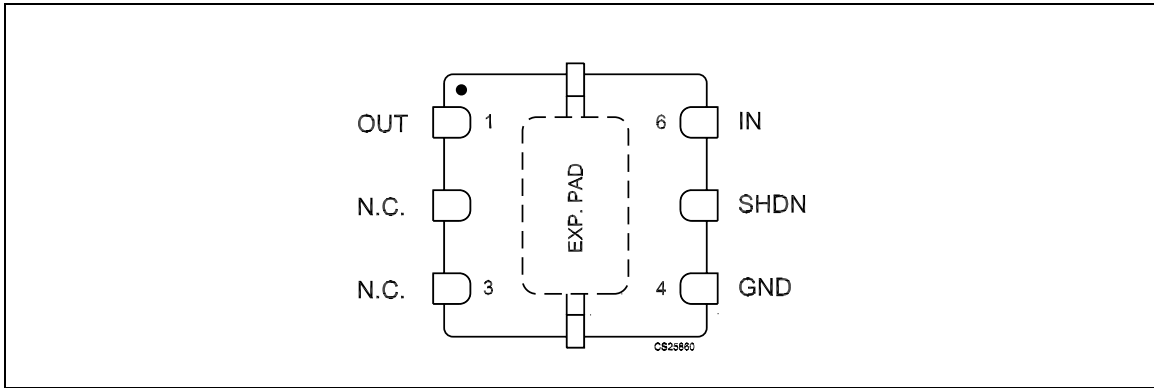


Table 1. Pin description

Pin N°	Symbol	Name and function
1	OUT	Output Voltage of the LDO
2, 3	NC	Not connected
4	GND	Common ground.
5	SHDN	SHUTDOWN Input Voltage: Active-Low Shutdown input. A logic Low reduces supply current to below 1µA. Connect to IN or logic high for normal operation
6	IN	Input Voltage of the LDO

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W

2 Maximum ratings

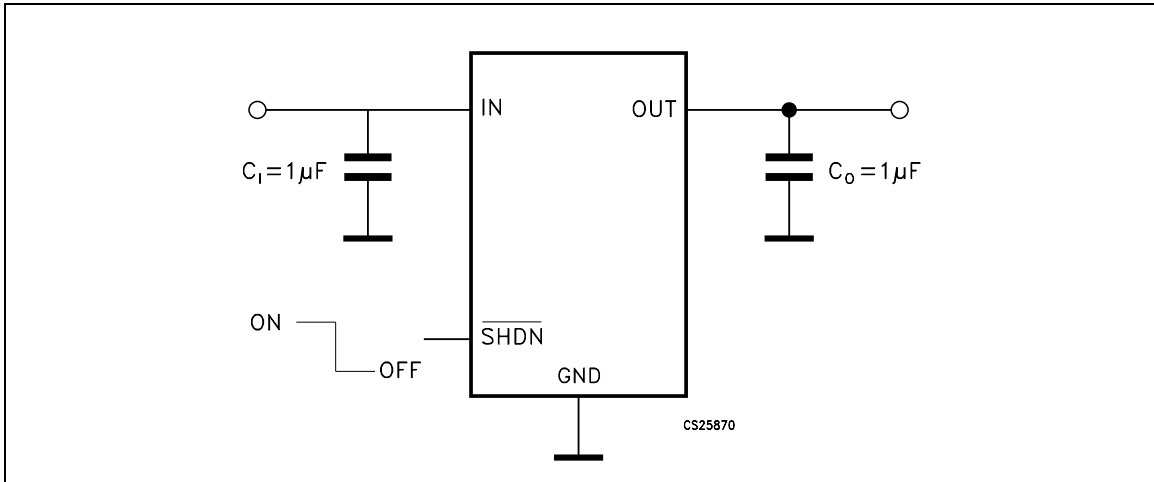
Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC Input voltage	-0.3 to 4.6	V
V_O	DC Output voltage	-0.3 to $V_I + 0.3$	V
V_{SHDN}	Shutdown input voltage	-0.3 to $V_I + 0.3$	V
V_{RESET}	Reset output voltage	-0.3 to $V_I + 0.3$	V
I_O	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-65 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 85	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

3 Typical application

Figure 2. Application circuit



4 Electrical characteristics

Table 4. Electrical characteristics ($T_J = 25^\circ\text{C}$, $V_I = V_{O(NOM)} + 0.5\text{V}$, $C_I = C_O = 1\mu\text{F}$, $I_O = 1\text{mA}$, $V_{SHDN} = V_I$, unless otherwise specified) (*Note: 1*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage		1.7		3.6	V
V_O	V_O Accuracy	$I_O = 300\text{mA}$	-1.0		+1.0	%
		$T_J = -40^\circ$ to 85°C	-2.0		+2.0	
ΔV_O	Line regulation	$V_I = V_O + 0.5\text{V}$ to 3.6V , $I_O = 1\text{mA}$	-0.15	0.01	+0.15	%/V
ΔV_O	Load regulation	$I_O = 1\text{mA}$ to 300mA		0.2	0.3	%/mA
V_{DROP}	Dropout voltage (<i>Note 2</i>)	$I_O = 300\text{mA}$, $V_O \geq 1.8\text{V}$ $T_J = -40^\circ$ to 85°C		130	150	mV
e_N	Output noise voltage	10Hz to 100KHz, $I_O = 10\text{mA}$,		110.7		$\mu\text{V}_{\text{RMS}}/V_O$
SVR	Supply voltage rejection (<i>Figure 7.</i>)	$V_I = V_{O(NOM)} + 0.5\text{V} \pm V_{\text{RIPPLE}}$ $V_{\text{RIPPLE}} = 0.1\text{V}$, $f = 1\text{KHz}$, $I_O = 10\text{mA}$		60		dB
		$V_{\text{IN}} = V_{O(NOM)} + 0.5\text{V} \pm V_{\text{RIPPLE}}$ $V_{\text{RIPPLE}} = 0.1\text{V}$, $f = 10\text{KHz}$, $I_O = 10\text{mA}$		58		
I_Q	Quiescent current ON MODE: $V_{SHDN} = 1.4\text{V}$	$I_O = 0\text{mA}$		90		μA
		$I_O = 0\text{mA}$, $T_J = -40^\circ$ to 85°C			110	
		$I_O = 0$ to 300mA		105		
		$I_O = 0$ to 300mA , $T_J = -40^\circ$ to 85°C			130	
	Quiescent current OFF MODE: $V_{SHDN} = \text{GND}$	V_I input current		0.15	0.5	
I_{SC}	Short circuit current	$R_L = 0$		650		mA
$I_{O(PK)}$	Peak output current	$V_O \geq V_{O(NOM)} - 5\%$		610		mA
V_{SHDN}	Shutdown input logic low	$V_I = 1.6\text{V}$ to 3.6V , $T_J = -40^\circ$ to 85°C			0.4	V
	Shutdown input logic high		1.4			
I_{SHDN}	Shutdown input current	$V_{SHDN} = \text{GND}$ or V_I		0.1	100	nA
T_{ON}	Turn on time	<i>Note 3</i>		120		μs
T_{SHDN}	Thermal shutdown	<i>Note 4</i>		140		$^\circ\text{C}$
C_O	Output capacitor	Capacitance	1		10	μF
		ESR	10		5000	$\text{m}\Omega$

- Note:*
- For $V_{O(NOM)} < 1.2\text{V}$, $V_I = 1.7\text{V}$
 - Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for output voltages below 1.7V.
 - Turn-on time is time measured between the enable input just exceeding V_{SHDN} High Value and the output voltage just reaching 95% of its nominal value
 - Typical thermal protection hysteresis is 15°C .

5 Typical characteristics

Figure 3. Output voltage vs temperature

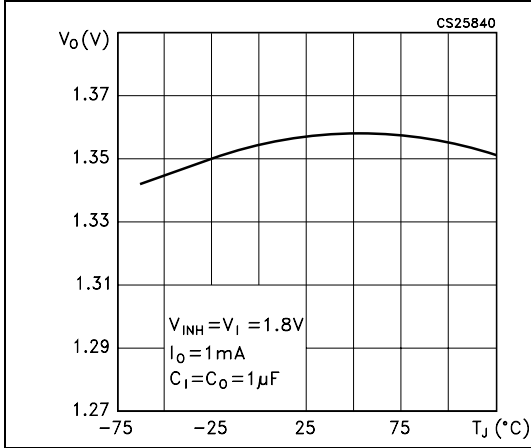


Figure 4. Output voltage vs input voltage

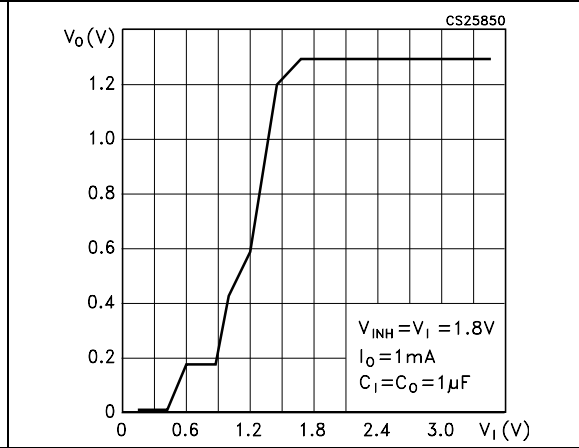


Figure 5. Inhibit voltage vs temperature

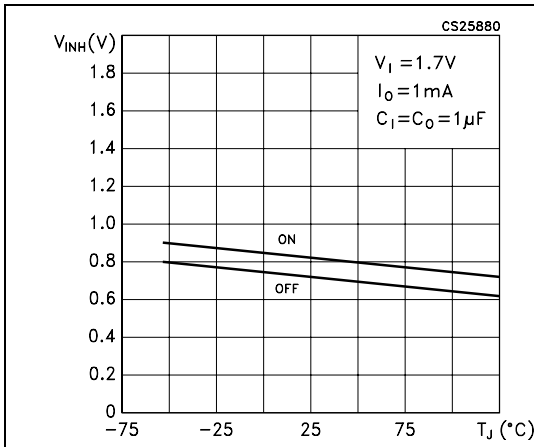


Figure 6. Dropout voltage vs temperature

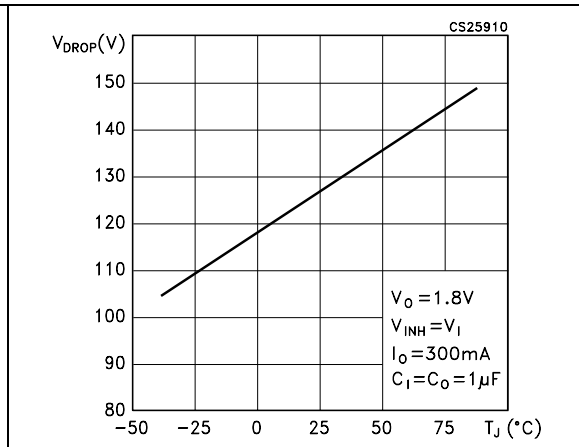


Figure 7. S.V.R. vs frequency

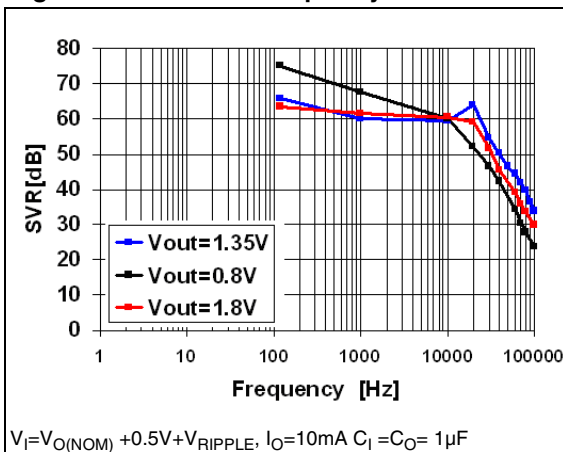


Figure 8. Stability value

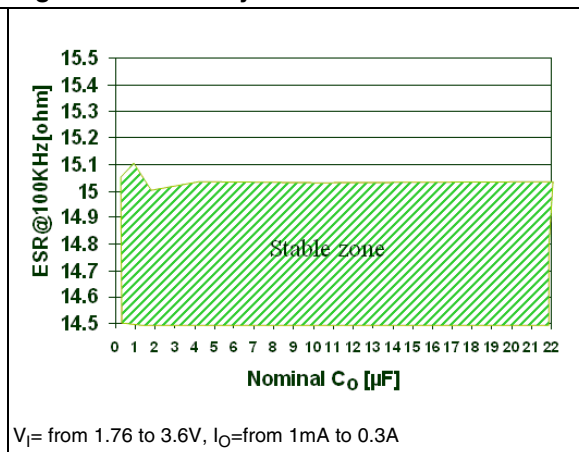


Figure 9. Stability value

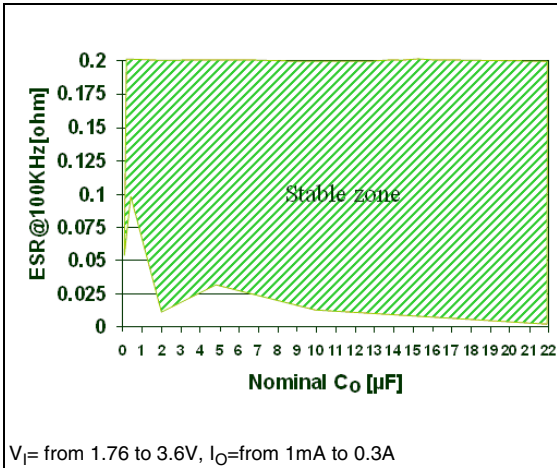


Figure 10. Load transient

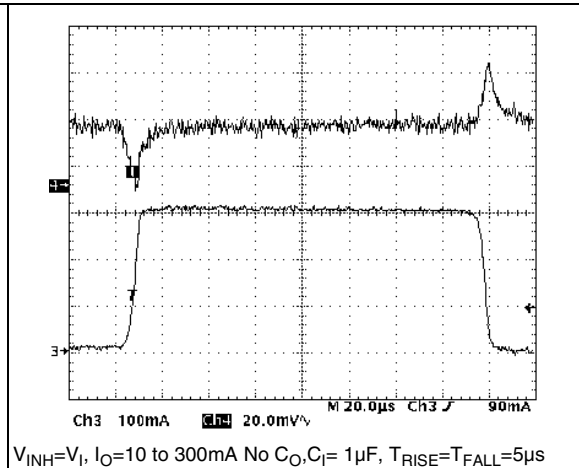
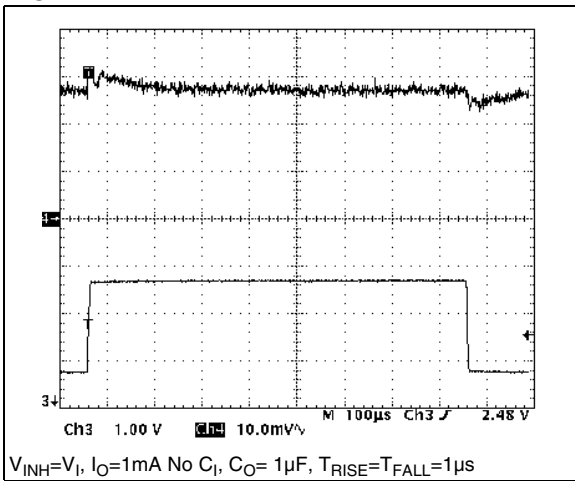


Figure 11. Line transient



6 Detailed description

The device is a low-dropout, low quiescent current linear regulator designed primarily for battery-powered applications. It supplies a regulated output voltage for load currents up to 300mA. The LD3980 consists of a precision bandgap, error amplifier, output p-channel MOS. The 0.7V bandgap reference is connected to the error amplifier. The error amplifier compares this reference to the feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than reference voltage, the pass transistor is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the pass transistor gate is driven higher, allowing less current to pass the output. The output voltage is feedback through an internal resistor voltage connected to OUT. Additional blocks include an output current limiter, a thermal sensor and shutdown logic.

6.1 Shutdown

Drive SHDN low to place the LD3980 in shutdown mode for DFN versions.

In shutdown mode, the pass transistor, control circuit, reference and all biases are turned off, reducing the supply current to typically 0.5µA. Connecting SHDN to IN every block is in normal operation.

6.2 Current limit

The device includes short-circuit protection. It includes a current limiter that controls the pass transistor's gate voltage to limit the output current to about 600mA.

6.3 Thermal overload protection

The Thermal over load protection limits total power dissipation in the device. When the junction temperature (T_J) exceeds +140°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the device to cool. The pass transistor turns on again after the device's junction temperature typically cools by 15°C, resulting in a pulsed output during continuous thermal overload conditions.

6.4 Power dissipation

Maximum power dissipation of the LD3980 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated by the device is:

$$P_D = I_O (V_I - V_O)$$

The maximum power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A) / \theta_{JA}$$

Where: $T_{JMAX} = +150^\circ\text{C}$

T_A is the ambient temperature

θ_{JA} thermal resistance.

The device's pins perform the dual function of providing an electrical connection as well as channeling heat away from the die. Use wide circuit-board traces and large, solid copper polygons to improve power dissipation. Using multiple vias to buried ground planes further enhances thermal conductivity.

6.5 Output capacitance

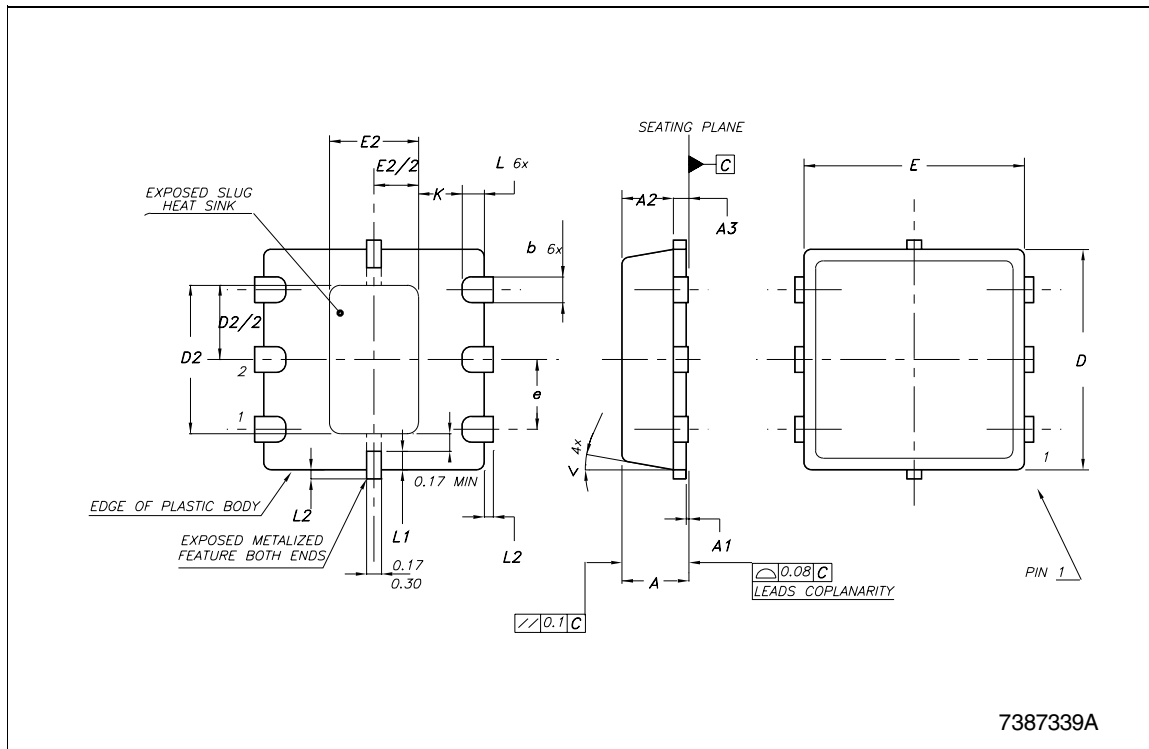
The device is specifically designed to employ ceramic output capacitors as low as $1\mu\text{F}$. Ceramic capacitors below $10\mu\text{F}$ offer significant cost and space savings, along with high frequency noise filtering. Higher values and other types of capacitor may be used, but their equivalent series resistance should be maintained in the range of the table.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

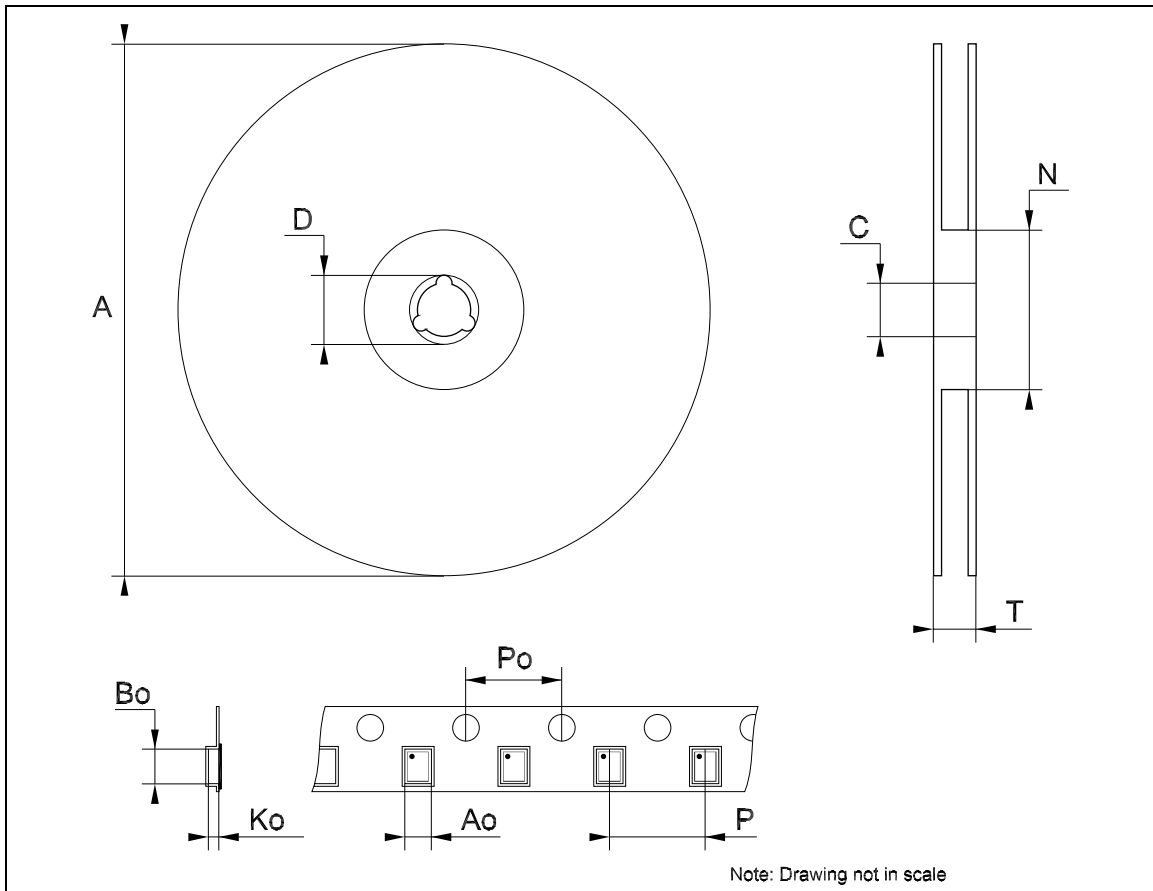
DFN6 (3x3) MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	31.5		39.4
A1	0		0.05	0.0		2.0
A2	0.65		0.75	25.6		29.5
A3		0.20			7.9	
b	0.33		0.43	13.0		16.9
D	2.90	3.00	3.10	114.2	118.1	122.0
D2	1.92		2.12	75.6		83.5
E	2.90	3.00	3.10	114.2	118.1	122.0
E2	1.11		1.31	43.7		51.6
e		0.95			37.4	
L	0.20		0.45	7.9		17.7
L1		0.24			9.4	
L2			0.13			5.1
K	0.20			7.9		



Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



8 Order code

Table 5. Order code

Part number	Output voltage ⁽¹⁾
LD3980PM08R	0.8 V
LD3980PM12R	1.2 V ⁽²⁾
LD3980PM13R	1.3 V ⁽²⁾
LD3980PM135R	1.35 V
LD3980PM15R	1.5 V ⁽²⁾
LD3980PM18R	1.8 V
LD3980PM30R	3.0 V ⁽²⁾

1. Other values of V_O available on request

2. Available on request

9 Revision history

Table 6. Revision history

Date	Revision	Changes
05-Dec-2006	1	First release.

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