Standard Variable Output LDO Regulators

2A Standard Variable Output LDO Regulator

BD00D0AWHFP

No.11023EBT04

●Description

The BD00D0AWHFP is low-saturation regulator. The output voltage can be arbitrarily configured using the external resistance. This IC has a built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal shutdown circuit that protects the IC from thermal damage due to overloading.

●Features

1) Output Current : 2A
2) High Output Voltage Precision : ±1%
3) Low saturation with PDMOS output
4) Built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits
5) Built-in thermal shutdown circuit for protecting the IC from thermal damage due to overloading
6) Low ESR Capacitor
7) HRP5 packaging

●Applications

Audiovisual equipments, FPDs, televisions, personal computers or any other consumer device

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply Voltage *1	Vcc	-0.3～+35.0	V
Output Control Voltage	V_{CTL}	-0.3～+35.0	V
Power Dissipation *2	Pd	1.6	W
Operating Temperature Range	Topr	-40～+105	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 HRP5: Reduced by 12.8mW / ℃ over Ta = 25℃, when mounted on glass epoxy board: 70mm × 70mm × 1.6mm.
NOTE: This product is not designed for protection against radioactive rays.

●Operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	4.0	25.0	V
Output Control Voltage	V_{CTL}	0	25.0	V
Output Current	Io	0	2.0	A
Output Voltage	Vo	3.0	15.0	V

●Electrical characteristics

(Unless otherwise specified, Ta=25℃, Vcc=10V,V_{CTL}=5V,Io=0mA,Vo=5.0Vsetting)
(The resistor of between ADJ and Vo =56.7kΩ,ADJ and GND =10kΩ)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shut Down Current	Isd	−	0	10	μA	V_{CTL}=0V
Bias Current	Ib	−	0.5	1.0	mA	
ADJ Terminal Voltage	VADJ	0.742	0.750	0.758	V	Io=50mA
Dropout Voltage	ΔVd	−	0.40	0.55	V	Vcc=Vo×0.95, Io=1A
Ripple Rejection	R.R.	45	55	−	dB	f=120Hz,ein※1=1Vrms, Io=100mA
Line Regulation	Reg.I	−	20	60	mV	Vcc=6→25V
Load Regulation	Reg.L	−	Vo×0.007	Vo×0.014	V	Io=5mA→1A
Temperature Coefficient of Output Voltage	Tcvo.1	−	+0.04	−	%/℃	Io=5mA,Tj=-40～-20℃
	Tcvo.2	−	±0.005	−	%/℃	Io=5mA,Tj=-20～+105℃
CTL ON Mode Voltage	VthH	2.0	−	−	V	ACTIVE MODE
CTL OFF Mode Voltage	VthL	−	−	0.8	V	OFF MODE
CTL Bias Current	I_{CTL}	−	25	50	μA	

*1 ein : Input Voltage Ripple

●Electrical characteristic curves (Reference data)

(Unless otherwise specified, Ta=25℃, Vcc=10V,V_{CTL}=5V,Io=0mA,Vo=5.0Vsetting)
(The resistor of between ADJ and Vo =56.7kΩ,ADJ and GND =10kΩ)

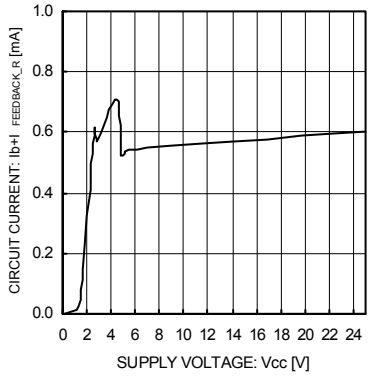


Fig.1 Circuit Current
($I_{FEEDBACK\_R}$≒75μA)

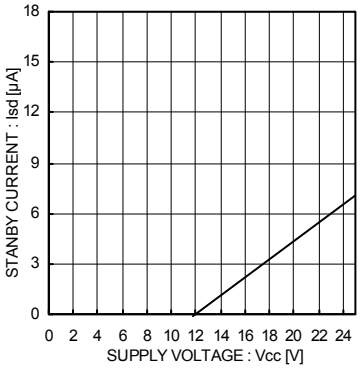


Fig.2 Shut Down Current

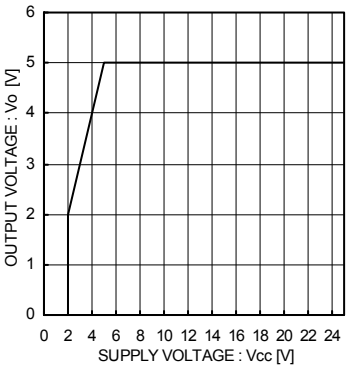


Fig.3 Line Regulation
(Io=0mA)

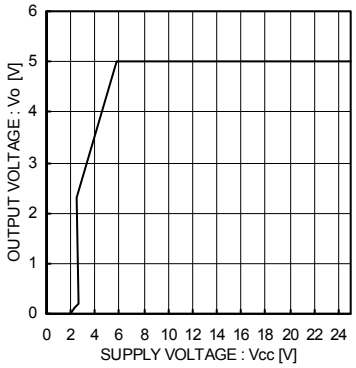


Fig.4 Line Regulation
(Io=1000mA)

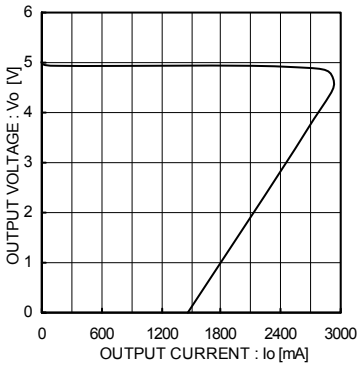


Fig.5 Load Regulation

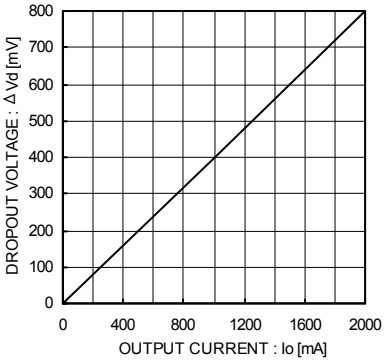


Fig.6 Dropout Voltage
(Vcc＝4.75V)
(Io=0mA→2000mA)

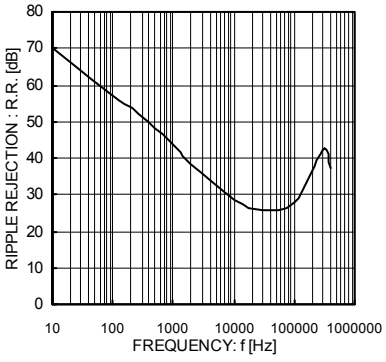


Fig.7 Ripple Rejection

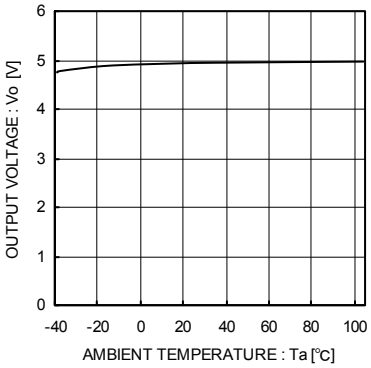


Fig.8 Output Voltage
Temperature Characteristics

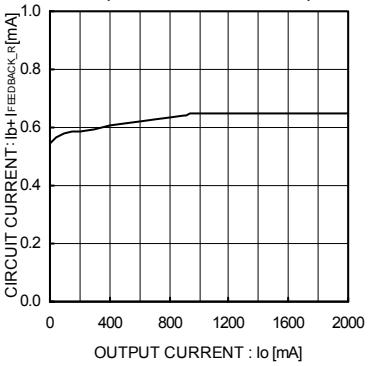


Fig.9 Circuit Current
($I_{FEEDBACK\_R}$≒75μA)

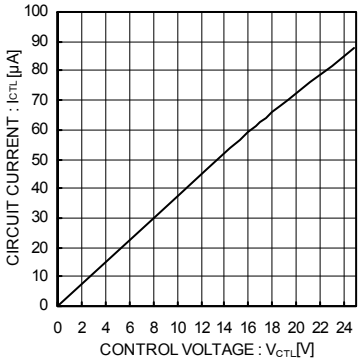


Fig.10 CTL Voltage vs CTL Current

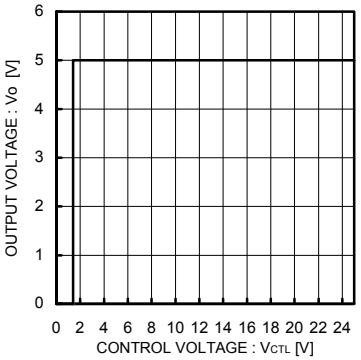


Fig.11 CTL Voltage vs Output Voltage

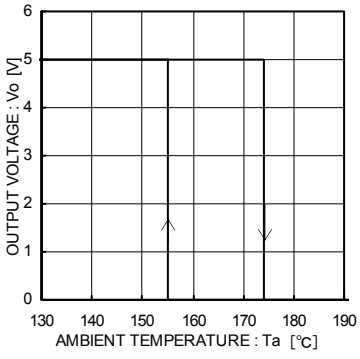
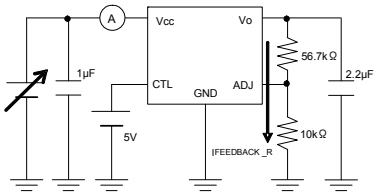
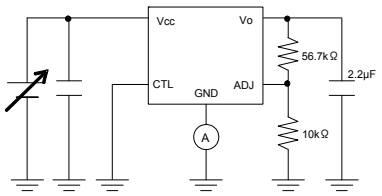


Fig.12 Thermal Shutdown
Circuit Characteristics

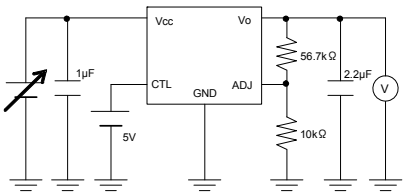
●Measurement Circuit for Reference Data



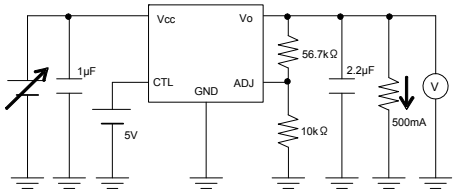
Measurement Circuit of Fig.1



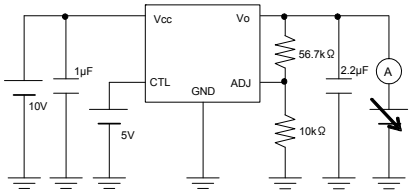
Measurement Circuit of Fig.2



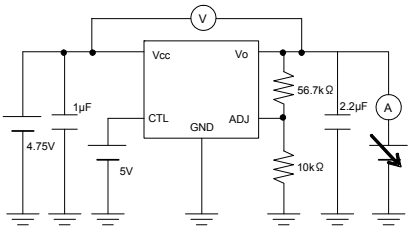
Measurement Circuit of Fig.3



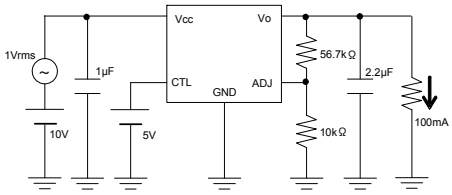
Measurement Circuit of Fig.4



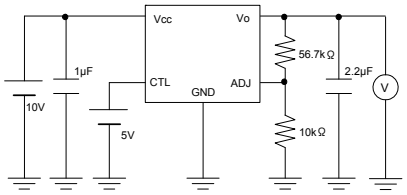
Measurement Circuit of Fig.5



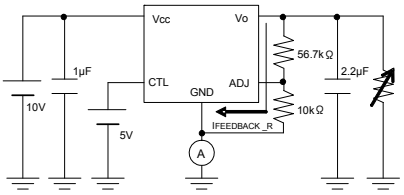
Measurement Circuit of Fig.6



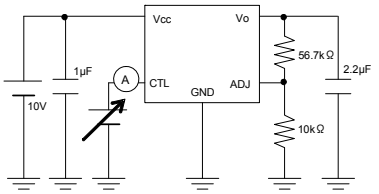
Measurement Circuit of Fig.7



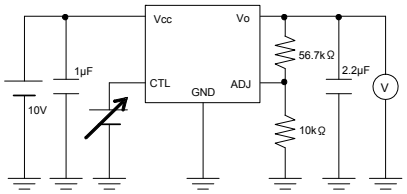
Measurement Circuit of Fig.8



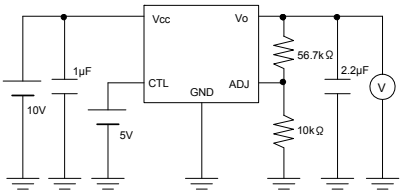
Measurement Circuit of Fig.9



Measurement Circuit of Fig.10



Measurement Circuit of Fig.11



Measurement Circuit of Fig.12

●Block diagrams

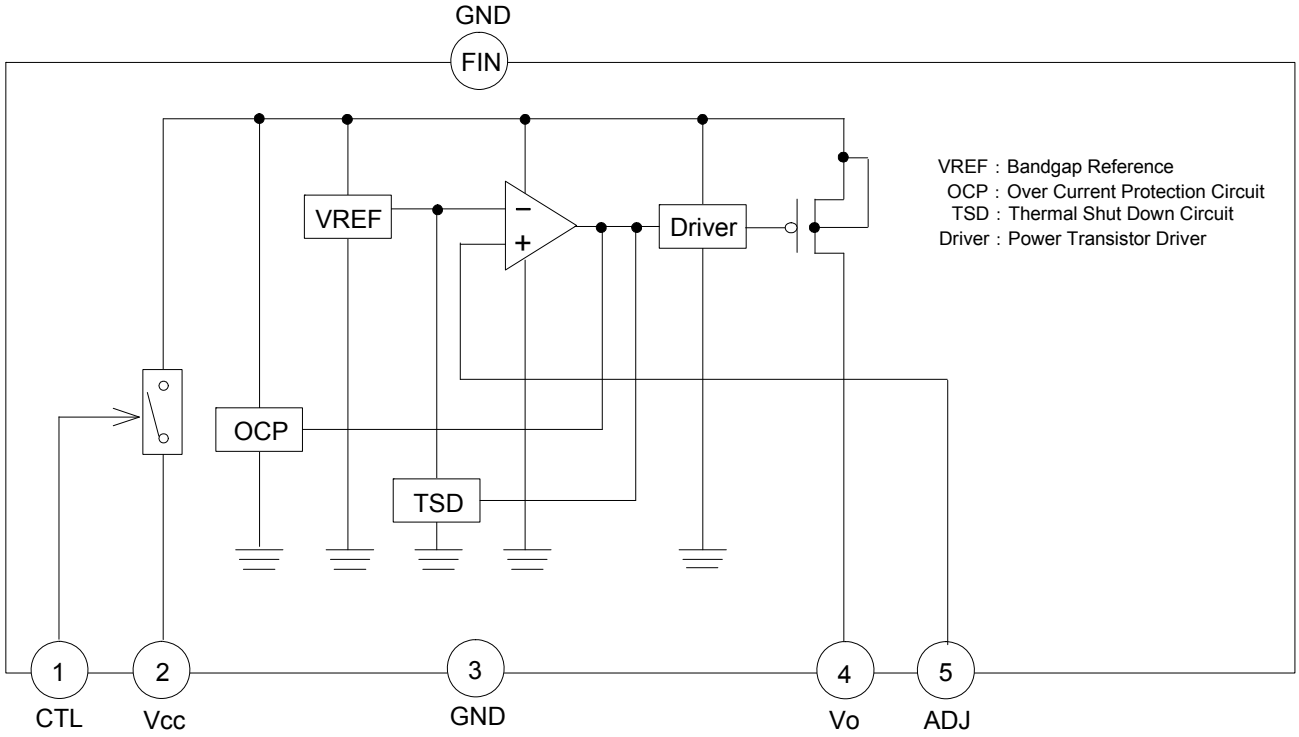
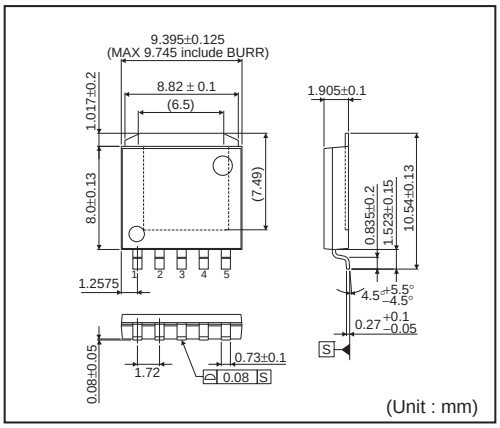


Fig.13

Pin No.	Pin Name	Function
1	CTL	Output Control Pin
2	Vcc	Power Supply Pin
3	GND	GND
4	Vo	Output Pin
5	ADJ	Adjustable Pin
Fin	GND	GND

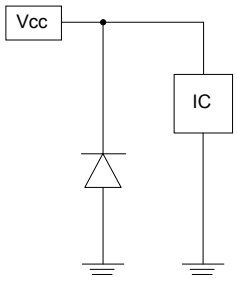
●TOP VIEW〈Package dimension〉

HRP5

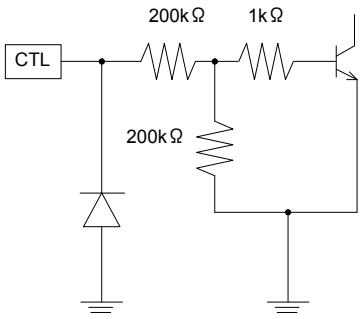


●Input / Output Equivalent Circuit Diagrams

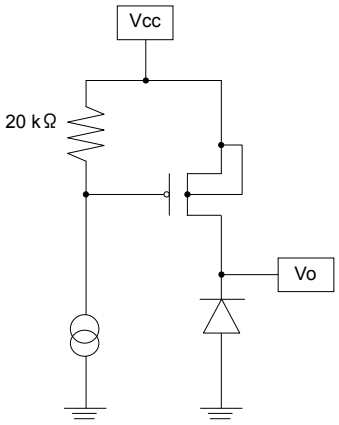
Vcc Pin



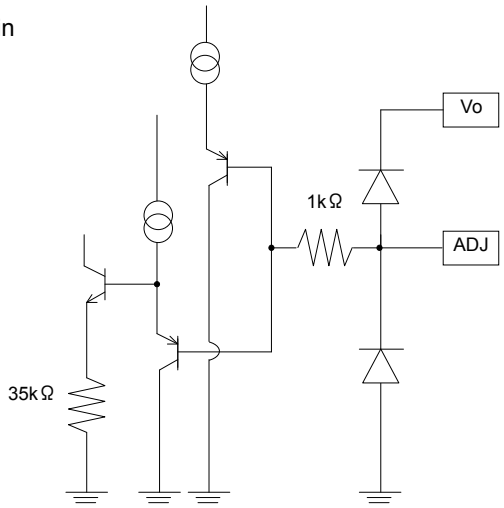
CTL Pin



Vo Pin

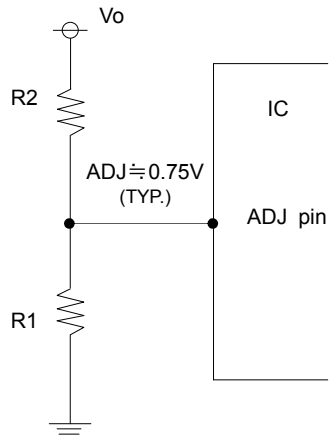


ADJ Pin



●Output Voltage Configuration Method

Please connect resistors R1 and R2 (which determines the output voltage) as shown in Fig.14.
Please be aware that the offset due to the current that flows from the ADJ terminal becomes large when resistors with large values are used. The use of resistors with R1=5kΩ to 10kΩ is recommended.



$$Vo \fallingdotseq ADJ \times (R1+R2) / R1$$

Fig.14

●Thermal Design

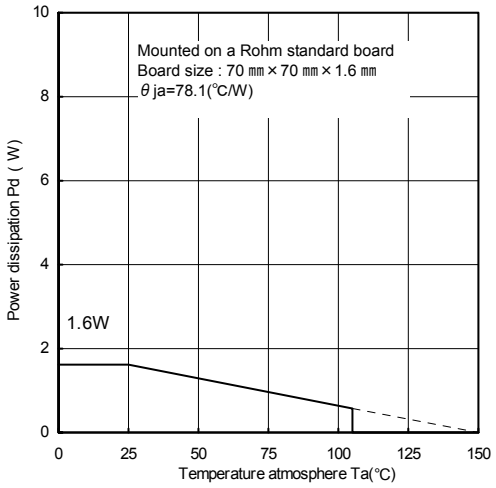


Fig.15

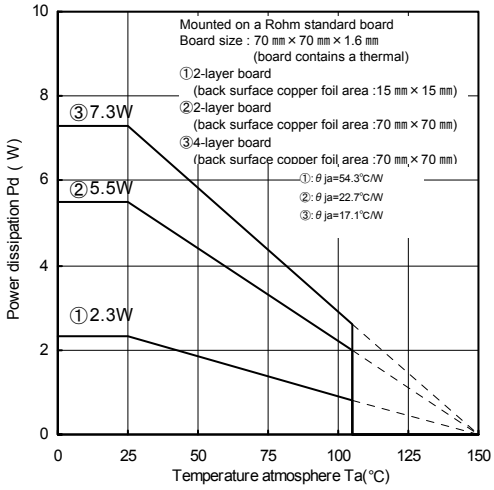


Fig.16 (Reference data)

When using at temperatures over Ta=25℃, please refer to the heat reducing characteristics shown in Fig.15. and Fig.16. The IC characteristics are closely related to the temperature at which the IC is used, so it is necessary to operate the IC at temperatures less than the maximum junction temperature Tjmax.

Fig.15 and Fig.16 shows the acceptable loss and heat reducing characteristics of the HRP5 package. Even when the ambient temperature Ta is a normal temperature (25℃), the chip (junction) temperature Tj may be quite high so please operate the IC at temperatures less than the acceptable loss Pd.

The calculation method for power consumption Pc(W) is as follows :(Fig.16③)

$Pc=(Vcc-Vo)\times Io+Vcc\times Ib$

Acceptable loss $Pd \geqq Pc$

Vcc: Input voltage
Vo: Output voltage
Io: Load current
Ib: Circuit current
Ishort: Short current

Solving this for load current Io in order to operate within the acceptable loss,

$$Io \leqq \frac{Pd-Vcc\times Ib}{Vcc-Vo}$$ (Please refer to Fig.9 for Ib.)

It is then possible to find the maximum load current Io_{Max} with respect to the applied voltage Vcc at the time of thermal design.

Calculation Example)When Ta=85℃,Vcc=10V,Vo=5V

$$Io \leqq \frac{3.796-10\times Ib}{5}$$

$Io \leqq 758.2mA$ (Ib:0.5mA)

(Fig.16③: θja=17.1℃/W → -58.4mW/℃
25℃=7.3W → 85℃=3.796W)

Please refer to the above information and keep thermal designs within the scope of acceptable loss for all operating temperature ranges. The power consumption Pc of the IC when there is a short circuit (short between Vo and GND) is :

$Pc=Vcc\times(Ib+Ishort)$ (Please refer to Fig. 5 for Ishort)

●Notes for use

1. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

3. GND potential
   The potential of the GND pin must be the minimum potential in the system in all operating conditions.
   Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.

4. Ground wiring pattern
   When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.
   The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. Inter-pin shorts and mounting errors
   Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.

6. Operation in strong electromagnetic fields
   Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

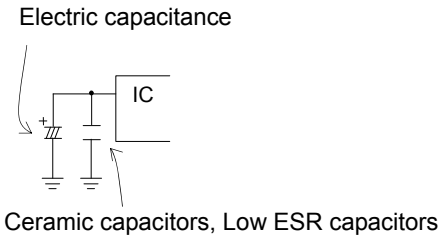
7. Testing on application boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Thermal consideration
   Use a thermal design that allows for a sufficient margin in light of the Pd in actual operating conditions.
   Consider Pc that does not exceed Pd in actual operating conditions. (Pd≧Pc)

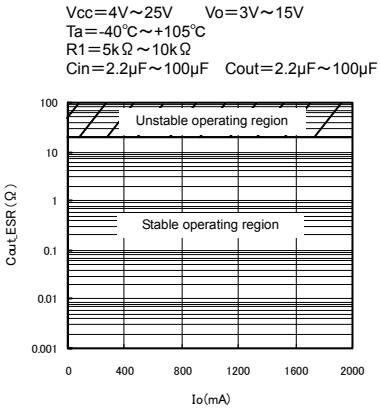
   (Tjmax : Maximum junction temperature=150[℃] , Ta : Peripheral temperature[℃] ,
   θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
   Pc : Power dissipation [W], Vcc : Input Voltage, Vo : Output Voltage, Io : Load, Ib : Bias Current)

   Package Power dissipation : Pd (W)=(Tjmax－Ta)/θja
   Power dissipation : Pc (W)=(Vcc－Vo)×Io+Vcc×Ib

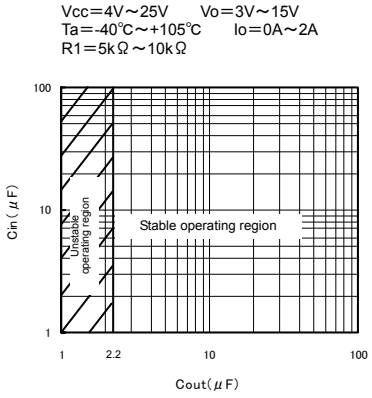
9. Vcc pin
   Insert a capacitor(Vo≧5V:capacitor≧1μF～, Vo＜5V:capacitor≧2.2μF～) between the Vcc and GND pins.
   The appropriate capacitance value varies by application. Be sure to allow a sufficient margin for input voltage levels.



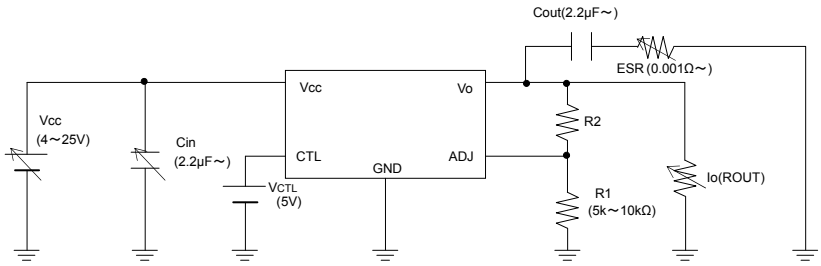
10. Output pin
It is necessary to place capacitors between each output pin and GND to prevent oscillation on the output. Usable capacitance values range from 2.2μF to 1000μF. Ceramic capacitors can be used as long as their ESR value is low enough to prevent oscillation (0.001Ω to 20Ω). Abrupt fluctuations in input voltage and load conditions may affect the output voltage.



Cout_ESR vs Io(reference data)



Cin vs Cout(reference data)



※Operation Notes 10 Measurement circuit

11. CTL pin
Do not make voltage level of chip enable pin keep floating level, or in between VthH and VthL. Otherwise, the output voltage would be unstable or indefinite.

12. For a steep change of the Vcc voltage
Because MOS FET for output Transistor is used when an input voltage change is very steep, it may evoke large current. When selecting the value of external circuit constants, please make sure that the operation on the actual application takes these conditions into account.

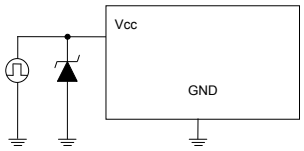
13. For an infinitesimal fluctuations of output voltage.
At the use of the application that infinitesimal fluctuations of output voltage caused by some factors (e.g. disturbance noise, input voltage fluctuations, load fluctuations, etc.), please take enough measures to avoid some influence (e.g. insert the filter, etc.).

14. Over current protection circuit (OCP)
The IC incorporates an integrated over-current protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. It is also designed to limit output current (without latching) in the event of a large and instantaneous current flow from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuits.

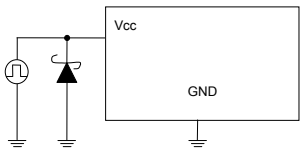
15. Thermal shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

16. Applications or inspection processes where the potential of the Vcc pin or other pins may be reversed from their normal state may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000μF or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. Insert a diode in series with Vcc to prevent reverse current flow, or insert bypass diodes between Vcc and each pin.

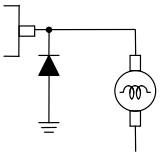
17. Positive voltage surges on VCC pin
A power zener diode should be inserted between VCC and GND for protection against voltage surges of more than 35V on the VCC pin.



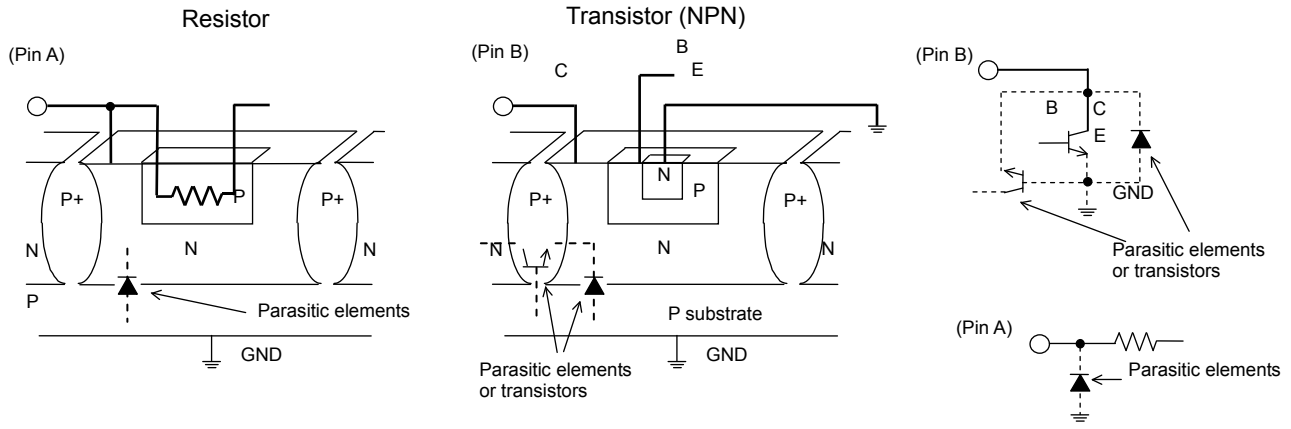
18. Negative voltage surges on VCC pin
A schottky barrier diode should be inserted between VCC and GND for protection against voltages lower than GND on the VCC pin.



19. Output protection diode
Loads with large inductance components may cause reverse current flow during startup or shutdown. In such cases, a protection diode should be inserted on the output to protect the IC.



20. Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):
○When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
○When GND > Pin B, the PN junction operates as a parasitic transistor
Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



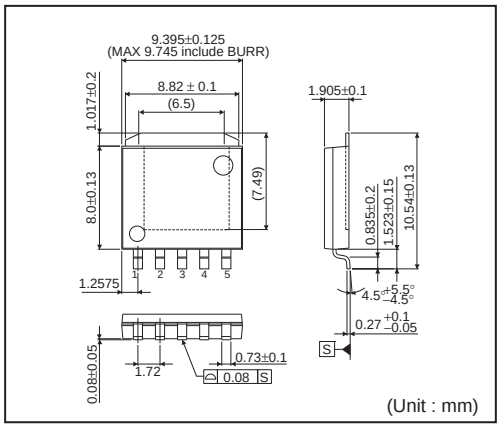
Example of Simple Monolithic IC Architecture

●Ordering part number

B	D	0	0	D	0	A	W	H	F	P	-	T	R

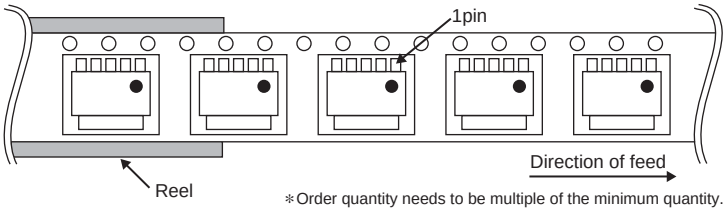
- ROHM model Name
- Output Voltage 00:Variable
- Current capacity D0A:2A
- Shutdown switch W : With switch None : Without switch
- Package HFP: HRP5
- Packaging and forming specification TR:Embossed tape and reel

HRP5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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