## Standard CMOS LDO Regulators

－Description
The BH $\square \square F B 1 W$ ，BH $\square \square L B 1 W$ and BH $\square \square$ MA3W series are low dropout CMOS regulators with 150 mA and 300 mA output that have $\pm 1 \%$ high accuracy output voltage．
The BHロロFB1W series combines $40 \mu \mathrm{~A}$ low current consumption and a 70 dB high ripple rejection ratio by utilizing output level CMOS technology．The components can be easily mounted into the small standard SSOP5 and the ultra－small HVSOF5／HVSOF6 packages．
－Features
1）High accuracy output voltage：$\pm 1 \%$
2）High ripple rejection ratio： 70 dB （BHロロFB1WHFV／WG，BH $\square \square L B 1$ WHFV／WG）
3）Low dropout voltage： 60 mV （when current is 100 mA ）（BHロपMA3WHFV）
4）Stable with ceramic output capacitors
5）Low Bias current ： $40 \mu \mathrm{~A}(\mathrm{lo}=50 \mathrm{~mA})(\mathrm{BH} \square \square \mathrm{FB} 1 \mathrm{WHFV} / \mathrm{WG})$
6）Output voltage ON／OFF control
7）Built－in over－current protection and thermal shutdown circuits
8）Ultra－small power package：HVSOF5（BHロपFB1WHFV，BH $\square \square$ LB1WHFV）
9）Ultra－small power package：HVSOF6（BHロロMA3WHFV）
－Applications
Battery－driven portable devices and etc．
－Line up
－150mA BH $\square \square F B 1 W$ and BH $\square \square L B 1 W$ Series

| Part Number | 1.5 | 1.8 | 1.85 | 2.5 | 2.8 | 2.9 | 3.0 | 3.1 | 3.3 | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BHDロFB1WG | － | － | － | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | SSOP5 |
| BHDロFB1WHFV | － | － | － | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | HVSOF5 |
| BH口ロLB1WG | $\checkmark$ | $\checkmark$ | － | － | － | － | － | － | － | SSOP5 |
| BH口ロLB1WHFV | $\checkmark$ | $\checkmark$ | $\checkmark$ | － | － | － | － | － | － | HVSOF5 |

－300mA BHロロMA3WHFV series

| Part Number | 1.5 | 1.8 | 2.5 | 2.8 | 2.9 | 3.0 | 3.1 | 3.3 | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BHロロMA3WHFV | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | HVSOF6 |



| Symbol | Details |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| a | Output Voltage Designation |  |  |  |
|  | $\square \square$ | OutputVoltage（V） | $\square \square$ | Output Voltage（V） |
|  | 15 | 1.5 V （Typ．） | 29 | 2.9 V （Typ．） |
|  | 18 | 1．8V（Typ．） | 30 | 3．0V（Typ．） |
|  | 1 J | 1.85 V （Typ．） | 31 | 3．1V（Typ．） |
|  | 25 | 2.5 V （Typ．） | 33 | 3．3V（Typ．） |
|  | 28 | 2.8 V （Typ．） |  |  |
| b | Package： | G：SSOP5 HFV：HVSOF5 |  |  |

Part Number：BH $\square \square$ MA 3 W $\square$

| Symbol | Details |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Output Voltage Designation |  |  |  |
|  | $\square \square$ | OutputVoltage（V） | $\square \square$ | OutputVoltage（V） |
|  | 15 | 1.5 V （Typ．） | 29 | 2.9 V （Typ．） |
|  | 18 | 1.8 V （Typ．） | 30 | 3.0 V （Typ．） |
|  | 25 | 2.5 V （Typ．） | 31 | 3.1 V （Typ．） |
|  | 28 | 2.8 V （Typ．） | 33 | 3.3 V （Typ．） |
| b | Package： | HFV ：HVSOF6 |  |  |

－Absolute maximum ratings（ $\mathrm{Ta}=25^{\circ} \mathrm{C}$ ）

| Parameter | Symbol | Limits | Unit |
| :---: | :---: | :---: | :---: |
| Applied supply voltage | VMAX | $-0.3 \sim+6.5$ | V |
| Power dissipation | Pd | $680{ }^{* 1}$（HVSOF6） | mW |
|  |  | $410{ }^{*} 2$（HVSOF5） |  |
|  |  | $540{ }^{* 3}$（SSOP5） |  |
| Operating temperature range | Topr | $-40^{*} 4 \sim+85$ | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | Tstg | $-55 \sim+125$ | ${ }^{\circ} \mathrm{C}$ |

＊ 1 Derated at $6.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for temperature above $\mathrm{Ta}=25^{\circ} \mathrm{C}$ ，when mounted on a glass epoxy PCB（ 70 mm X 1.6 mm ）．
2 Derated at $4.1 \mathrm{~mW} /{ }^{\circ}$ C for temperature above $T a=25^{\circ} \mathrm{C}$ ，when mounted on a glass epoxy $\mathrm{PCB}(7 \mathrm{~mm} \times 1.6 \mathrm{~mm})$
＊${ }^{*} 3$ Derated at $5.4 \mathrm{~mW} / /^{\circ} \mathrm{C}$ for temperature above $\mathrm{Ta}=25^{\circ} \mathrm{C}$ ，when mounted on a glass epoxy $\mathrm{PCB}(70 \mathrm{~mm} \times 1.6 \mathrm{~mm})$ ．
＊ 4 BHD $\square F B 1 W$ series：$-30^{\circ} \mathrm{C}$ and up
－Recommended operating range

| Parameter |  | Symbol | Min． | Typ． | Max． | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power supply voltage |  | VIN | 2.5 | － | 5.5 | V |
| Output current | BHロロMA3W | IOUT | － | － | 300 | mA |
|  | BHロロFB1W |  | － | － | 150 | mA |
|  | BH口口LB1W |  | － | － | 150 | mA |

## －Recommended operating conditions

| Parameter | Symbol | Min． | Typ． | Max． | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :--- |
| Input capacitor | CIN | $0.1^{{ }^{*} 1}$ | - | - | $\mu \mathrm{F}$ | Ceramic capacitor recommended |
| Output capacitor | Co | $1.0^{{ }^{*} 2}$ | - | - | $\mu \mathrm{F}$ | Ceramic capacitor recommended |
| Noise decrease capacitor | Cn | - | 0.01 | 0.22 | $\mu \mathrm{~F}$ | Ceramic capacitor recommended |

＊ 1 BHロロMA3WHFV： $1.0 \mu \mathrm{~F}$
＊ 2 The output may become unstable at low temperatures and with light loads，so a capacitance of $2.2 \mu \mathrm{~F}$ or much more is recommended when using at low temperatures．（BH $\square \square \mathrm{FB} 1 \mathrm{~W}$
－Electrical characteristics（Unless otherwise noted， $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VIN}=\mathrm{VouT}+1 \mathrm{~V}^{*}, \mathrm{STBY}=1.5 \mathrm{~V}, \mathrm{CIN}=0.1 \mu \mathrm{~F}, \mathrm{Co}=1 \mu \mathrm{~F}$ ）
■BHDロFB1WHFV／WG，BH口ロLB1WHFV／WG

| Parameter |  | Symbol | Min． | Typ． | Max． | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output voltage＊1 |  | Vout | Vout X 0.99 | Vout | Vout X 1.01 | V | lout $=1 \mathrm{~mA}$ |
| Circuit current |  | I GND | － | 40 | 70 | $\mu \mathrm{A}$ | lout $=50 \mathrm{~mA}$ |
| Circuit current（STBY） |  | I STBY | － | － | 1.0 | $\mu \mathrm{A}$ | STBY $=0 \mathrm{~V}$ |
| Ripple rejection ratio |  | RR | － | 70 | － | dB | $V R R=-20 \mathrm{dBv}$ ，fRR＝1kHz，lout $=10 \mathrm{~mA}$ |
| Load response 1 |  | LTV1 | － | 50 | － | mV | lout $=1 \mathrm{~mA}$ to 30 mA |
| Load response 2 |  | LTV2 | － | 50 | － | mV | lout $=30 \mathrm{~mA}$ to 1 mA |
| Dropout voltage＊3 |  | VSAT | － | 250 | 450 | mV | Vin $=0.98$ X Vout，lout $=100 \mathrm{~mA}$ |
| Line regulation |  | VDL1 | － | 2 | 20 | mV | $\mathrm{VIN}=$ Vout $+0.5 \mathrm{~V}{ }^{\text {＂4 }}$ to 5.5 V |
| Load regulation |  | VDL01 | － | 10 | 30 | mV | lout $=1 \mathrm{~mA}$ to 100 mA |
| Over current protection limit current＊3 |  | ILMAX | － | 250 | － | mA | Vo＝Vout X 0.98 |
| Short current＊3 |  | I SHORT | － | 50 | － | mA | V o $=0 \mathrm{~V}$ |
| STBY pull－down resistor |  | RSTB | 550 | 1100 | 2200 | $\mathrm{k} \Omega$ |  |
| STBY control voltage | ON | VSTBH | 1.5 | － | Vin | V |  |
|  | OFF | VSTBL | －0．3 | － | 0.3 | V |  |

＊This product is not designed for protection against radio active rays．
$\begin{array}{ll}* 2 & \text { BH15，18LB1WHFV／WG：} \pm 25 \mathrm{mV} \text { precision }=3.5 \mathrm{~V}\end{array} \quad{ }^{*} 3$ Excluding BH15，18LB1WHFV／WG ${ }^{*} 4$ BH15，18LB1WHFV／WG：ViN $=3.0$ to 5.5 V
－Electrical characteristics（Unless otherwise noted， $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VIN}=\mathrm{Vout}+1 \mathrm{~V}^{*}{ }^{*}, \mathrm{STBY}=1.5 \mathrm{~V}, \mathrm{ClN}=1 \mu \mathrm{~F}, \mathrm{Co}=1 \mu \mathrm{~F}$ ）
■BHDロMA3WHFV

| Parameter | Symbol | Min． | Typ． | Max． | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output voltage＊1 | Vout | VouT $¥ 0.99$ | Vout | Vout $¥ 1.01$ | V | lout $=1 \mathrm{~mA}$ |
| Circuit current | I GND | － | 65 | 95 | $\mu \mathrm{A}$ | lout $=1 \mathrm{~mA}$ |
| Circuit current（STBY） | I STBY | － | － | 1.0 | $\mu \mathrm{A}$ | STBY $=0 \mathrm{~V}$ |
| Ripple rejection ratio | RR | － | 60 | － | dB | VRR $=-20 \mathrm{dBv}$ ，fRR＝1kHz，lout $=10 \mathrm{~mA}$ |
| Dropout voltage ${ }^{*}{ }^{2}$ | VSAT1 | － | 60 | 90 | mV | Vin $=0.98$ X Vout，lout $=100 \mathrm{~mA}$ |
| Line regulation | VDL1 | － | 2 | 20 | mV | $\mathrm{VIN}=\mathrm{Vout}+0.5 \mathrm{~V}$ to 5.5 V |
| Load regulation 1 | VDL01 | － | 6 | 30 | mV | lout $=1 \mathrm{~mA}$ to 100 mA |
| Load regulation 2 | VDL02 | － | 18 | 90 | mV | lout $=1 \mathrm{~mA}$ to 300 mA |
| Output voltage temperature | －Vout／DT | － | $\pm 100$ | － | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | lout $=1 \mathrm{~mA}, \mathrm{Ta}=-40$ to $+85^{\circ} \mathrm{C}$ |
| Over current protection limit current | ILMAX | － | 600 | － | mA | Vo＝Vout X 0.85 |
| Short current | I SHORT | － | 100 | － | mA | $\mathrm{Vo}=0 \mathrm{~V}$ |



- Typical characteristics


## - Output voltage-input voltage



Fig. 1

- GND current-input voltage


Fig. 4

## - Output voltage-output current



Fig. 8


Fig. 9

## - Dropout voltage-output current



Fig. 10


Fig. 11


Fig. 7


Fig. 5


Fig. 3


Fig. 6


Fig. 2


Fig. 12


Fig. 13


Fig. 14

## - Ripple reflection-frequency



Fig. 15


Fig. 16


Fig. 17

- Load response characteristics ( $\mathrm{CO}=1.0 \mu \mathrm{~F}$ )


Fig. 18


Fig. 19


Fig. 20

## - Output voltage startup time



Fig. 21


IOUT $=50 \mathrm{~mA}$ (ROUT $=56 \Omega$ )
Fig. 22


IOUT $=300 \mathrm{~mA}($ ROUT $=10 \Omega)$
Fig. 23

Block diagrams


- Power dissipation Pd

1. Power dissipation

Power dissipation calculation include estimates of power dissipation characteristics and internal IC power consumption and should be treated as guidelines. In the event that the IC is used in an environment where this power dissipation is exceeded, the attendant rise in the junction temperature will trigger the thermal shutdown circuit, reducing the current capacity and otherwise degrading the IC's design performance. Allow for sufficient margins so that this power dissipation is not exceeded during IC operation.

Calculating the maximum internal IC power consumption (PMAX)

$$
\text { PMAX=(VIN-VoUT) } \times \text { IOUT(MAX.) }\left\{\begin{array}{r}
\text { VIN : Input voltage } \\
\text { VoUT : Output voltage } \\
\text { IOUT(MAX.) : Output current }
\end{array}\right.
$$

2. Power dissipation characteristics (Pd)


Fig. 26: HVSOF6
Power Dissipation/
Power Dissipation Reduction (Example)

HVSOF5


Fig. 27: HVSOF5
Power Dissipation/
Power Dissipation Reduction (Example)

SSOP5


Fig. 28: SSOP5
Power Dissipation/
Power Dissipation Reduction (Example)

* Circuit design should allow a sufficient margin for the temperature range so that $\mathrm{Pmax}<\mathrm{Pd}$.

O Input capacitor
It is recommended to insert bypass capacitors between input and GND pins, positioning them as close to the pins as possible. These capacitors will be used when the power supply impedance increases or when long wiring routes are used, so they should be checked once the IC has been mounted.
Ceramic capacitors generally have temperature and DC bias characteristics. When selecting ceramic capacitors, use X5R or X7R or better models that offer good temperature and DC bias characteristics and high torelant voltages.

Examples of ceramic capacitor characteristics


Fig. 29: Capacitance-bias characteristics (Y5V)


Fig. 30: Capacitance-bias characteristics (X5R, X7R)


Fig. 31: Capacitance-temperature characteristics

Output capacitor
To prevent oscillation at the output, it is recommended that the IC be operated at the stable region show in below Fig. It operates at the capacitance of more than $1.0 \mu \mathrm{~F}$. As capacitance is larger, stability becomes more stable and characteristic of output load fluctuation is also improved.

## BH $\square \square L B 1 W H F V / W G$



Fig. 32 BH $\square \square L B 1 W H F V / W G$
Stable operating region characteristics (Example)
$B H \square \square F B 1 W H F V / W G$


Fig. 33 BH $\square \square F B 1$ WHFV/WG
Stable operating region characteristics (Example)

BH $\square \square M A 3 W H F V$


Fig. 34 BHDपMA3WHFV
Stable operating region characteristics (Example)

## - Other precautions

- Over current protection circuit

The IC incorporates a built-in over current protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuits use fold-back type current limiting and are designed to limit current flow by not latching up in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits.

- Thermal shutdown circuit

This system has a built-in thermal shutdown circuit for the purpose of protecting the IC from thermal damage. As shown above, this must be used within the range of power dissipation, but if the power dissipation happens to be continuously exceeded, the chip temperature increases, causing the thermal shutdown circuit to operate. When the thermal shutdown circuit operates, the operation of the circuit is suspended. The circuit resumes operation immediately after the chip temperature decreases, so the output repeats the ON and OFF states. There are cases in which the IC is destroyed due to thermal runaway when it is left in the overloaded state. Be sure to avoid leaving the IC in the overloaded state.

- Actions in strong magnetic fields

Use caution when using the IC in the presence of a strong magnetic field as such environments may occasionally cause the chip to malfunction.

- Back current

In applications where the IC may be exposed to back current flow, it is recommended to create a route t dissipate this current by inserting a bypass diode between the VIN and Vout pins.

- GND potential

Ensure a minimum GND pin potential in all operating conditions.
In addition, ensure that no pins other than the GND pin carry a voltage less than or equal to the GND pin, including during actual transient phenomena.

- Noise terminal (BHロロMA3WHFV)

The terminal is directly connected to inward normal voltage source. Because this has low current ability, load exceeding 100nA will cause some instability at the output. For such reasons, we urge you to use ceramic capacitors which have less leak current. When choosing noise the current reduction capacitor, there is a trade-off between boot-up time and stability. A bigger capacitor value will result in lesser oscillation but longer boot-up time for VOUT.


Fig. 35: Vout startup time vs. noise-filtering capacitor capacitance characteristics (Example)

- Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. $\mathrm{P} / \mathrm{N}$ junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when a resistor and transistor are connected to pins as shown in Fig. 37
$\bigcirc$ The $\mathrm{P} / \mathrm{N}$ junction functions as a parasitic diode when GND $>(\operatorname{Pin} \mathrm{A})$ for the resistor or GND > (Pin B) for the transistor (NPN).
OSimilarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltage lower than the GND (P substrate) voltage to input pins.


Fig. 36: Example of bypass diode connection


Fig. 37


Part number selection



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