Triple Voltage Monitors, POR, 2 kbit EEPROM Memory, and Single/Dual DCP

FEATURES

- Triple Voltage Monitors
  - —User Programmable Threshold Voltage
  - —Power-on Reset (POR) Circuitry
  - —Software Selectable Reset timeout
  - —Manual Reset Input
- 2-Wire industry standard Serial Interface
- 2 kbit EEPROM with Write Protect & Block Lock™
- Digitally Controlled Potentiometers (DCP)

X4023X Family Selector Guide

X=	256 tap	100 tap	64 Tap
1			1
3		1	
5	1		
7	1		1
9	1	1	

  - —Total Resistance
    256 Tap = 100kΩ, 100 Tap or 64 Tap = 10kΩ
  - —Nonvolatile wiper position
  - —Write Protect Function
- Single Supply Operation
  - —2.7V to 5.5V
- 16 Pin SOIC (300) package
  - —SOIC

DESCRIPTION

The X4023x family of Integrated System Management ICs combine CPU Supervisor functions (V_{CC} Power-onpower-on Reset (POR) circuitry, two additional programmable voltage monitor inputs with software and hardware indicators), integrated EEPROM with Block Lock™ protection and one or two Intersil Digitally Controlled Potentiometers (XDCP). All functions of the X4023x are accessed by an industry standard 2-Wire serial interface.

APPLICATIONS

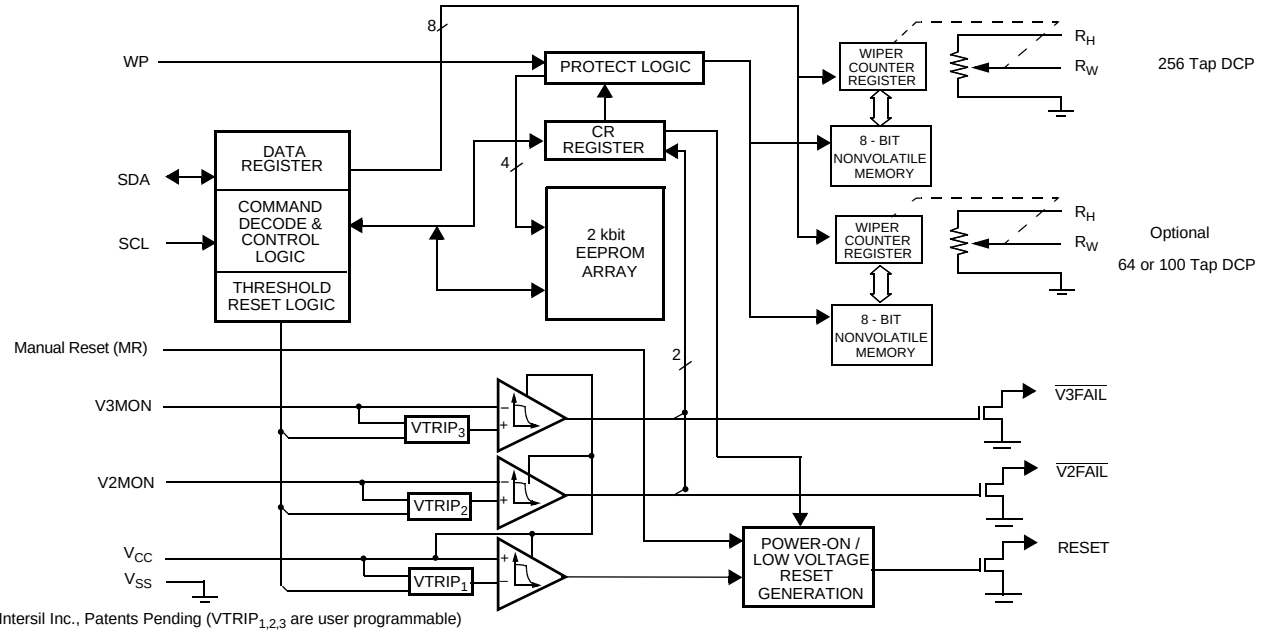
The DCP of the X4023x may be utilized to software control analog voltages for:

– LCD contrast, LCD purity, or Backlight control.
– Power Supply settings such as PWM frequency, Voltage Trimming or Margining (temperature offset control).
– Reference voltage setting (e.g. DDR-SDRAM SSTL-2)

The 2 kbit integrated EEPROM may be used to store ID, manufacturer data, maintenance data and module definition data.

The programmable POR circuit insures V_{CC} is stable before RESET is removed and protects against brown-outs and power failures. The programmable voltage monitors have on-chip independent reference alarm levels. With separate outputs, the voltage monitors can be used for power-on sequencing.

BLOCK DIAGRAM

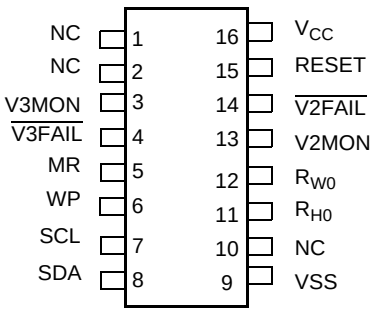


PIN CONFIGURATION

SINGLE XDCP

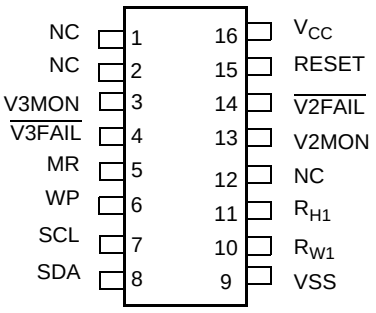
X40231

16 Pin SOIC



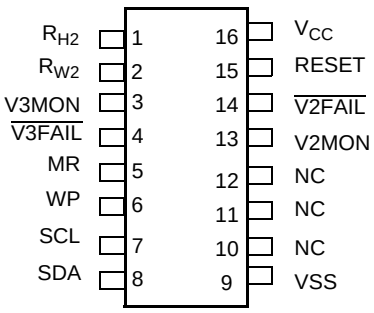
X40233

16 Pin SOIC



X40235

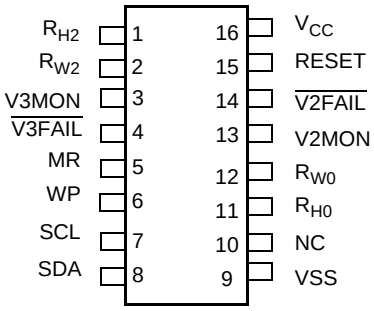
16 Pin SOIC



DUAL XDCP

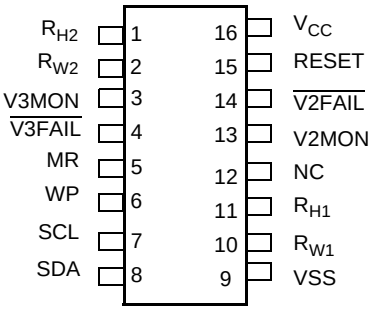
X40237

16 Pin SOIC



X40239

16 Pin SOIC



X40231 PIN ASSIGNMENT

SOIC	Name	Function
1	NC	**No Connect**
2	NC	**No Connect**
3	V3MON	**V3MON Voltage Monitor Input.** V3MON i s the input to a non-inverting voltage comparator circuit. When the V3MON input is higher than the V_{TRIP3} threshold voltage, $\overline{V3FAIL}$ makes a transition to a HIGH level. Connect V3MON to V_{SS} when not used.
4	$\overline{V3FAIL}$	**V3MON RESET Output.** This open drain output makes a transition to a HIGH level when V3MON is greater than V_{TRIP3} and goes LOW when V3MON is less than VTRIP3. There is no delay circuitry on this pin. The $\overline{V3FAIL}$ pin requires the use of an external “pull-up” resistor.
5	MR	**Manual Reset.** MR is a TTL level compatible input. Pulling the MR pin active (HIGH) initiates a reset cycle to the RESET pin (V_{CC} RESET Output pin). RESET will remain HIGH for time t_{PURST} after MR has returned to it’s normally LOW state. The reset time can be selected using bits PUP1 and PUP0 in the CR Register. The MR pin requires the use of an external “pull-down” resistor.
6	WP	**Write Protect Control Pin.** WP pin is a TTL level compatible input. When held HIGH, Write Protection is enabled. In the enabled state, this pin prevents all nonvolatile “write” operations. Also, when the Write Protection is enabled, and the device Block Lock feature is active (i.e. the Block Lock bits are NOT [0,0]), then no “write” (volatile or nonvolatile) operations can be performed in the device (including the wiper position of any of the integrated Digitally Controlled Potentiometers (DCPs). The WP pin uses an internal “pull-down” resistor, thus if left floating the write protection feature is disabled.
7	SCL	**Serial Clock.** This is a TTL level compatible input pin used to control the serial bus timing for data input and output.
8	SDA	**Serial Data.** SDA is a bidirectional TTL level compatible pin used to transfer data into and out of the device. The SDA pin input buffer is always active (not gated). This pin requires an external pull up resistor.
9	VSS	**Ground**.
10	NC	**No Connect**
11	R_{H0}	**Connection to end of resistor array for (the 64 Tap) DCP.**
12	R_{W0}	**Connection to terminal equivalent to the “Wiper” of a mechanical potentiometer for DCP.**
13	V2MON	**V2MON Voltage Monitor Input.** V2MON is the input to a non-inverting voltage comparator circuit. When the V2MON input is greater than the V_{TRIP2} threshold voltage, $\overline{V2FAIL}$ makes a transition to a HIGH level. Connect V2MON to V_{SS} when not used.
14	$\overline{V2FAIL}$	**V2MON RESET Output.** This open drain output makes a transition to a HIGH level when V2MON is greater than V_{TRIP2}, and goes LOW when V2MON is less than V_{TRIP2}. There is no power-up reset delay circuitry on this pin. The $\overline{V2FAIL}$ pin requires the use of an external “pull-up” resistor.
15	RESET	**V_{CC} RESET Output.** This is an active HIGH, open drain output which becomes active whenever V_{CC} falls below V_{TRIP1}. RESET becomes active on power-up and remains active for a time t_{PURST} after the power supply stabilizes (t_{PURST} can be changed by varying the PUP0 and PUP1 bits of the internal control register). The RESET pin requires the use of an external “pull-up” resistor. The RESET pin can be forced active (HIGH) using the manual reset (MR) input pin.
16	V_{CC}	**Supply Voltage.**

X40233 PIN ASSIGNMENT

SOIC	Name	Function
1	NC	**No Connect**
2	NC	**No Connect**
3	V3MON	**V3MON Voltage Monitor Input.** V3MON is the input to a non-inverting voltage comparator circuit. When the V3MON input is higher than the V_{TRIP3} threshold voltage, $\overline{V3FAIL}$ makes a transition to a HIGH level. Connect V3MON to V_{SS} when not used.
4	$\overline{V3FAIL}$	**V3MON RESET Output.** This open drain output makes a transition to a HIGH level when V3MON is greater than V_{TRIP3} and goes LOW when V3MON is less than VTRIP3. There is no delay circuitry on this pin. The $\overline{V3FAIL}$ pin requires the use of an external “pull-up” resistor.
5	MR	**Manual Reset.** MR is a TTL level compatible input. Pulling the MR pin active (HIGH) initiates a reset cycle to the RESET pin (V_{CC} RESET Output pin). RESET will remain HIGH for time t_{PURST} after MR has returned to it’s normally LOW state. The reset time can be selected using bits PUP1 and PUP0 in the CR Register. The MR pin requires the use of an external “pull-down” resistor.
6	WP	**Write Protect Control Pin.** WP pin is a TTL level compatible input. When held HIGH, Write Protection is enabled. In the enabled state, this pin prevents all nonvolatile “write” operations. Also, when the Write Protection is enabled, and the device Block Lock feature is active (i.e. the Block Lock bits are NOT [0,0]), then no “write” (volatile or nonvolatile) operations can be performed in the device (including the wiper position of any of the integrated Digitally Controlled Potentiometers (DCPs). The WP pin uses an internal “pull-down” resistor, thus if left floating the write protection feature is disabled.
7	SCL	**Serial Clock.** This is a TTL level compatible input pin used to control the serial bus timing for data input and output.
8	SDA	**Serial Data.** SDA is a bidirectional TTL level compatible pin used to transfer data into and out of the device. The SDA pin input buffer is always active (not gated). This pin requires an external pull up resistor.
9	VSS	**Ground.**
10	R_{W1}	**Connection to terminal equivalent to the “Wiper” of a mechanical potentiometer for DCP.**
11	R_{H1}	**Connection to end of resistor array for (the 100 Tap) DCP.**
12	NC	**No Connect**
13	V2MON	**V2MON Voltage Monitor Input.** V2MON is the input to a non-inverting voltage comparator circuit. When the V2MON input is greater than the V_{TRIP2} threshold voltage, $\overline{V2FAIL}$ makes a transition to a HIGH level. Connect V2MON to V_{SS} when not used.
14	$\overline{V2FAIL}$	**V2MON RESET Output.** This open drain output makes a transition to a HIGH level when V2MON is greater than V_{TRIP2}, and goes LOW when V2MON is less than V_{TRIP2}. There is no power-up reset delay circuitry on this pin. The $\overline{V2FAIL}$ pin requires the use of an external “pull-up” resistor.
15	RESET	**V_{CC} RESET Output.** This is an active HIGH, open drain output which becomes active whenever V_{CC} falls below V_{TRIP1}. RESET becomes active on power-up and remains active for a time t_{PURST} after the power supply stabilizes (t_{PURST} can be changed by varying the PUP0 and PUP1 bits of the internal control register). The RESET pin requires the use of an external “pull-up” resistor. The RESET pin can be forced active (HIGH) using the manual reset (MR) input pin.
16	V_{CC}	**Supply Voltage.**

X40235 PIN ASSIGNMENT

SOIC	Name	Function
1	R_{H2}	**Connection to end of resistor array for (the 256 Tap) DCP.**
2	R_{W2}	**Connection to terminal equivalent to the "Wiper" of a mechanical potentiometer for DCP.**
3	V3MON	**V3MON Voltage Monitor Input.** V3MON is the input to a non-inverting voltage comparator circuit. When the V3MON input is higher than the V_{TRIP3} threshold voltage, $\overline{\text{V3FAIL}}$ makes a transition to a HIGH level. Connect V3MON to V_{SS} when not used.
4	$\overline{\text{V3FAIL}}$	**V3MON RESET Output.** This open drain output makes a transition to a HIGH level when V3MON is greater than V_{TRIP3} and goes LOW when V3MON is less than VTRIP3. There is no delay circuitry on this pin. The $\overline{\text{V3FAIL}}$ pin requires the use of an external "pull-up" resistor.
5	MR	**Manual Reset.** MR is a TTL level compatible input. Pulling the MR pin active (HIGH) initiates a reset cycle to the RESET pin (V_{CC} RESET Output pin). RESET will remain HIGH for time t_{PURST} after MR has returned to it's normally LOW state. The reset time can be selected using bits PUP1 and PUP0 in the CR Register. The MR pin requires the use of an external "pull-down" resistor.
6	WP	**Write Protect Control Pin.** WP pin is a TTL level compatible input. When held HIGH, Write Protection is enabled. In the enabled state, this pin prevents all nonvolatile "write" operations. Also, when the Write Protection is enabled, and the device Block Lock feature is active (i.e. the Block Lock bits are NOT [0,0]), then no "write" (volatile or nonvolatile) operations can be performed in the device (including the wiper position of any of the integrated Digitally Controlled Potentiometers (DCPs). The WP pin uses an internal "pull-down" resistor, thus if left floating the write protection feature is disabled.
7	SCL	**Serial Clock.** This is a TTL level compatible input pin used to control the serial bus timing for data input and output.
8	SDA	**Serial Data.** SDA is a bidirectional TTL level compatible pin used to transfer data into and out of the device. The SDA pin input buffer is always active (not gated). This pin requires an external pull up resistor.
9	VSS	**Ground**.
10	NC	**No Connect**
11	NC	**No Connect**
12	NC	**No Connect**
13	V2MON	**V2MON Voltage Monitor Input.** V2MON is the input to a non-inverting voltage comparator circuit. When the V2MON input is greater than the V_{TRIP2} threshold voltage, $\overline{\text{V2FAIL}}$ makes a transition to a HIGH level. Connect V2MON to V_{SS} when not used.
14	$\overline{\text{V2FAIL}}$	**V2MON RESET Output.** This open drain output makes a transition to a HIGH level when V2MON is greater than V_{TRIP2}, and goes LOW when V2MON is less than V_{TRIP2}. There is no power-uppower-up reset delay circuitry on this pin. The $\overline{\text{V2FAIL}}$ pin requires the use of an external "pull-up" resistor.
15	RESET	**V_{CC} RESET Output.** This is an active HIGH, open drain output which becomes active whenever V_{CC} falls below V_{TRIP1}. RESET becomes active on power-up and remains active for a time t_{PURST} after the power supply stabilizes (t_{PURST} can be changed by varying the PUP0 and PUP1 bits of the internal control register). The RESET pin requires the use of an external "pull-up" resistor. The RESET pin can be forced active (HIGH) using the manual reset (MR) input pin.
16	V_{CC}	**Supply Voltage.**

X40237 PIN ASSIGNMENT

SOIC	Name	Function
1	R_{H2}	**Connection to end of resistor array for (the 256 Tap) DCP2.**
2	R_{W2}	**Connection to terminal equivalent to the "Wiper" of a mechanical potentiometer for DCP2.**
3	V3MON	**V3MON Voltage Monitor Input.** V3MON is the input to a non-inverting voltage comparator circuit. When the V3MON input is higher than the V_{TRIP3} threshold voltage, $\overline{V3FAIL}$ makes a transition to a HIGH level. Connect V3MON to V_{SS} when not used.
4	$\overline{V3FAIL}$	**V3MON RESET Output.** This open drain output makes a transition to a HIGH level when V3MON is greater than V_{TRIP3} and goes LOW when V3MON is less than VTRIP3. There is no delay circuitry on this pin. The $\overline{V3FAIL}$ pin requires the use of an external "pull-up" resistor.
5	MR	**Manual Reset. MR is a TTL level compatible input.** Pulling the MR pin active (HIGH) initiates a reset cycle to the RESET pin (V_{CC} RESET Output pin). RESET will remain HIGH for time t_{PURST} after MR has returned to it's normally LOW state. The reset time can be selected using bits PUP1 and PUP0 in the CR Register. The MR pin requires the use of an external "pull-down" resistor.
6	WP	**Write Protect Control Pin.** WP pin is a TTL level compatible input. When held HIGH, Write Protection is enabled. In the enabled state, this pin prevents all nonvolatile "write" operations. Also, when the Write Protection is enabled, and the device Block Lock feature is active (i.e. the Block Lock bits are NOT [0,0]), then no "write" (volatile or nonvolatile) operations can be performed in the device (including the wiper position of any of the integrated Digitally Controlled Potentiometers (DCPs). The WP pin uses an internal "pull-down" resistor, thus if left floating the write protection feature is disabled.
7	SCL	**Serial Clock.** This is a TTL level compatible input pin used to control the serial bus timing for data input and output.
8	SDA	**Serial Data.** SDA is a bidirectional TTL level compatible pin used to transfer data into and out of the device. The SDA pin input buffer is always active (not gated). This pin requires an external pull up resistor.
9	VSS	**Ground.**
10	NC	**No Connect**
11	R_{H0}	**Connection to end of resistor array for (the 64 Tap) DCP0.**
12	R_{W0}	**Connection to terminal equivalent to the "Wiper" of a mechanical potentiometer for DCP0.**
13	V2MON	**V2MON Voltage Monitor Input.** V2MON is the input to a non-inverting voltage comparator circuit. When the V2MON input is greater than the V_{TRIP2} threshold voltage, $\overline{V2FAIL}$ makes a transition to a HIGH level. Connect V2MON to V_{SS} when not used.
14	$\overline{V2FAIL}$	**V2MON RESET Output.** This open drain output makes a transition to a HIGH level when V2MON is greater than V_{TRIP2}, and goes LOW when V2MON is less than V_{TRIP2}. There is no power-uppower-up reset delay circuitry on this pin. The $\overline{V2FAIL}$ pin requires the use of an external "pull-up" resistor.
15	RESET	**V_{CC} RESET Output.** This is an active HIGH, open drain output which becomes active whenever V_{CC} falls below V_{TRIP1}. RESET becomes active on power-up and remains active for a time t_{PURST} after the power supply stabilizes (t_{PURST} can be changed by varying the PUP0 and PUP1 bits of the internal control register). The RESET pin requires the use of an external "pull-up" resistor. The RESET pin can be forced active (HIGH) using the manual reset (MR) input pin.
16	V_{CC}	**Supply Voltage.**

X40239 PIN ASSIGNMENT

SOIC	Name	Function
1	R_{H2}	**Connection to end of resistor array for (the 256 Tap) DCP2.**
2	R_{W2}	**Connection to terminal equivalent to the "Wiper" of a mechanical potentiometer for DCP2.**
3	V3MON	**V3MON Voltage Monitor Input.** V3MON is the input to a non-inverting voltage comparator circuit. When the V3MON input is higher than the V_{TRIP3} threshold voltage, $\overline{V3FAIL}$ makes a transition to a HIGH level. Connect V3MON to V_{SS} when not used.
4	$\overline{V3FAIL}$	**V3MON RESET Output.** This open drain output makes a transition to a HIGH level when V3MON is greater than V_{TRIP3} and goes LOW when V3MON is less than V_{TRIP3}. There is no delay circuitry on this pin. The $\overline{V3FAIL}$ pin requires the use of an external "pull-up" resistor.
5	MR	**Manual Reset. MR is a TTL level compatible input.** Pulling the MR pin active (HIGH) initiates a reset cycle to the RESET pin (V_{CC} RESET Output pin). RESET will remain HIGH for time t_{PURST} after MR has returned to it's normally LOW state. The reset time can be selected using bits PUP1 and PUP0 in the CR Register. The MR pin requires the use of an external "pull-down" resistor.
6	WP	**Write Protect Control Pin.** WP pin is a TTL level compatible input. When held HIGH, Write Protection is enabled. In the enabled state, this pin prevents all nonvolatile "write" operations. Also, when the Write Protection is enabled, and the device Block Lock feature is active (i.e. the Block Lock bits are NOT [0,0]), then no "write" (volatile or nonvolatile) operations can be performed in the device (including the wiper position of any of the integrated Digitally Controlled Potentiometers (DCPs). The WP pin uses an internal "pull-down" resistor, thus if left floating the write protection feature is disabled.
7	SCL	**Serial Clock.** This is a TTL level compatible input pin used to control the serial bus timing for data input and output.
8	SDA	**Serial Data.** SDA is a bidirectional TTL level compatible pin used to transfer data into and out of the device. The SDA pin input buffer is always active (not gated). This pin requires an external pull up resistor.
9	VSS	**Ground.**
10	R_{W1}	**Connection to terminal equivalent to the "Wiper" of a mechanical potentiometer for DCP1.**
11	R_{H1}	**Connection to end of resistor array for (the 100 Tap) DCP1.**
12	NC	**No Connect**
13	V2MON	**V2MON Voltage Monitor Input.** V2MON is the input to a non-inverting voltage comparator circuit. When the V2MON input is greater than the V_{TRIP2} threshold voltage, $\overline{V2FAIL}$ makes a transition to a HIGH level. Connect V2MON to V_{SS} when not used.
14	$\overline{V2FAIL}$	**V2MON RESET Output.** This open drain output makes a transition to a HIGH level when V2MON is greater than V_{TRIP2}, and goes LOW when V2MON is less than V_{TRIP2}. There is no power-up reset delay circuitry on this pin. The $\overline{V2FAIL}$ pin requires the use of an external "pull-up" resistor.
15	RESET	**V_{CC} RESET Output.** This is an active HIGH, open drain output which becomes active whenever V_{CC} falls below V_{TRIP1}. RESET becomes active on power-up and remains active for a time t_{PURST} after the power supply stabilizes (t_{PURST} can be changed by varying the PUP0 and PUP1 bits of the internal control register). The RESET pin requires the use of an external "pull-up" resistor. The RESET pin can be forced active (HIGH) using the manual reset (MR) input pin.
16	V_{CC}	**Supply Voltage.**

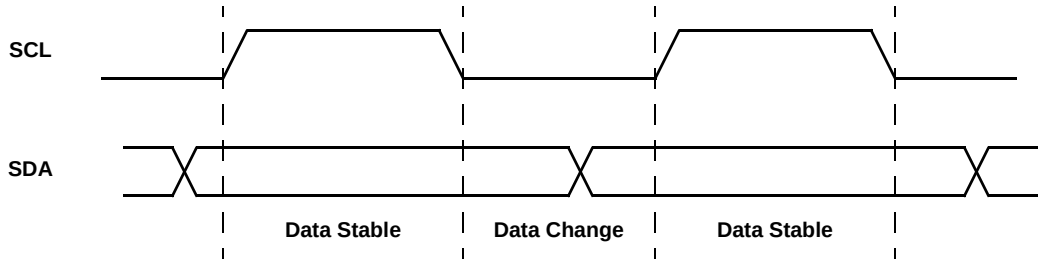


Figure 1. Valid Data Changes on the SDA Bus

DETAILED DEVICE DESCRIPTION

The X4023x combines One or Two Intersil Digitally Controlled Potentiometer (XDCP) devices, V_{CC} power-on reset control, V_{CC} low voltage reset control, two supplementary voltage monitors with independent outputs, and integrated EEPROM with Block Lock™ protection, in one package. The integrated functionality of the X4023x lowers system cost, increases reliability, and reduces board space requirements.

DCPs allow for the “set-and-forget” adjustment during production test or in-system updating via the industry standard 2-wire interface.

Applying voltage to V_{CC} activates the Power-on Reset circuit which sets the RESET output HIGH, until the supply voltage stabilizes for a period of time (50-300 msec selectable via software). The RESET output then goes LOW. The Low Voltage Reset circuit sets the RESET output HIGH when V_{CC} falls below the minimum V_{CC} trip point. RESET remains HIGH until V_{CC} returns to proper operating level and stabilizes for a period of time (t_{PURST}). A Manual Reset (MR) input allows the user to externally activate the RESET output.

Two supplementary Voltage Monitor circuits, V2MON and V3MON, continuously compare their inputs to individual trip voltages (independent on-chip voltage references factory set and user programmable). When an input voltage exceeds it’s associated trip level, the corresponding output ($\overline{V3FAIL}$, $\overline{V2FAIL}$) goes HIGH. When the input voltage becomes lower than it’s associated trip level, the corresponding output is driven LOW. A corresponding binary representation of the two monitor circuit outputs ($\overline{V2FAIL}$ and $\overline{V3FAIL}$) are also stored in latched, volatile (CR) register bits. The status of these two monitor outputs can be read out via the 2-wire serial port. The bits will remain SET, even after the alarm condition is removed, allowing advanced recovery algorithms to be implemented.

Intersil’s unique circuits allow for all internal trip voltages to be individually programmed with high accuracy, either by Intersil at final test or by the user during their production process. Some distributors offer V_{TRIP} reprogramming as a value added service. This gives the designer great flexibility in changing system parameters, either at the time of manufacture, or in the field.

The memory portion of the device is a CMOS serial EEPROM array with Intersil’s Block Lock™ protection. This memory may be used to store module manufacturing data, serial numbers, or various other system parameters. The EEPROM array is internally organized as x 8, and utilizes Intersil’s proprietary Direct Write™ cells providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

The device features a 2-Wire interface.

PRINCIPLES OF OPERATION

SERIAL INTERFACE

Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. The X4023x operates as a slave in all applications.

Serial Clock and Data

Data states on the SDA line can change only while SCL is LOW (see Figure 1). SDA state changes while SCL is HIGH are reserved for indicating START and STOP conditions. See Figure 1. On power-up of the X4023x, the SDA pin is in the input mode.

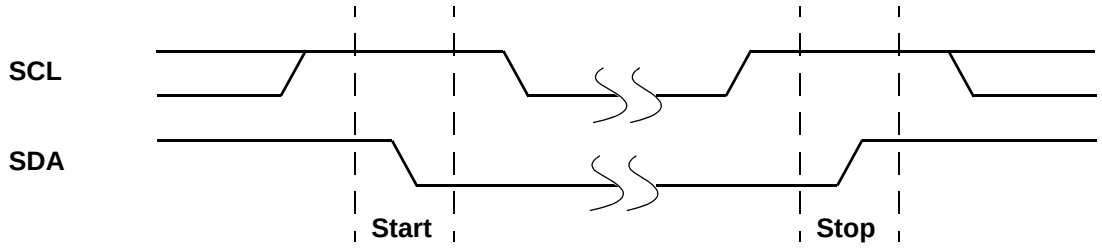


Figure 2. Valid Start and Stop Conditions

Serial Start Condition

All commands are preceded by the START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition has been met. See Figure 2.

Serial Stop Condition

All communications must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. The STOP condition is also used to place the device into the Standby power mode after a read sequence. A STOP condition can only be issued after the transmitting device has released the bus. See Figure 2.

Serial Acknowledge

An ACKNOWLEDGE (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKNOWLEDGE that it received the eight bits of data. Refer to Figure 3

The device will respond with an ACKNOWLEDGE after recognition of a START condition if the correct Device Identifier bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an ACKNOWLEDGE after the receipt of each subsequent eight bit word.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an ACKNOWLEDGE. If an ACKNOWLEDGE is detected and no STOP condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an ACKNOWLEDGE is not detected. The master must then issue a STOP condition to place the device into a known state.

DEVICE INTERNAL ADDRESSING

Addressing Protocol Overview

The user addressable internal components of the X4023x can be split up into three main parts:

—One or Two Digitally Controlled Potentiometers (DCPs)

—EEPROM array

—Control and Status (CR) Register

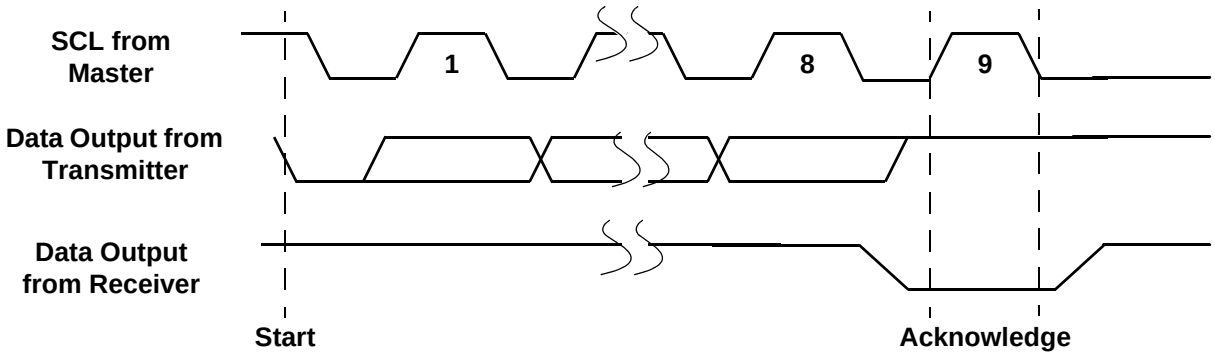


Figure 3. Acknowledge Response From Receiver

Depending upon the operation to be performed on each of these individual parts, a 1, 2 or 3 Byte protocol is used. All operations however must begin with the Slave Address Byte being issued on the SDA pin. The Slave address selects the part of the X4023x to be addressed, and specifies if a Read or Write operation is to be performed.

It should be noted that in order to perform a write operation to either a DCP or the EEPROM array, the Write Enable Latch (WEL) bit must first be set (See “BL1, BL0: Block Lock protection bits - (Nonvolatile)” on page 18.)

Slave Address Byte

Following a START condition, the master must output a Slave Address Byte (Refer to Figure 4). This byte consists of three parts:

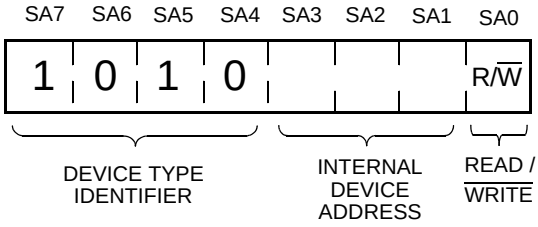
—The Device Type Identifier which consists of the most significant four bits of the Slave Address (SA7 - SA4). The Device Type Identifier must always be set to 1010 in order to select the X4023x.

—The next three bits (SA3 - SA1) are the Internal Device Address bits. Setting these bits to 000 internally selects the EEPROM array, while setting these bits to 111 selects the DCP structures in the X4023x. The CR Register may be selected using the Internal Device Address 010.

—The Least Significant Bit of the Slave Address (SA0) Byte is the R/$\overline{W}$ bit. This bit defines the operation to be performed on the device being addressed (as defined in the bits SA3 - SA1). When the R/$\overline{W}$ bit is “1”, then a READ operation is selected. A “0” selects a WRITE operation (Refer to Figure 4)

Nonvolatile Write Acknowledge Polling

After a nonvolatile write command sequence (for either the EEPROM array, the Non Volatile Memory of a DCP (NVM), or the CR Register) has been correctly issued (including the final STOP condition), the X4023x initiates an internal high voltage write cycle. This cycle typically requires 5 ms. During this time, no further Read or Write commands can be issued to the device. Write Acknowledge Polling is used to determine when this high voltage write cycle has been completed.



Internal Address (SA3 - SA1)	Internally Addressed Device
000	EEPROM Array
010	CR Register
111	DCP

Bit SA0	Operation
0	WRITE
1	READ

Figure 4. Slave Address Format

To perform acknowledge polling, the master issues a START condition followed by a Slave Address Byte. The Slave Address issued must contain a valid Internal Device Address. The LSB of the Slave Address (R/$\overline{W}$) can be set to either 1 or 0 in this case. If the device is still busy with the high voltage cycle then no ACKNOWLEDGE will be returned. If the device has completed the write operation, an ACKNOWLEDGE will be returned and the host can then proceed with a read or write operation. (Refer to Figure 5)

DIGITALLY CONTROLLED POTENTIOMETERS

DCP Functionality

The X4023x includes one or two independent resistor arrays. For the 64, 100 or 256 tap XDCPs, these arrays respectively contain 63, 99 discrete resistive segments that are connected in series. (the 256 tap resistor achieves an equivalent end to end resistance.) The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer. At one end of the resistor array the terminal connects to the R_{Hx} pin (x = 0,1,2).The other end of the resistor array is connected to V_{SS} inside the package.

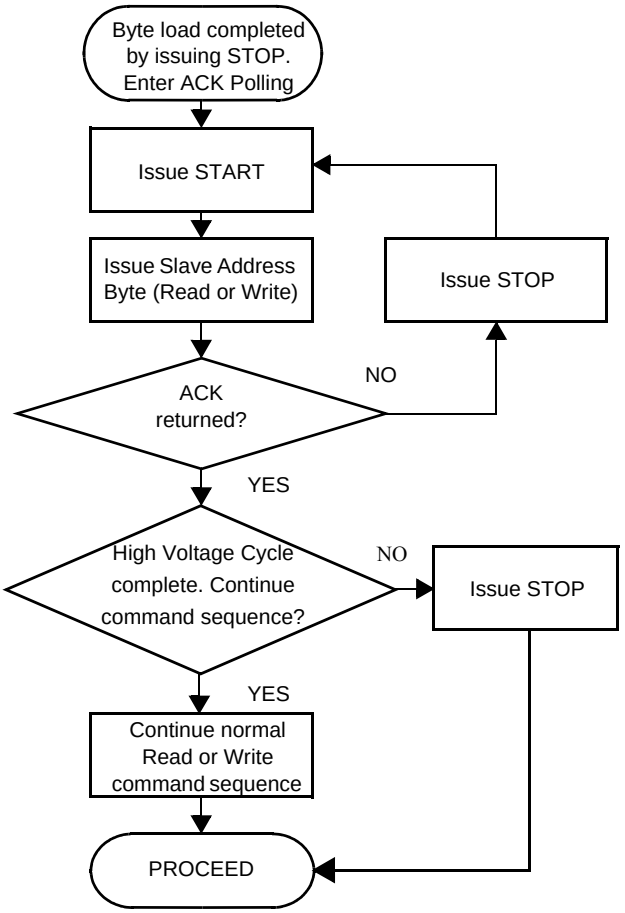


Figure 5. Acknowledge Polling Sequence

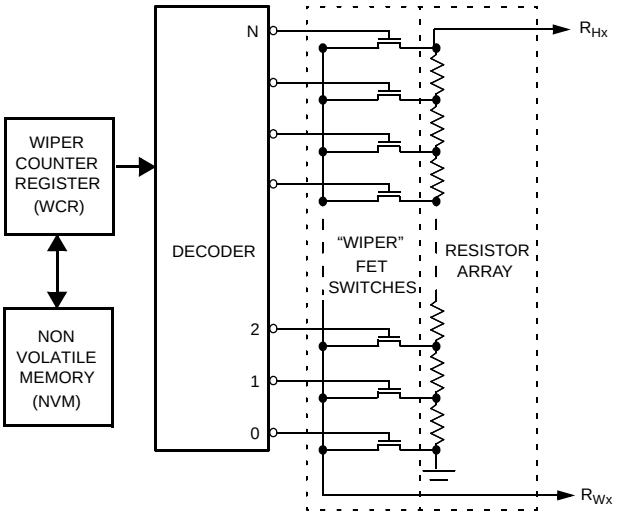


Figure 6. DCP Internal Structure

At both ends of each array and between each resistor segment there is a CMOS switch connected between the resistor array and the wiper (R_{Wx}) output. Within each individual array, only one switch may be turned on at any one time. These switches are controlled by the Wiper Counter Register (WCR) (See Figure 6). The WCR is a volatile register.

On power-up of the X4023x, wiper position data is automatically loaded into the WCR from its associated Non Volatile Memory (NVM) Register. The Table below shows the Initial Values of the DCP WCR's before the contents of the NVM is loaded into the WCR.

DCP	Initial Values Before Recall
R_0 (64 TAP)	V_H (TAP = 63)
R_1 (100 TAP)	V_L (TAP = 0)
R_2 (256 TAP)	V_H (TAP = 255)

The data in the WCR is then decoded to select and enable one of the respective FET switches. A "make before break" sequence is used internally for the FET switches when the wiper is moved from one tap position to another.

Hot Pluggability

Figure 7 shows a typical waveform that the X4023x might experience in a Hot Pluggable situation. On power-up, V_{CC} applied to the X4023x may exhibit some amount of ringing, before it settles to the required value.

The device is designed such that the wiper terminal (R_{Wx}) is recalled to the correct position (as per the last stored in the DCP NVM), when the voltage applied to V_{CC} exceeds V_{TRIP1} for a time exceeding t_{PURST} (the Power-on Reset time, set in the CR Register - See "CONTROL AND STATUS REGISTER" on page 18.).

Therefore, if t_{trans} is defined as the time taken for V_{CC} to settle above V_{TRIP1} (Figure 7): then the desired wiper terminal position is recalled by (a maximum) time: $t_{trans} + t_{PURST}$. It should be noted that t_{trans} is determined by system hot plug conditions.

DCP Operations

In total there are three operations that can be performed on any internal DCP structure:

—DCP Nonvolatile Write

—DCP Volatile Write

—DCP Read

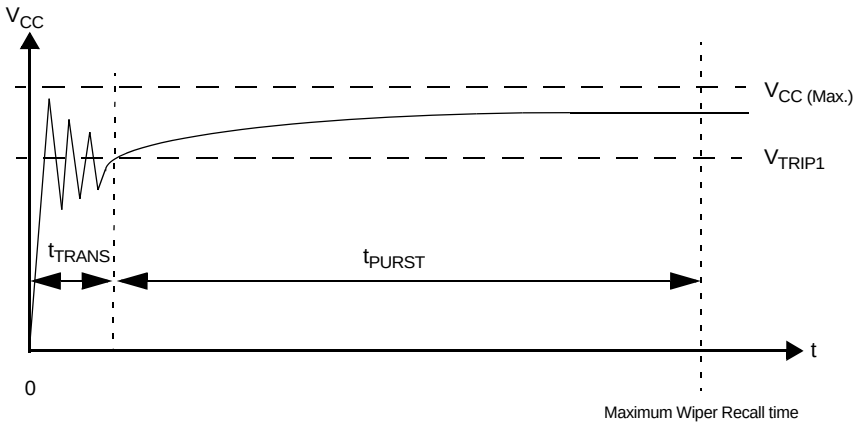


Figure 7. DCP Power-up

A nonvolatile write to a DCP will change the "wiper position" by simultaneously writing new data to the associated WCR and NVM. Therefore, the new "wiper position" setting is recalled into the WCR after V_{CC} of the X4023x is powered down and then powered back up.

A volatile write operation to a DCP however, changes the "wiper position" by writing new data to the associated WCR only. The contents of the associated NVM register remains unchanged. Therefore, when V_{CC} to the device is powered down then back up, the "wiper position" reverts to that last position written to the DCP using a nonvolatile write operation.

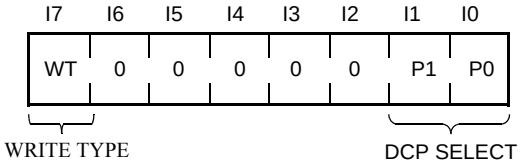
Both volatile and nonvolatile write operations are executed using a three byte command sequence: (DCP) Slave Address Byte, Instruction Byte, followed by a Data Byte (See Figure 9)

A DCP Read operation allows the user to "read out" the current "wiper position" of the DCP, as stored in the associated WCR. This operation is executed using the Random Address Read command sequence, consisting of the (DCP) Slave Address Byte followed by an Instruction Byte and the Slave Address Byte again (Refer to Figure 10).

Instruction Byte

While the Slave Address Byte is used to select the DCP devices, an Instruction Byte is used to determine which DCP is being addressed.

The Instruction Byte (Figure 8) is valid only when the Device Type Identifier and the Internal Device Address bits of the Slave Address are set to 1010111. In this case, the two Least Significant Bit's (I1 - I0) of the Instruction Byte are used to select the particular DCP (0 - 2). In the case of a Write to any of the DCPs (i.e. the LSB of the Slave Address is 0), the Most Significant Bit of the Instruction Byte (I7), determines the Write Type (WT) performed.



WT†	Description
0	Select a Volatile Write operation to be performed on the DCP pointed to by bits P1 and P0
1	Select a Nonvolatile Write operation to be performed on the DCP pointed to by bits P1 and P0

†This bit has no effect when a Read operation is being performed.

Figure 8. Instruction Byte Format

If WT is "1", then a Nonvolatile Write to the DCP occurs. In this case, the "wiper position" of the DCP is changed by simultaneously writing new data to the associated WCR and NVM. Therefore, the new "wiper position" setting is recalled into the WCR after V_{CC} of the X4023x has been powered down then powered back up.

If WT is "0" then a DCP Volatile Write is performed. This operation changes the DCP "wiper position" by writing new data to the associated WCR only. The contents of the associated NVM register remains unchanged. Therefore, when V_{CC} to the device is powered down then back up, the "wiper position" reverts to that last written to the DCP using a nonvolatile write operation.

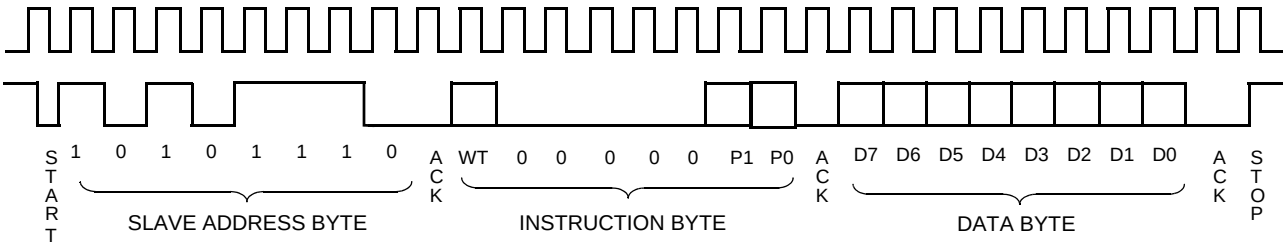


Figure 9. DCP Write Command Sequence

DCP Write Operation

A write to DCPx (x=0,1,2) can be performed using the three byte command sequence shown in Figure 9.

In order to perform a write operation on a particular DCP, the Write Enable Latch (WEL) bit of the CR Register must first be set (See “BL1, BL0: Block Lock protection bits - (Nonvolatile)” on page 18.)

The Slave Address Byte 10101110 specifies that a Write to a DCP is to be conducted. An ACKNOWLEDGE is returned by the X4023x after the Slave Address, if it has been received correctly.

Next, an Instruction Byte is issued on SDA. Bits P1 and P0 of the Instruction Byte determine which WCR is to be written, while the WT bit determines if the Write is to be volatile or nonvolatile. If the Instruction Byte format is valid, another ACKNOWLEDGE is then returned by the X4023x.

Following the Instruction Byte, a Data Byte is issued to the X4023x over SDA. The Data Byte contents is latched into the WCR of the DCP on the first rising edge of the clock signal, after the LSB of the Data Byte (D0) has been issued on SDA (See Figure 34).

The Data Byte determines the “wiper position” (which FET switch of the DCP resistive array is switched ON) of the DCP. The maximum value for the Data Byte depends upon which DCP is being addressed (see following table).

P1- P0		DCPx	# Taps	Max. Data Byte
0	0	x = 0	64	3Fh
0	1	x = 1	100	Refer to Appendix 1
1	0	x = 2	256	FFh
1	1	Reserved		

Using a Data Byte larger than the values specified above results in the “wiper terminal” being set to the highest tap position. The “wiper position” does NOT roll-over to the lowest tap position.

For DCP0 (64 Tap) and DCP2 (256 Tap), the Data Byte maps one to one to the “wiper position” of the DCP “wiper terminal”. Therefore, the Data Byte 00001111 (15_{10}) corresponds to setting the “wiper terminal” to tap position 15. Similarly, the Data Byte 00011100 (28_{10}) corresponds to setting the “wiper terminal” to tap position 28. The mapping of the Data Byte to “wiper position” data for DCP1 (100 Tap), is shown in “APPENDIX 1” . An example of a simple C language function which “translates” between the tap position (decimal) and the Data Byte (binary) for DCP1, is given in “APPENDIX 2” .

It should be noted that all writes to any DCP of the X4023x are random in nature. Therefore, the Data Byte of consecutive write operations to any DCP can differ by an arbitrary number of bits. Also, setting the bits P1 = 1, P0 = 1 is a reserved sequence, and will result in no ACKNOWLEDGE after sending an Instruction Byte on SDA.

The factory default setting of all “wiper position” settings is with 00h stored in the NVM of the DCPs. This corresponds to having the “wiper terminal” R_{WX} (x = 0,1,2) at the “lowest” tap position, Therefore, the resistance between R_{WX} and R_{LX} is a minimum (essentially only the Wiper Resistance, R_W).

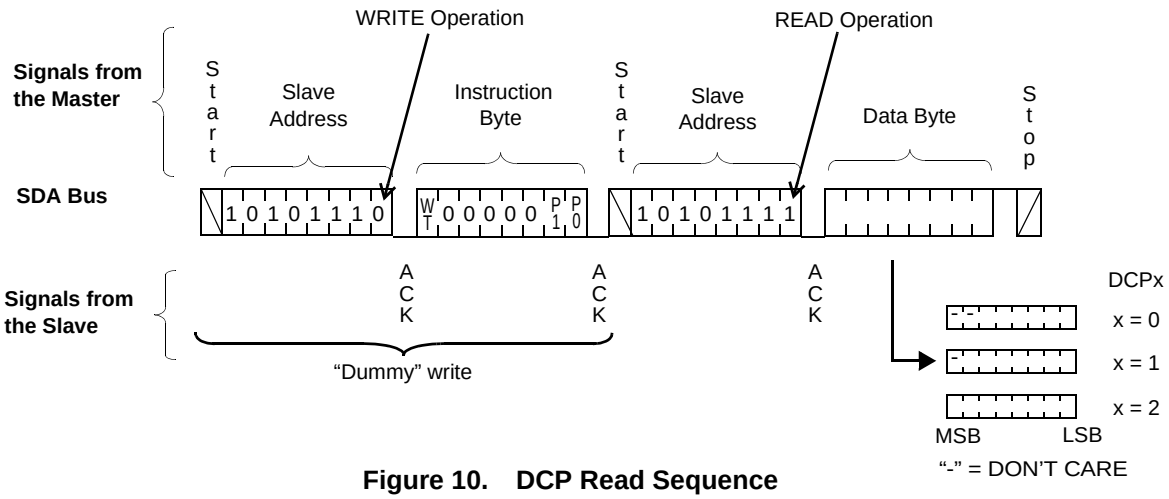


Figure 10. DCP Read Sequence

DCP Read Operation

A read of DCPx (x = 0,1,2) can be performed using the three byte random read command sequence shown in Figure 10.

The master issues the START condition and the Slave Address Byte 10101110 which specifies that a "dummy" write" is to be conducted. This "dummy" write operation sets which DCP is to be read (in the preceding Read operation). An ACKNOWLEDGE is returned by the X4023x after the Slave Address if received correctly. Next, an Instruction Byte is issued on SDA. Bits P1-P0 of the Instruction Byte determine which DCP "wiper position" is to be read. In this case, the state of the WT bit is "don't care". If the Instruction Byte format is valid, then another ACKNOWLEDGE is returned by the X4023x.

Following this ACKNOWLEDGE, the master immediately issues another START condition and a valid Slave address byte with the R/$\overline{W}$ bit set to 1. Then the X4023x issues an ACKNOWLEDGE followed by Data Byte, and finally, the master issues a STOP condition.

The Data Byte read in this operation, corresponds to the "wiper position" (value of the WCR) of the DCP pointed to by bits P1 and P0.

It should be noted that when reading out the data byte for DCP0 (64 Tap), the upper two most significant bits are "unknown" bits. For DCP1 (100 Tap), the upper most significant bit is an "unknown". For DCP2 (256 Tap) however, all bits of the data byte are relevant (See Figure 10).

2 kbit EEPROM ARRAY

Operations on the 2 kbit EEPROM Array, consist of either 1, 2 or 3 byte command sequences. All operations on the EEPROM must begin with the Device Type Identifier of the Slave Address set to 1010000. A Read or Write to the EEPROM is selected by setting the LSB of the Slave Address to the appropriate value R/$\overline{W}$ (Read = "1", Write = "0").

In some cases when performing a Read or Write to the EEPROM, an Address Byte may also need to be specified. This Address Byte can contain the values 00h to FFh.

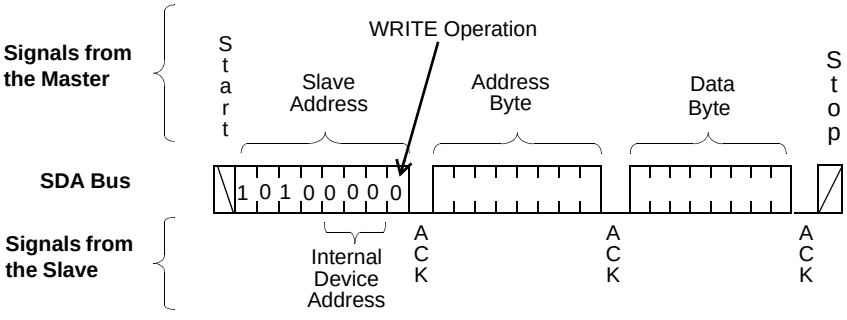


Figure 11. EEPROM Byte Write Sequence

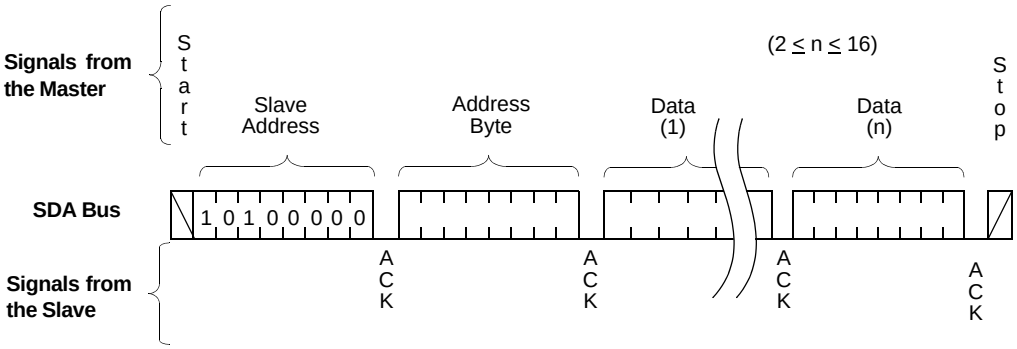


Figure 12. EEPROM Page Write Operation

EEPROM Byte Write

In order to perform an EEPROM Byte Write operation to the EEPROM array, the Write Enable Latch (WEL) bit of the CR Register must first be set (See "BL1, BL0: Block Lock protection bits - (Nonvolatile)" on page 18.)

For a write operation, the X4023x requires the Slave Address Byte and an Address Byte. This gives the master access to any one of the words in the array. After receipt of the Address Byte, the X4023x responds with an ACKNOWLEDGE, and awaits the next eight bits of data. After receiving the 8 bits of the Data Byte, it again responds with an ACKNOWLEDGE. The master then terminates the transfer by generating a STOP condition, at which time the X4023x begins the internal write cycle to the nonvolatile memory (See Figure 11). During this internal write cycle, the X4023x inputs are disabled, so it does not respond to any requests from the master. The SDA output is at high impedance. A write to a region of EEPROM memory which has been protected with the Block-Lock feature (See "BL1, BL0: Block Lock protection bits - (Nonvolatile)" on page 18.), suppresses the ACKNOWLEDGE bit after the Address Byte.

EEPROM Page Write

In order to perform an EEPROM Page Write operation to the EEPROM array, the Write Enable Latch (WEL) bit of the CR Register must first be set (See "BL1, BL0: Block Lock protection bits - (Nonvolatile)" on page 18.)

The X4023x is capable of a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the X4023x responds with an ACKNOWLEDGE, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it "rolls over" and goes back to '0' on the same page.

For example, if the master writes 12 bytes to the page starting at location 11 (decimal), the first 5 bytes are written to locations 11 through 15, while the last 7 bytes are written to locations 0 through 6. Afterwards, the address counter would point to location 7. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time (See Figure 13).

The master terminates the Data Byte loading by issuing a STOP condition, which causes the X4023x to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. See Figure 12 for the address, ACKNOWLEDGE, and data transfer sequence.

Stops and EEPROM Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and receiving the subsequent ACKNOWLEDGE signal. If the master issues a STOP within a Data Byte, or before the X4023x issues a corresponding ACKNOWLEDGE, the X4023x cancels the write operation. Therefore, the contents of the EEPROM array does not change.

EEPROM Array Read Operations

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current EEPROM Address Read, Random EEPROM Read, and Sequential EEPROM Read.

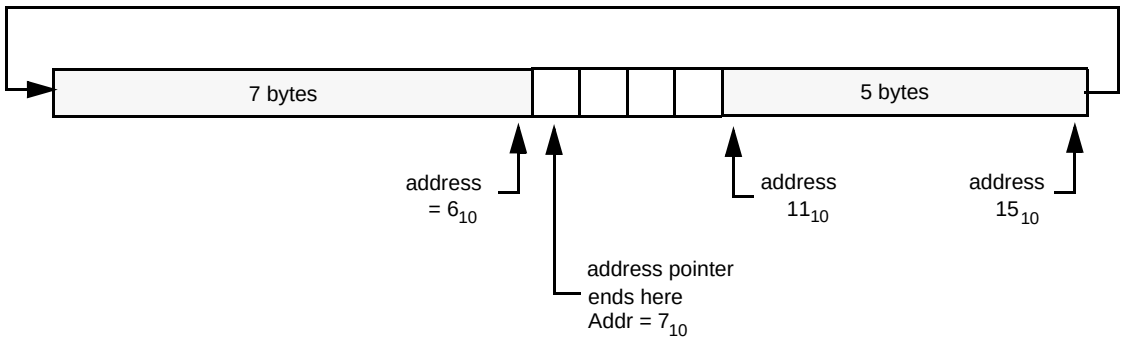


Figure 13. Example: Writing 12 bytes to a 16-byte page starting at location 11.

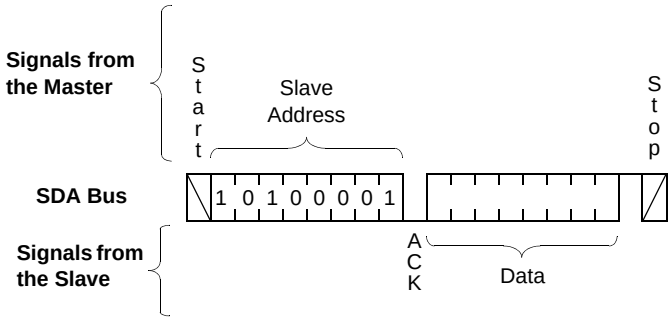


Figure 14. Current EEPROM Address Read Sequence

Current EEPROM Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an ACKNOWLEDGE and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an ACKNOWLEDGE during the ninth clock and then issues a STOP condition (See Figure 14 for the address, ACKNOWLEDGE, and data transfer sequence).

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a STOP condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a STOP condition.

Another important point to note regarding the “Current EEPROM Address Read” , is that this operation is not available if the last executed operation was an access to a DCP or the CR Register (i.e.: an operation using the Device Type Identifier 1010111 or 1010010). Immediately after an operation to a DCP or CR Register is performed, only a “Random EEPROM Read” is available. Immediately following a “Random EEPROM Read” , a “Current EEPROM Address Read” or “Sequential EEPROM Read” is once again available (assuming that no access to a DCP or CR Register occur in the interim).

Random EEPROM Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the START condition and the Slave Address Byte, receives an ACKNOWLEDGE, then issues an Address Byte. This “dummy” Write operation sets the address pointer to the address from which to begin the random EEPROM read operation.

After the X4023x acknowledges the receipt of the Address Byte, the master immediately issues another START condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an ACKNOWLEDGE from the X4023x and then by the eight bit word.

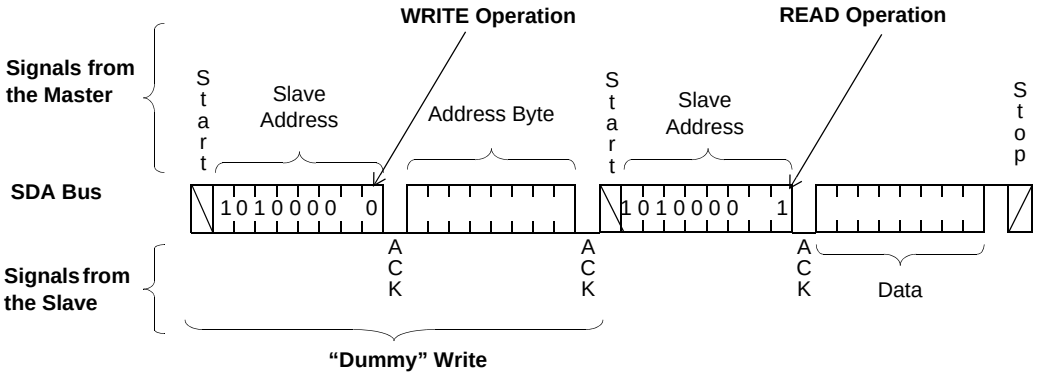


Figure 15. Random EEPROM Address Read Sequence

The master terminates the read operation by not responding with an ACKNOWLEDGE and instead issuing a STOP condition (Refer to Figure 15).

A similar operation called "Set Current Address" also exists. This operation is performed if a STOP is issued instead of the second START shown in Figure 15. In this case, the device sets the address pointer to that of the Address Byte, and then goes into standby mode after the STOP bit. All bus activity will be ignored until another START is detected.

Sequential EEPROM Read

Sequential reads can be initiated as either a current address read or random address read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an ACKNOWLEDGE, indicating it requires additional data. The X4023x continues to output a Data Byte for each ACKNOWLEDGE received. The master terminates the read operation by not responding with an ACKNOWLEDGE and instead issuing a STOP condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through the entire memory contents to be serially read during one operation. At the end of the address space the counter "rolls over" to address 00h and the device continues to output data for each ACKNOWLEDGE received (Refer to Figure 16).

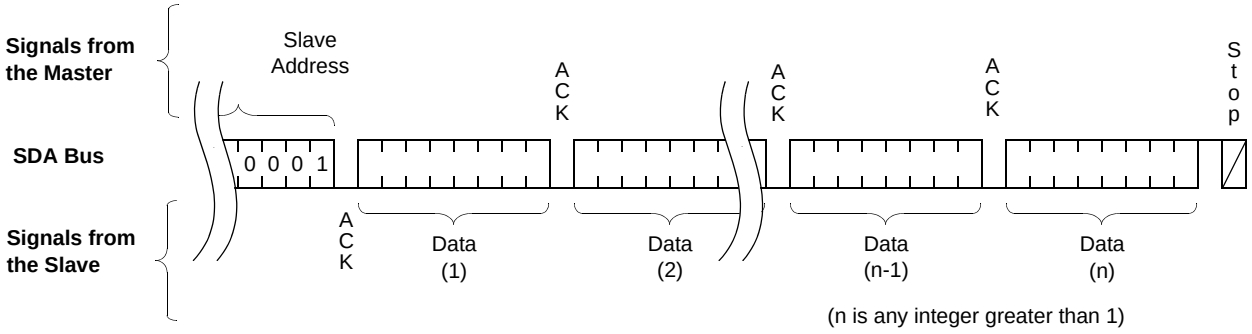
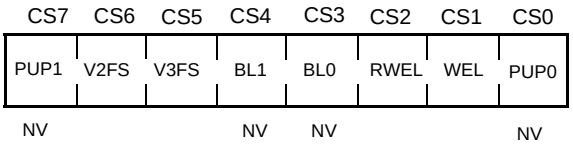


Figure 16. Sequential EEPROM Read Sequence



Bit(s)	Description
WEL	Write Enable Latch bit
RWEL	Register Write Enable Latch bit
V2FS	V2MON Output Flag Status
V3FS	V3MON Output Flag Status
BL1 - BL0	Sets the Block Lock partition
PUP1 - PUP0	Sets the Power-on Reset time

NOTE: Bits labelled NV are nonvolatile (See “CONTROL AND STATUS REGISTER”).

Figure 17. CR Register Format

CONTROL AND STATUS REGISTER

The Control and Status (CR) Register provides the user with a mechanism for changing and reading the status of various parameters of the X4023x (See Figure 17).

The CR register is a combination of both volatile and nonvolatile bits. The nonvolatile bits of the CR register retain their stored values even when V_{CC} is powered down, then powered back up. The volatile bits however, will always power-up to a known logic state “0” (irrespective of their value at power-down).

A detailed description of the function of each of the CR register bits follows:

WEL: Write Enable Latch (Volatile)

The WEL bit controls the Write Enable status of the entire X4023x device. This bit must first be enabled before ANY write operation (to DCPs, EEPROM memory array, or the CR register). If the WEL bit is not first enabled, then ANY proceeding (volatile or nonvolatile) write operation to DCPs, EEPROM array, as well as the CR register, is aborted and no ACKNOWLEDGE is issued after a Data Byte.

The WEL bit is a volatile latch that powers up in the disabled, LOW (0) state. The WEL bit is enabled / set by writing 00000010 to the CR register. Once enabled, the WEL bit remains set to “1” until either it is reset to “0” (by writing 00000000 to the CR register) or until the X4023x powers down, and then up again.

Writes to the WEL bit do not cause an internal high voltage write cycle. Therefore, the device is ready for another operation immediately after a STOP condition is executed in the CR Write command sequence (See Figure 18).

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit controls the (CR) Register Write Enable status of the X4023x. Therefore, in order to write to any of the bits of the CR Register (except WEL), the RWEL bit must first be set to “1”. The RWEL bit is a volatile bit that powers up in the disabled, LOW (“0”) state.

It must be noted that the RWEL bit can only be set, once the WEL bit has first been enabled (See "CR Register Write Operation").

The RWEL bit will reset itself to the default “0” state, in one of three cases:

—After a successful write operation to any bits of the CR register has been completed (See Figure 18).

—When the X4023x is powered down.

—When attempting to write to a Block Lock protected region of the EEPROM memory (See "BL1, BL0: Block Lock protection bits - (Nonvolatile)", below).

BL1, BL0: Block Lock protection bits - (Nonvolatile)

The Block Lock protection bits (BL1 and BL0) are used to:

—Inhibit a write operation from being performed to certain addresses of the EEPROM memory array

—Inhibit a DCP write operation (changing the “wiper position”).

The region of EEPROM memory which is protected / locked is determined by the combination of the BL1 and BL0 bits written to the CR register. It is possible to lock the regions of EEPROM memory shown in the table below:

BL1	BL0	Protected Addresses (Size)	Partition of array locked
0	0	None (Default)	None (Default)
0	1	$C0_h$ - FF_h (64 bytes)	Upper 1/4
1	0	80_h - FF_h (128 bytes)	Upper 1/2
1	1	00_h - FF_h (256 bytes)	All

If the user attempts to perform a write operation on a protected region of EEPROM memory, the operation is aborted without changing any data in the array.

When the Block Lock bits of the CR register are set to something other than BL1 = 0 and BL0 = 0, then the “wiper position” of the DCPs cannot be changed - i.e. DCP write operations cannot be conducted:

BL1	BL0	DCP Write Operation Permissible
0	0	YES (Default)
0	1	NO
1	0	NO
1	1	NO

The factory default setting for these bits are BL1 = 0, BL0 = 0.

IMPORTANT NOTE: If the Write Protect (WP) pin of the X4023x is active (HIGH), then all nonvolatile write operations to both the EEPROM memory and DCPs are inhibited, irrespective of the Block Lock bit settings (See "WP: Write Protection Pin").

PUP1, PUP0: Power-on Reset bits – (Nonvolatile)

Applying voltage to V_{CC} activates the Power-on Reset circuit which holds RESET output HIGH, until the supply voltage stabilizes above the V_{TRIP1} threshold for a period of time, t_{PURST} (See Figure 30).

The Power-on Reset bits, PUP1 and PUP0 of the CR register determine the t_{PURST} delay time of the Power-on Reset circuitry (See "VOLTAGE MONITORING FUNCTIONS"). These bits of the CR register are nonvolatile, and therefore power-up to the last written state.

The nominal Power-on Reset delay time can be selected from the following table, by writing the appropriate bits to the CR register:

PUP1	PUP0	Power-on Reset delay ($t_{PURESET}$)
0	0	50ms
0	1	100ms (Default)
1	0	200ms
1	1	300ms

The default for these bits are PUP1 = 0, PUP0 = 1.

V2FS, V3FS: Voltage Monitor Status Bits (Volatile)

Bits V2FS and V3FS of the CR register are latched, volatile flag bits which indicate the status of the Voltage Monitor reset output pins $\overline{V2FAIL}$ and $\overline{V3FAIL}$.

At power-up the VxFS (x=2,3) bits default to the value “0”. These bits can be set to a “1” by writing the appropriate value to the CR register. To provide consistency between the $\overline{VxFAIL}$ and V_{xFS} however, the status of the V_{xFS} bits can only be set to a “1” when the corresponding $\overline{VxFAIL}$ output is HIGH.

Once the VxFS bits have been set to “1”, they will be reset to “0” if:

—The device is powered down, then back up,

—The corresponding V_{xFAIL} output becomes LOW.

CR Register Write Operation

The CR register is accessed using the Slave Address set to 1010010 (Refer to Figure 4). Following the Slave Address Byte, access to the CR register requires an Address Byte which must be set to FFh. Only one data byte is allowed to be written for each CR register Write operation. The user must issue a STOP, after sending this byte to the register, to initiate the nonvolatile cycle that stores the BP1, BP0, PUP1 and PUP0 bits. The X4023x will not ACKNOWLEDGE any data bytes written after the first byte is entered (Refer to Figure 18).

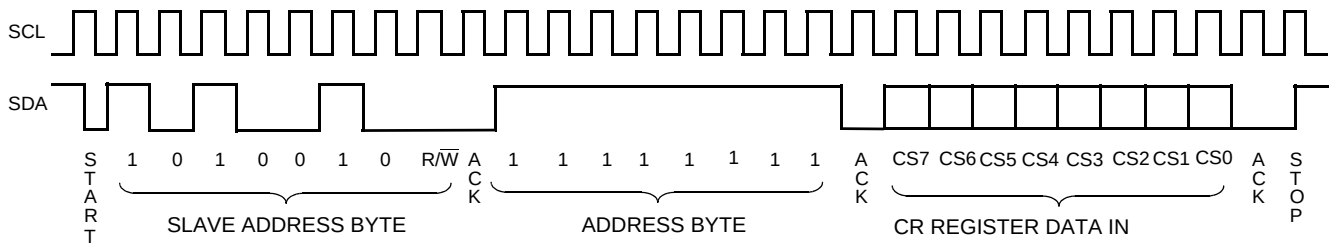


Figure 18. CR Register Write Command Sequence

Prior to writing to the CR register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps

—Write a 02H to the CR Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a START and ended with a STOP).

—Write a 06H to the CR Register to set the Register Write Enable Latch (RWEL) AND the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceded by a START and ended with a STOP).

—Write a one byte value to the CR Register that has all the bits set to the desired state. The CR register can be represented as qxyst01r in binary, where xy are the Voltage Monitor Output Status (V2FS and V3FS) bits, st are the Block Lock Protection (BL1 and BL0) bits, and qr are the Power-on Reset delay time (t_{PURST}) control bits (PUP1 - PUP0). This operation is proceeded by a START and ended with a STOP bit. Since this is a nonvolatile write cycle, it will typically take 5ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to ‘1’ in this third step (qxys t11r) then the RWEL bit is set, but the V2FS, V3FS, PUP1, PUP0, BL1 and BL0 bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and the X4023x does not return an ACKNOWLEDGE.

For example, a sequence of writes to the device CR register consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the CR Register to “0”.

It should be noted that a write to any nonvolatile bit of CR register will be ignored if the Write Protect pin of the X4023x is active (HIGH) (See "WP: Write Protection Pin").

CR (Control) Register Read Operation

The contents of the CR Register can be read at any time by performing a random read (See Figure 18). Using the Slave Address Byte set to 10100101, and an Address Byte of FFh. Only one byte is read by each register read operation. The X4023x resets itself after the first byte is read. The master should supply a STOP condition to be consistent with the bus protocol.

After setting the WEL and / or the RWEL bit(s) to a “1”, a CR register read operation may o$_{CC}$ur, without interrupting a proceeding CR register write operation.

DATA PROTECTION

There are a number of levels of data protection features designed into the X4023x. Any write to the device first requires setting of the WEL bit in the CR register. A write to the CR register itself, further requires the setting of the RWEL bit. Block Lock protection of the device enables the user to inhibit writes to certain regions of the EEPROM memory, as well as to all the DCPs. One further level of data protection in the X4023x, is incorporated in the form of the Write Protection pin.

WP: Write Protection Pin

When the Write Protection (WP) pin is active (HIGH), it disables nonvolatile write operations to the X4023x.

The table below (X4023x Write Permission Status) summarizes the effect of the WP pin (and Block Lock), on the write permission status of the device.

Additional Data Protection Features

In addition to the preceding features, the X4023x also incorporates the following data protection functionality:

—The proper clock count and data bit sequence is required prior to the STOP bit in order to start a nonvolatile write cycle.

VOLTAGE MONITORING FUNCTIONS

V_{CC} Monitoring

The X4023x monitors the supply voltage and drives the RESET output HIGH (using an external “pull up” resistor) if V_{CC} is lower than V_{TRIP1} threshold. The RESET output will remain HIGH until V_{CC} exceeds V_{TRIP1} for a minimum time of t_{PURST}. After this time, the RESET pin is driven to a LOW state. See Figure 30.

For the Power-on / Low Voltage Reset function of the X4023x, the RESET output may be driven HIGH down to a V_{CC} of 1V (V_{RVALID}). See Figure 30. Another feature of the X4023x, is that the value of t_{PURST} may be selected in software via the CR register (See “PUP1, PUP0: Power-on Reset bits – (Nonvolatile)” on page 19.).

It is recommended to stop communication to the device while RESET is HIGH. Also, setting the Manual Reset (MR) pin HIGH overrides the Power-on / Low Voltage circuitry and forces the RESET output pin HIGH (See "MR: Manual Reset").

MR: Manual Reset

The RESET output can be forced HIGH externally using the Manual Reset (MR) input. MR is a de-bounced, TTL compatible input, and so it may be operated by connecting a push-button directly from V_{CC} to the MR pin.

RESET remains HIGH for time t_{PURST} after MR has returned to its LOW state (See Figure 19). An external “pull down” resistor is required to hold this pin (normally) LOW.

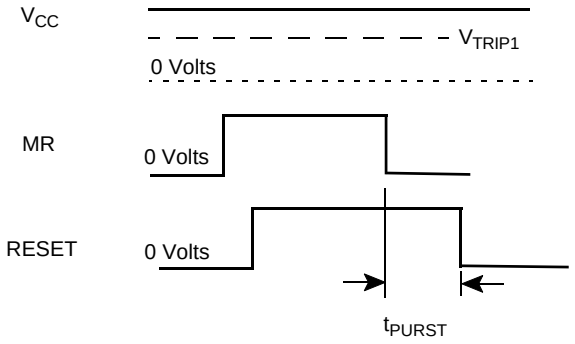


Figure 19. Manual Reset Response

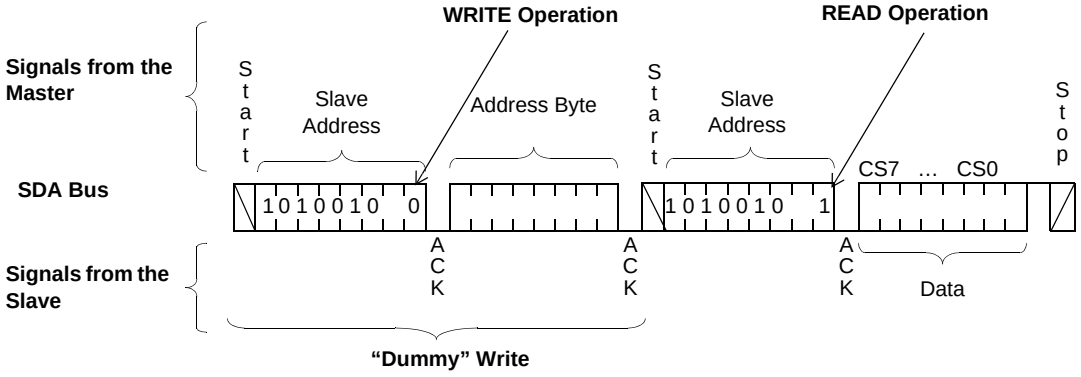


Figure 20. CR Register Read Command Sequence

X4023x Write Permission Status

Block Lock Bits		WP	DCP Volatile Write Permitted	DCP Nonvolatile Write Permitted	Write to EEPROM Permitted	Write to CR Register Permitted	
BL0	BL1					Volatile Bits	Nonvolatile Bits
x	1	1	NO	NO	NO	YES	NO
1	x	1	NO	NO	NO	YES	NO
0	0	1	YES	NO	NO	YES	NO
x	1	0	NO	NO	Not in locked region	YES	YES
1	x	0	NO	NO	Not in locked region	YES	YES
0	0	0	YES	YES	Yes (All Array)	YES	YES

V2MON Monitoring

The X4023x asserts the $\overline{\text{V2FAIL}}$ output HIGH if the voltage V2MON exceeds the corresponding V_{TRIP2} threshold (See Figure 21). The bit V2FS in the CR register is then set to a “0” (assuming that it has been set to “1” after system initialization).

The $\overline{\text{V2FAIL}}$ output may remain active HIGH with V_{CC} down to 1V. (See Figure 21)

V3MON Monitoring

The X4023x asserts the $\overline{\text{V3FAIL}}$ output HIGH if the voltage V3MON exceeds the corresponding V_{TRIP3} threshold (See Figure 21). The bit V3FS in the CR register is then set to a “0” (assuming that it has been set to “1” after system initialization).

The $\overline{\text{V3FAIL}}$ output may remain active HIGH with V_{CC} down to 1V. V_{TRIPx} Thresholds (x = 1,2,3)

The X4023x is shipped with pre-programmed threshold (V_{TRIPx}) voltages. In applications where the required thresholds are different from the default values, or if a higher precision / tolerance is required, the X4023x trip points may be adjusted by the user, using the steps detailed below.

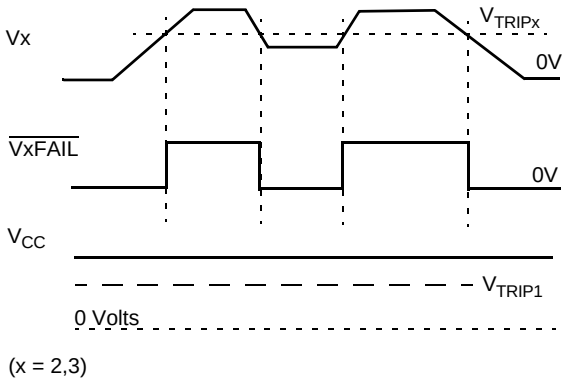


Figure 21. Voltage Monitor Response

Setting a V_{TRIPx} Voltage (x = 1,2,3)

There are two procedures used to set the threshold voltages (V_{TRIPx}), depending if the threshold voltage to be stored is higher or lower than the present value. For example, if the present V_{TRIPx} is 2.9 V and the new V_{TRIPx} is 3.2 V, the new voltage can be stored directly into the V_{TRIPx} cell. If however, the new setting is to be lower than the present setting, then it is necessary to “reset” the V_{TRIPx} voltage before setting the new value.

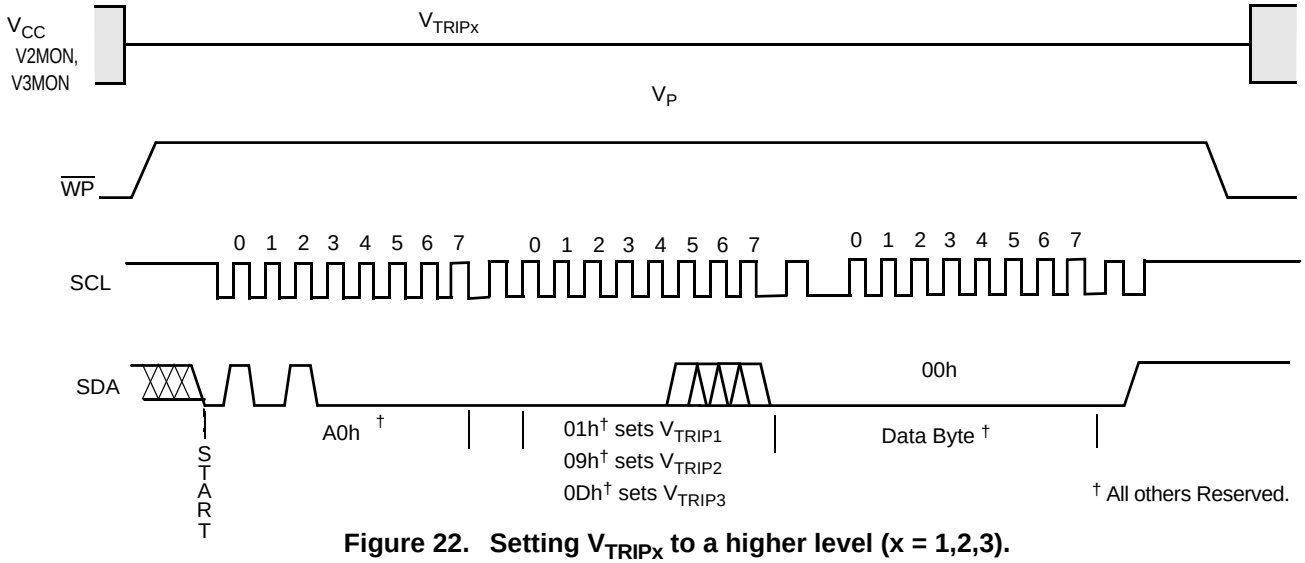


Figure 22. Setting V_{TRIPx} to a higher level (x = 1,2,3).

Setting a Higher V_{TRIPx} Voltage (x = 1,2,3)

To set a V_{TRIPx} threshold to a new voltage which is higher than the present threshold, the user must apply the desired V_{TRIPx} threshold voltage to the corresponding input pin (V_{CC}, V2MON or V3MON). Then, a programming voltage (Vp) must be applied to the WP pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h, followed by the Byte Address 01h for V_{TRIP1}, 09h for V_{TRIP2}, and 0Dh for V_{TRIP3}, and a 00h Data Byte in order to program V_{TRIPx}. The STOP bit following a valid write operation initiates the programming sequence. Pin WP must then be brought LOW to complete the operation (See Figure 23). The user does not have to set the WEL bit in the CR register before performing this write sequence.

Setting a Lower V_{TRIPx} Voltage (x = 1,2,3).

In order to set V_{TRIPx} to a lower voltage than the present value, then V_{TRIPx} must first be “reset” according to the procedure described below. Once V_{TRIPx} has been “reset”, then V_{TRIPx} can be set to the desired voltage using the procedure described in “Setting a Higher V_{TRIPx} Voltage”.

Resetting the V_{TRIPx} Voltage (x = 1,2,3).

To reset a V_{TRIPx} voltage, apply the programming voltage (Vp) to the WP pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h followed by the Byte Address 03h for V_{TRIP1}, 0Bh for V_{TRIP2}, and 0Fh for V_{TRIP3}, followed by 00h for the Data Byte in order to reset V_{TRIPx}. The STOP bit following a valid write operation initiates the programming sequence. Pin WP must then be brought LOW to complete the operation (See Figure 23). The user does not have to set the WEL bit in the CR register before performing this write sequence.

After being reset, the value of V_{TRIPx} becomes a nominal value of 1.7V.

V_{TRIPx} Accuracy (x = 1,2,3).

The accuracy with which the V_{TRIPx} thresholds are set, can be controlled using the iterative process shown in Figure 24.

If the desired threshold is less that the present threshold voltage, then it must first be “reset” (See "Resetting the V_{TRIPx} Voltage (x = 1,2,3).").

The desired threshold voltage is then applied to the appropriate input pin (V_{CC}, V2MON or V3MON) and the procedure described in Section “Setting a Higher V_{TRIPx} Voltage“ must be followed.

Once the desired V_{TRIPx} threshold has been set, the error between the desired and (new) actual set threshold can be determined. This is achieved by applying V_{CC} to the device, and then applying a test voltage higher than the desired threshold voltage, to the input pin of the voltage monitor circuit whose V_{TRIPx} was programmed. For example, if V_{TRIP2} was set to a desired level of 3.0 V, then a test voltage of 3.4 V may be applied to the voltage monitor input pin V2MON. In the case of setting of V_{TRIP1} then only V_{CC} need be applied. In all cases, care should be taken not to exceed the maximum input voltage limits.

After applying the test voltage to the voltage monitor input pin, the test voltage can be decreased (either in discrete steps, or continuously) until the output of the voltage monitor circuit changes state. At this point, the error between the actual/measured, and desired threshold levels is calculated.

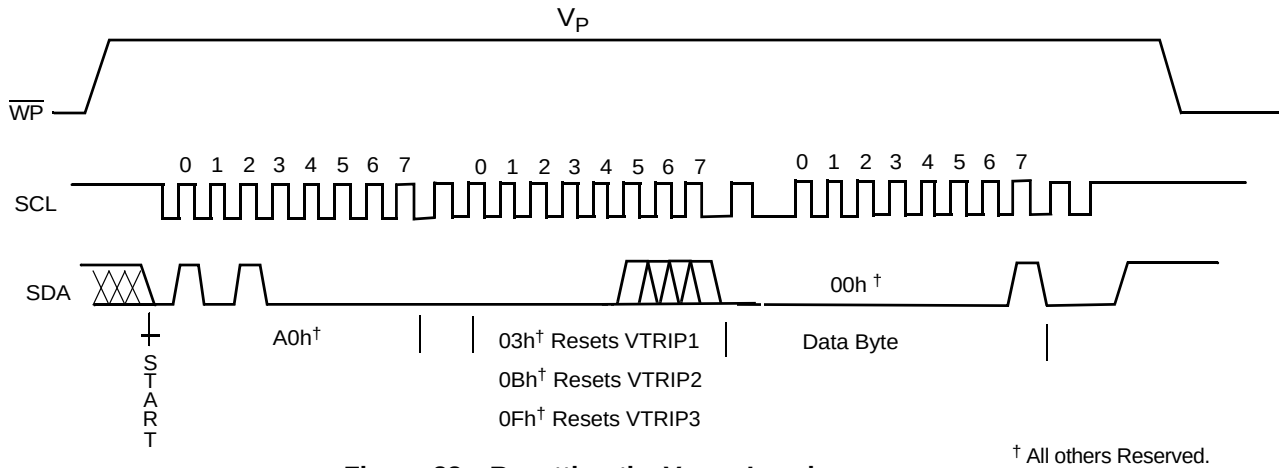


Figure 23. Resetting the V_{TRIPx} Level

For example, the desired threshold for V_{TRIP2} is set to 3.0 V, and a test voltage of 3.4 V was applied to the input pin V2MON (after applying power to V_{CC}). The input voltage is decreased, and found to trip the associated output level of pin $\overline{V2FAIL}$ from a LOW to a HIGH, when V2MON reaches 3.09 V. From this, it can be calculated that the programming error is 3.09 - 3.0 = 0.09 V.

If the error between the desired and measured V_{TRIPx} is less than the maximum desired error, then the programming process may be terminated. If however, the error is greater than the maximum desired error, then another iteration of the V_{TRIPx} programming sequence can be performed (using the calculated error) in order to further increase the accuracy of the threshold voltage.

If the calculated error is greater than zero, then the V_{TRIPx} must first be “reset”, and then programmed to the a value equal to the previously set V_{TRIPx} minus the calculated error. If it is the case that the error is less than zero, then the V_{TRIPx} must be programmed to a value equal to the previously set V_{TRIPx} plus the absolute value of the calculated error.

Continuing the previous example, we see that the calculated error was 0.09V. Since this is greater than zero, we must first “reset” the V_{TRIP2} threshold, then apply a voltage equal to the last previously programmed voltage, minus the last previously calculated error. Therefore, we must apply V_{TRIP2} = 2.91 V to pin V2MON and execute the programming sequence (See "Setting a Higher V_{TRIPx} Voltage (x = 1,2,3)").

Using this process, the desired accuracy for a particular V_{TRIPx} threshold may be attained using a successive number of iterations.

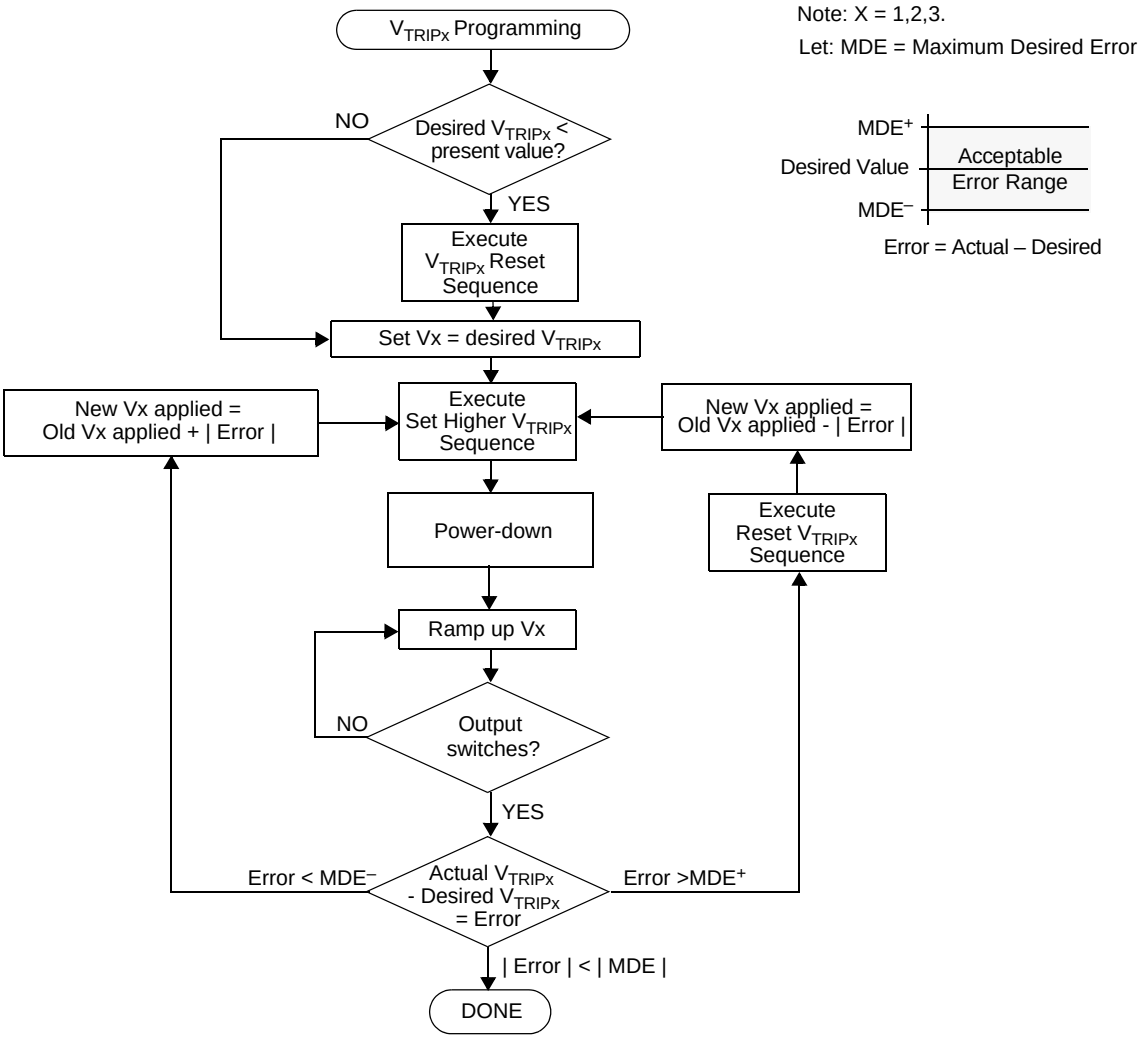


Figure 24. V_{TRIPx} Setting / Reset Sequence (x = 1,2,3)

ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Max.	Units
Temperature under Bias	-65	+135	°C
Storage Temperature	-65	+150	°C
Voltage on WP pin (With respect to VSS)	-1.0	+15	V
Voltage on other pins (With respect to VSS)	-1.0	+7	V
Voltage on R_{Hx} - Voltage on R_{Lx} (x = 0,1,2. Referenced to V_{SS})		V_{CC}	V
D.C. Output Current (SDA,RESETRESET,$\overline{V2FAIL}$,$\overline{V3FAIL}$)	0	5	mA
Lead Temperature (Soldering, 10 seconds)		300	°C
Supply Voltage Limits (Applied V_{CC} voltage, referenced to V_{SS})	2.7	7	V

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.	Units
Industrial	-40	+85	°C

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 25. Equivalent A.C. Circuit

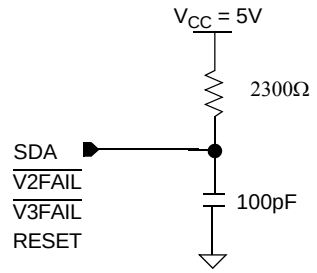
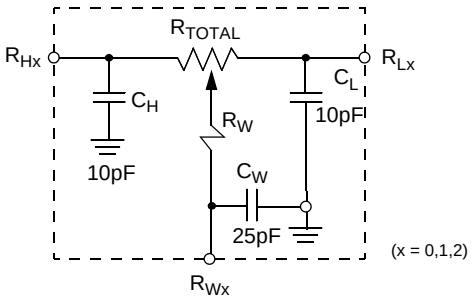


Figure 26. DCP SPICE Macromodel



TIMING DIAGRAMS

Figure 27. Bus Timing

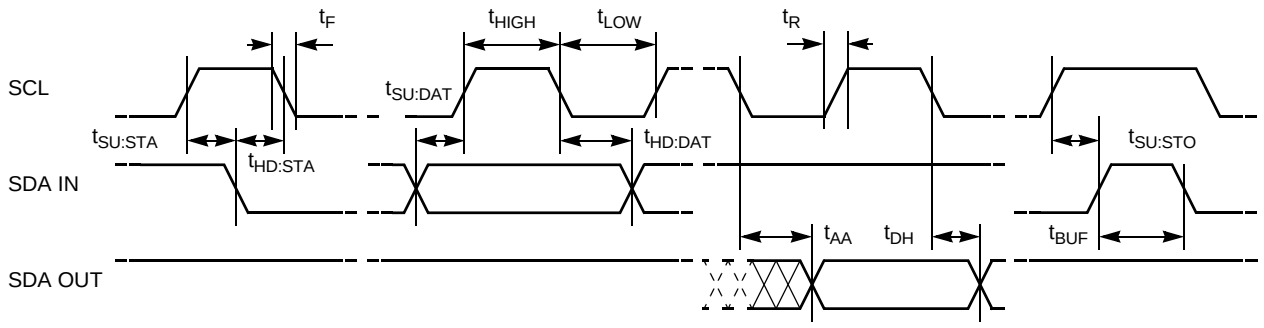


Figure 28. WP Pin Timing

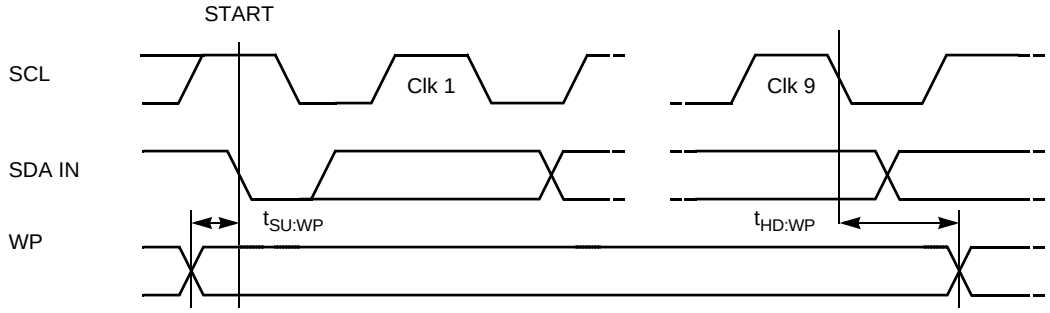


Figure 29. Write Cycle Timing

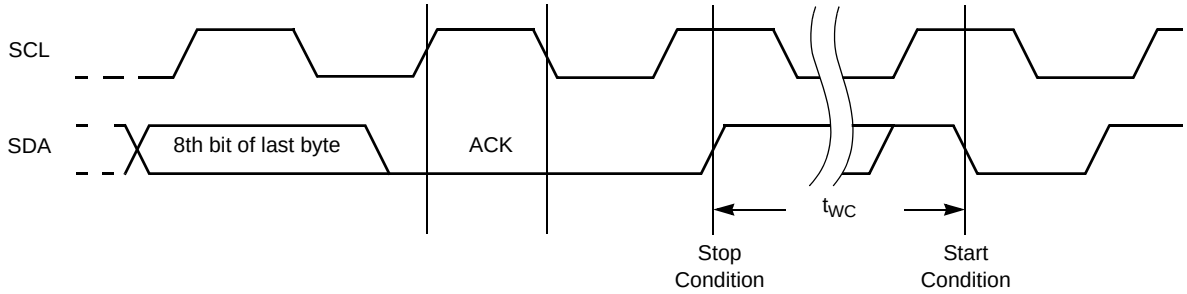


Figure 30. Power-Up and Power-Down Timing

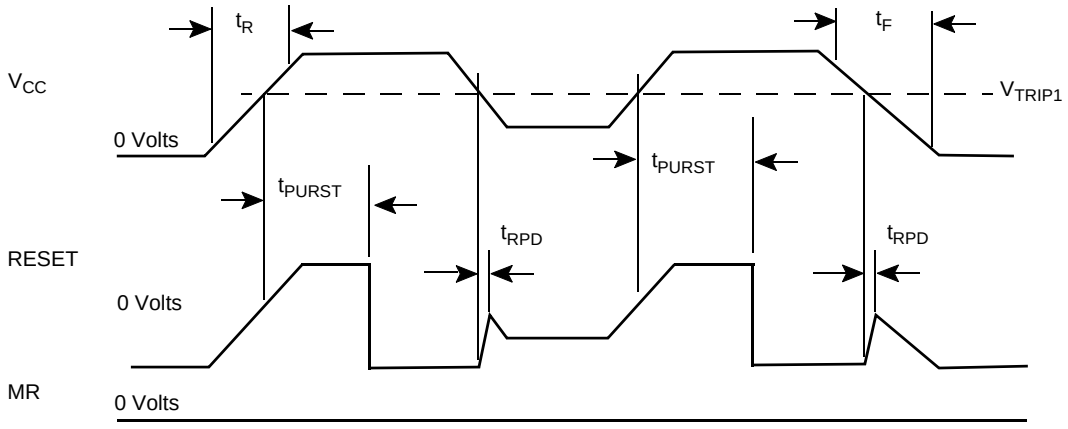


Figure 31. Manual Reset Timing Diagram

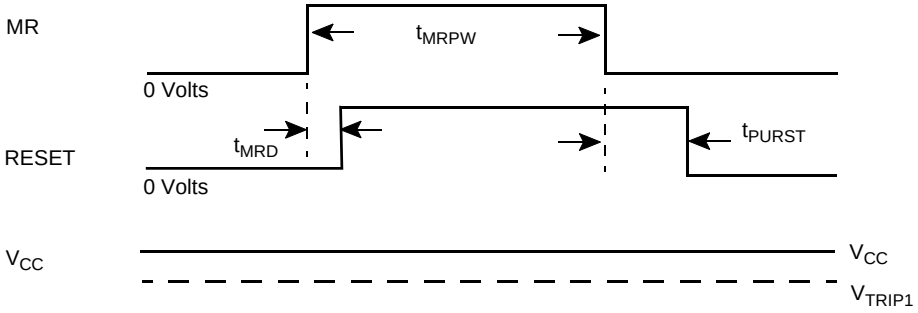
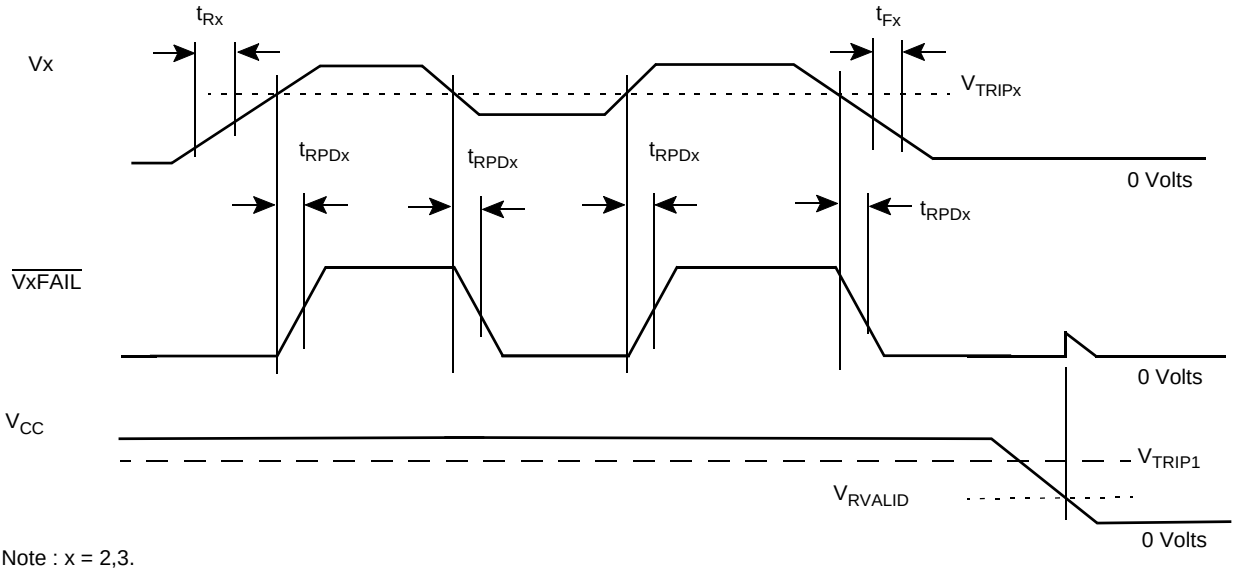


Figure 32. V2MON, V3MON Timing Diagram



Note : x = 2,3.

Figure 33. V_{TRIPX} Programming Timing Diagram (x=1,2,3).

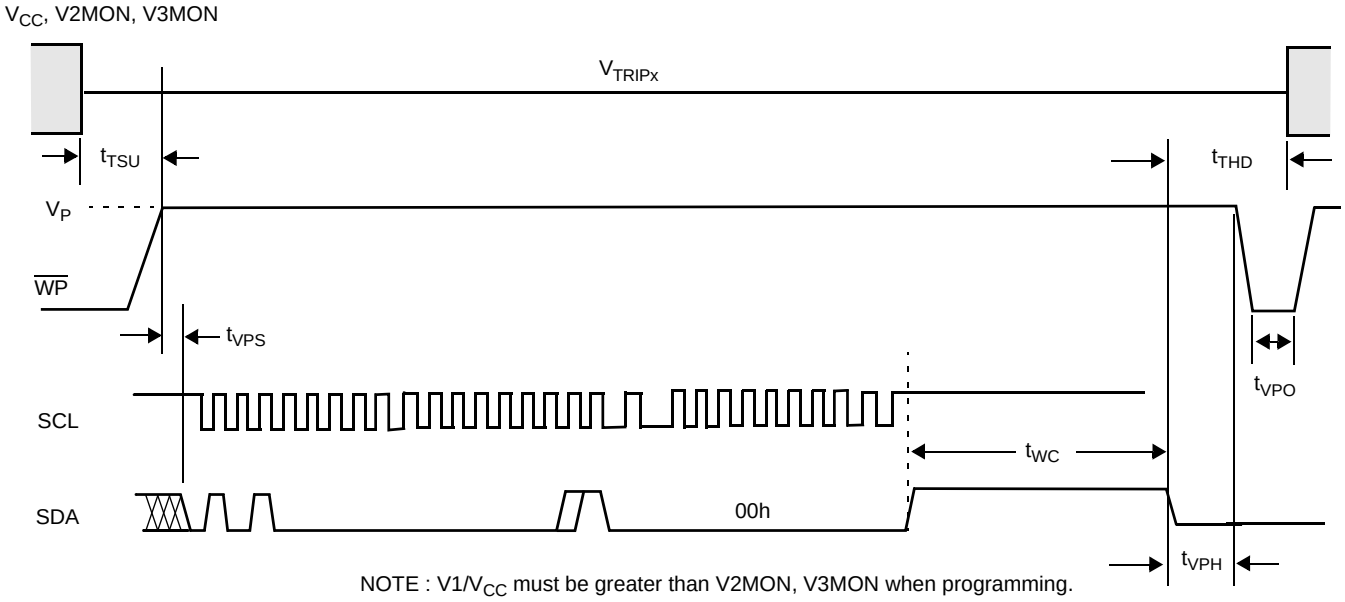
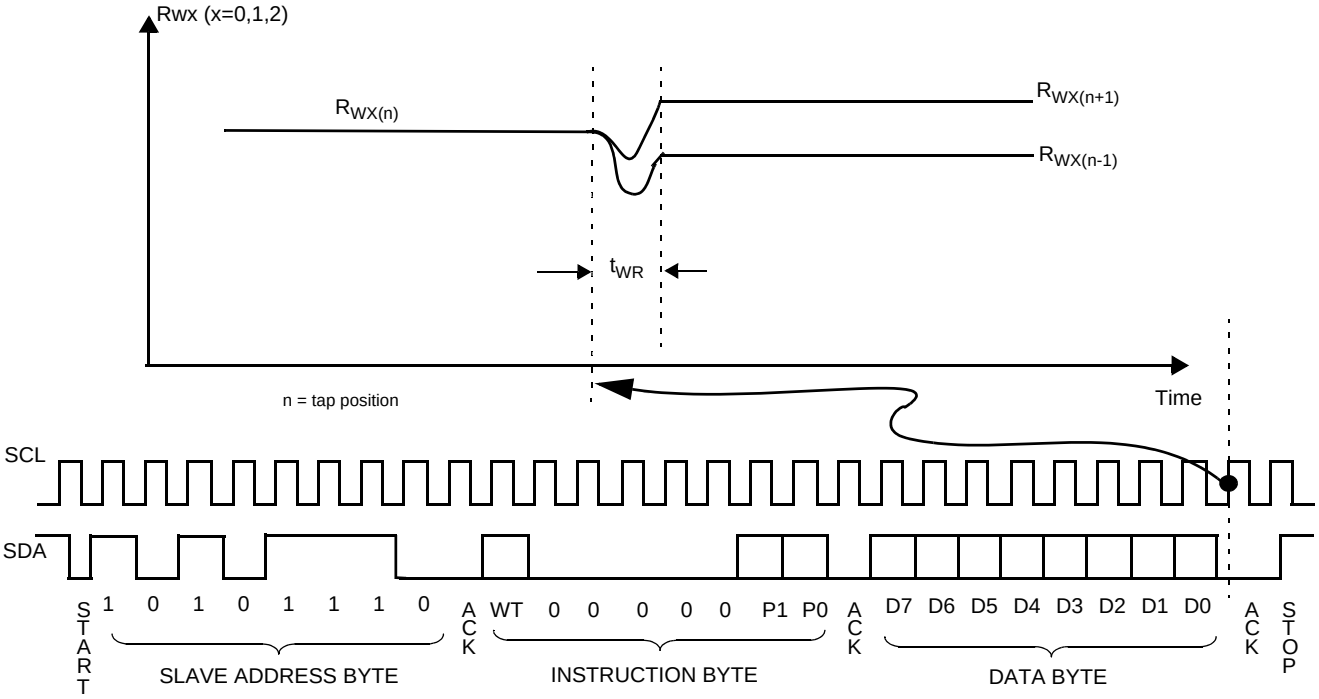


Figure 34. DCP "Wiper Position" Timing



D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
V_{CC}		2.7		5.5	V	Requires $V_{CC} > V_{TRIP1}$ or chip will not operate.
I_{CC1}(1)	Current into V_{CC} Pin (X4023x: Active) Read memory array (3) Write nonvolatile memory V_{CC} = 3.5V			 0.4 1.5	mA	f_{SCL} = 400KHz
I_{CC2}(2)	Current into V_{CC} Pin (X4023x:Standby) With 2-Wire bus activity (3) No 2-Wire bus activity V_{CC} = 3.5V			 50.0 50.0	µA	$V_{SDA} = V_{CC}$ MR = VSS WP = VSS or Open/Floating $V_{SCL} = V_{CC}$ (when no bus activity else f_{SCL} = 400kHz)
I_{LI}	Input Leakage Current (SCL, SDA, MR)		0.1	10	µA	V_{IN}(4) = GND to V_{CC}.
	Input Leakage Current (WP)			10	µA	
I_{LO}	Output Leakage Current (SDA, RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$)		0.1	10	µA	V_{OUT}(5) = GND to V_{CC}. X4023x is in Standby(2)
$V_{TRIP1PR}$	V_{TRIP1} Programming Range	2.75		4.70	V	
$V_{TRIPxPR}$	V_{TRIPx} Programming Range (x = 2,3)	1.75		3.50	V	
V_{TRIP1}(6)	Pre - programmed V_{TRIP1} threshold	2.8 4.3	2.95 4.45	3.00 4.50	V	Factory shipped default option A Factory shipped default option B
V_{TRIP2}(6)	Pre - programmed V_{TRIP2} threshold	2.05 2.8	2.20 2.95	2.25 3.00	V	Factory shipped default option A Factory shipped default option B
V_{TRIP3}(6)	Pre - programmed V_{TRIP3} threshold	1.60 1.60	1.75 1.75	1.80 1.80	V	Factory shipped default option A Factory shipped default option B
t_{RPDx}	V_{CC}, V2MON, V3MON to RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$ propagation delay (respectively)			20	µs	See (8)
I_{Vx}	V2MON Input leakage current V3MON Input leakage current			1 1	µA	$V_{SDA} = V_{SCL} = V_{CC}$ Others = GND or V_{CC}
V_{IL}(7)	Input LOW Voltage (SCL, SDA, WP, MR)	-0.5		0.8	V	
V_{IH}(7)	Input HIGH Voltage (SCL,SDA, WP, MR)	2.0		V_{CC} +0.5	V	
V_{OLx}	RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$, SDA Output Low Voltage			0.4	V	I_{SINK} = 2.0mA

Notes: 1. The device enters the Active state after any START, and remains active until: 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200nS after a STOP ending a read operation; or t_{WC} after a STOP ending a write operation.

Notes: 2. The device goes into Standby: 200nS after any STOP, except those that initiate a high voltage write cycle; t_{WC} after a STOP that initiates a high voltage cycle; or 9 clock cycles after any START that is not followed by the correct Device Select Bits in the Slave Address Byte.

Notes: 3. Current through external pull up resistor not included.

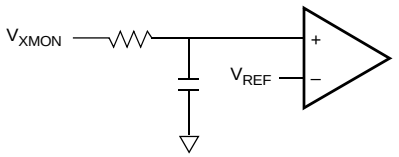
Notes: 4. V_{IN} = Voltage applied to input pin.

Notes: 5. V_{OUT} = Voltage applied to output pin.

Notes: 6. See “ORDERING INFORMATION” on page 36.

Notes: 7. V_{IL} Min. and V_{IH} Max. are for reference only and are not tested

Notes: 8. Equivalent input circuit for V_{XMON}



A.C. CHARACTERISTICS (See Figure 27, Figure 28, Figure 29)

Symbol	Parameter	400kHz		
		Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	400	kHz
t_{IN}(5)	Pulse width Suppression Time at inputs	50		ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus free before start of new transmission	1.3		µs
t_{LOW}	Clock LOW Time	1.3		µs
t_{HIGH}	Clock HIGH Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Output Hold Time	50		ns
t_R(5)	SDA and SCL Rise Time	20 +.1Cb(2)	300	ns
t_F(5)	SDA and SCL Fall Time	20 +.1Cb(2)	300	ns
$t_{SU:WP}$	$\overline{WP}$ Setup Time	0.6		µs
$t_{HD:WP}$	$\overline{WP}$ Hold Time	0		µs
Cb	Capacitive load for each bus line		400	pF

A.C. TEST CONDITIONS

Input Pulse Levels	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$0.5V_{CC}$
Output Load	See Figure 25

NONVOLATILE WRITE CYCLE TIMING

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(4)	Nonvolatile Write Cycle Time		5	10	ms

CAPACITANCE (T_A = 25°C, F = 1.0 MHZ, V_{CC} = 5V)

Symbol	Parameter	Max	Units	Test Conditions
C_{OUT}(5)	Output Capacitance (SDA, RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$)	8	pF	V_{OUT} = 0V
C_{IN}(5)	Input Capacitance (SCL, WP, MR)	6	pF	V_{IN} = 0V

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V

Notes: 2. Cb = total capacitance of one bus line in pF.

Notes: 3. Over recommended operating conditions, unless otherwise specified

Notes: 4. t_{WC} is the time from a valid STOP condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

Notes: 5. This parameter is not 100% tested.

POTENTIOMETER CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
R_{TOL}	End to End Resistance Tolerance	-20		+20	%	In a ratiometric circuit, R_{TOTAL} divides out of the equation and accuracy is determined by XDCP resolution.
V_{RHx}	R_H Terminal Voltage (x = 0,1,2)	VSS		V_{CC}	V	
V_{RLx}	R_L Terminal Voltage (x = 0,1,2)	VSS		VSS	V	R_L Terminal internally tied to gnd.
P_R	Power Rating(1)			10	mW	R_{TOTAL} = 10kΩ (DCP0, DCP1)
				5	mW	R_{TOTAL} = 100kΩ (DCP2)
R_W	DCP Wiper Resistance		200	400	Ω	V_{CC} = 5 V, V_{RHx} = V_{CC}, V_{RLx} = VSS (x = 0,1,2), I_W = 50 uA /500 uA (100/10kΩ).
			400	1200	Ω	V_{CC} = 2.7 V, V_{RHx} = V_{CC}, V_{RLx} = VSS (x = 0,1,2), I_W = 27 uA /270 uA (100/10 kΩ).
I_W	Wiper Current			4.4	mA	
	Noise				$\frac{mV}{\sqrt{(Hz)}}$	R_{TOTAL} = 10kΩ (DCP0, DCP1)
					$\frac{mV}{\sqrt{(Hz)}}$	R_{TOTAL} = 100kΩ (DCP2)
	Absolute Linearity(2)	-1		+1	MI(4)	$R_{w(n)(actual)}$ - $R_{w(n)(expected)}$
	Relative Linearity(3)	-1		+1	MI(4)	$R_{w(n+1)}$ - [$R_{w(n)}$ + MI]
	R_{TOTAL} Temperature Coefficient		±300		ppm/°C	R_{TOTAL} = 10kΩ (DCP0, DCP1)
			±300		ppm/°C	R_{TOTAL} = 100kΩ (DCP2)
	Ratiometric Temperature Coefficient			±30	ppm/°C	(Voltage divider configuration)
$C_H/C_L/C_W$	Potentiometer Capacitances		10/10/25		pF	See Figure 26.
t_{wr}	Wiper Response time			200	µs	See Figure 34.

Notes: 1. Power Rating between the wiper terminal $R_{WX(n)}$ and the end terminals R_{HX} V_{SS} - for ANY tap position n, (x = 0,1,2).

Notes: 2. Absolute Linearity is utilized to determine actual wiper resistance versus, expected resistance = ($R_{wx(n)}$(actual) - $R_{wx(n)}$(expected)) = ±1 Ml Maximum (x = 0,1,2).

Notes: 3. Relative Linearity is a measure of the error in step size between taps = $R_{Wx(n+1)}$ - [$R_{wx(n)}$ + Ml] = ±0.2 Ml (x = 0,1,2)

Notes: 4. 1 Ml = Minimum Increment = R_{TOT} / (Number of taps in DCP - 1).

Notes: 5. Typical values are for T_A = 25°C and nominal supply voltage.

Notes: 6. This parameter is periodically sampled and not 100% tested.

V_{TRIPX} (X = 1,2,3) PROGRAMMING PARAMETERS (See Figure 33)

Parameter	Description	Min	Typ	Max	Units
t_{VPS}	V_{TRIPx} Program Enable Voltage Setup time	10			µs
t_{VPH}	V_{TRIPx} Program Enable Voltage Hold time	10			µs
t_{TSU}	V_{TRIPx} Setup time	10			µs
t_{THD}	V_{TRIPx} Hold (stable) time	10			µs
t_{VPO}	V_{TRIPx} Program Enable Voltage Off time (Between successive adjustments)	1			ms
t_{WC}	V_{TRIPx} Write Cycle time		5	10	ms
V_P	Programming Voltage	10		15	V
V_{ta}	V_{TRIPx} Program Voltage accuracy Programmed at 25°C.)	-100		+100	mV
V_{tv}	V_{TRIP} Program variation after programming (-40 - 85°C). (Programmed at 25°C.)	-25	+10	+25	mV

Notes: 100% tested.

RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$ OUTPUT TIMING. (See Figure 30, Figure 31, Figure 32)

Symbol	Description	Condition	Min.	Typ.	Max.	Units
t_{PURST}	Power-on Reset delay time	PUP1 = 0, PUP0 = 0	25	50	75	ms
		PUP1 = 0, PUP0 = 1	50	100	150	ms
		PUP1 = 1, PUP0 = 0	100	200	300	ms
		PUP1 = 1, PUP0 = 1	150	300	450	ms
t_{MRD}(31)(2)	MR to RESET propagation delay	See (1)(2)(4)			5	µs
t_{MRDPW}	MR pulse width		500			ns
t_{RPDx}	V_{CC}, V2MON, V3MON to RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$ propagation delay (respectively)	See (5)			20	µs
t_{Fx}	V_{CC}, V2MON, V3MON Fall Time		20			mV/µs
t_{Rx}	V_{CC}, V2MON, V3MON Rise Time		20			mV/µs
V_{RVALID}	V_{CC} for RESET, $\overline{V2FAIL}$, $\overline{V3FAIL}$ Valid(3).		1			V

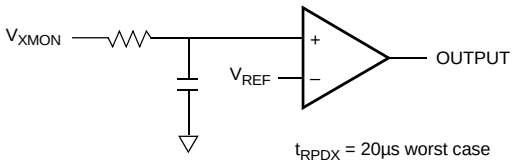
Notes: 1. See Figure 31 for timing diagram.

Notes: 2. See Figure 25 for equivalent load.

Notes: 3. This parameter describes the lowest possible V_{CC} level for which the outputs RESET, $\overline{V2FAIL}$, and $\overline{V3FAIL}$ will be correct with respect to their inputs (V_{CC}, V2MON, V3MON).

Notes: 4. From MR rising edge crossing V_{IH}, to RESET rising edge crossing V_{OH}.

Notes: 5. Equivalent input circuit for V_{XMON}



APPENDIX 1

DCP1 (100 Tap) Tap position to Data Byte translation Table

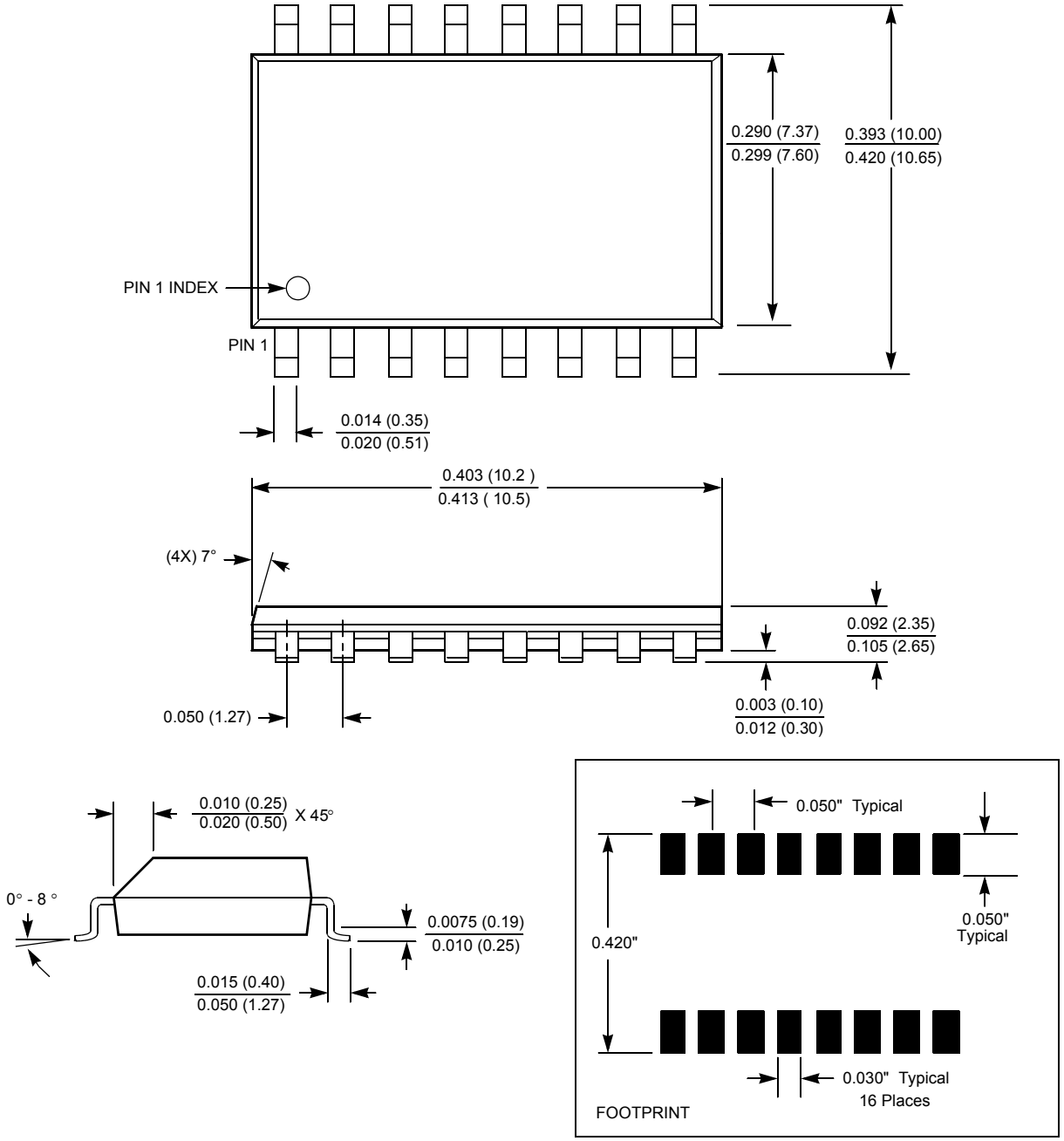
Tap Position	Data Byte	
	Decimal	Binary
0	0	0000 0000
1	1	0000 0001
.	.	.
.	.	.
23	23	0001 0111
24	24	0001 1000
25	56	0011 1000
26	55	0011 0111
.	.	.
.	.	.
48	33	0010 0001
49	32	0010 0000
50	64	0100 0000
51	65	0100 0001
.	.	.
.	.	.
73	87	0101 0111
74	88	0101 1000
75	120	0111 1000
76	119	0111 0111
.	.	.
.	.	.
98	97	0110 0001
99	96	0110 0000

APPENDIX 2

DCP1 (100 Tap) tap position to Data Byte translation algorithm example.

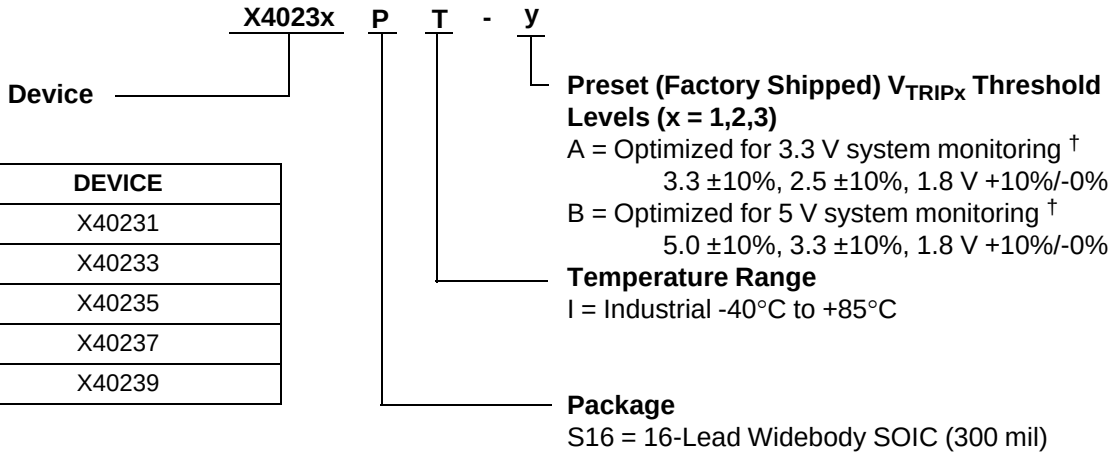
```
unsigned DCP1_TAP_Position(int tap_pos)
{
        int block;
        int i;
        int offset;
        int wcr_val;

        offset   = 0;
        block    = tap_pos / 25;

        if (block < 0) return ((unsigned)0);

        else if (block <= 3)
        {       switch(block)
                {       case (0): return ((unsigned)tap_pos) ;

                        case (1):
                        {
                                wcr_val = 56;
                                offset = tap_pos - 25;
                                for (i=0; i<= offset; i++) wcr_val-- ;
                                return ((unsigned) wcr_val);
                        }

                        case (2):
                        {
                                wcr_val = 64;
                                offset = tap_pos - 50;
                                for (i=0; i<= offset; i++) wcr_val++ ;
                                return ((unsigned) wcr_val);
                        }

                        case (3):
                        {
                                wcr_val = 120;
                                offset = tap_pos - 75;
                                for (i=0; i<= offset; i++) wcr_val-- ;
                                return ((unsigned) wcr_val);
                        }
                }
        }
        return((unsigned)01100000);
}
```

16-Lead Plastic, SOIC (300-mil body), Package Code S16



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

ORDERING INFORMATION



x	DEVICE
1	X40231
3	X40233
5	X40235
7	X40237
9	X40239

† For details of preset threshold values, See "D.C. OPERATING CHARACTERISTICS"

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