Voltage Detector IC Series

Bipolar
Voltage Detector IC
BD47□□G Series

Pb Free
ROHM Electronic Components

●General Description

The BD47□□G Series is a reset IC that was developed to prevent system errors at transient state when the power of CPU or logic circuit switches ON/OFF or momentary shut down. These ICs consist of three terminals (power supply, GND and reset output) to detect power supply voltages and outputs reset signals of various systems. These ICs are ultra-compact and are realized low current consumption, making them ideal for portable products.

●Features

1) Detection voltage range: 0.1-volt step line-up 1.9-4.6V (Typ.)
2) High accuracy voltage detection: ±1%
3) Low current consumption
4) Open collector "L" reset output
5) Compact SSOP5 package

●Applications

All electronic devices that use microcontrollers and logic circuits

●Selection Guide

Part Number : BD47□ □ G
①

Number	Specifications	Description
①	Detection Voltage	Example: Voltage range over 1.9V-4.6V in 0.1V increments. 2.9V is marked as "29"

●Lineup

Marking	Detection Voltage	Part Number	Marking	Detection Voltage	Part Number	Marking	Detection Voltage	Part Number
B2	4.6V	BD4746	BR	3.6V	BD4736	BH	2.6V	BD4726
B1	4.5V	BD4745	BQ	3.5V	BD4735	BG	2.5V	BD4725
BZ	4.4V	BD4744	BP	3.4V	BD4734	BF	2.4V	BD4724
BY	4.3V	BD4743	B4	3.3V	BD4733	BE	2.3V	BD4723
BX	4.2V	BD4742	BN	3.2V	BD4732	BD	2.2V	BD4722
BW	4.1V	BD4741	BM	3.1V	BD4731	BC	2.1V	BD4721
BV	4.0V	BD4740	BL	2.0V	BD4730	BB	2.0V	BD4720
BU	3.9V	BD4739	BK	2.9V	BD4729	BA	1.9V	BD4719
BT	3.8V	BD4738	BJ	2.8V	BD4728			
BS	3.7V	BD4737	B3	2.7V	BD4727			

●Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	VCC	-0.3 ~ +10	V
Output Voltage	Po	-0.3 ~ +10	V
Power Dissipation *1 *2	Pd	540	mW
Operating Temperature	Topr	-40 ~ +75	℃
Ambient Storage Temperature	Tstg	-55 ~ +125	℃

*1 When a ROHM standard circuit board (70mm×70mm×1.6mm glass epoxy board) is mounted.

*2 When used at temperatures higher than Ta=25℃, the power is reduced by 5.4mW/℃

●Electrical Characteristics (Unless specified otherwise, Ta=-25℃~+105℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Detection Voltage	VS	VS (T)×0.99	VS (T)	VS (T)×1.01	V	RL=470kΩ,VDD=H→L
Detection Voltage Temperature Coefficient	VS/ΔT	—	±0.01	—	%/℃	RL=4.7kΩ,Ta=-20～+75℃ (Designed Guarantee)
Hysteresis Voltage	ΔVS	30	50	100	mV	RL=4.7kΩ,VCC=L→H→L
"H" Transmission Delay Time *1	TPLH	—	20	50	μs	CL=100pF,RL=4.7kΩ
"L" Transmission Delay Time *2	TPHL	—	60	120	μs	CL=100pF,RL=4.7kΩ
"L" Output Voltage	VOL	—	0.1	0.4	V	VCC=VSMin.-0.05V,RL=4.7kΩ
Circuit Current at ON	ICC1	—	1.5	3.0	μA	VCC=VSMin.-0.05V,RL=∞
Circuit Current at OFF	ICC2	—	1.6	3.2	μA	VCC=VSTyp./0.85V,RL=∞
Operating Voltage Range	VOPL	—	0.65	0.85	V	RL=4.7kΩ,VOL≦0.4V
"Low" Output Current	IOL	3.0	15.0	—	mA	Vo=0.4V,VCC=VsMin.-0.05V

Note: VS(T) = Setting Detection Voltage Value (1.9V～4.6V, 0.1V step)

*1 TPLH: VCC =(VS Typ.-0.4V)→(VS Typ.+0.4V)

*2 TPHL: VCC =(VS Typ.+0.4V)→(VS Typ.-0.4V)

Designed Guarantee. (Outgoing inspection is not done an all products.)

●Block Diagrams

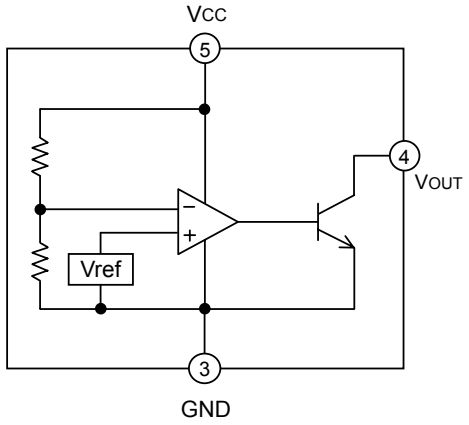


Fig.1

SSOP5

PIN No.	Symbol	Function
1	N.C.	Unconnected Terminal
2	SUB	Substrate*
3	GND	GND
4	VOUT	Reset Output
5	VCC	Power Supply Voltage

*Substrate Pin should be connected with GND

●Reference Data (Unless specified otherwise, Ta=25℃)

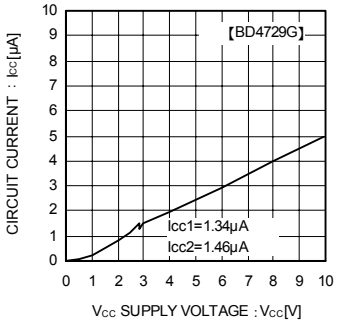


Fig.2 Circuit Current

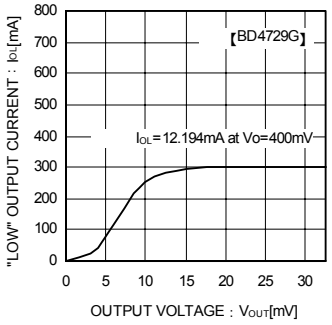


Fig.3 “Low” Output Current

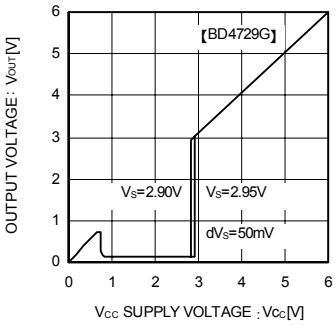


Fig.4 I/O Characteristics

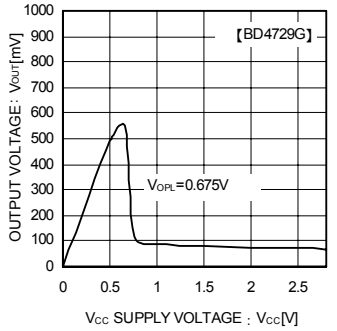


Fig.5 Operating Limit Voltage

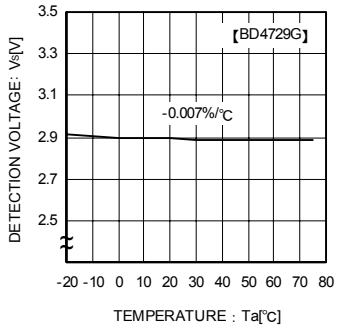


Fig.6 Detection Voltage

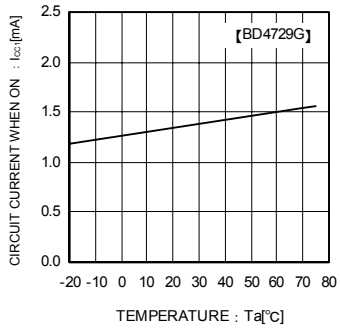


Fig.7 Circuit Current when ON

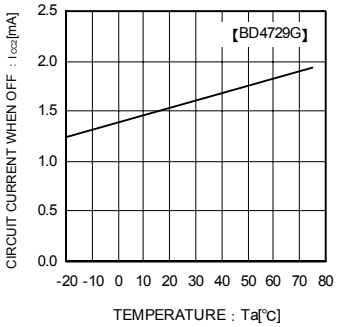


Fig.8 Circuit Current when OFF

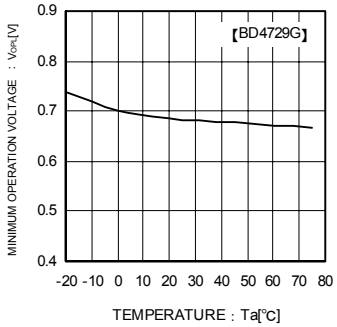


Fig.9 Operating Limit Voltage

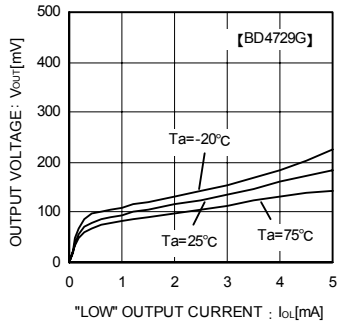


Fig.10 Output Saturation Voltage

●Explanation of Operation

BD47□□G series has the detection voltages and release voltages as threshold voltages and, as the voltages applied to the input reach their respective threshold voltages, the output switches from “High” to “Low” and from “Low” to “High”. The release voltage has a hysteresis that is the detection voltage +50mV (Typ.), preventing chattering in the output. When the input is greater than the release voltage, the output is in a “High” state. When the input is lowered from that state, the output switches to “Low” on the detection voltage. When the input is less than the detection voltage, the output is in a “Low” state. When the input is raised from that state, the output switches to “High” with the release voltage. Additionally, at least 0.85V is required for the circuit to operate fully. When the input falls below the operating limit voltage, the output becomes unsettled.

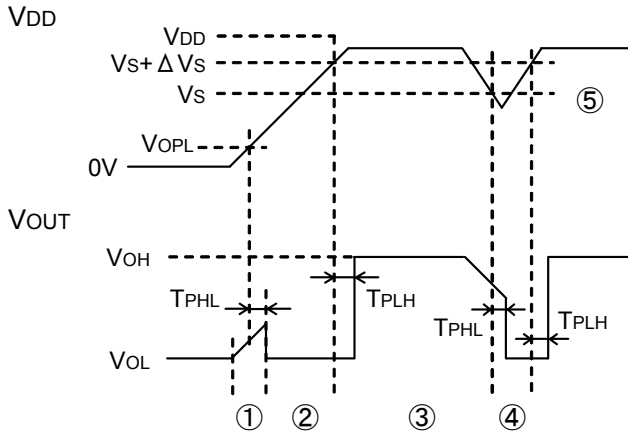


Fig.11 Timing Waveform

① When the power supply is turned on, the output is unsettled from after over the operating limit voltage (VOPL) until TPHL. There fore it is possible that the reset signal is not outputted when the rise time of VDD is faster than TPHL.

② When VDD is greater than VOPL but less than the reset release voltage (VS + ΔVS), the output voltages will switch to Low.

③ If VDD exceeds the reset release voltage (VS + ΔVS), then VOUT switches from L to H.

④ If VDD drops below the detection voltage (VS) when the power supply is powered down or when there is a power supply fluctuation, VOUT switches to L (with a delay of TPHL).

⑤ The potential difference between the detection voltage and the release voltage is known as the hysteresis width (ΔVS). The system is designed such that the output does not flip-flop with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

Precautions

Please be aware that when there is resistance on the power supply line, the detection voltage varies with voltage drops caused by the IC current consumption.

Please connect a capacitor between VCC and GND when the power supply line has high impedance.

●Circuit Applications

1） The following is an example of an application circuit using Reset IC for normal power supply detection. BD47□□G series requires a pull up resistor on the output terminal. The pull up resister value should be decided. As the application with enough confirmation of power supply level and output current capability. When a capacitor has been inserted into the output terminal to delay the output time or to remove noise, the output will be slower during starting or stopping. Please be careful to select the appropriate pull up resistors, output current and capacitor when inserting a bypass capacitor between input and GND. Please be aware that if an extremely large capacitor is used, the response time will become excessively slow.

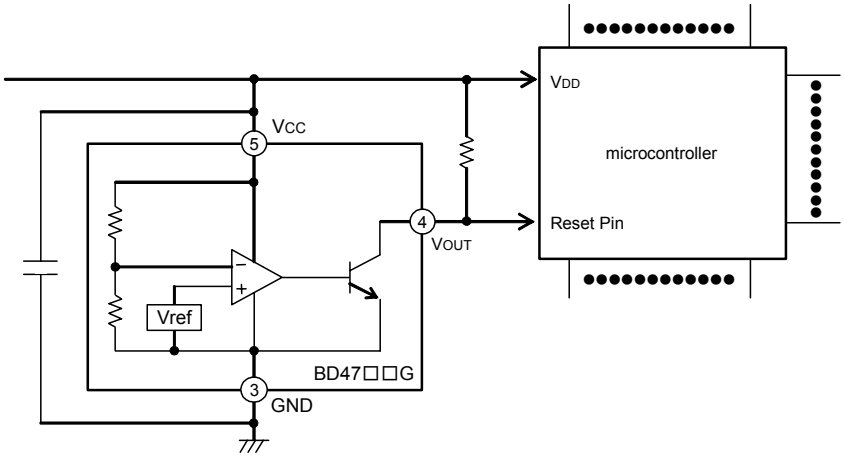


Fig.12

2） The following shows an example of adding delay time to a reset signal. It is possible to set the delay time using the capacitor CL and the resistor RL connected to the output terminal as shown below. At VCC start up, CL will be charged by RL. The CL and RL time constants and the threshold voltage of the Reset terminal determine the charge delay time. When VCC is decreased, CL is discharged through the Reset IC. The sum of the respective times plus the delay time of the IC itself becomes the reset signal delay time.

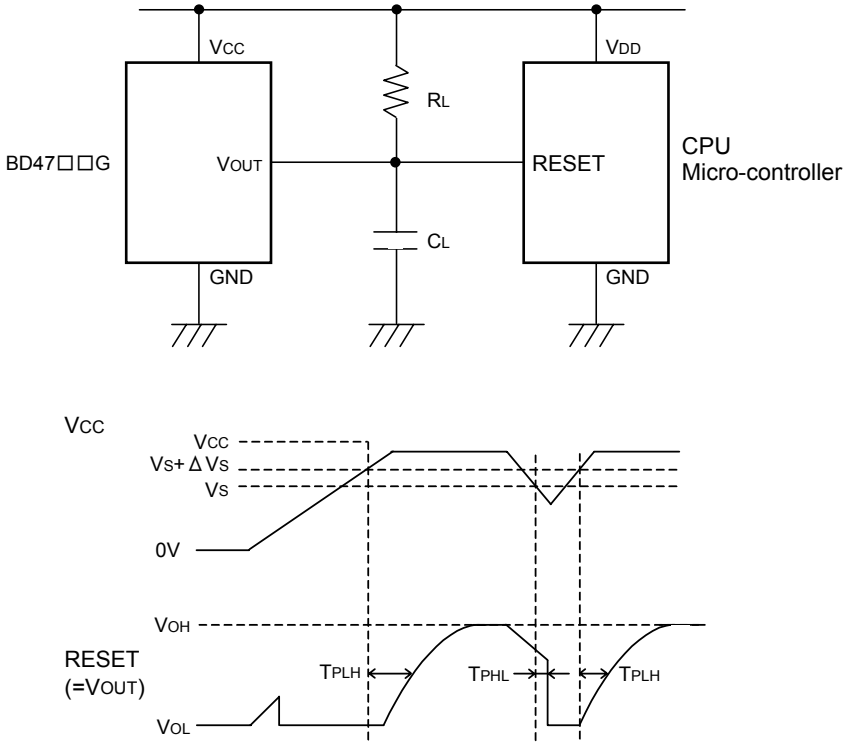


Fig.13

3）The following is an example of an application circuit in which an OR connection between two types of detection voltage.

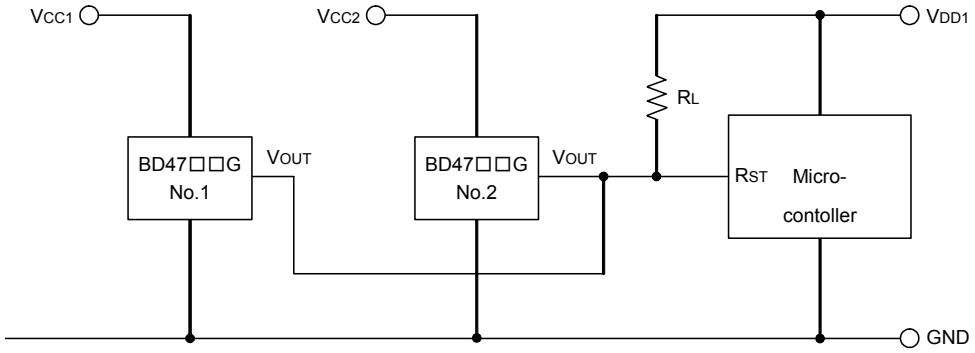


Fig.14

When there are several system power supplies and it is necessary to monitor power supplies VCC1 and VCC2 independently as well as reset the microcontroller, the following application (as shown in Fig. 14) is possible. The output voltage “High” is matched to the microcontroller power supply VDD1 by using an OR connection to pull up to an arbitrary voltage (VDD1).

4） The output of the BD47□□G series consists of a bipolar NPN transistor. When the input voltage is at or below the detection voltage (VS), VOUT will be set to “Low”. This configuration makes it easier to secure output current capacity even when the output voltage falls as well as when the pull up resistor (RL) at the output has to be made smaller or when many reset terminals have to be driven by a single reset IC (Fig. 16).

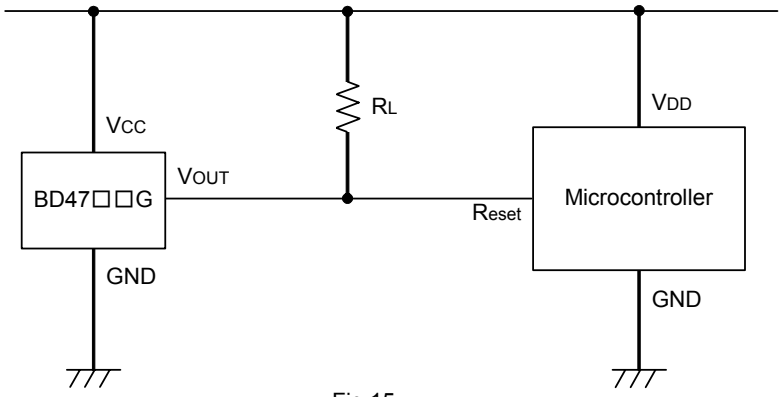


Fig.15

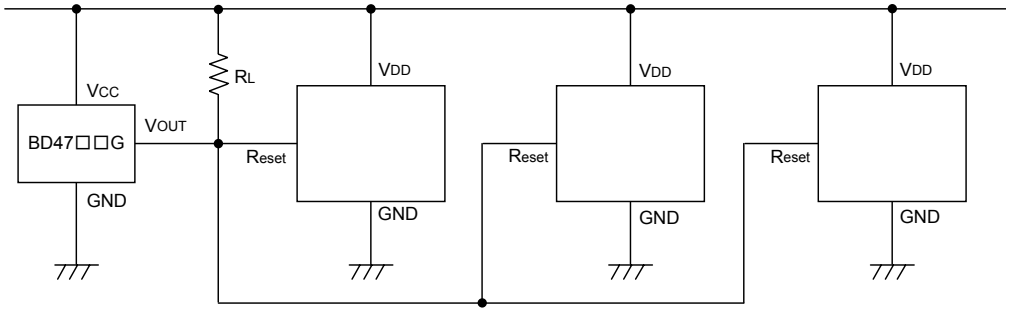


Fig.16

● Operation Notes

1. Absolute maximum range
   Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. GND potential
   GND terminal should be a lowest voltage potential every state. Please make sure all pins, which are over ground even if, include transient feature.

3. Electromagnetic Field
   Mal-function may happen when the device is used in the strong electromagnetic field.

4. Bypass Capacitor for Noise Rejection
   Please put into the capacitor between VCC pin and GND, to reject noise. If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5. Short Circuit between Terminal and Soldering
   Don't short-circuit between Output pin and VCC pin, Output pin and GND pin, or VCC pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If the leakage is assumed between the VOUT terminal and the GND terminal, the pull-up resistor should be less than 1/10 of the assumed leak resistance.

7. External parameters
   The recommended parameter range for RL is 2kΩ～1MΩ. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

8. Power on reset operation
   Please note that the power on reset output varies with the VDD rise up time. Please verify the actual operation.

9. Precautions for board inspection
   Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation.
   To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

10. When the power supply, is turned on because of in certain cases, momentary Rash-current flow into the IC at the logic unsettled, the couple capacitance, GND pattern of width and leading line must be considered.

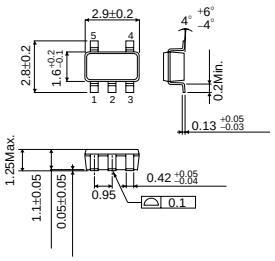
● Part Number Selection

B	D	4	7			G	–	T	R

- B D 4 7: Bipolar Reset
- Detection Voltage: Example: 1.9V→19
- G: SSOP5 Package
- T R: Taping Specifications — Embossed Taping

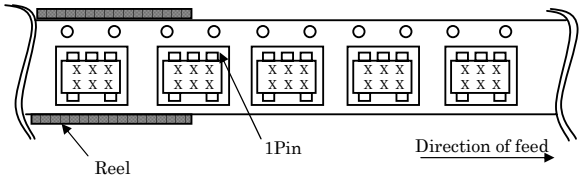
SSOP5

<Dimension> (Unit : mm)



<Tape and Reel information> SSOP5

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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