Features

- Supported Data Rate 0.5k to 20kBit/s Manchester (Higher Data Rates in Transparent Mode)
- Programmable RX-IF Bandwidth 25kHz to 360kHz (Approx. 10% Increments)
- Frequency Ranges 310MHz to 318MHz, 418MHz to 477MHz, and 836MHz to 928MHz
  - 315.00MHz/433.92MHz/868.30MHz and 915.00MHz with 24.305MHz Crystal Freq.
- Programmable Channel Frequency with Fractional PLL
  - 92Hz Resolution for Low Band
  - 184Hz Resolution for High Band
- FSK Deviation ±0.375kHz to ±90kHz
- FSK Sensitivity (Manchester) at 433.92MHz
  - –106dBm at 20kBit/s, Δf = ±20kHz, IFBW = 165kHz
  - –109dBm at 10kBit/s, Δf = ±10kHz, IFBW = 165kHz
  - –111dBm at 5kBit/s, Δf = ±5kHz, IFBW = 165kHz
  - –119dBm at 0.75kBit/s, Δf = ±0.75kHz, IFBW = 25kHz
- ASK Sensitivity (Manchester) at 433.92MHz
  - –108dBm at 20kBit/s, BW = 360kHz
  - –116dBm at 1kBit/s, BW = 360kHz
- Excellent Blocking (IFBW = 165kHz): 64dBC at Freq. Offset = 1MHz and 50dBC at 225kHz
- High Image Rejection Typ. 55dB (315MHz/433.92MHz); Typ. 50dB (868.3MHz/915MHz) without Calibration
- Input 1dB Compression Point
  - Typ. –35dBm (Full Sensitivity Level)
  - Typ. –20dBm (15dB Reduced Sensitivity)
- Digital RSSI with Accuracy of ±5dB and 0.5dB Resolution
- Low Current Consumption
  - Typ. 9.3mA for RX (Low Band) Typ. 580µA 3 Channel Polling
- Max. Power Down Current Consumption of 600nA at V_S = 3.6V and T = 85°C
- Programmable Clock Output Derived from Crystal Frequency
- 24Kbyte of ROM with Atmel Firmware
- 512 Bytes of EEPROM Data Memory for Receiver Configuration and 768 Bytes of SRAM
- SPI Interface for RX Data Access and Receiver Configuration
- IRQ Signal Indicates the IC Condition Status
- Automatic Application Channel Polling (3 RKE Channels, TPMS, RS)
- ID Scanning Up to 18 Different IDs (ID Lengths of up to 4 Bytes)
- Supply Voltage Range 1.9V to 3.6V and 4.5V to 5.5V
- Temperature Range –40°C to +105°C
- Excellent ESD Protection at All Pins (±4kV HBM, ±200V MM, ±750V FCDM)
- Small 5mm × 5mm QFN 32 Package Pin/Pitch 0.5mm
- Pin Compatible IC with Rx Performance Identical with the Atmel ATA5830 Transceiver
- Appropriate for Application Systems Compliant with EN 300 220 and FCC 15

UHF ASK/FSK Receiver

Atmel ATA5780

Summary

Preliminary

NOTE: This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

9207BS–RKE–01/11

1. General Product Description

1.1 Overview

The Atmel® ATA5780 is a universal, highly integrated, low-power UHF ASK/FSK single chip RF receiver. This IC contains the RF part, digital baseband and the AVR® microcontroller core. The core is a low-power CMOS 8-bit microcontroller with enhanced RISC architecture. The receiver is designed for ISM frequency bands in the 310MHz to 318MHz, 418MHz to 477MHz, and 836MHz to 928MHz ranges respectively while featuring a high degree of integration, which reduces the number of external elements. Outstanding RF performance and sophisticated baseband signal processing enables robust wireless communication. The receiver is designed using super heterodyne architecture with an integrated low-IF double quadrature mixer. This architecture features high image rejection and excellent blocking performance. Its flexible, configurable baseband signal processing also allows the receiver to operate in several scanning, wake-up, and automatic self-polling scenarios. During scanning the IC can seek specific message content (IDs) and in case of a valid telegram the data is stored in the FIFO data buffer. The two fully independent receiving baseband paths enable receiving and processing of two different incoming signals. The configuration of these signals can differ in modulation, data rate or wake-up scenario. The autonomous scanning of three different application channels with varying configuration is supported. The settings of the receiver are stored in a 512-byte EEPROM. The device can be configured and accessed via an SPI interface.

1.2 Application

1.2.1 Target Applications

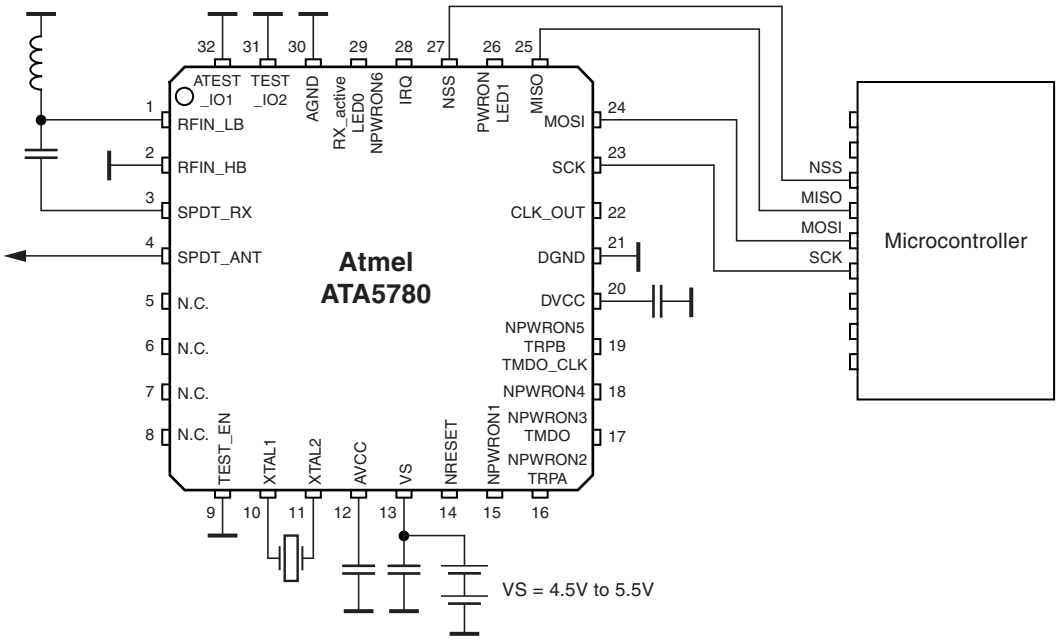
The receiver is designed for use in the following application areas:

- Remote *Keyless Entry System (RKE)*
- *Tire Pressure Monitoring System (TPMS)*
- *Remote Start System (RS)*
- *Remote Control System, e.g. garage door openers*
- *Smart RF Appl*ications

Because of its flexibility the receiver can combine up to three different application types in the autonomous self-polling setting.

1.2.2 Typical Application Circuits

Figure 1-1. Typical 5V Application Circuits



1.3 Main Extended Features of the ATA5780

1.3.1 Outstanding RF Performance

The Atmel® ATA5780 UHF receiver is highly sensitive. Its high image rejection and outstanding blocking performance make a robust application against interferer possible in a low cost design. The programmable channel filter bandwidth additionally provides flexibility to address different system requirements.

1.3.2 Automatic Self-polling and Multi-channel Capability

The autonomous self-polling supports the automatic scanning of three different applications. In the automotive car access market the Remote Keyless Entry (RKE), Tire Pressure Monitoring System (TPMS), and Remote Start (RS) application can be supported with a single IC. In addition, multi-channel systems of up to three frequencies can be used. All five different frequencies can be scanned in the autonomous polling scheme, three frequencies for RKE, a single frequency for TPMS, and also a single frequency for RS. Completely different and unique configuration of each application type is supported. This is possible due to the flexibility of the digital baseband and two different baseband reception paths. The IC can be operated without having to be initial configured by an external microcontroller.

1.3.3 Wake-up Scenario and ID Scanning

The baseband signal processing is designed to reduce host controller processing load. For this purpose the receiver has to find the right telegram (message content) first before the host controller is woken up. The criterion for the wake-up can be determined using a pattern and ID within the telegram. Before the host controller is woken up, the receiver has to find both the correct pattern in the preburst and the valid ID.

1.3.4 Two Separated Reception Paths

The receiver's demodulator contains two separate data paths. The parameters for either path can be set differently, e.g. the modulation type or data rate. Both paths generally work simultaneously, but the first valid data from one of the both paths is stored on the buffer, which can be read by using the SPI command.

1.3.5 Channel Statistic

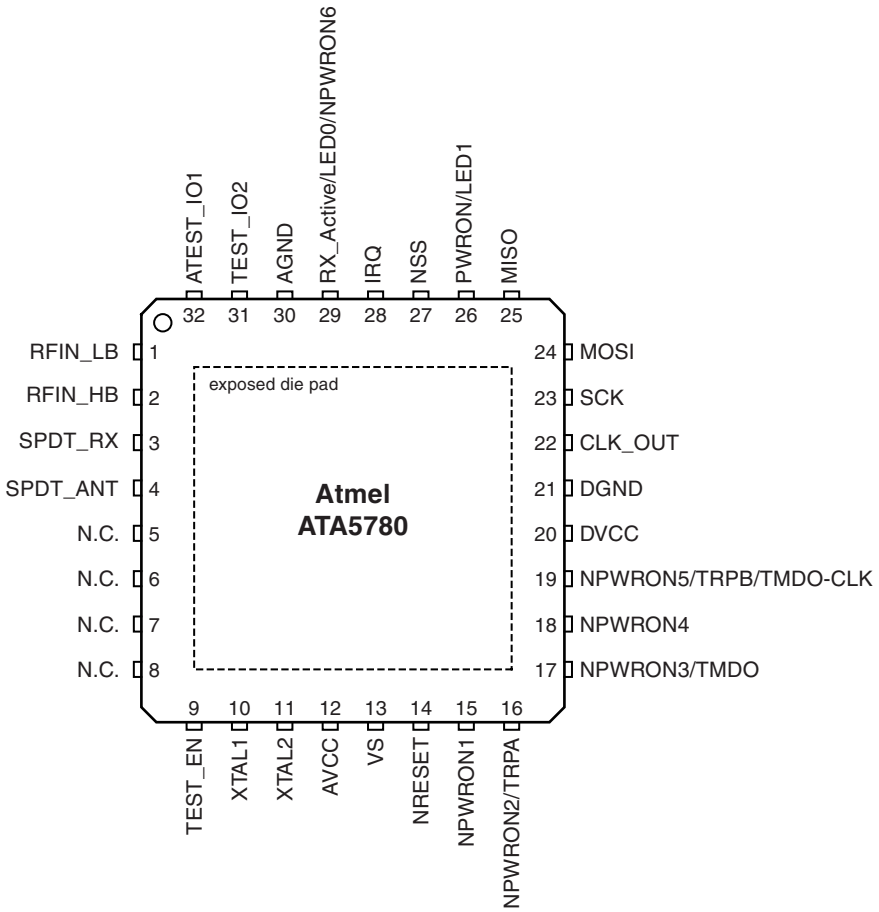
In order to accelerate the communication in multi-channeling the Atmel ATA5780 offers a feature defined as channel statistic. If this feature is activated, the IC will find the best channel having the least interference within the three frequency channels and select the best channel as the first operating frequency during transmission.

1.3.6 Application Firmware

All the functionality described in the datasheet is implemented in 24-Kbyte ROM firmware.

1.4 Pin Diagram and Configuration of Atmel ATA5780

Figure 1-2. Pin Diagram



Note: The exposed die pad is connected to the internal die

Table 1-1. Pin Configuration

Pin No.	Pin Name	Type	Function
1	RFIN_LB	Analog	LNA input for low-band frequency range (< 500MHz)
2	RFIN_HB	Analog	LNA input for high-band frequency range (> 500MHz)
3	SPDT_RX	Analog	RX switch output (damped signal output)
4	SPDT_ANT	Analog	Antenna input for the switch
5	NC		Not connected
6	NC		Not connected
7	NC		Not connected
8	NC		Not connected
9	TEST_EN		Test enable, works with AVCC voltage
10	XTAL1	Analog	Crystal oscillator pin1 (input)
11	XTAL2	Analog	Crystal oscillator pin2 (output)
12	AVCC	Analog	RF front-end supply regulator output
13	VS	Analog	Main supply voltage input
14	NRESET	Digital	NRESET
15	NPWRON1	Digital	NPWRON1
16	NPWRON2 / TRPA	Digital	NPWRON2/TRPA
17	NPWRON3 / TMDO	Digital	NPWRON3/TMDO
18	NPWRON4	Digital	NPWRON4
19	NPWRON5 / TRPB / TMDO_CLK	Digital	NPWRON5/TRPB/TMDO_CLK
20	DVCC		Digital supply voltage
21	DGND		Digital ground
22	CLK_OUT	Digital	CLK_OUT
23	SCK	Digital	SCK
24	MOSI	Digital	MOSI (Master Out/SPI Slave In)
25	MISO	Digital	MISO (Master Int/SPI Slave Out)
26	PWRON / LED1	Digital	PWRON/LED1 (strong high-side driver)
27	NSS	Digital	NSS
28	IRQ	Digital	IRQ (software-controlled external microcontroller interrupt flag)
29	NPWRON6 / RX_ACTIVE / LED0	Digital	NPWRON6/RX_ACTIVE (strong high-side driver)/LED0 (strong low-side driver)
30	AGND		Analog ground
31	TEST_IO2		RF front-end test input/output 2
32	ATEST_IO1		RF front-end test input/output 1
	GND		Ground/backplane on exposed die pad

1.5 Compatibility with the Atmel UHF Transceiver ATA5830

This IC is pin compatible to the transceiver ATA5830. The IC has the identical RX performance of the Atmel® ATA5830 RX path. The difference is on the digital block. The receiver does not contain a free usable microcontroller and is operated using a ROM-only programmed AVR® as state machine without flash or TX part. This receiver is therefore fully compatible with the transceiver and can also be customized via EEPROM settings.

2. System Operation Modes

2.1 Operation Mode Overview

This section provides an overview of the standard modes and the transition between them.

In the OFF mode all the circuit blocks of the receiver are deactivated. The IC can be woken up by activating the PWRON pin or NPWRON pins.

In the idle modes most receiver circuits are deactivated. If not, at minimum the oscillators are deactivated. The Atmel® ATA5780 features two idle modes. The first is IDLE_RC which only activates the RC oscillator in the microcontroller section. The second one is IDLE_XTO; in this mode the Crystal oscillator is active in additional to the RC oscillators.

In RX mode all the circuits necessary for receiving telegrams are active.

In polling mode the receiver is switched between active mode and sleep mode to reduce current consumption. During active mode the receiver scans for a valid signal. If no valid signal is available, the receiver automatically goes into sleep mode. The polling cycle and the wake-up criteria can be set in the EEPROM of the receiver. In the polling scenario three different applications can be covered: the Remote Keyless Entry (RKE), the Tire Pressure Monitoring System (TPMS), and the Remote Start (RS). For the RKE up to three operating frequencies can be used. Because of the flexibility of the IC the wake-up criteria and polling cycle for each application can be defined separately in the EEPROM.

3. Description of System Functions

3.1 OFF Mode

The purpose of this mode is to set the device in a condition with very low current consumption. For example a current consumption of 5nA can be typically expected for a 3V application, which is a benefit for the battery application. All the circuits of the receiver, AVCC, and DVCC are deactivated while in this mode so that the device will not be sensitive to any RF signals or SPI commands. Furthermore, all the ports are set as an input. To leave the mode, the receiver must be woken up using the PWRON pin or NPWRON pins.

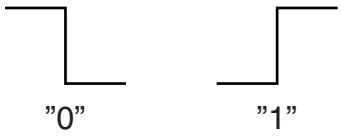
3.2 IDLE Mode

Most parts of the circuit are deactivated in idle mode. It is advisable to set the AVR® core to power-down mode in order to achieve the lowest current consumption. The Atmel® ATA5780 receiver provides 2 different idle modes, Idle RC and Idle XTO. For Idle RC the DVCC power supply is active and the AVR core runs with either slow RC oscillator (SRC) or fast RC oscillator (FRC). DVCC, AVCC, and XTO are active in Idle XTO mode.

3.3 Coding Schemes and Modulation Option

The Atmel receiver ATA5780 works with Manchester and NRZ coding for system design flexibility. Figure 3-1 shows the Manchester coding polarity which is usually used in the application. Because of its flexibility, system designers can configure the Atmel receiver ATA5780 using another polarity of the Manchester coding. This can be set in the EEPROM configuration.

Figure 3-1. Manchester Coding Polarity



3.4 Receiving (RX) Mode

The receiver’s RX mode can be started in two ways, first by using the “Start_RX_EEPROM” SPI command. In this case the command leads the loading of all channel parameters from the EEPROM and starts RX mode. Secondly, the RX mode starts after power on automatically as preselected in the EEPROM. In this condition the IC automatically leaves OFF mode, checks the receiver configuration in the EEPROM (TC2), loads all channel parameters from the EEPROM and starts RX mode.

3.4.1 RX Transparent Mode and Buffered Mode

If the transmitter or receiver buffer mode is set, the received telegram is stored in the 32-byte RX buffer first before it can be read via SPI command. The Atmel ATA5780’s demodulator contains two different paths whose parameters can be set separately, e.g. the modulation type and data rate. Both paths generally work simultaneously until the device receives initial valid data from one of the both paths. Only this initial valid data is stored in the RX buffer. Because the buffer is a ring buffer, a special interrupt is defined for the microcontroller (e.g., the AVR block) so that the stored data can be read out quickly.

In transparent mode, after the receiver recognizes the valid wake-up criterion the received data stream and a corresponding data clock are generated on TMDO and TMDO_CLK directly. The wake-up criteria must be set in the EEPROM. The first criterion is detection of BitCheck and the start bit. This is the criterion for a standard telegram format. The second one is the wake-up pattern and the SFID, which are part of a flexible telegram format. If the two demodulator reception paths (path A and path B) are activated, the signals generated on pin TMDO and TMDO_CLK come from the path which has recognized the first successfully wake-up criterion.

For analysis and monitoring purposes the IC offers another type of transparent signal. The pin TRPA and TRPB can be used for this purpose. The raw data received is generated at the selected pin.

3.4.2 Modulation in Receiving Mode

Atmel® ATA5780 supports the typical modulation types in short-range device applications, as well as ASK and FSK modulation types. The novel feature of this Atmel receiver is its ability to receive GFSK modulated telegrams.

3.4.3 Data Rate

Using the buffer mode the receiver supports the data rate from 0.5kBps to 20kBps in Manchester coding, whereas in NRZ coding the supported data rate range is between 1kBps and 40kBps.

One of the important parameters for system sensitivity is the data rate tolerances. Atmel ATA5780 supports the receiving of signal with a data rate tolerance of up to ±10% without any sensitivity loss. The guaranteed sensitivity loss is just 1dB for data rate tolerance of up to ±20%.

3.4.4 RX Error Handling

This section describes the behavior of the device if a bit error or an ID scan error occurs during the reception process. The discussed condition in this section is the receiving mode's state after the successful detection of an SFID or start bit. The RX error handlings can be set to receiver configuration 6 (TC6) in the EEPROM.

3.4.5 Controlling an External LNA

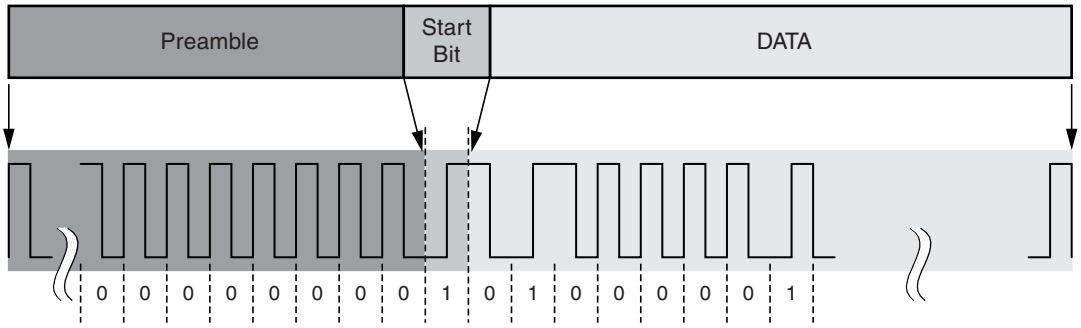
Depending on the system requirement, higher reception path sensitivity may be required. An external low noise amplifier should be used to boost sensitivity. This device offers an RXACTIVE output pin which can be used to bias the external LNA. Basically, the pin shows the active time of the receiver path and can supply a maximum of 4mA current consumption. The polarity of the RX_ACTIVE pin can be set in the EEPROM (IRQ/event configuration).

3.4.6 Protocol and Telegram Handling

3.4.6.1 Simple Telegram (FTS = 0)

A simple telegram consists of a preamble, start bit and data stream. The start bit is the part of the first data byte which must be different from the preamble sequence. If the preamble sequence is “0000…” the start bit must be “1”. Conversely, the start bit must be “0” if the preamble sequence is “1111…”.

Figure 3-2. Principle of the Simple Telegram



Whether a telegram is valid or not is decided using the bit check function and start bit as the synchronization point. This telegram has less sustainability against noise. In order to guarantee that the receiver will not be woken up very often by environmental noise the bit number to be checked must be set to higher than 6.

3.4.6.2 Flexible Telegram Support Enabled (FTS = 1)

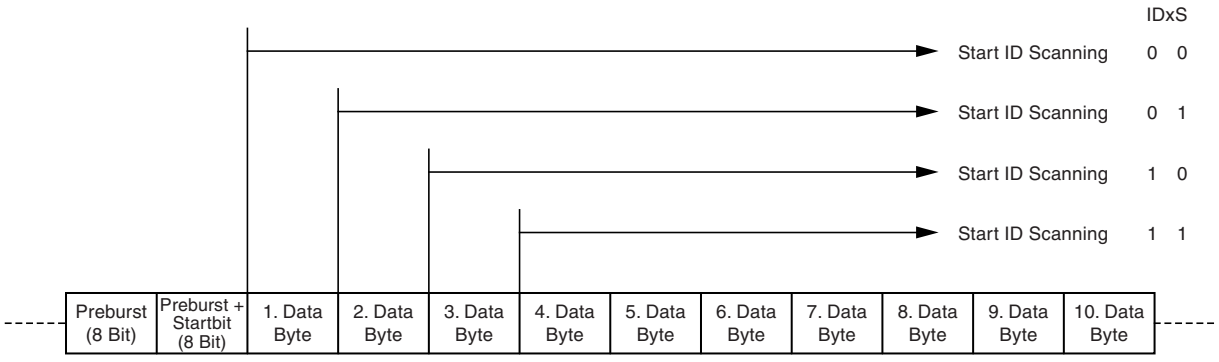
This kind of telegram offers more sustainability for the communication link. This flexible telegram consists of a wake-up pattern (WUP), a relatively short preamble and SFID preceding the data stream. Between the WUP and preamble a space can be inserted in which no carrier signal occurs. An optional stop bit may come at the end of the telegram. This is not absolutely necessary because the end of the telegram is recognized when a Manchester code violation is detected.

Figure 3-3. Principle of the Flexible Telegram

3.4.7 ID Scanning

One novel feature of the receiver is ID scanning used in combination with RX buffer mode. The receiver compares the received ID with the stored IDs in the EEPROM memory. Up to 18 IDs can be stored and each ID can be 4 bytes long at the most. The number of the IDs to be activated can be set in the ID_EN control register. The ID length and the position of the ID in the data stream can be specified in the IDx_CTRL control registers. Figure 3-4 illustrates where the ID could be positioned in a data stream.

Figure 3-4. Possible ID Position in a Data Stream



Note: If a telegram with a valid ID is received the receiver automatically reverts to idle mode.

3.4.8 RSSI Measurement

The receiver offers digital RSSI values and measures the RSSI value of the received signal at regular intervals. This feature works in RX mode only. The measurement intervals must be set in the RSSI configuration of the EEPROM.

The measurement interval can be configured to be between 0.25ms and 4.0ms. The measured RSSI values are stored in a 32-byte RSSI buffer.

The RSSI sampling is started the moment the start bit or SFID is successfully recognized. In case the RX mode is restarted or when the ID check fails during polling, the RSSI buffer pointer is set to the initial values. Depending on a defined buffer fill level the device can generate an event or interrupt which can be used to trigger the microcontroller. The following receiver states allow the RSSI request to be activated:

- Demodulator_stable
- Bit/WUP check or
- RX_Mode

The RSSI can be used in both RX buffer and Rx transparent mode.

As a part of the flexible telegram support (FTS = 1) the Atmel® ATA5780 receiver allows the minimum and maximum RSSI value to be defined as additional wake-up criteria.

The minimum and maximum values are stored in SRAM with the initial values of 0x00 (min) and 0xFF (maximum). With this initialization there is no restricted area and all telegrams with a valid WUP check are accepted.

3.5 Polling Mode

3.5.1 Overview

The use of polling mode in the Atmel ATA5780 reduces current consumption. In this mode the receiver path alternates between active and sleep mode. During the short active mode the device scans for the valid telegram. During a relative short active period the wake-up (WUP) logic verifies the incoming signal by checking the telegram for a valid wake-up pattern or bit check. The device is able to detect two different telegram types. The first one is the standard telegram type for which the wake-up criteria are the bit check and start bit. The second telegram type is a flexible telegram which is validated using a wake-up criteria pattern, SFID, etc. If no valid telegram is detected, the receiver returns to sleep mode. The device stays in active mode if a valid telegram is detected.

The autonomous polling scenario of the Atmel ATA5780 allows three different application types to be combined: Remote Keyless Entry (RKE), Tire Pressure Monitoring System (TPMS), and Remote Start (RS). The receiver path automatically scans for the valid telegrams of the three applications. For the RKE a multi-channel system of up to three operating frequencies can be used. All polling scenario settings can be selected when configuring the EEPROM. The frequency ranges, modulation, data rate, and the wake-up criteria of the three different application channels can be completely different. Even the polling cycle of the RKE, TPMS, and RS system can uniquely be defined in the EEPROM. This flexibility allows the combination of three different application systems using a single device, which helps reduce system costs.

3.5.2 Polling Cycle Time

The polling cycle time determines the average current consumption in RX polling mode. This is the time period between activation of two receiver paths. The cycle time can be programmed to be between 0ms and 4000ms and is determined when setting timer 1.

If reception path activation depends on the EEPROM configuration, the polling mode is also started. This begins with a bit check or scanning for a valid WUP. One enhanced feature of the device is the RF carrier detection during this phase in FSK applications. This shortens the active time when no signal can be detected. If a bit check/WUP scan fails, the receiver goes into sleep mode or skips into the next defined frequency channel and application channel respectively.

3.5.3 RKE Channel Statistic During Polling Mode

This feature is only active in combination if a flexible telegram type is not supported (FTS = 0).

The receiver is able to use as many as three channels for RKE/PEG applications, thus enhancing sensitivity and making the receiver resistant to disturbance. The RKE channel with the best reception characteristic is constantly detected in RX polling mode and fast polling mode. This is done by measuring and comparing the RSSI value for each RKE channel during bit check/WUP check. The channel with the lowest RSSI signal is stored as the “best channel” in the status register FLAG3 (BCRKE 3:1). Before transmission commences, the connected microcontroller can read out the best channel information and is able to begin transmission on this channel.

Note: The TPM and RS channel are not considered in the channel statistic!

Follow these steps to identify the best RKE channel during polling mode:

During each polling cycle, the RKE channel with the best reception behavior is determined and stored in a status register (FLAG 3, BCRKE2:0). This is done by reading the RSSI value during bit check/WUP for each channel. The channel with the lowest RSSI value (= undisturbed) is the channel with the best reception characteristic.

When using multiple RKE channels, transmitting should always start with the channel which had the best reception characteristic in the past. This can be determined by reading the best channel status information (FLAG3) and starting transmission on the corresponding channel. This minimizes the response time for passive entry go applications.

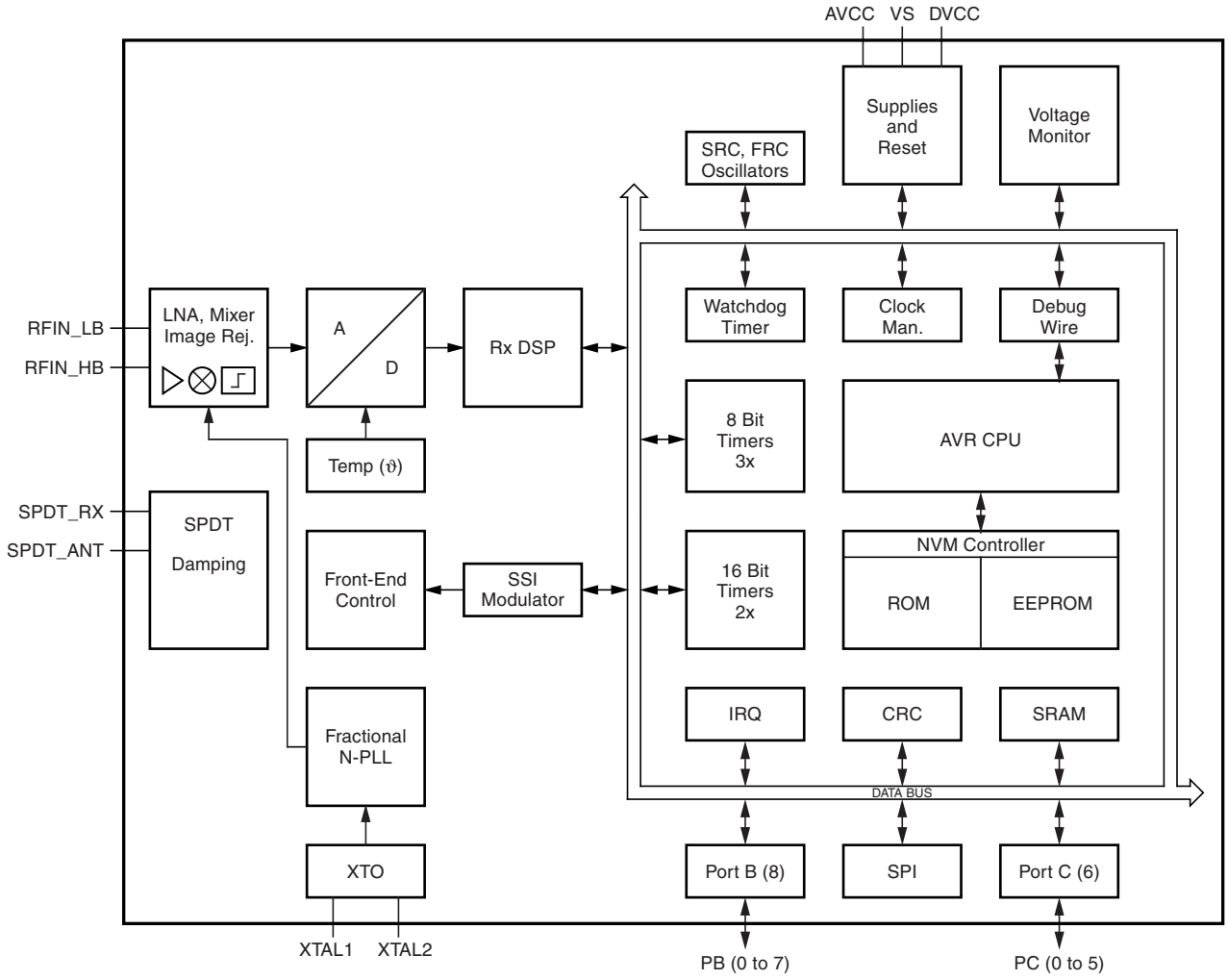
4. Block Description

4.1 General Circuit Description (System Block (Module))

Figure 4-1 shows the simple system block diagram of ATA5780.

The crystal oscillator and the fractional-N PLL generate the reference signal for the mixer which down-converts the incoming signal to the IF frequency of approx. 251kHz. The Atmel® ATA5780 covers the worldwide ISM frequency ranges of 315MHz, 434MHz, 868MHz, and 915MHz. Two completely different low noise amplifiers (LNA) were designed for the low- and high-frequency band. The IF signals are sampled using high resolution ADC. The baseband signal processing is performed using the digital signal after the ADC. The digital RSSI signal is measured after the channel filter. Two completely different reception paths A and B can be set, making the combination of settings more flexible.

Figure 4-1. Simple System Block Diagram



4.2 Fractional-N PLL and VCO

4.2.1 VCO Calibration

The VCO calibration must be enabled in the EEPROM (register CALCONF1 bit VCOCALE = 1). The maximum time for the calibration routine is approx. 150µs. The operating frequency of the VCO is approx. 1.5GHz to 2.0GHz

The front-end register FEVCT contains the 4bit digital control word for the VCO.

4.3 Receive Path

4.3.1 Overview

Two LNAs, for high band and low band respectively, are provided for optimal matching for each frequency range.

An RF detector is included after the LNA successfully detects overload of the receiver by a blocker. An overload event of this kind can be read out from the FE_SPI address space. A switch with 0dB/15dB damping is included to allow reception in the presence of strong blockers. The damping is switched on and off by a control register bit located in the FE_SPI address.

This detector is activated during the PLL start and the result is used to control the damping switches located in front of the LNA to reduce the LNA overload (the LNA is the first overloaded component in the reception path, damping after LNA therefore does not increase large-signal capability).

Damping 15dB before the LNA therefore causes a sensitivity loss of 15dB but enables the receiver to receive data in the presence of modulated blockers 15dB exceeding I1dBKP = –35dBm. This means, for example, that at 165kHz IF bandwidth and a modulated blocker with a peak value of –17dBm at a distance of 5MHz, reception of a signal with 20kBit/s ±20kHz dev is possible with a sensitivity of –91dBm.

The resistors and capacitors in the process technology used have a tolerance of about 20%. Digital correction is performed on-chip to ensure accurate resistors and capacitors and enable their use as a reference resistor for the PA, as load capacitors for the XTO, and as an accurate loop filter for the PLL.

The resistors are calibrated with an on-chip reference resistor and the result is stored in the factory-locked EPROM (XRow). The capacitor is calibrated by the frequency deviation in the XTO and the result is stored in the factory-locked EEPROM, resulting in highly accurate integrated load capacitors for the XTO and less accurate capacitors in the loop filter.

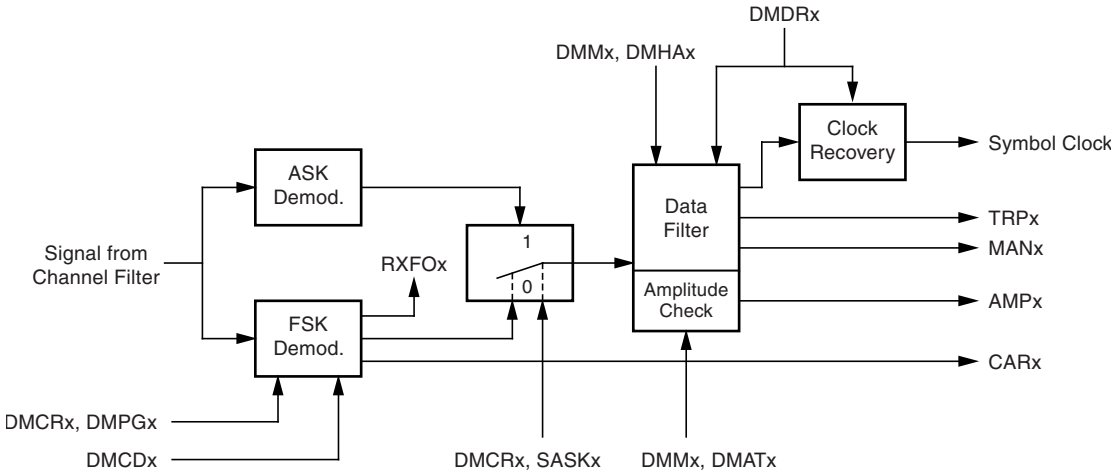
In RX mode the receiver is sensitive to signals coming from one corresponding transmitter (RKE1, 2, 3, TPM or RS channel). RX mode is started after power on if it is preselected in the EEPROM or if it can be started with an SPI command.

4.3.2 Rx Digital Signal Processing

The Rx DSP block performs digital signal processing, decoding, and checking of the Rx samples from the ADC. It delivers the raw data at the TRPA/B pins, the decoded data at the TMDO output and finally the buffered data words from the Rx buffer.

4.3.2.1 Demodulator

Figure 4-2. Simplified Demodulator and Clock Recovery Block for One Path



Note: x represents path A and B

Dedicated demodulators are available for reception path A and B. This allows unique settings for each data path. The only limiting factor for differences is the common channel filter fixing a common bandwidth for both data paths. ASK/FSK modulation, data rates, and deviation can be set independently.

The demodulator supports the following modulation schemes:

- ASK
- FSK with a deviation range of 0.5KHz to 80KHz
- GFSK

Fading up to 1dB per bit is tolerated by the demodulator.

Data rates for NRZ or symbol rates for other coding schemes:

- Min: 0.5KBaud
- Max: 40Kbaud

A matched filter is available for Manchester coding; therefore the supported data rates are higher than calculated from the symbol rate. The Manchester data rate range is: 0.25Kbit to 80Kbits.

The demodulator provides DPLL-based data clock recovery for optimized sampling positions that tolerates single-bit errors.

The internal states of the demodulator are reset by disabling the complete Rx DSP(RDCR.RDEN=0), by activating the power reduction for the channel filter (RDPR.PRFLT=1), or by activating only the power reduction for the reception path A/B (RDPR.PRPTA/B=1).

In the demodulator block the signal is processed in two identical paths A and B operated in parallel. Each single path consists of the following:

- Demodulating part
- Post-detection filtering
- Data slicer
- Clock recovery
- Symbol check

FSK Demodulation

The demodulator is based on a digital PLL. The demodulating process starts with carrier frequency detection of the useful signal, which is the (assumed) dominant frequency within the spectrum in the channel filter. The demodulator is centered using the measured frequency offset approaching the desired frequency. The time constant of the regulation loop is changed stepwise for this purpose. The final setting depends on the deviation and data rate of the signal to be received and is stored separately for path A and B (in the value DMCRx.DMPGx). The effective bandwidth for the demodulation process is therefore smaller, resulting in a higher CNR.

The duration of the carrier frequency detection and centering depends on the selected loop gain in DMCRx.DMPGx. The loop gain must be set to achieve an appropriate output signal for the expected deviation and data rate.

Please note that for a certain setting the supported frequency deviation range and data rate is limited. This block provides the frequency offset value RXFOx of the received signal.

The loop coefficients of path A and path B is changed during the first stage of reception in order to lock to the signal. The final value of A depends on DMPGx and B is 1/2048.

ASK Demodulation

The ASK demodulation is achieved by calculating the magnitude of the complex (I-Q) baseband signal in a logarithmic scale. Before the signal enters the filters it is limited to achieve the amplitude range from detected peak level down to 23dB. The parameters of the peak detection are scaled by the selected data rate range in each path.

Post-detection Filtering (Data Filter)

Further filtering and decimation is done for signal paths A and B by a 2-stage filter followed by a data slicer. The first stage contains 2^{nd} order CIC architecture with programmable down-sampling. The down-sampling ratio is $2^{DMDRx.DMDNx}$. In addition, the signal is processed by a moving average filter whose length is derived from the DMDRx.DMAx value.

This block has two outputs:

- Manchester matched (MANx)
- Symbol-based (TRPx also available to ext. pin)

The symbol-based filter needs DC compensation which is performed by a feedback loop. This loop is invoked a certain time after an edge at the data slicer output has been detected. Then the compensation value is held until the next edge. The control signal DMHx = 0 limits this hold sequence to the duration of three symbols.

Clock Recovery

A recovered clock based on detected edges is provided for sampling the filtered signal. The start sequence of a telegram is used to match to the data/symbol rate. The initial symbol rate is obtained from the DMDRA/DMDRB register.

RSSI (Digital)

The RSSI is calculated from the magnitude of the baseband signal and corrected by the gain of the channel filter. Depending on the setting of DMDRA/DMDNA (data rate path A), a number of 2DMDNA raw samples are put together and an average value built. The peak value from these results is held and stored to the RSSI register. The read process for the RSSI value resets the max-hold circuit.

Symbol Check

This block checks the incoming signal quality needed to control the receiver.

There are four checks which generate a pass or fail signal:

1. Carrier check (FSK only) is derived from the FSK demodulator (similar to a lock detect)
2. Modulation amplitude check (signal out of the post detection filter)
3. Symbol timing check (compares the signal edge positions in relation to clock recovery)
4. Manchester check (checks if the sampled symbols conform with Manchester code)

An OK signal is generated if there is no fail during a number of symbols/bits, which can be programmed.

4.3.2.2 Rx Buffer

Two reception buffers are available. They are connected to the reception path A and B data outputs. This allows simultaneous reception of both modulation types or reception of the same modulation type with different data rate settings (TPM, RKE). Each buffer has its own interrupt for AVR® wake-up to allow data read-out before the next byte is received. If the data is not read out, it is overwritten by the following byte.

A 32-byte receive buffer is available in the receiver and can be used for data reception. When starting RX mode the RX buffer pointer is set to the initial values (reset).

4.3.3 Transparent RX Mode

4.3.3.1 TMDO / TMDO_CLK

The received data stream and a corresponding data clock are available on pin 17 (TMDO) and 19 (TMDO_CLK) if the following conditions are fulfilled,

- RX transparent mode is enabled
- Successful bitcheck/wake-up check
- Valid startbit/SFID

If the demodulator path A and path B are enabled, the first path to get a successful bit check or valid start bit/SFID is passed through to pin TMDO (pin17) and pin TMDO_CLK (pin 19).

4.3.3.2 TRPA / TRPB

This transparent signal is a raw signal directly from the demodulator output.

4.3.4 RSSI

An RSSI buffer is provided to analyze the signal strength profile based on the telegram length. The RSSI buffer length is 32 bytes. The RSSI sample rate can be programmed to be between 250µs and 4ms. The RSSI buffer is organized as a ring-buffer and the customer must ensure there is buffer overflow. RSSI sampling is started with the start bit/SFID okay. When starting RX mode or when the ID check fails during polling, the RSSI buffer pointer is set to the initial values (reset).

4.4 SPDT Block

4.4.1 Receiver Damping

This feature allows a desired signal to be received in the presence of strong blockers. If the damping is activated, the reception path has 15dB more attenuation. This damping can be set by a control register bit located in the front-end register. An RF detector is implemented in the LNA circuitry which detects overload power in the LNA stage. This condition can be read out via an SPI command. This detector is activated during PLL start and based on this result the damping switches are set. Because the damping in this case is located in the front of the LNA, overloading can be reduced.

Of course this overload protection of 15dB leads to a sensitivity loss of 15dB, but it still enables data reception in the presence of modulated blockers 15dB above the 1dB compression point (ICP1dB = –35dBm).

4.5 Power Management

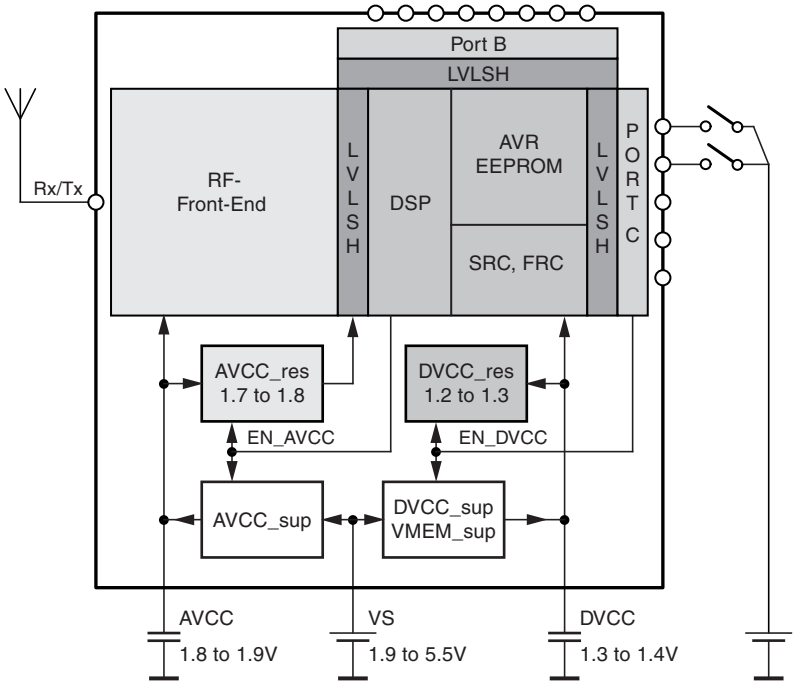
4.5.1 Introduction

The IC has three power domains:

- Vs - the unregulated battery voltage from the supply pin.
- DVCC - the regulated digital supply voltage.
- AVCC - the regulated RF-front-end supply.

Each supply regulator has a corresponding reset. The reset thresholds ensure correct operation of the supplied circuits when the reset is de-asserted. This keeps inadvertent memory content loss from happening without notice. The AVCC regulator has an additional threshold above the reset to ensure that the analog circuits are working properly.

Figure 4-3. Power Supply Management Overview



4.5.2 Supplies

The DVCC supply is enabled by a pin power-up. A pin power up happens when PWRON is set to high or NPWRONx, are set to low for a time period longer than $T_{power\_on\_REQ}$. The actual power-up source can be determined by reading the corresponding input ports.

4.5.2.1 AVCC Supply Regulator

The AVCC supply regulator provides the supply for the RF front end. It delivers a high output current while retaining close control of voltage. Load transitions up to 3mA do not trigger the AVCC low and reset indicators. This is necessary to allow timely activation of all front-end circuits.

At supply voltages above 2.1V AVCC load transients of more than 8mA are allowed without triggering the reset circuit.

4.5.2.2 VS_PA Supply Regulator

This regulator provides the supply voltage for the power amplifier in the RF front end. It has to be enabled every time a transmit operation is performed.

4.5.3 Resets

During reset, all I/O registers are set to their initial values and the program starts execution from the reset vector. The instruction placed at the reset vector must be a JMP - Absolute Jump - instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used and regular program code can be placed at these locations. This is also the case if the reset vector is in the application section while the interrupt vectors are in the boot section or vice-versa. The circuit diagram in Figure 4-4 on page 20 shows the reset logic.

The I/O ports of the AVR® are immediately reset to their initial state when a reset source becomes active. This does not require a clock source to be running.

After all reset sources have gone inactive, a delay counter is invoked, stretching the internal reset. This allows the power to reach a stable level before normal operation starts. The time-out period of the delay counter is defined by the hardware.

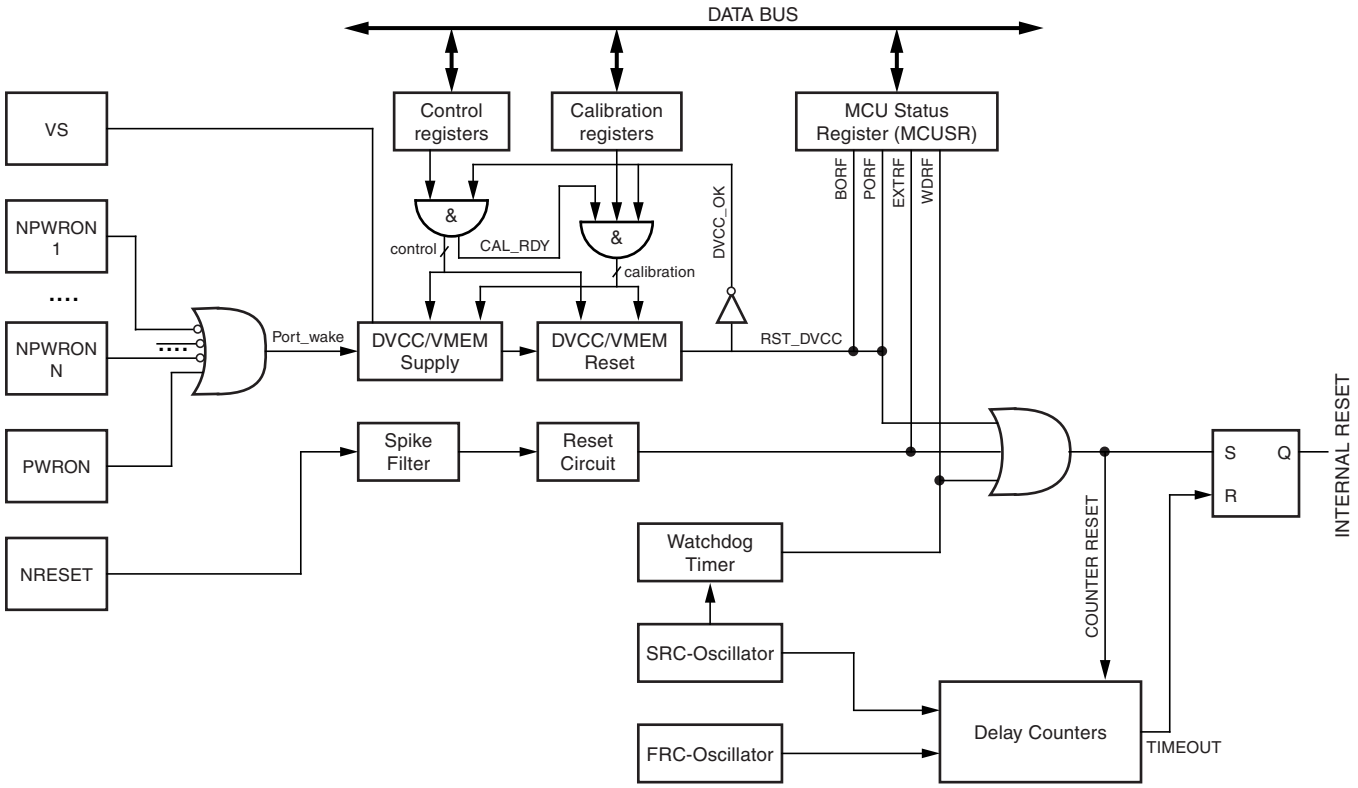
4.5.4 Reset Sources

There are three sources for reset:

- Brown-out (DVCC) reset. The MCU is reset when the supply voltage DVCC is below the brown-out reset threshold (VBOT). The brown-out detector is always enabled.
- External reset. The MCU is reset when a low level is present on the NRESET pin at the external NRESET input for longer than the minimum pulse length.
- Watchdog reset. The MCU is reset when the watchdog is enabled and the watchdog timer period expires.

The RF front end has a separate reset circuit for monitoring AVCC voltage.

Figure 4-4. Reset Logic



4.5.4.1 *AVCC Voltage Supervision*

The AVCC voltage is enabled by the AVEN flag in the SUPCR. Two thresholds are defined for AVCC voltage monitoring:

- Th_RST_AVCC - indicates that the voltage is below the safe operating range of the digital circuits
- Th_avcc_low - the voltage is below the safe operating voltage of the analog RF front end circuits

Both thresholds have a hysteresis and trigger a signal with a guaranteed minimum pulse to allow proper operation.

4.5.4.2 *Watchdog Reset*

When the watchdog times out, it will generate a short reset pulse of one CK cycle duration. On the falling edge of this pulse, the delay timer starts counting the time-out period t_{TOUT}.

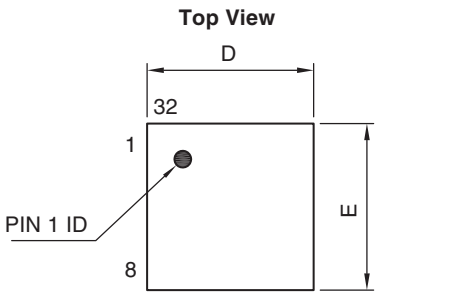
4.5.4.3 *External NRESET*

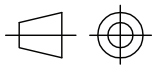
An external reset is generated by a low level on the NRESET pin. Reset pulses falling below the minimum pulse width will generate a reset, even if the clock is not running. Shorter pulses do not necessarily generate a reset. When the applied signal reaches the reset threshold voltage - VRST - on its positive edge, the delay counter starts the MCU after the time-out period - t_{TOUT} - has elapsed.

5. Ordering Information

Extended Type Number	Package	Remarks
ATA5780-PNQW	QFN32	5mm × 5mm PB free

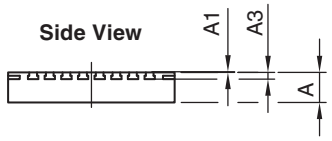
6. Package Information

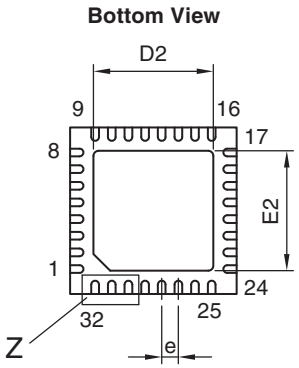




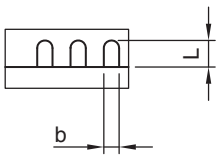
technical drawings
according to DIN
specifications

Dimensions in mm





Z 10:1



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.9	1	
A1	0.0	0.02	0.05	
A3	0.15	0.2	0.25	
D	4.9	5	5.1	
D2	3.45	3.6	3.75	
E	4.9	5	5.1	
E2	3.45	3.6	3.75	
L	0.3	0.4	0.5	
b	0.16	0.23	0.3	
e		0.5 BSC		

10/12/10

	TITLE	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Package: VQFN_5x5_32L** Exposed pad 3.6x3.6	6.543-5124.01-4	2

7. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9207BS-RKE-01/11	• Section 5 “Ordering Information” on page 21 changed

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