20V P-Channel Enhancement-Mode MOSFET

V_{DS}= -20V

$R_{DS(ON)}$, Vgs@-4.5V, Ids@-4.7A = 60 mΩ

$R_{DS(ON)}$, Vgs@-2.5V, Ids@-1.0A = 100 mΩ

Features

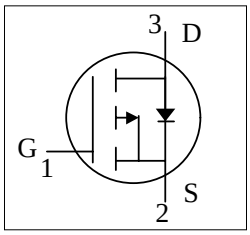
Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

we declare that the material of product compliance with RoHS requirements.

LP3443LT1G

SOT– 23 (TO–236AB)



▼ **Simple Drive Requirement**

▼ **Small Package Outline**

▼ **Surface Mount Device**

ORDERING INFORMATION

Device	Marking	Shipping
LP3443LT1G	P34	3000/Tape&Reel
LP3443LT3G	P34	10000/Tape&Reel

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current		I_D	-4.7	A
Pulsed Drain Current 1)		I_{DM}	-20	
Maximum Power Dissipation	TA = 25°C	P_D	1.1	W
	TA = 75°C		0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Case Thermal Resistance		R_{qJC}		°C/W
Junction-to-Ambient Thermal Resistance (PCB mounted) 2)		R_{qJA}	110	

Note: 1. Repetitive Rating: Pulse width limited by the Maximum junction temperation

2. 1-in^2 2oz Cu PCB board

3. Guaranteed by design; not subject to production testing

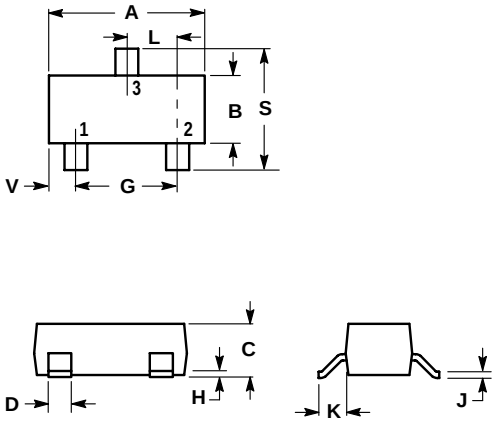
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-20			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -4.7A		48.0	60.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -2.7V, I_D = -3.8A		63.0	90.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -2.5V, I_D = -1.0A		65.0	100.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	-0.6	-0.85	-1.4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0V			±100	nA
Forward Transconductance	g_{fs}	V_{DS} = -10V, I_D = -4.7A		8		S
Dynamic[3)]						
Total Gate Charge	Q_g	V_{DS} = -10V, I_D = -4.7A V_{GS} = -4.5V		24	36	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			2.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10V, R_D=10Ω I_D = -1A, V_{GS} = -4.5V R_G = 6Ω		22	35	ns
Turn-On Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Turn-Off Fall Time	t_f			25	40	
Source-Drain Diode						
Max. Diode Forward Current	I_S				-1.7	A
Diode Forward Voltage	V_{SD}	I_S = -1.7A, V_{GS} = 0V			-1.2	V

Note：Pulse test: pulse width <= 300us, duty cycle<= 2%

LP3443LT1G

SOT−23



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60