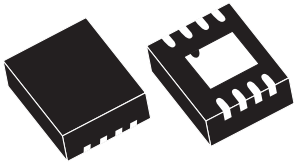
STM11

Power control switch

Features

- Operating voltage 2.5 V to 5.5 V
- Supply current of 2.0 µA (typ.)
- Low on-resistance P-channel MOSFET:
  - Continuous drain current 3.7 A
  - Typical $R_{DS(ON)}$ of 0.065 Ω at 4.5 V
- Slew rate controlled switching to prevent glitches on supply rails
- Factory-trimmed voltage threshold 3.1 V (3.0 V to 3.6 V in 50 mV increments available)
- ± 3% voltage detection threshold accuracy across temperature
- Temperature range –30 °C to 85 °C
- DFN 8-lead 2.5 mm x 3 mm package.



DFN 8-lead
2.5 mm x 3 mm

Applications

- Portable devices
- Cell phones/smart phones
- PDA
- Palmtops
- Portable audio/video players
- Portable terminals.

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1 Description

The STM11 power control switch contains a low on-resistance P-channel power MOSFET driven by built-in control circuitry. Its low on-resistance allows switching of continuous current up to 3.7 A. The low current consumption of 2 µA and small DFN package make this device a perfect solution for mobile and portable applications.

The device is equipped with 3 inputs to detect a power request and provide switch control between the battery and the application (see *Table 1*). The PB input includes voltage monitoring with hysteresis to prevent circuit wake-up until battery voltage is at sufficient level. The threshold voltage level is optimized for single cell Li-Ion or Li-Polymer batteries.

Table 1. Truth table

PB_{BYP}	PS_{HOLD}	PB	V_{OUT}
X	V_{IH}	X	connected to V_{IN}
X	X	$V_{IN} > V_{TH+}$	connected to V_{IN}
V_{IH}	X	X	connected to V_{IN}
V_{IL}	V_{IL}	$V_{IN} < V_{TH+}$	disconnected from V_{IN}

2 Operation

2.1 Power-on sequence

- First the momentary push-button switch 'PB' is pressed (and held), at which point the battery voltage is detected, and if above the threshold, the MOSFET is turned ON, providing power supply to the application. If the battery voltage is below the threshold, the MOSFET will remain OFF.
- Assuming the battery voltage is above the threshold, after some delay, the controller begins to drive 'PS_{HOLD}' high and keeps the MOSFET ON even after the momentary push-button 'PB' signal is released.
- The test jig providing the input 'PB_{BYP}', is used only during manufacturing and bypasses the normal power ON sequence.

2.2 Power-off sequence

- The 'PB' is again pressed (and held), at which point the controller initiates a power-off sequence by taking 'PS_{HOLD}' low.
- At this point, once the push-button 'PB' signal is released, the MOSFET is turned OFF and the V_{OUT} output goes low.

Figure 1. Block diagram

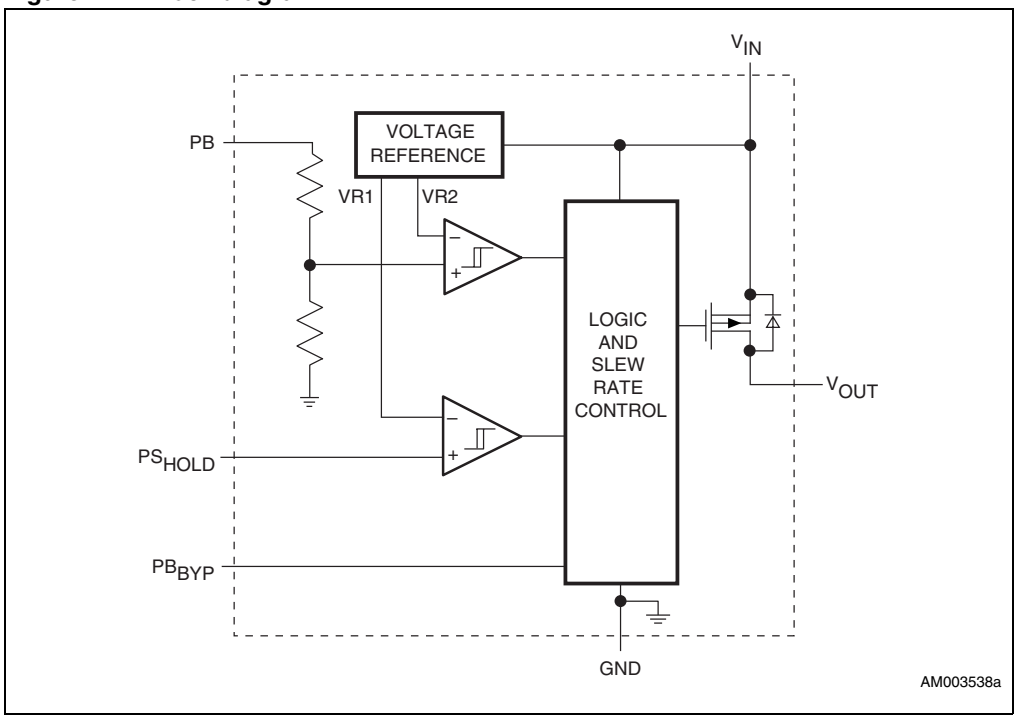
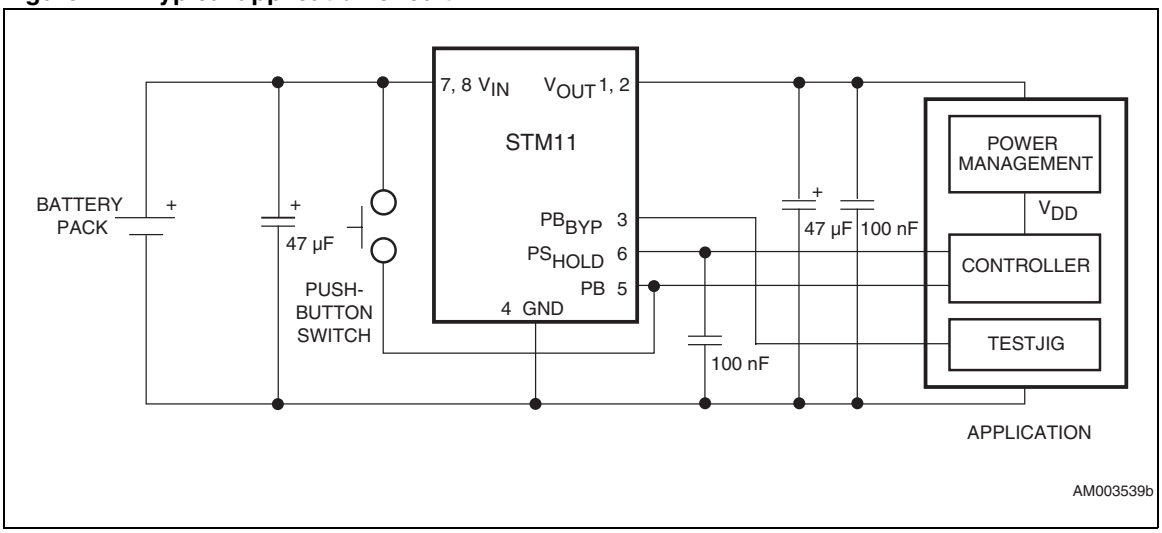


Figure 2. Typical application circuit(1)



1. All capacitors shown are optional components.

Figure 3. Logic diagram

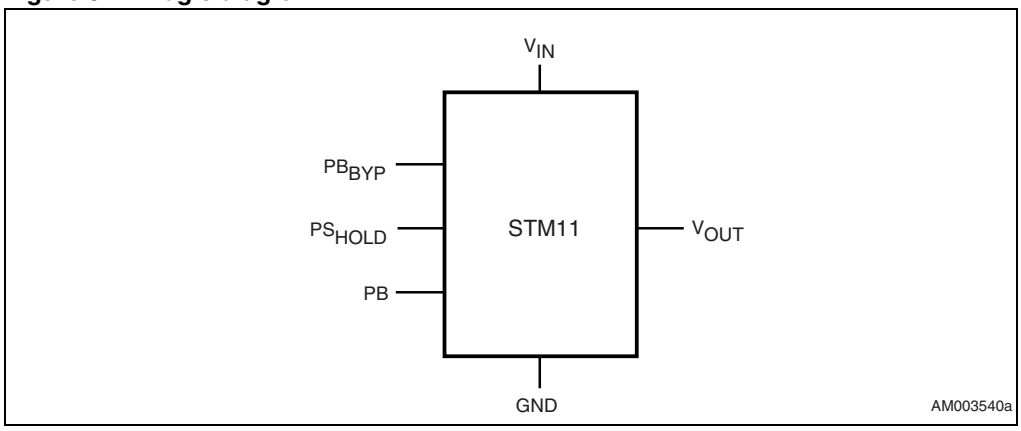
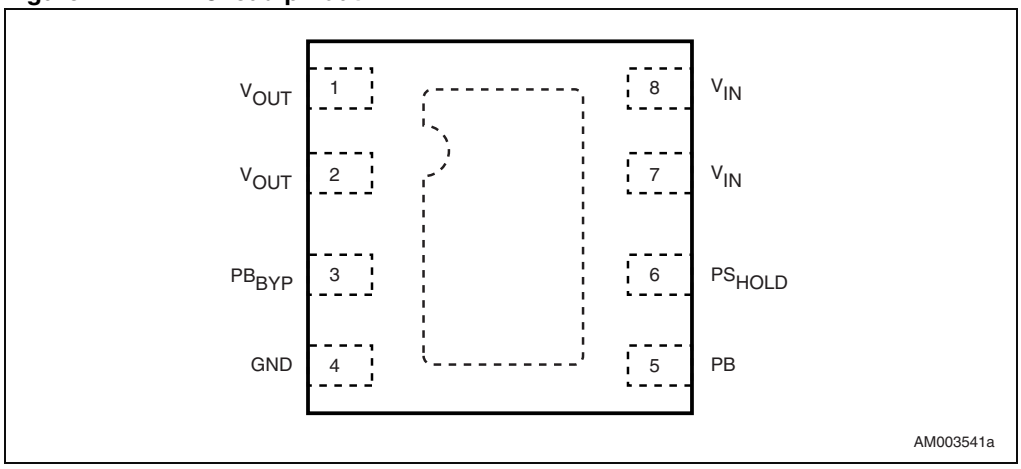


Table 2. Signal names and description

Symbol	Type	Description
V_{IN}	Supply	Voltage input
V_{OUT}	Output	Voltage output
PB_{BYP}	Input	Push-button bypass
PS_{HOLD}	Input	Power supply hold input
PB	Input	Push-button input
GND	Supply	Ground

Figure 4. DFN 8-lead pinout



1. The exposed pad at the bottom side is internally connected to the V_{OUT} pins.

Table 3. Pin description(1)

Pin	Name	Description
1, 2	V_{OUT}	Voltage output
3	PB_{BYP}	Push-button bypass
4	GND	Ground
5	PB	Push-button input
6	PS_{HOLD}	Power supply hold input
7, 8	V_{IN}	Voltage input

1. The exposed pad at the bottom side is internally connected to the V_{OUT} pins.

2.3 Pin descriptions

2.3.1 V_{OUT} (pins 1, 2)

Voltage output. The drain of internal MOSFET. The output ON/OFF switching slew rate is internally limited to improve the EMI parameters and to prevent glitches on the supply rails. Maximum output current is 3.7 A.

2.3.2 PB_{BYP} (pin 3)

Push-button bypass. This is standard CMOS logical input. This input bypasses the voltage monitoring and forces the output ON or OFF (assuming no other input is driven high, see *Table 1*).

2.3.3 GND (pin 4)

Ground.

2.3.4 PB (pin 5)

Push-button input. This input is equipped with voltage detector with a factory-trimmed threshold. A momentary push-button switch to V_{IN} is connected to this pin. When the switch is pressed and held, the battery voltage is detected and the MOSFET is turned ON only if the battery voltage is above the threshold V_{TH+} (see *Table 10 on page 20* for available factory-trimmed thresholds).

2.3.5 PS_{HOLD} (pin 6)

Power supply hold input. This input may be driven by the application controller, and allows a wide range of input levels (for use with 1.8 V or 2.85 V controller I/O voltage range).

2.3.6 V_{IN} (pins 7, 8)

Voltage input and power supply pin. The source of internal MOSFET. Operating voltage range is 2.5 to 5.5 V.

2.3.7 Exposed pad

The exposed pad is internally connected to V_{OUT} (pins 1, 2). It must be connected to pins 1, 2 on the PCB. This pad is not the primary V_{OUT} output.

3 Typical operating characteristics

Measuring conditions: T_A = 25 °C, V_{IN} = 3.6 V, R_L = 1 kΩ (connected between the V_{OUT} and GND pins).

Figure 5. PB_{BYP} to V_{OUT} (ON) delay

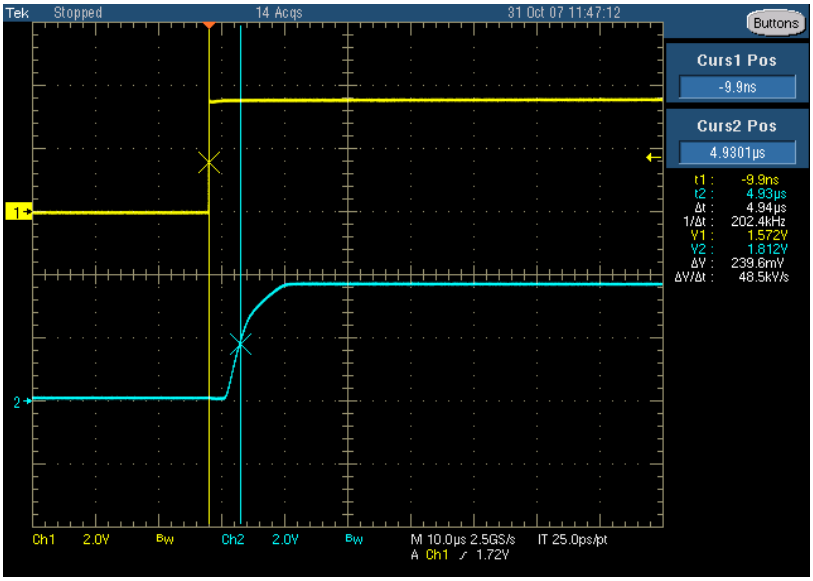


Figure 6. PB_{BYP} to V_{OUT} (OFF) delay

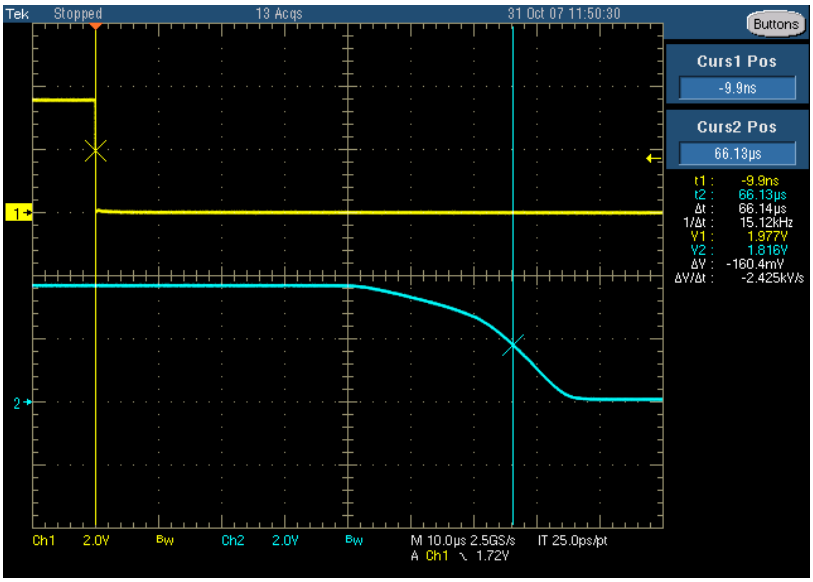


Figure 7. PS_{HOLD} to V_{OUT} (ON) delay

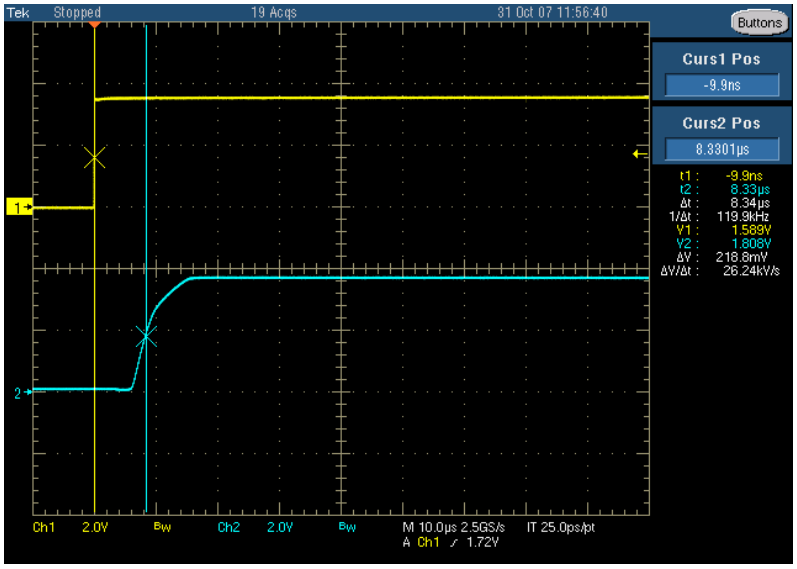


Figure 8. PS_{HOLD} to V_{OUT} (OFF) delay

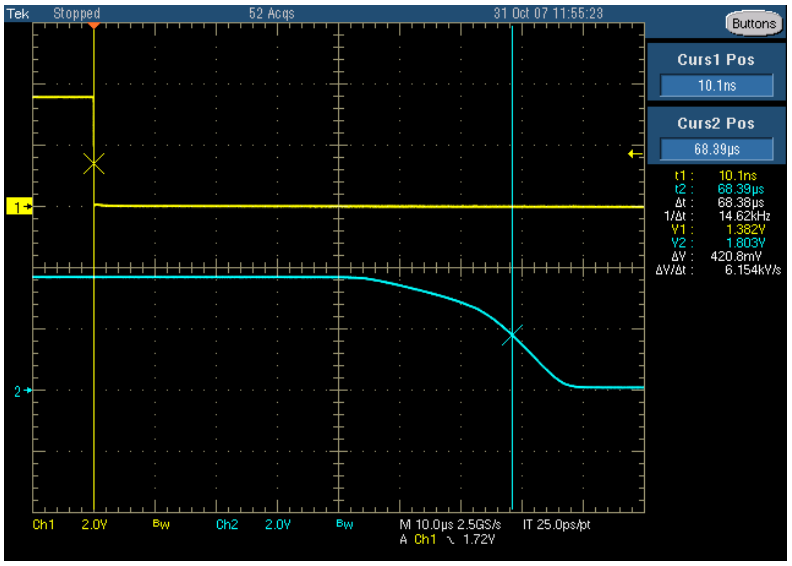


Figure 9. PB to V_{OUT} (ON) delay

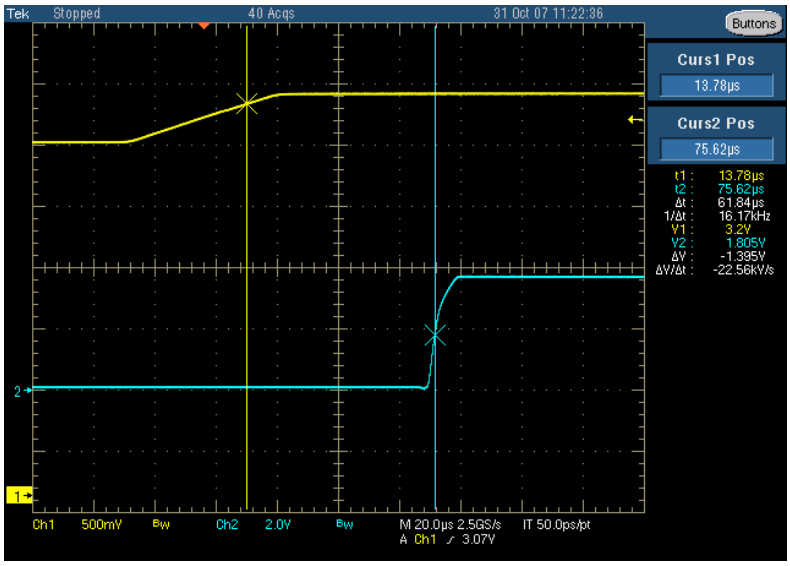
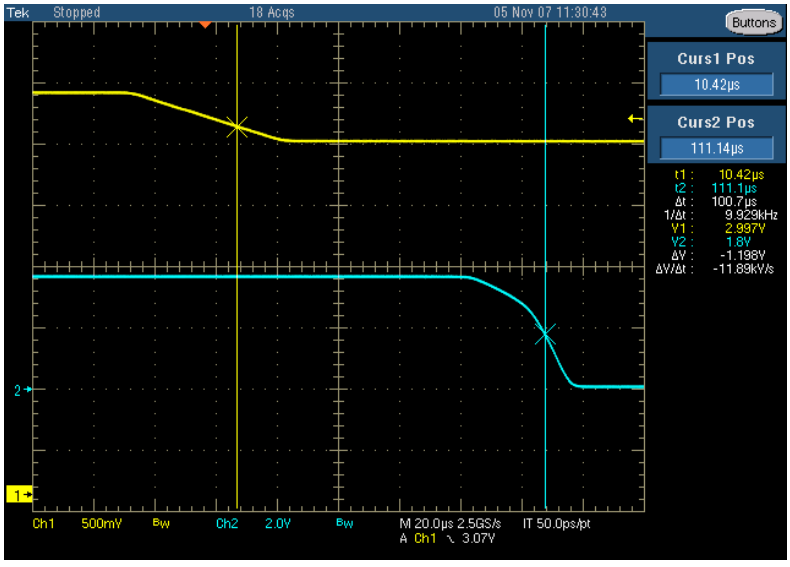


Figure 10. PB to V_{OUT} (OFF) delay



4 Maximum rating

Stressing the device above the rating listed in the *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{IN} OFF)	–50 to 125	°C
T_A	Specified ambient temperature range	–30 to 85	°C
T_J	Junction operating temperature	105	°C
T_{SLD}(1)	Lead solder temperature for 10 s	260	°C
V_{IO}	Input or output voltage	–0.3 to 7.0	V
V_{IN}	Supply voltage	–0.3 to 7.0	V
I_{OUT}(2)	Output current (continuous) at T_A = 25 °C	3.7	A
	Output current (continuous) at T_A = 85 °C	1.8	A
P_{TOT}	Total power dissipation at T_A = 25 °C	1.6	W
	Power derating factor	0.02	W/°C

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. For more details see *Figure 11*.

Figure 11. Maximum I_{OUT} vs. temperature

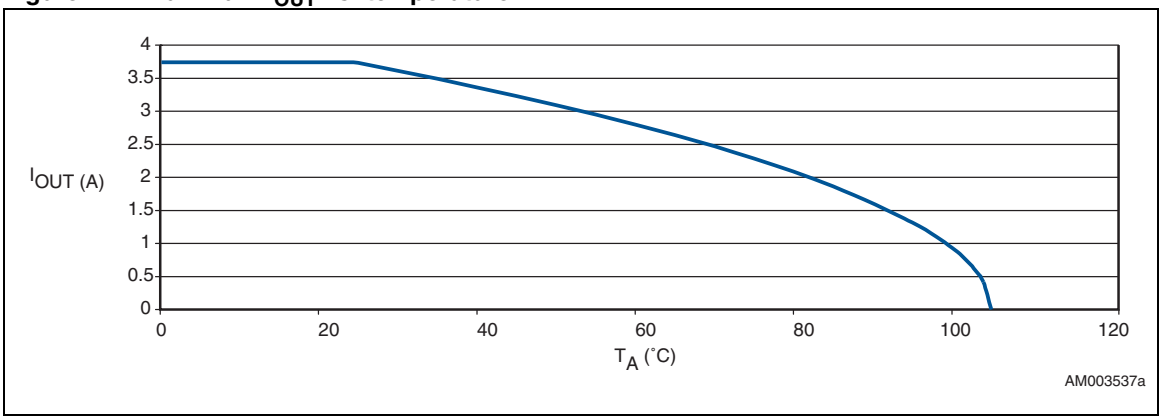


Table 5. Thermal data(1)

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (max)	50	°C/W

1. The device is mounted on a JEDEC test board.

5 DC and AC characteristics

This section summarizes the operating measurement conditions and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in *Table 6*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 6. Operating and AC measurement conditions

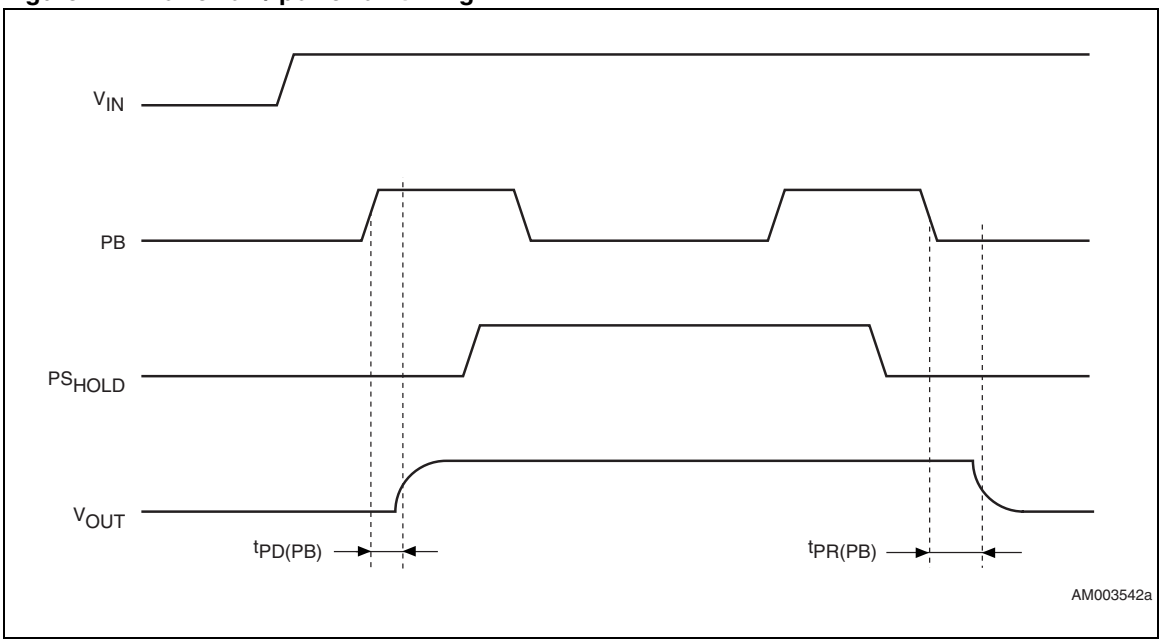
Parameter	Condition	Unit
V_{IN} supply voltage	2.5 to 5.5	V
Ambient operating temperature (T_A)	–30 to 85	°C
Input rise and fall times	≤5	ns
Input pulse voltages	0.2 V_{IN} to 0.8 V_{IN}	V

Table 7. DC and AC characteristics

Sym	Description	Test condition[1]	Min	Typ	Max	Unit
V_{IN}	Operating voltage		2.5		5.5	V
I_{IN}	Supply current	V_{IN} = 3.0 V, no load		1.9	3.5	µA
		V_{IN} = 4.0 V, no load		2.0	4.0	
PB_{BYP} input (from TEST JIG)						
V_{IL}	Input low voltage	V_{IN} = 2.5 V to 5.5 V			0.35 V_{IN}	V
V_{IH}	Input high voltage	V_{IN} = 2.5 V to 5.5 V	0.65 V_{IN}			V
	Glitch immunity		1			µs
	Input leakage current		–1		+1	µA
PS_{HOLD} input						
V_{IL}	Input low voltage	V_{DD} = 1.8 V ± 5% or 2.85 V ± 5%			0.35 V_{DD}	V
V_{IH}	Input high voltage	V_{DD} = 1.8 V ± 5% or 2.85 V ± 5%	0.65 V_{DD}			V
	Glitch immunity		1			µs
	Input leakage current		–1		+1	µA
PB input						
V_{TH+}	Detect threshold		–3%	V_{TH+}[2]	+3%	V
V_{TH-}	Release voltage			$V_{TH+} - V_{HYS}$		V
V_{HYS}	Threshold hysteresis		0.02 V_{TH+}	0.05 V_{TH+}	0.08V_{TH+}	V
V_{OUT} output						
$R_{DS(on)}$	Static Drain-Source ON Resistance	V_{IN} = 4.5 V, I_{OUT} = 1.8 A V_{IN} = 2.5 V, I_{OUT} = 1.8 A		0.065 0.085	0.080 0.100	Ω Ω
$T_{PD(PB)}$	PB to V_{OUT} (ON) Output Delay	V_{IN} rising from (V_{TH+} –200 mV) to (V_{TH+} +100 mV) at 10 mV / µs		60		µs
$T_{PR(PB)}$	PB_{BYP} to V_{OUT} (OFF) Output Delay	V_{IN} falling from (V_{TH-} + 200 mV) to (V_{TH-} –100 mV) at 10 mV / µs		110		µs
$T_{PD(PB_{BYP})}$	PB_{BYP} to V_{OUT} (ON) Output Delay			10		µs
$T_{PR(PB_{BYP})}$	PB_{BYP} to V_{OUT} (OFF) Output Delay			70		µs

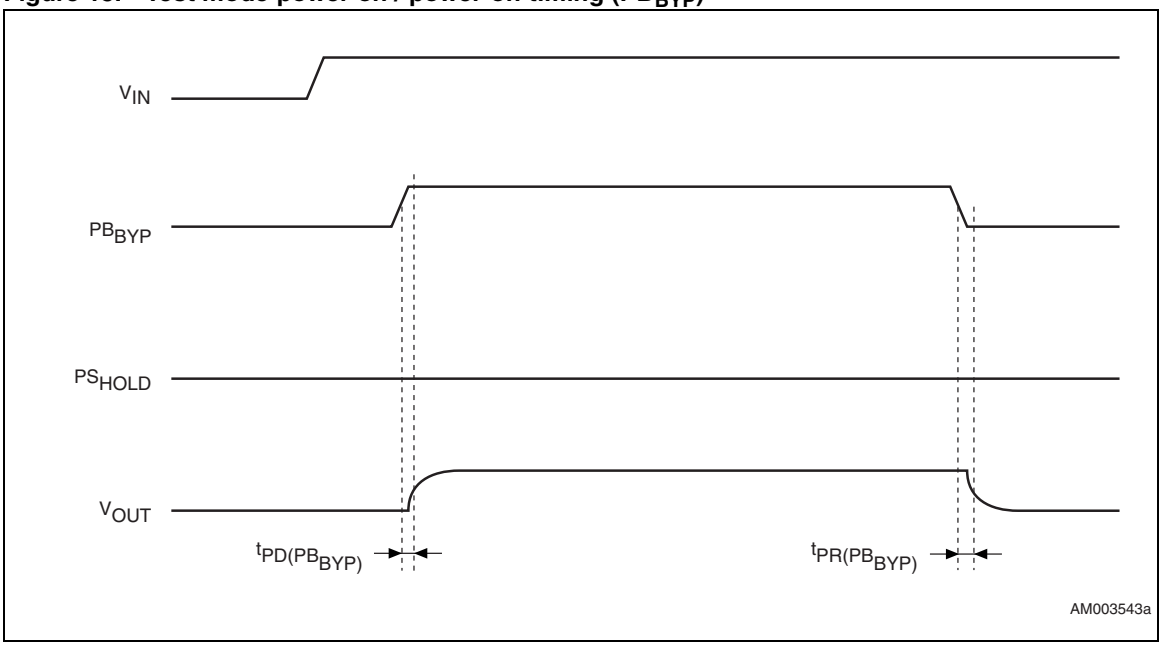
1. Test conditions described in *Table 6* (except where noted). All voltages are related to GND pin potential.
2. See *Table 10: Factory-trimmed thresholds with topside marking on page 20*.

Figure 12. Power-on / power-off timing



Note: PB_{BYP} is low.

Figure 13. Test mode power-on / power-off timing (PB_{BYP})

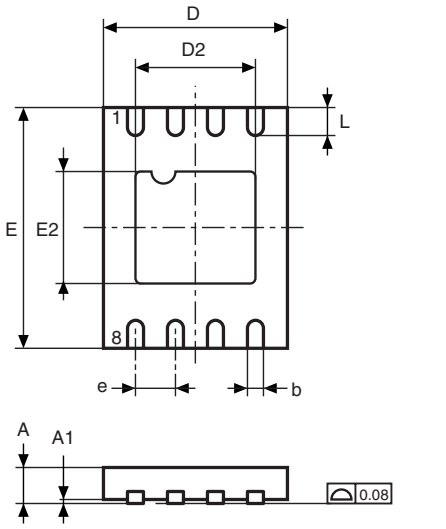


Note: PB is low.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 14. DFN 8-lead 2.5 x 3 mm package mechanical drawing



1. The exposed pad is internally connected to the V_{OUT} (pins 1, 2).

Table 8. DFN 8-lead 2.5 x 3 mm package mechanical data

Symbol	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.00	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
ddd		0.08			0.003	
D		2.50			0.098	
D2	1.86	2.02	2.12	0.073	0.080	0.083
E		3.00			0.118	
e		0.65			0.026	
E2	1.39	1.54	1.64	0.055	0.061	0.065
L	0.30	0.40	0.50	0.012	0.016	0.020
N	8			8		

7 Part numbering

Table 9. Ordering information scheme

Example: **STM11 C10 DF 4P2 8 F**

Device type

STM11

Threshold voltage

C10: 3.10 V (see options in *Table 10*)

Package

DF: DFN-8L (2.5 x 3 mm)

MOSFET

4P2: 3.7 A, P-Channel, 20 V

Temperature range

8: –30 °C to 85 °C

Shipping method

F = ECOPACK package, tape and reel

Note: Contact local ST sales office for availability of device versions other than STM11C10DF4P28F.

Table 10. Factory-trimmed thresholds with topside marking

Part number	Threshold voltage VTH+ (V)			Topside marking[1]
	Min (–3%)	Typ	Max (+3%)	
STM11C00xxxxxxx	2.910	3.000	3.090	ST 11A yww
STM11C05xxxxxxx	2.959	3.050	3.142	ST 11B yww
STM11C10xxxxxxx	3.007	3.100	3.193	ST 11C yww
STM11C15xxxxxxx	3.056	3.150	3.245	ST 11D yww
STM11C20xxxxxxx	3.104	3.200	3.296	ST 11E yww
STM11C25xxxxxxx	3.153	3.250	3.348	ST 11F yww
STM11C30xxxxxxx	3.201	3.300	3.399	ST 11G yww
STM11C35xxxxxxx	3.250	3.350	3.451	ST 11H yww
STM11C40xxxxxxx	3.298	3.400	3.502	ST 11I yww
STM11C45xxxxxxx	3.347	3.450	3.554	ST 11J yww
STM11C50xxxxxxx	3.395	3.500	3.605	ST 11K yww
STM11C55xxxxxxx	3.444	3.550	3.657	ST 11L yww
STM11C60xxxxxxx	3.492	3.600	3.708	ST 11M yww

1. Where "y" = assembly year (0 to 9) and "ww" = assembly work week (01 to 52).

Note: Contact local ST sales office for availability of device versions other than STM11C10DF4P28F.

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
30-Aug-2007	1	Initial release.
10-Jan-2008	2	Added: *Applications*, *Section 2: Operation*, *Figure 2*, *Figure 11*, *Table 5*, paragraph *2.3.7*, *Section 3: Typical operating characteristics*. Modified: *Features*, package, paragraph *2.1*, *2.2*, *2.3*, *Figure 1*, *Figure 3*, *Figure 12*, *Figure 13*, *Figure 14*, *Table 1*, *Table 2*, *Table 3*, *Table 4*, *Table 6*, *Table 7*, *Table 8*, *Table 9*, *Table 10*.
04-Nov-2008	2.1	Modified: *Table 2*, *Table 3*, *Section 2.3.2*, *Table 5*, *Table 7*, *Table 8*, *Chapter 6*. Reformatted: *Figure 1* to *Figure 1*, *Figure 11* to *Figure 13*.
08-Jan-2009	3.0	Updated *Applications*, *Figure 2*, *Chapter 2.3.6*, value of V_{IO} and V_{BAT} and *Note 1* in *Table 4*, *Figure 11*, ECOPACK text in *Chapter 6: Package mechanical data*.
17-Feb-2009	4.0	Renamed pins and signals: Test mode power ON input - HP_POWER to PB_{BYP} - Push-button bypass, $I_{BAT\ to}\ I_{IN}$, I_{V_DC} to I_{OUT}, $I_{(V\_DC)\ to}\ I_{OUT}$, Power ON switch - ON_SW to PB - Push-button input, Power ON hold - PS_HOLD to PS_{HOLD} - Power supply hold input, $T_{PD(ON_SW)}$to $T_{PD(PB)}$, $t_{PD(HP\_POWER)}$ to $t_{PD}(PB_{BYP})$, $T_{PR(ON\_SW)\ to}\ T_{PR(PB)}$, $t_{PR(HP\_POWER)}$ to $t_{PR}(PB_{BYP})$, Source of P-channel MOSFET - V_{BAT} to V_{IN} - Voltage input, Drain of P-channel MOSFET - V_DC to V_{OUT} - Voltage output.

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