IC Card Interface ICs

IC Card Interface ICs with Built-in Low Noise LDO Regulator

BD8918F,BD8918FV,BD8919F,BD8919FV

No.09056EDT01

●Overview

This is an interface IC for a 5V smart card.
It works as a bidirectional signal buffer between a smart card and a controller. Also, it supplies 5V power to a smart card.
With an electrostatic breakdown voltage of more than HBM; ±6000V, it protects the card contact pins.

●Features

1) 1 half duplex bidirectional buffers
2) Protection against short-circuit for all the card contact pins
3) 5V power source for the card (VCC)
4) Over-current protection for card power source
5) Built-in thermal shutdown circuit
6) Built-in supply voltage detector
7) Automatic activation/deactivation sequence function for card contact pin
   Activation sequence: driven by a signal from controller (CMDVCCB↓)
   Deactivation sequence: driven by a signal from controller (CMDVCCB↑) and fault detection (card removal, short circuit of card power, IC overheat detection, VDD or VDDP drop)
8) Card contact pin ESD voltage ≧ ±6000V
9) Recommend frequency of crystal oscillator: 8MHz (BD8918F/FV), 16MHz (BD8919F/FV)
10) Programmable for card clock division of output signal: 1/1 and 1/2(BD8918F/FV), 1/2 and 1/4(BD8919F/FV).
11) RST output control by RSTIN input signal (positive output)
12) One multiplexed card status output by OFFB signal

●Applications

Interface for CLASS A smart cards
Interface for B-CAS cards

●Line up matrix

Part No	Card clock Ratio of dividing frequency	Package
BD8918F	1/1f, 1/2f	SOP16
BD8918FV		SSOP-B16
BD8919F	1/2f, 1/4f	SOP16
BD8919FV		SSOP-B16

●**Absolute maximum ratings (Ta=25°C)**

Parameter	Symbol	Ratings	Unit	Notes
VDD Input Voltage	V_{DD}	-0.3 ~ 6.5	V	
VDDP Input Voltage	V_{DDP}	-0.3 ~ 6.5	V	
I/O Pin Voltage	V_{MIN} V_{MOUT}	-0.3 ~ +6.5	V	Pin: XTAL1, XTAL2, CLKSEL, RSTIN, IO_U CMDVCCB, OFFB
Card Contact Pin Voltage	V_{CD}	-0.3 ~ +6.5	V	Pin: PRES, CLK, RST, IO_C
Junction Temperature	T_{jmax}	+150	°C	
Storage Temperature	T_{stg}	-55 ~ +150	°C	
Power Dissipation	P_{tot}	0.375 *1 0.500 *2	W	T = -20 ~ +85°C (Refer to the following package power dissipation)

*1 BD8918F/BD8919F, *2 BD8918FV/BD8919FV
• This product is not designed to be radiation tolerant.
• Absolute maximum ratings are not meant for guarantee of operation.

●**Operating Conditions (Ta=25°C)**

Parameter	Symbol	Ratings			Unit	Notes
		MIN	TYP	MAX		
VDD Input Voltage	V_{DD}	2.7	-	5.5	V	
VDDP Input Voltage	V_{DDP}	4.75	-	5.5	V	VCC ≥ 4.55V
Operating Temperature	T_{opr}	-40	-	+85	°C	

●**Package Power Dissipation**

The power dissipation of a simple package in case of a boadless will be as follows.
Use of this device beyond the following the power dissipation may cause permanent damage.

BD8918F/BD8919F Pd=375mW; however, reduce 3mW per 1°C when used at Ta ≥ 25°C.
BD8918FV/BD8919FV Pd=500mW; however, reduce 4mW per 1°C when used at Ta ≥ 25°C.

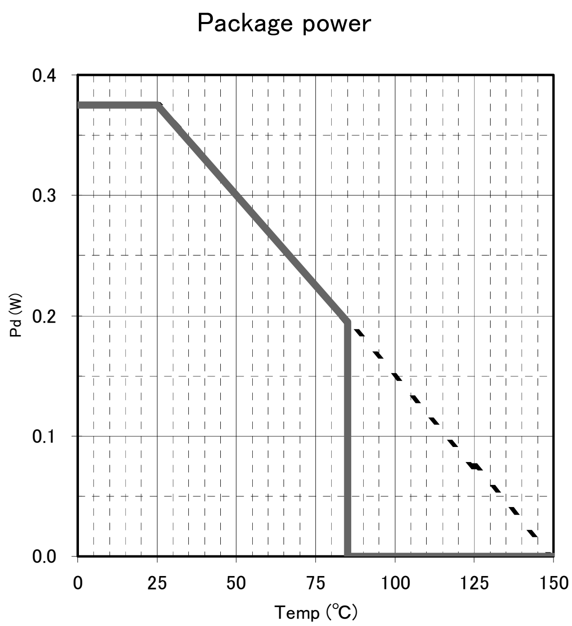


Fig. 1.1 BD8918F/BD8919F Power Dissipation

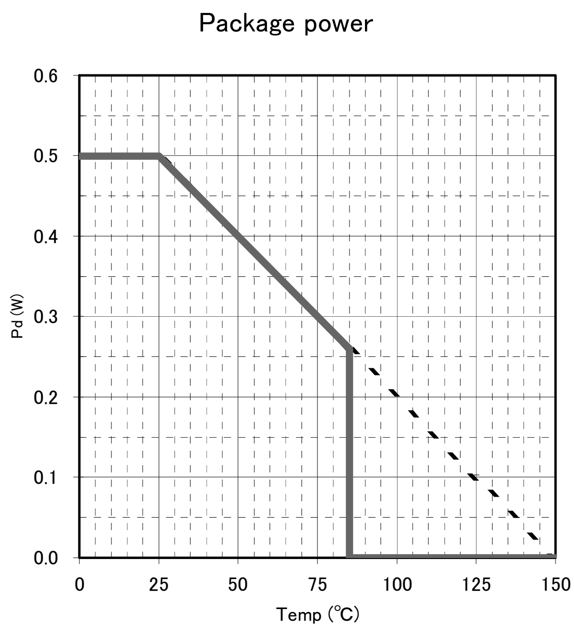


Fig. 1.2 BD8918FV/BD8919FV Power Dissipation

●**Block Diagram**

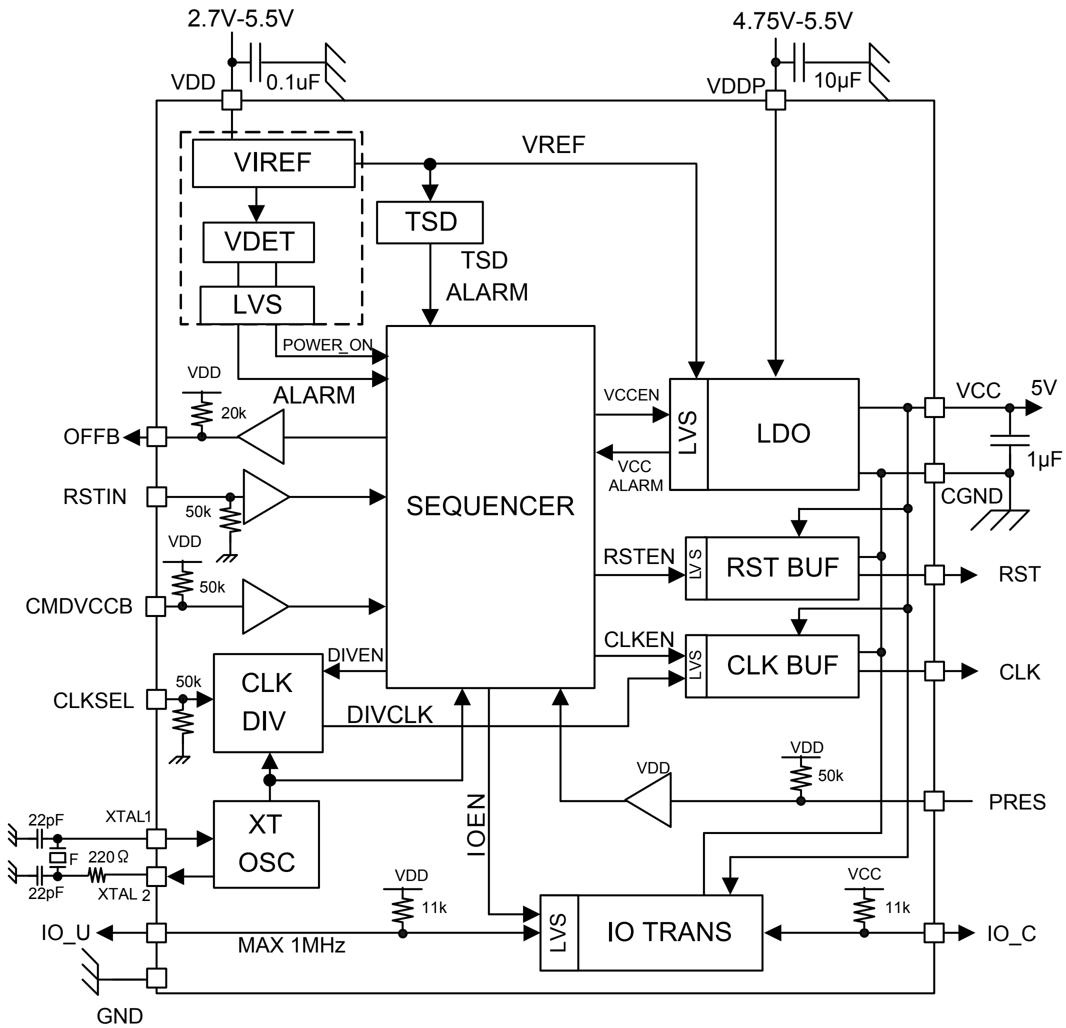


Fig. 2

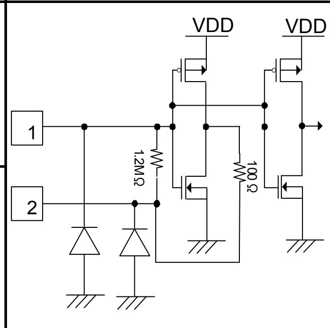
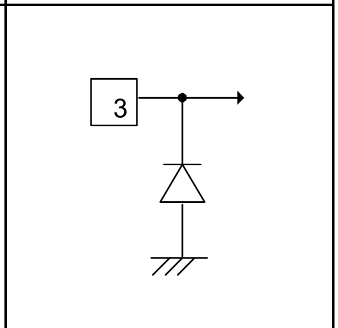
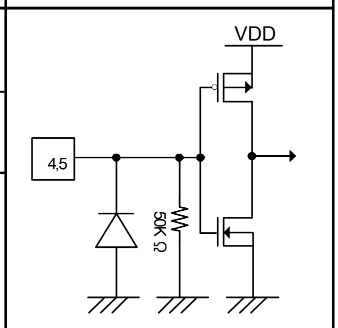
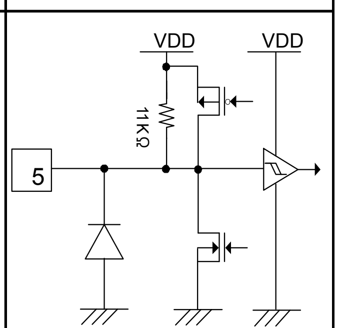
BD8918F/FV F=8MHz
BD8919F/FV F=16MHz

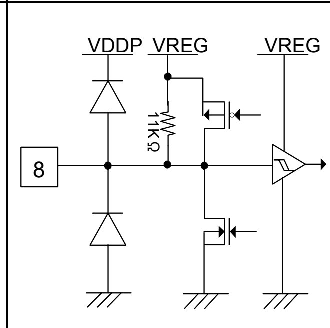
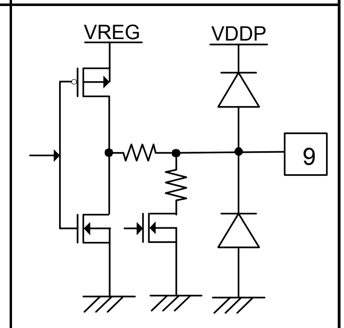
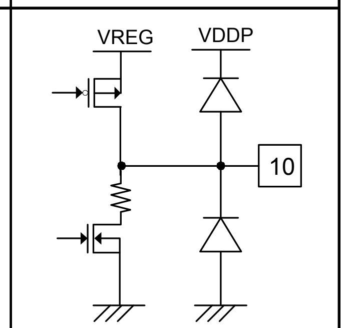
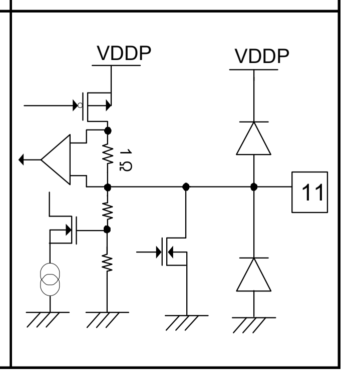
●**Pin Description**

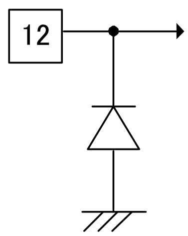
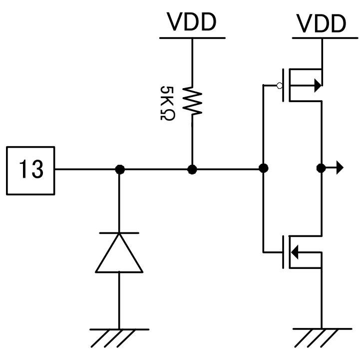
Pin No.	Pin Name	I/O	Signal Level	Pin Function	
1	XTAL1	I	VDD	Crystal connection or input for external clock	
2	XTAL2	O	VDD	Crystal connection (leave open pin when external clock source is used)	
3	VDD	S	VDD	3.3 V power source pin for host interface. Connect 0.1µF capacitor between the VDD and GND pins.	
4	CLKSEL	I	VDD	Input for clock frequency division setting. Pulled down to GND with a 50kΩ resistor.	BD8918F/FV H: 1/1 division; L: 1/2 division. BD8919F/FV H: 1/2 division; L: 1/4 division.
5	RSTIN	I	VDD	Card reset signal input. Pulled down to GND with a 50kΩ resistor.	
6	IO_U	I/O	VDD	Host data I/O line; Pulled up to VDD with an 11kΩ resistor	
7	CGND	S	GND	GND	
8	IO_C	I/O	VCC	I/O data line on the card side. Pulled up to VCC with an 11kΩresistor.	
9	RST	O	VCC	Card reset output	
10	CLK	O	VCC	Card clock output	
11	VCC	O	VCC	Card supply voltage. Connect 1µF capacitor between VCC and the CGND pins.	
12	VDDP	S	VDDP	5V power source pin for card power feed. Connect 10µF capacitor between the VDDP and CGND pins.	
13	PRES	I	VDD	Card presence contact input (“H” active). Pulled up to VDD with a 50kΩ resistor. Connected to a switch where GND level is inputted when no card is inserted and OPEN is inputted when a card is inserted. When “H” level is detected, a card is assumed to be inserted and waits for the CMDVCCB input for the confirmation, after the debounce time of typ. 8ms.	
14	OFFB	O	VDD	Alarm output pin (“L” active). NMOS open drain output. Pulled up to VDD with a 20kΩ resistor.	
15	CMDVCCB	I	VDD	Activation sequence command input; The activation sequence starts by signal input (H→L) from the host	
16	GND	S	GND	GND	

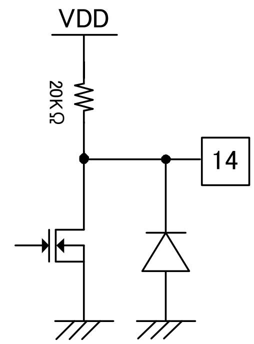
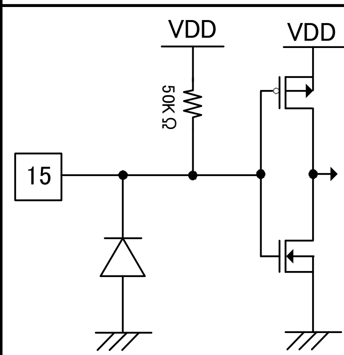
*Capacitors to be connected to VDD, VDDP and VCC should be placed immediately next to the pins (ESR<100mΩ).

●Pin Function Diagram

Pin No.	Pin Name	Pin function Diagram
1	XTAL1	
2	XTAL2	
3	VDD	
4	CLKSEL	
5	RSTIN	
6	IO_U	
7	CGND	------------------------

Pin No.	Pin Name	Pin function Diagram
8	IO_C	
9	RST	
10	CLK	
11	VCC	

Pin No.	Pin Name	Pin function Diagram
12	VDDP	
13	PRES	

Pin No.	Pin Name	Pin function Diagram
14	OFFB	
15	CMDVCCB	
16	GND	------------------------

●**Package**

Package Name: SOP16 Note : X is 8 or 9.

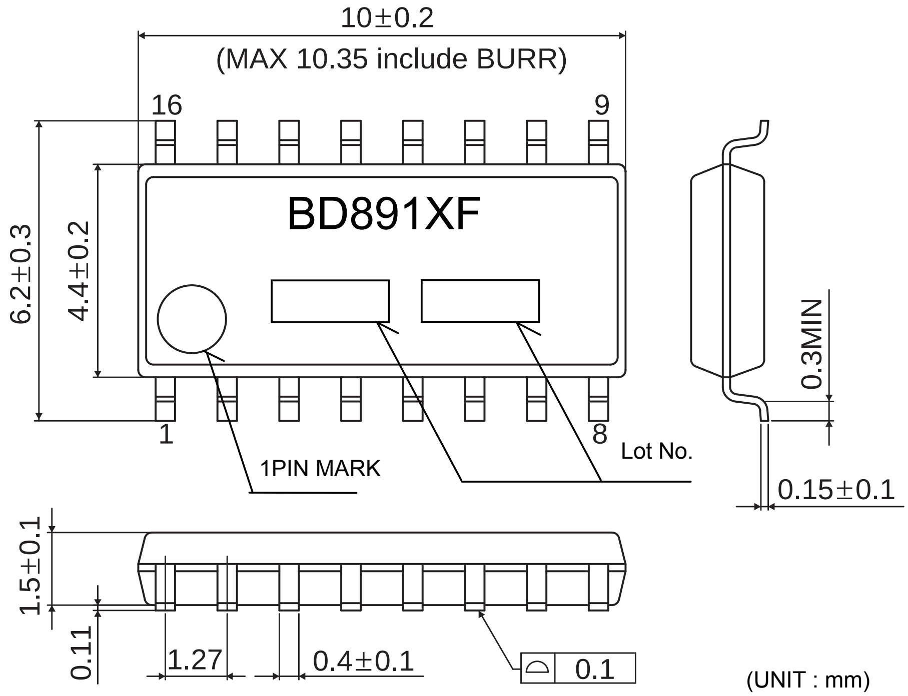


Fig. 3.1 SOP16 Package Dimension

Package Name: SSOP-B16

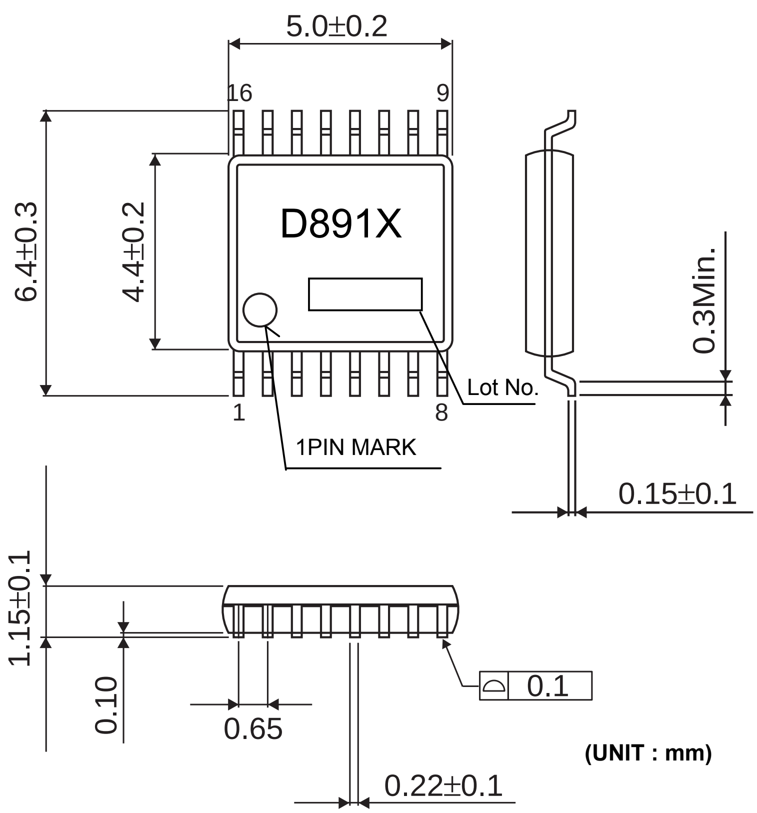


Fig. 3.2 SSOP-B16 Package Dimension

●Function

1) Power supply

Power supply pins are VDD and VDDP. Set VDD at the same voltage as the signal from the system controller side. VDDP and CGND are for the 5V power source and GND, respectively, on the card side.

2) Input voltage detector

The IC remains in wait mode until the power on reset is released 16ms after the VDD supply voltage is increased over Vthd and the VDDP supply voltage is increased over Vthp, making the CMDVCCB signal turn from H to L.

Vthd=1.7V(typ) Vthp=2.25V(typ)

3) Operation sequence

3-1) Wait mode

The IC remains in wait mode until the power on reset is released after the VDD supply voltage is increased over Vthd and the VDDP supply voltage is increased over Vthp, making the CMDVCCB signal turn from H to L.
In this mode, the VDD and VDDP supply voltage detector (VDET), thermal shutdown circuit (TSD), reference circuit (VREF) and crystal oscillation circuit (XT OSC) are activated.
IO_U is pulled up to VDD with an 11kΩ resistor and all the card contact pins are at Lo level.

3-2) Card presence

Card presence is detected by PRES pin. When the PRES pin is active, a card is assumed to be present.

Table 1

PRES	“High” active

When a card is present in wait mode, the card insertion identification pin, PRES (“H” active) becomes active and OFFB becomes “H” after approx. 8ms (debounce time).
If a card is present before the VDD and VDDP power sources are applied and the internal reset is released, it is internally reset and OFFB becomes “H” after the debounce time.
The PRES pin is pulled up to VDD with a 50kΩ resistor.

Descriptions of transition times (example. Debounce time: 8msec) for the operation sequences are adapted in the conditions of the following input frequency.

8MHz (BD8918F/ FV), 16MHz (BD8919F/ FV)

3-3) Activation sequence

When OFFB is in the “High” state and the CMDVCCB signal from the controller turns from H to L, the activation sequence starts to activate each functional block in the following order:
The RST outputs signals based on the RSTIN input, being reset approximately 472∝sec after the CMDVCCB signal turns from H to L. The RSTIN input becomes effective approximately 48∝s after I/O TRANS turns ON. If RSTIN becomes Lo after RSTIN becomes effective and the RST output is released, the CLK signal is output. If RSTIN is High when the RST output is released, the CLK signal is output as soon as the RST output is released. (Refer to Fig. 4-1, 4-2 and 4-3)

LDO ON (VCC output)
↓
I/O TRANS ON (IO_C, IO_U Bus: Pull-up)
↓
↓ ↓ When RSTIN remains High until RST is released
↓ (RSTIN≠Always High) ↓ (RSTIN=Always High)
↓ ↓
CLK BUF ON (CLK output) CLK, RST BUF ON (CLK output, RST release)
↓
RST BUF ON (RST release)

[Activation sequence under different RSTIN input timings]

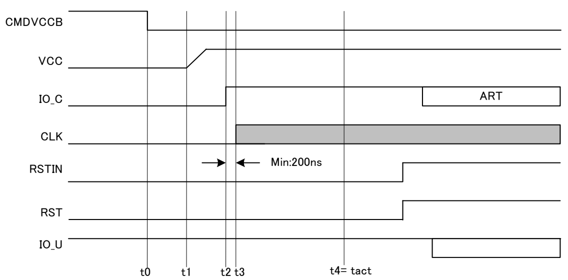


Fig. 4-1 Activation sequence 1

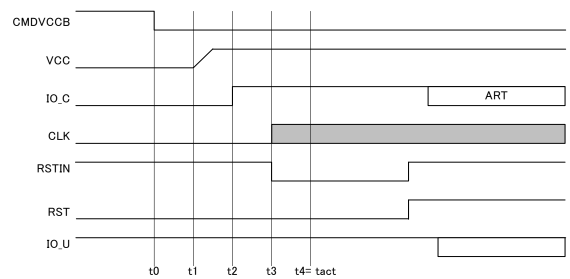


Fig. 4-2 Activation sequence 2

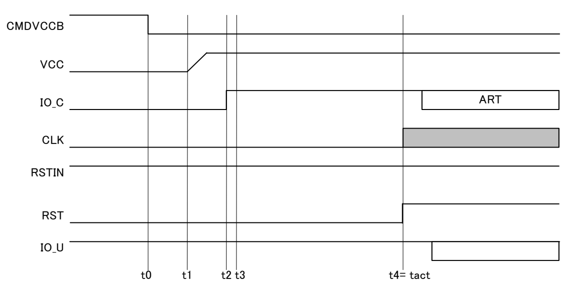


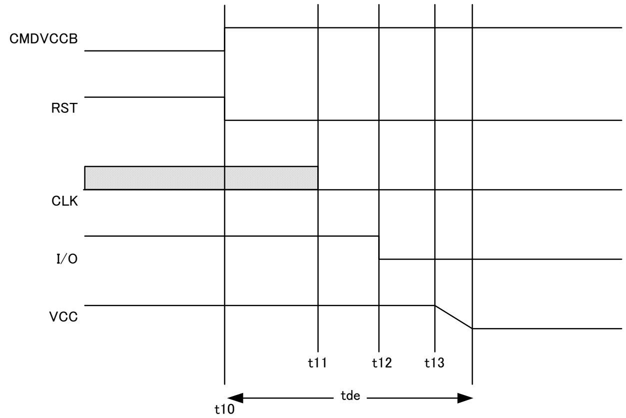
Fig. 4-3 Activation sequence 3
(RSTIN input sequence not specified by ISO7816)

t1: LDO startup time = typ. 24μs
t2: I/O ON time = typ. 424μs
t3: CLK output release time (t3-t2) = Min. 200ns
t4: RST release time = typ,472μs, max. 481µs
(Activation time)

3-4) Deactivation sequence

When the CMDVCCB input turns from L to H or the alarm signal (described later) is detected, the following deactivation sequence is initiated in the following order, transitioning to the wait mode.

RST BUF OFF (RST: Lo)
↓
CLK BUF OFF (CLK: Lo)
↓
I/O TRANS OFF (I/O Bus on the controller side: Pull-up)
↓ (I/O Bus on the card side: Lo)
↓
LDO OFF (VCC: Lo)



t11: CLK OFF time = typ. 10μs
t12: I/O OFF time = typ. 20μs
t13: Starting time of VCC fall = typ. 30μs
tde: Operational sequence completion time =Max. 200μs

Fig. 5 Deactivation sequence

4) LDO

LDO supplies power to the IC card through VCC pin.
This regulator has a built-in over-current limiter circuit. It generates an internal alarm with a load current of approximately 140mA or more and enters into the deactivation sequence. Also, the output voltage is regarded as abnormal if it drops to less than 1.6V and the output current is shut off; an internal alarm signal is generated and the deactivation sequence is initiated.
Connect a capacitor of 1μF or 2.2μF between VCC and CGND as close as possible to the VCC pin, in order to reduce the output voltage variation as much as possible. Also, ensure that ESR is kept at less than 100mΩ.
LDO output is also a power source for CLK, RST and IO_C output. Therefore, the CLK, RST and IO_C output level is the same as the VCC output level.

5) I/O data transitions

The data line, IO_C - IO_U, transmits/receives two-way data.
The IO_U pin for the controller side is pulled up with an 11kΩ resistor to High (VDD voltage) and card contact pins IO_C is set to Lo until I/O TRANS becomes ON by the activation sequence.
When I/O TRANS becomes On, IC becomes idle mode and the I/O pin is pulled up with an 11kΩ resistor to keep the IO_U pin to VDD voltage (High) and the IO_C pin to VCC voltage (High).

The pin which turns to L from H first becomes the master and the other output side becomes the slave between the pins on the controller side and card contact pins. Then the data are transferred from the master side to the slave side.
When the both signal levels become High, they become idle mode.
When the signal transits from L to H and it passes over a threshold, an active pull-up (100 ns or less) works to drive the data High at high speed. After the active pull-up is completed, the pin is pulled up with an 11kΩ resistor. After the active pull-up is completed, the pin is pulled up with an 11kΩ resistor. This function enables signal transmission up to 1MHz. Also, an over-current limiter of 30mA in the card contact pin, IO_C.

6) Card clock supply

Card clock is supplied from the CLK pin dividing the input frequency of XTAL1 pin with the CLKSEL pin setting. The clock division switching time is within the 8 clocks of the XTAL1 signal.
The input signal to the XTAL1 pin is made by a crystal oscillator (BD8918F/FV:8Hz, BD8919F/FV:16MHz) between the XTAL1 pin and XTAL2 pin or external pulse signal.
When a crystal oscillator is used, the voltage between XTAL1 and XTAL2 may decrease to become close to “-1V”, which is not a problem.
When an external pulse signal is applied to the XTAL1 pin (except for signal input by crystal oscillation), the duty of the XTAL1 pin should be 48% - 52% and the transition time of the XTAL1 pin should be within 5% of the signal cycle to ensure the duty factor of 45% - 55% at the CLK pin.

Table 2 Clock frequency selection (f_{XTAL}: Frequency at XTAL1)

	CLKSEL	f_{clk}
BD8918F/FV	1	f_{XTAL}
	0	$\frac{f_{XTAL}}{2}$

	CLKSEL	f_{clk}
BD8919F/FV	1	$\frac{f_{XTAL}}{2}$
	0	$\frac{f_{XTAL}}{4}$

7) RSTIN input, RST output

The RSTIN input becomes effective after the CMDVCCB signal input turns to L from H, activation sequence is initiated and approximately 48∝s after I/O TRANS turns ON. The RST output is released in approximately 472∝sec (max. 481∝sec) after the CMDVCCB signal turns from H to L to output a signal based on the RSTIN input.

8) Fault detection

When the following fault state is detected, the circuit enters the wait mode after it generates an internal alarm signal and is deactivated.
If a card is not present, it remains in the wait mode.

- When the VCC pin becomes less than 1.6V, or is loaded high current (TYP: 140mA)
- When VDDP voltage is less than the threshold voltage (detected by supply voltage detector)
- When a high temperature is detected by the thermal shutdown circuit
- When the card is removed during operation or the card is not present from the beginning (PRES=L)

9) OFFB output

The OFFB output pin indicates the IC is ready to operate. It is pulled up to VDD with a 20kΩ resistor.
When the IC is in the ready state, OFFB is High.
After activation, the OFFB outputs OFF state (Lo) when a fault state is detected.
When a card is present and CMDVCCB becomes High, the internal alarm is released and the OFFB output becomes High.

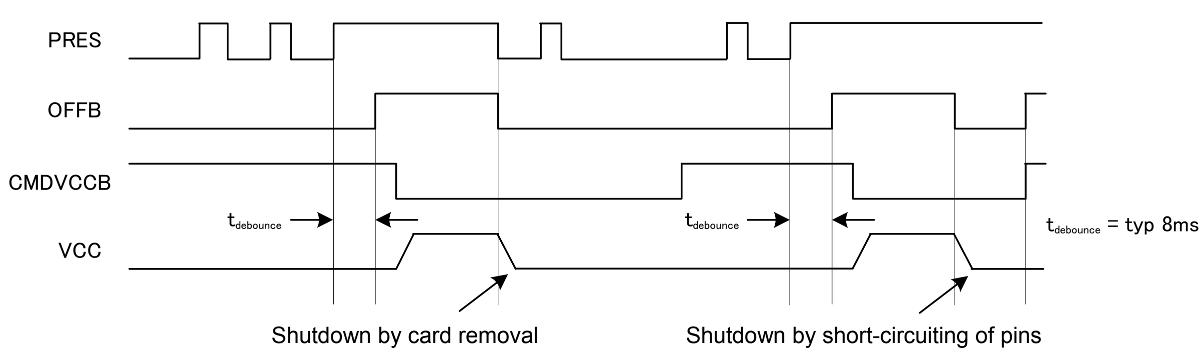


Fig. 6 OFFB, CMDVCCB, PRES, VCC operation

●An example of software control

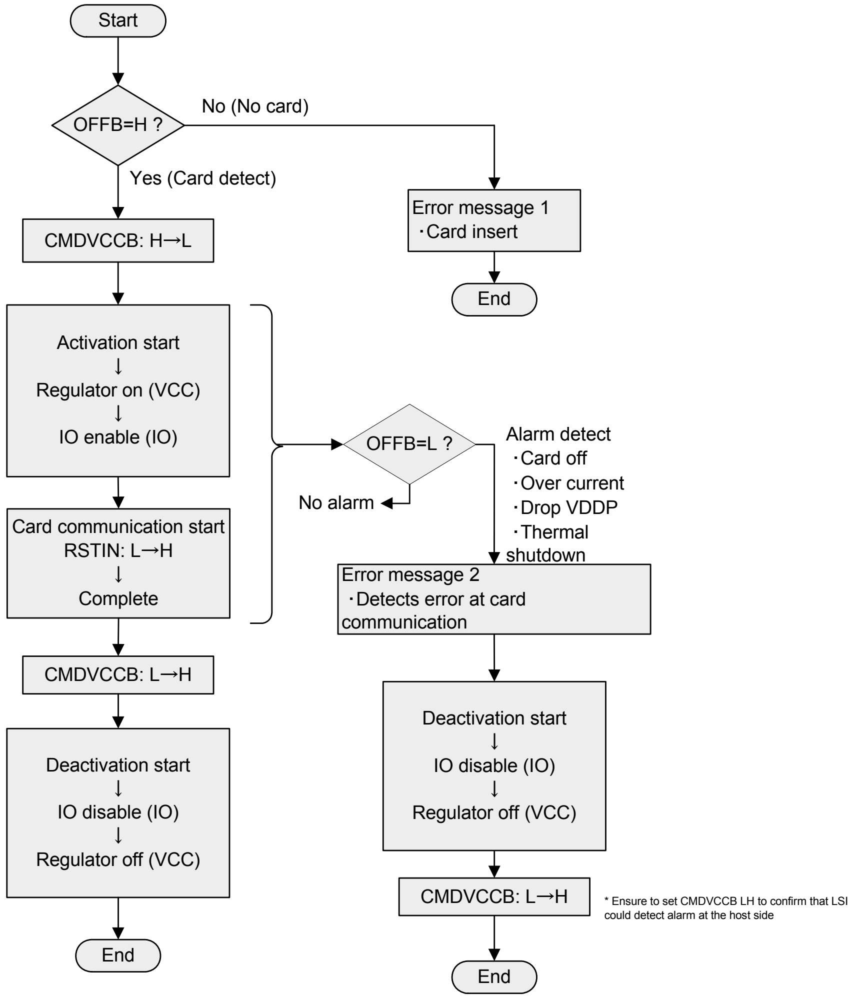


Fig. 7 An example of software control

●Application examples

BD8918F/FV application examples

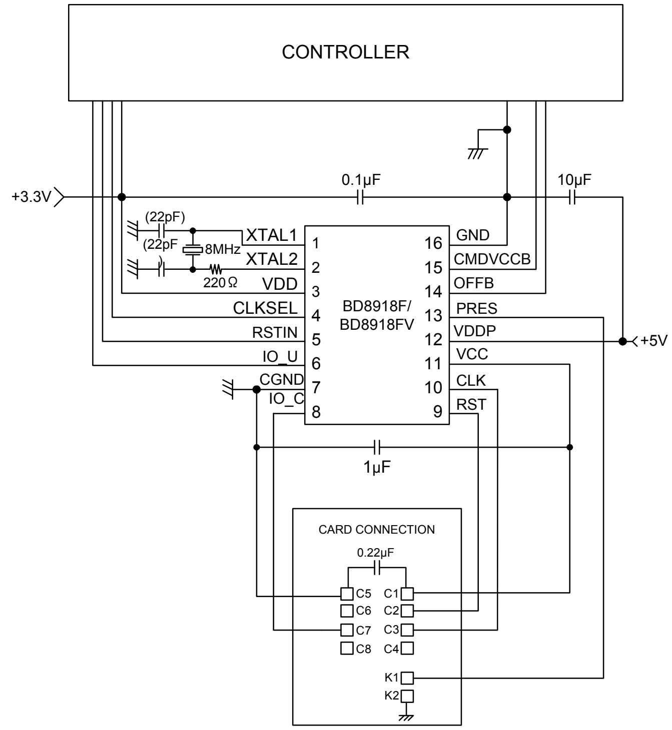


Fig.8

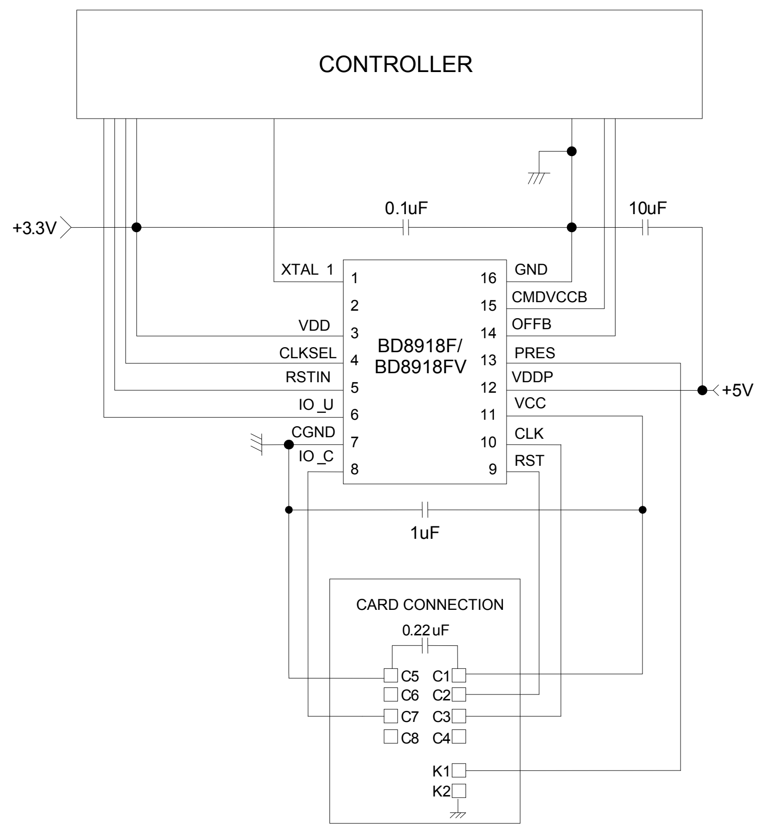
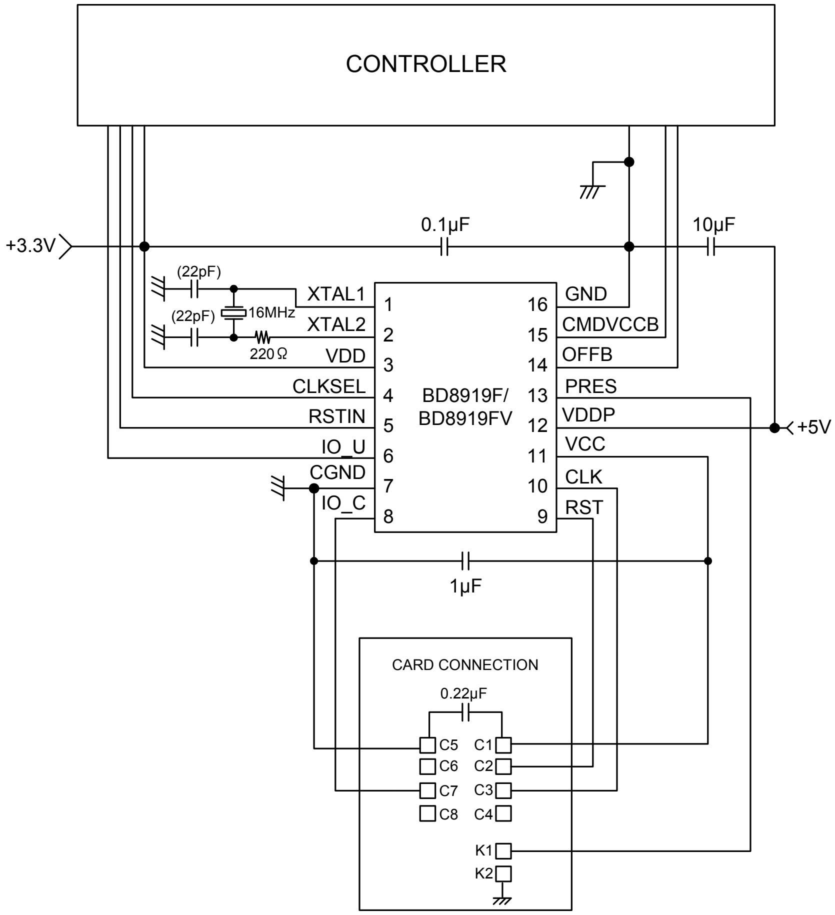


Fig.9

BD8919F/FV application examples



●Precautions for use

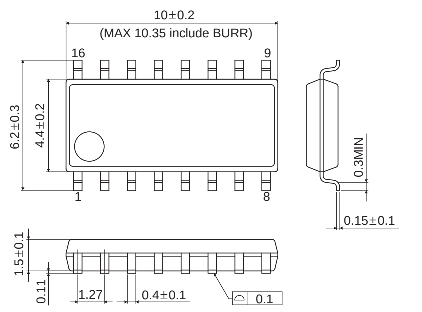
1) The capacitor for the VCC pin should be placed as close as possible to the IC between VCC and CGND so that the ESR becomes less than 100Ω
2) Connect a capacitor of over 0.1μF for VDD and over 10μF for VDDP as close as possible to the IC so that the ESR becomes less than 100mΩ to reduce the power line noise. We recommend the use of capacitors with the largest possible capacitance.

● **Ordering part number**

B	D		8	9	1	8		F	V	-	E	2

- Part No.
- Part No.: 8918, 8919
- Package: F: SOP16, FV: SSOP-B16
- Packaging and forming specification: E2: Embossed tape and reel

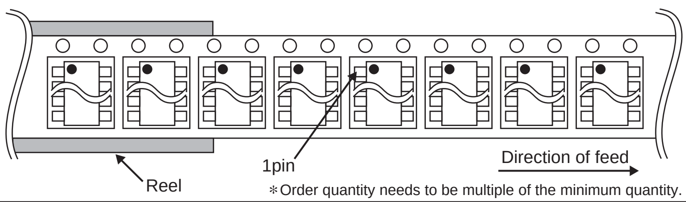
SOP16



(Unit : mm)

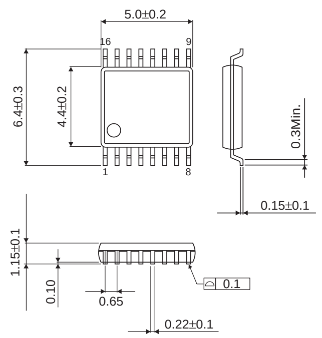
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

SSOP-B16



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<Tape and Reel information>

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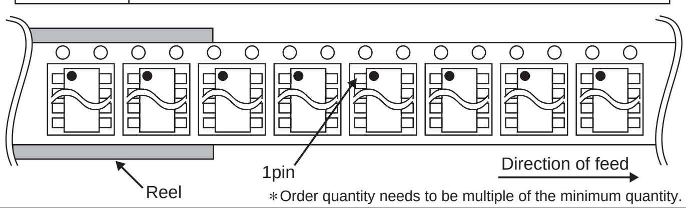

*Order quantity needs to be multiple of the minimum quantity.

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