

*4M x 1Bit CMOS Dynamic RAM with Fast Page Mode*

**DESCRIPTION**

This is a family of 4,194,304 x 1bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5V or +3.3V), access time (-5, -6 or -7), power consumption(Normal or Low power), and package type (SOJ or TSOP-II) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in Low power version.

This 4Mx1 Fast Page Mode DRAM family is fabricated using Samsung’s advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames and mini computers, personal computer and high performance microprocessor systems.

**FEATURES**

• **Part Identification**

- KM41C4000D/D-L(5V, 1K Ref.)
- KM41V4000D/D-L(3.3V, 1K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (3.3V, L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Common I/O using early write
- JEDEC Standard pinout
- Available in 26(20)-pin SOJ 300mil and TSOP(II) 300mil packages
- +5V±10% power supply(5V product)
- +3.3V±0.3V power supply(3.3V product)

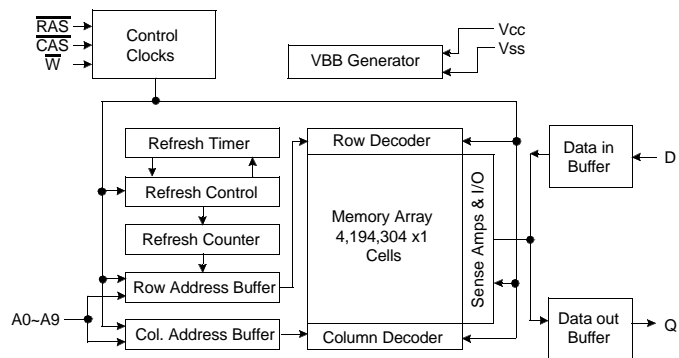
• **Refresh Cycles**

Part NO.	Refresh cycle	Refresh Period	
		Normal	L-ver
KM41C4000D	1K	16ms	128ms
KM41V4000D			

• **Performance Range**

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>	Remark
-5	50ns	15ns	90ns	35ns	5V only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V

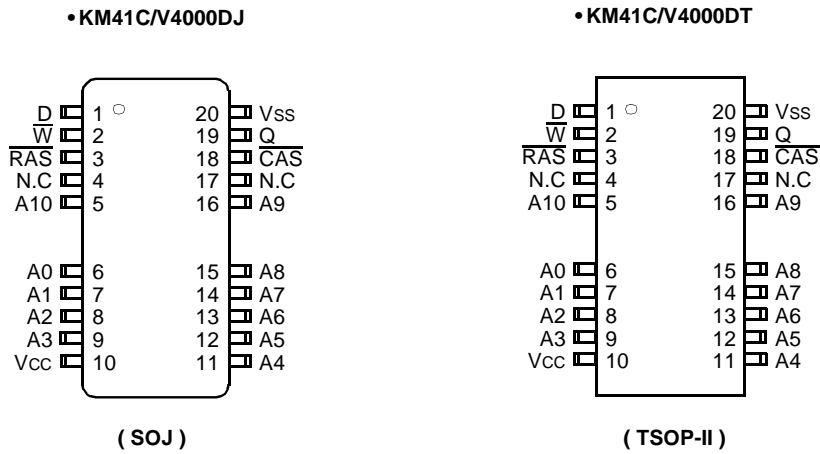
**FUNCTIONAL BLOCK DIAGRAM**



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PIN CONFIGURATION (Top Views)



Pin Name	Pin function
A0 - A10	Address Inputs
D	Data In
Q	Data out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
N.C	No Connection
Vcc	Power(+5V)
	Power(+3.3V)

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to +4.6	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	600	600	mW
Short Circuit Output Current	I <sub>OS</sub>	50	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, T<sub>A</sub>= 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3 <sup>*1</sup>	2.4	-	V <sub>CC</sub> +1.0 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-0.3 <sup>*2</sup>	-	0.8	-0.1 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub> +1.3V/15ns(3.3V), V<sub>CC</sub> +2.0V/20ns(5V), Pulse width is measured at V<sub>CC</sub>

\*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V<sub>SS</sub>

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V <sub>IN</sub> ≤V <sub>CC</sub> +0.3V, all other input pins not under test=0 Volt)	I <sub>I(L)</sub>	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V <sub>OUT</sub> ≤V <sub>CC</sub> )	I <sub>O(L)</sub>	-5	5	uA
	Output High Voltage Level(I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.4	-	V
	Output Low Voltage Level(I <sub>OL</sub> =2mA)	V <sub>OL</sub>	-	0.4	V
5V	Input Leakage Current (Any input 0≤V <sub>IN</sub> ≤V <sub>CC</sub> +0.5V, all other input pins not under test=0 Volt)	I <sub>I(L)</sub>	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V <sub>OUT</sub> ≤V <sub>CC</sub> )	I <sub>O(L)</sub>	-5	5	uA
	Output High Voltage Level(I <sub>OH</sub> =-5mA)	V <sub>OH</sub>	2.4	-	V
	Output Low Voltage Level(I <sub>OL</sub> =4.2mA)	V <sub>OL</sub>	-	0.4	V

## DC AND OPERATING CHARACTERISTICS (Recommend operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM41V4000D	KM41C4000D	
Icc1	Don't Care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
Icc2	Don't Care	Don't Care	1	2	mA
Icc3	Don't Care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
Icc4	Don't Care	-5	-	65	mA
		-6	45	55	mA
		-7	40	45	mA
Icc5	Normal L	Don't Care	0.5	1	mA
			100	200	uA
Icc6	Don't Care	-5	-	85	mA
		-6	60	75	mA
		-7	55	65	mA
Icc7	L	Don't Care	200	300	uA
Iccs	L	Don't Care	150	-	uA

Icc1\* : Operating Current ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min.)

Icc2 : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

Icc3\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$ , Address cycling @trc=min.)

Icc4\* : Fast Page Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$ , Address cycling @tpc=min.)

Icc5 : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$ )

Icc6\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage( $V_{IH}$ )= $V_{CC}-0.2V$ , Input low voltage( $V_{IL}$ )= $0.2V$ ,  $\overline{CAS}=0.2V$ ,

DQ=Don't Care,  $T_{RC}=125\mu s$ (L-ver.),  $T_{RAS}=T_{RASmin}\sim 300ns$

Iccs : Self refresh current

$\overline{RAS}=\overline{CAS}=V_{IL}$ ,  $\overline{W}=\overline{OE}=A0 \sim A10=D=V_{CC}-0.2V$  or  $0.2V$

**\*Note :** Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3 Icc6 and Icc7, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In Icc4, address can be changed maximum once within one fast page mode cycle time, tpc.

# KM41C4000D, KM41V4000D

# CMOS DRAM

## CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [D]	CIN1	-	5	pF
Input capacitance [A0 ~ A10]	CIN2	-	5	pF
Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{W}}$ ]	CIN3	-	7	pF
Output capacitance [Q]	COU1	-	7	pF

## AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V

Test condition (3.3V device) : VCC=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-5*1		-6		7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	110		130		150		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		15		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	12	0	12	0	17	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	15		15		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		70		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	15	10K	15	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	35	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		15		ns	

Note) \*1 : 5V only



**AC CHARACTERISTICS** (0°C ≤ T<sub>A</sub> ≤ 70°C, See note 2)

Parameter	Symbol	-5*1		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	15		15		20		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	50		60		70		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	25		30		35		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	30		35		40		ns	7
$\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page read-modify-write cycle time	tPRWC	53		60		70		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	tWRP	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	tWRH	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRASS	100		100		100		us	14,15,16
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRPS	90		110		130		ns	14,15,16
$\overline{\text{CAS}}$ Hold time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	14,15,16

Note) \*1 : 5V only

**TEST MODE CYCLE**

( Note 11 )

Parameter	Symbol	-5*1		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	95		115		135		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	113		135		160		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		55		65		75	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		18		20		25	ns	3,4,5
Access time from column address	t <sub>AA</sub>		30		35		40	ns	3,10
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	55	10K	65	10K	75	10K	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	18	10K	20	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	18		20		25		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	55		65		75		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	30		35		40		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	18		20		25		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	55		65		75		ns	7
Column Address to $\overline{\text{W}}$ delay time	t <sub>AWD</sub>	30		35		40		ns	7
Fast Page mode cycle time	t <sub>PC</sub>	40		45		50		ns	
Fast Page mode read-modify-write cycle	t <sub>PRWC</sub>	58		65		75		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t <sub>RASP</sub>	55	200K	65	200K	75	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>		35		40		45	ns	3

Note) \*1 : 5V only



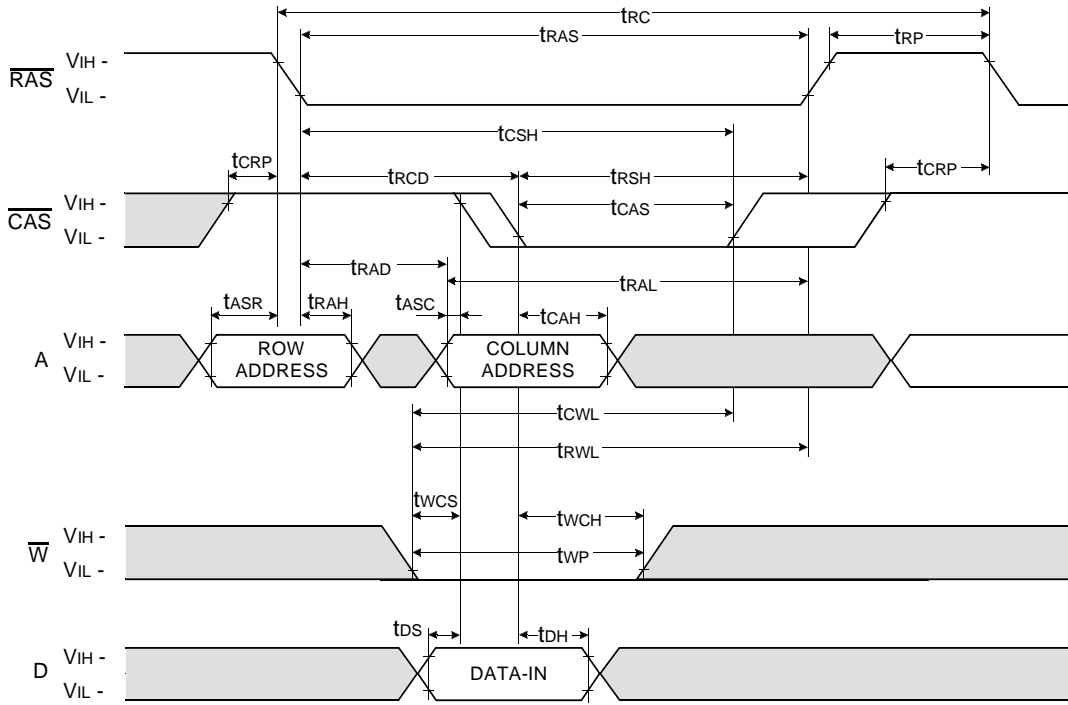
## NOTES

1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{oh}$  or  $V_{ol}$ .
7.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPWD}}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$  then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
9. These parameters are referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{W}}$  falling edge in read-modify-write cycles.
10. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13.  $t_{\text{OFF}}(\text{MAX})$  defines the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. If  $t_{\text{RAS}} \geq 100\text{us}$ , then  $\overline{\text{RAS}}$  precharge time must use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .
15. For  $\overline{\text{RAS}}$ -only refresh and burst  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh mode, 1024(1K) cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. For distributed  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  with 15.6us interval,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.



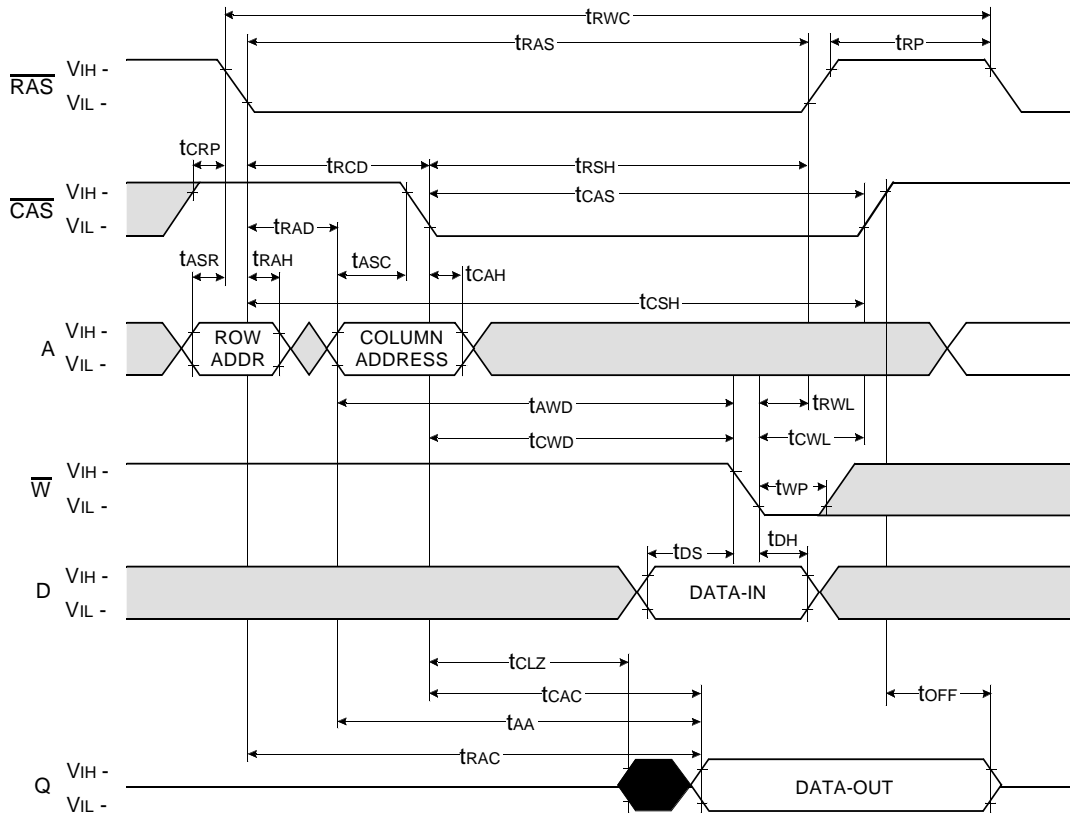


WRITE CYCLE ( EARLY WRITE )



Don't care  
 Undefined

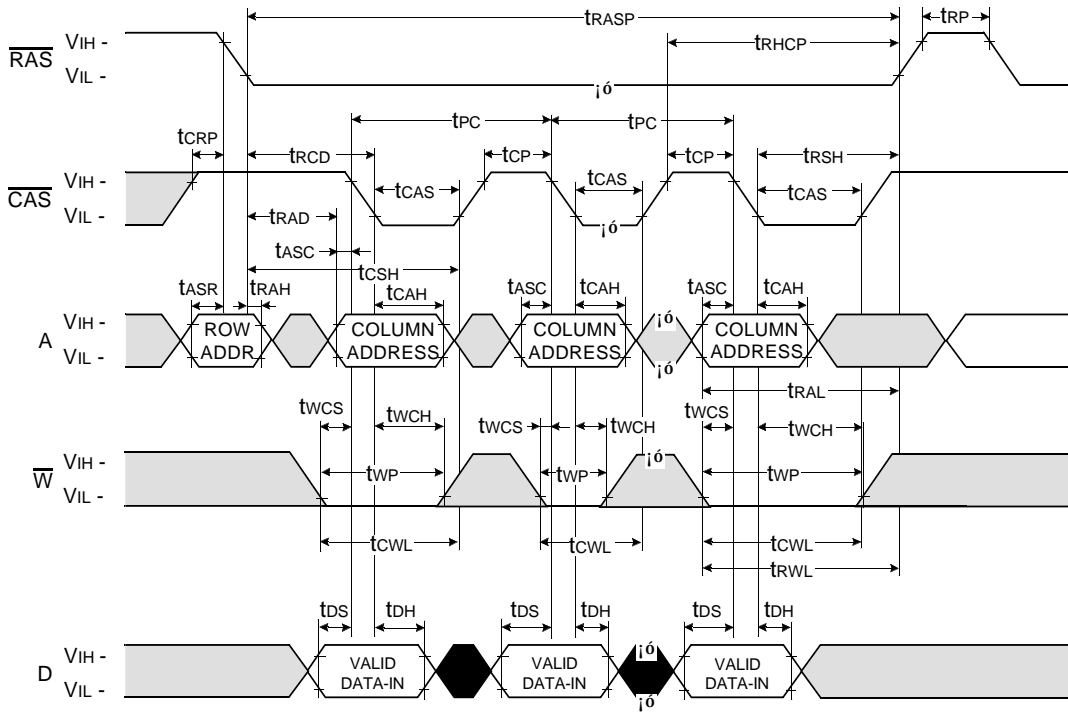
READ-WRITE / READ - MODIFY - WRITE CYCLE



Don't care  
 Undefined



FAST PAGE WRITE CYCLE ( EARLY WRITE )

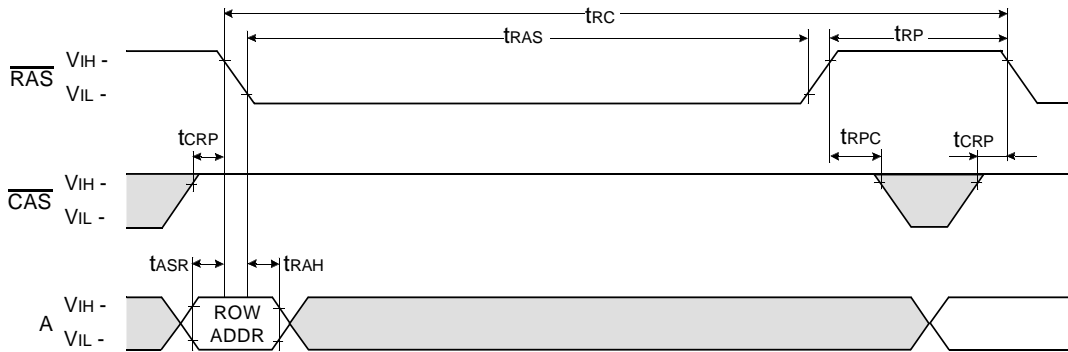




**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE**

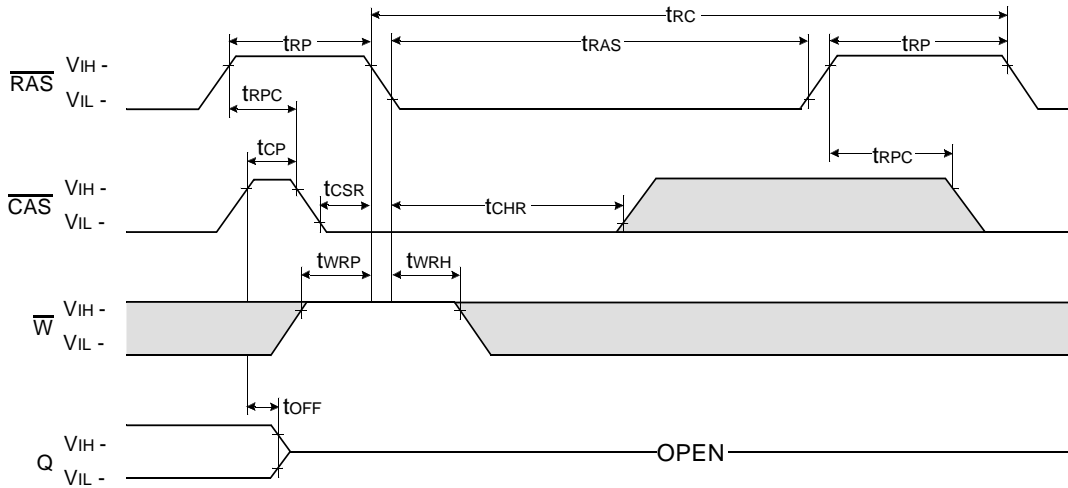
NOTE :  $\overline{\text{W}}$ ,  $\text{DIN}$  = Don't care

$\text{DOUT}$  = OPEN



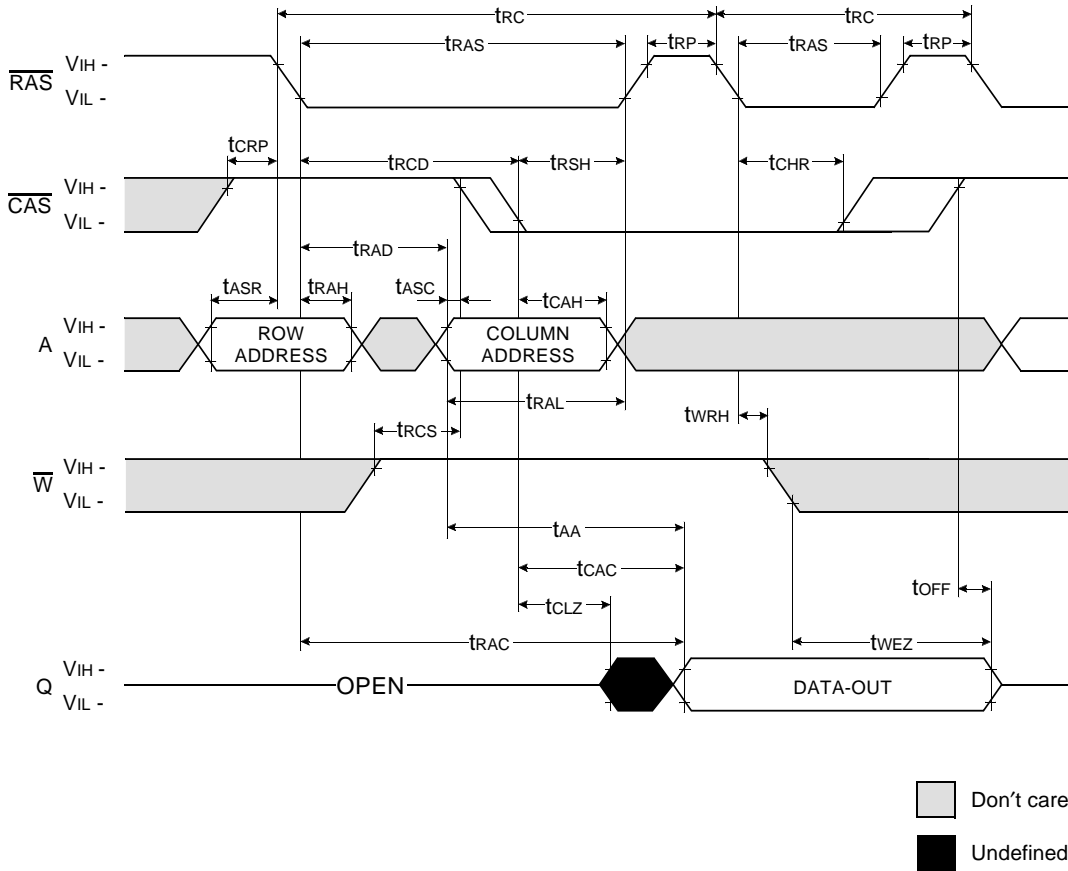
**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

NOTE :  $\text{A}$  = Don't care



Don't care  
 Undefined

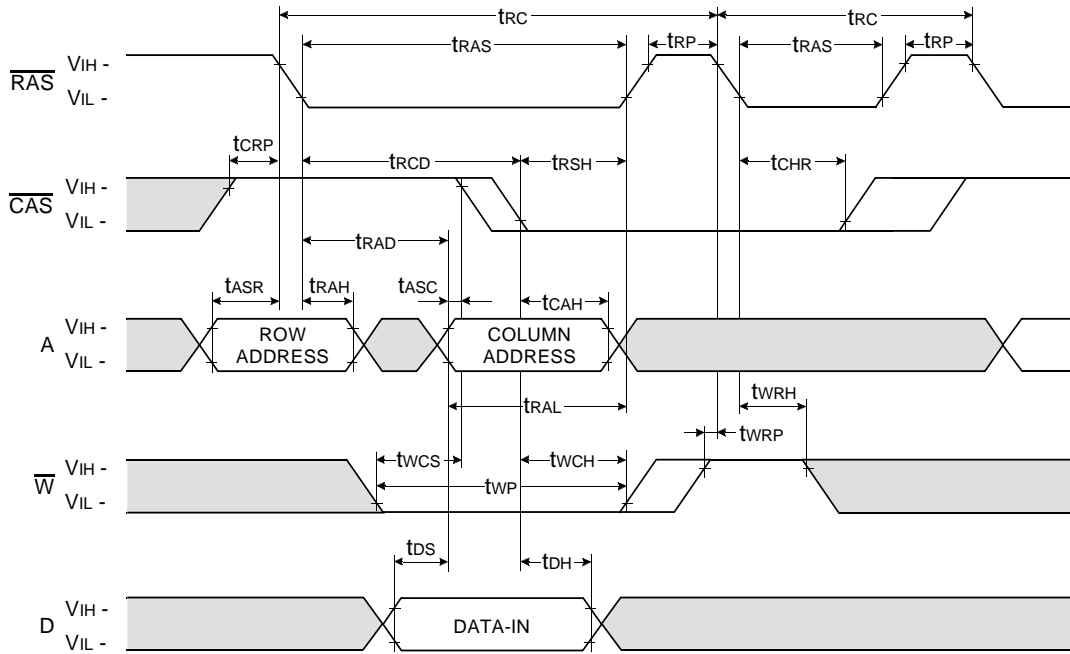
HIDDEN REFRESH CYCLE ( READ )





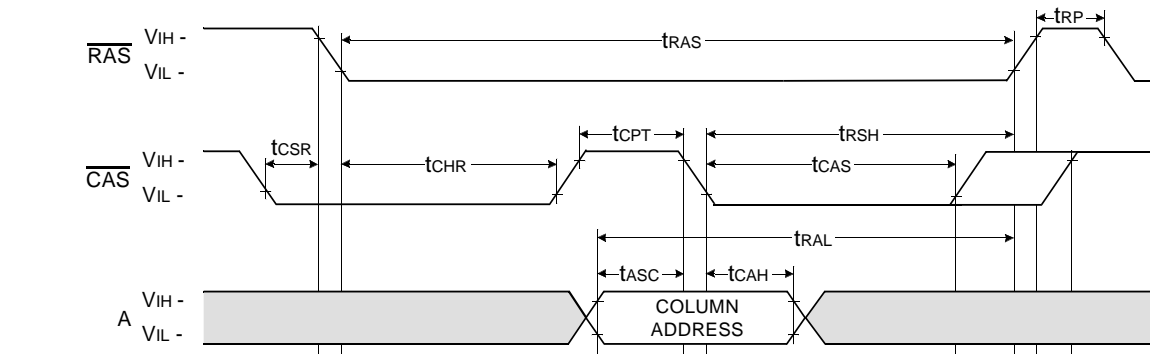
**HIDDEN REFRESH CYCLE ( WRITE )**

NOTE : DOUT = OPEN

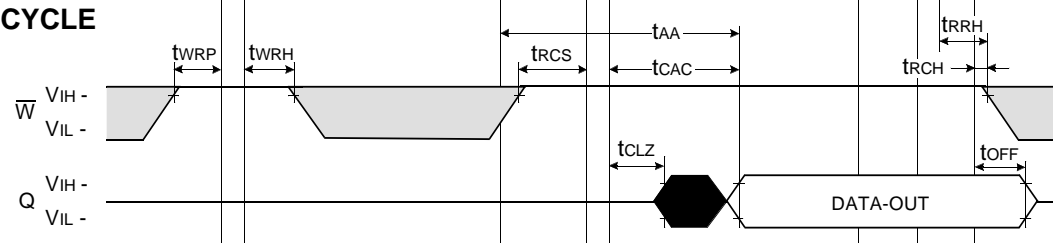


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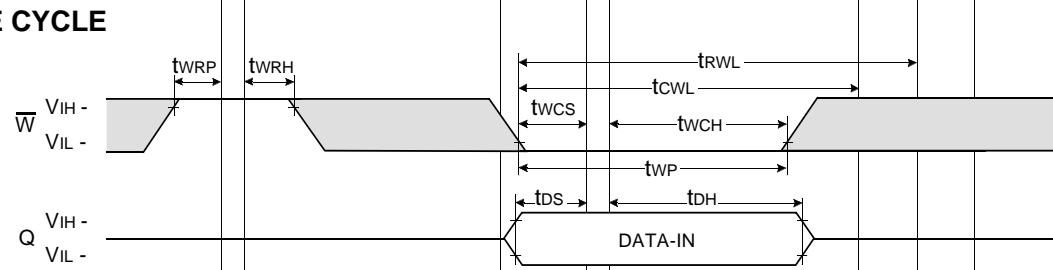
**CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE**



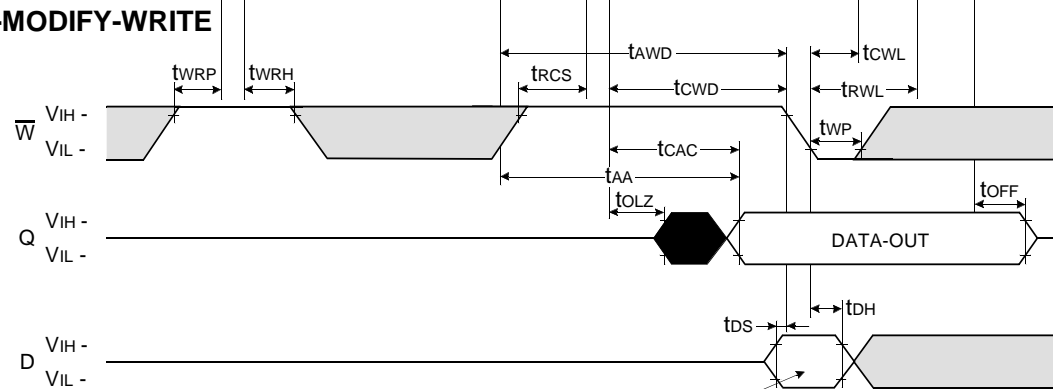
**READ CYCLE**



**WRITE CYCLE**



**READ-MODIFY-WRITE**



VALID DATA-IN

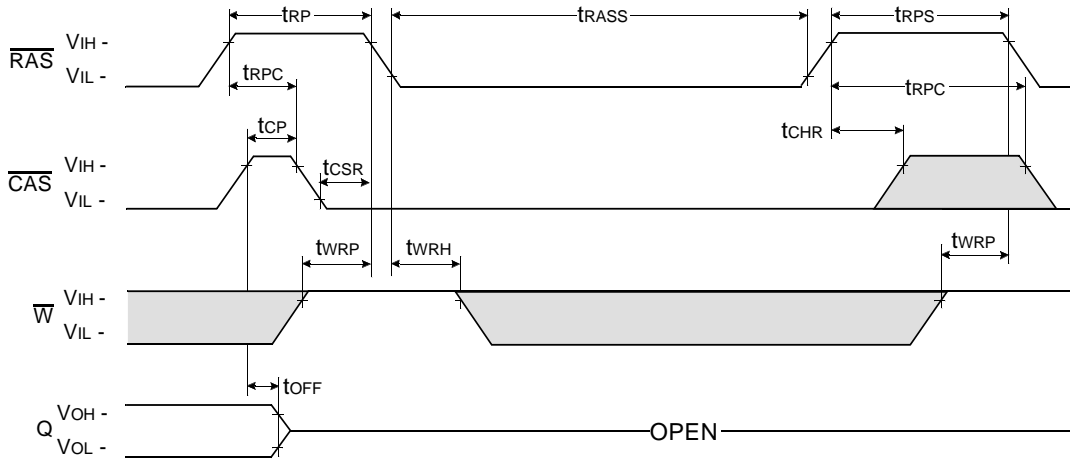
Don't care

Undefined



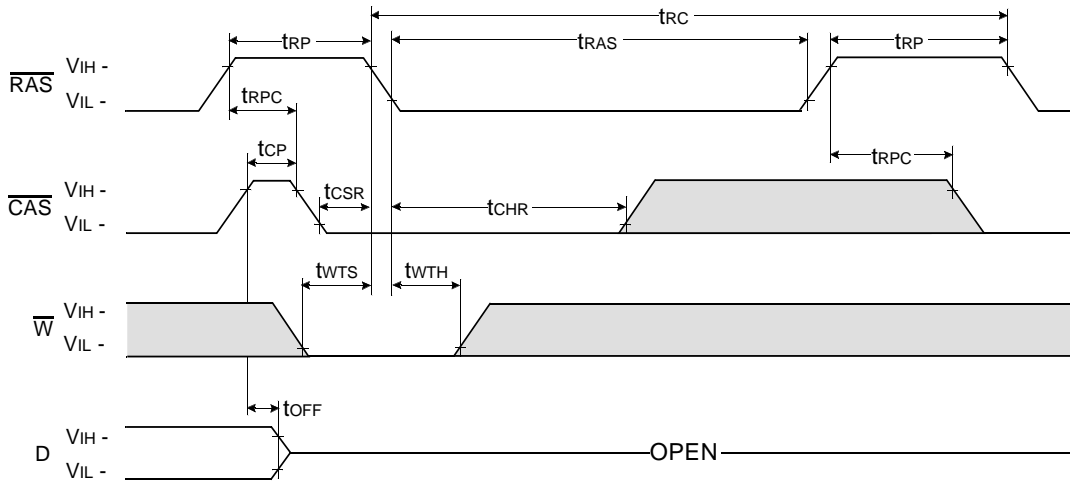
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE : A = Don't care



**TEST MODE IN CYCLE**

NOTE : D, A = Don't care



Don't care  
 Undefined

# KM41C4000D, KM41V4000D

# CMOS DRAM

## PLASTIC SMALL OUT-LINE J-LEAD

