

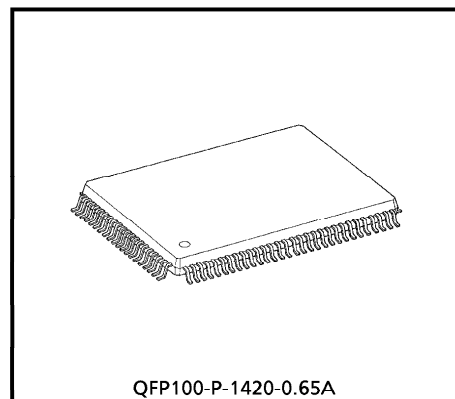
# TC90A17F

## PAP / PIP / POP CONTROLLER FOR NTCS / PAL WIDE TV

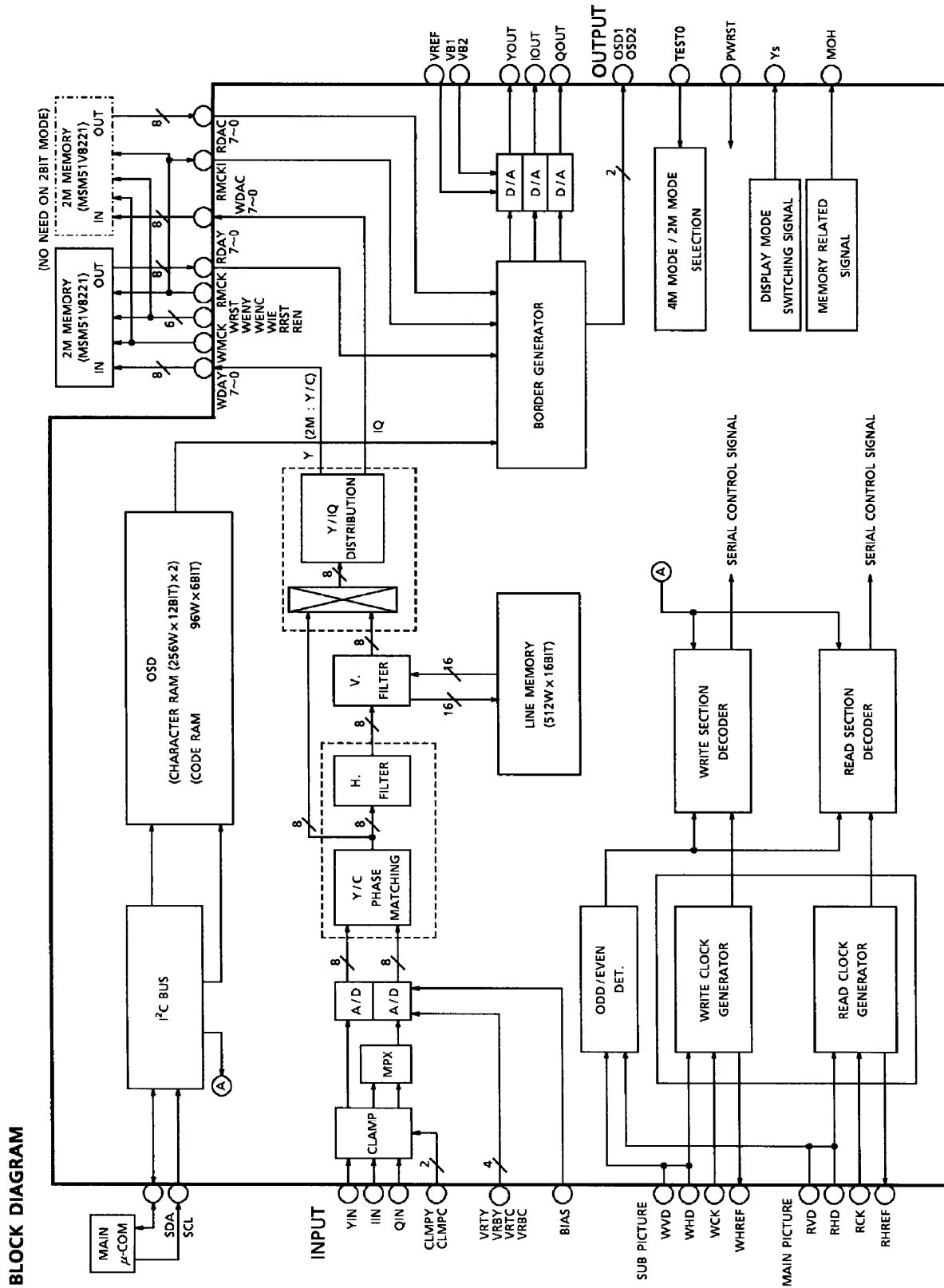
The TC90A17F is a PAP (picture and picture) / PIP / POP control IC with built in ADC and DAC. The control IC can be used for NTSC / PAL by combining with field memory and video signal processing IC. This IC is equipped with various display screen functions and is most suitable as a wide TV additional function controller.

### FEATURES

- Incorporates two 8bit A/D converters, three 8bit D/A converters, a clamping circuit, and a multiplexer into a single chip.
- External field memory and broadcast method
  - 2M bit mode : For NTSC only
  - 4M bit mode : For NTSC / PAL
- Display screen functions
  - PAP display : Display on 1/2 of the 16 : 9 screen (Animation mode and still mode can be set.)
  - PIP display : 4 : 3 or 16 : 9 (Animation mode and still mode can be set.)
  - POP display : 4 : 3 (The following modes can be set ; 3 screen still mode, 2 screen still mode with only 1 screen animation mode, and strobe mode)
  - Multiple still images : Up to 24 still images can be displayed on one screen by overlapping.
  - Channel search : 9 screen search or 12 screen search (Still mode, strobe mode, and 1 screen animation mode can be set.) A half screen or a full screen can be displayed.
  - Variable setting for frame width and frame color
    - : For frame color, 8 bits are available to indicate brightness ; R-Y or B-Y can be set in high-order 4 bits. The setting without frame is possible.
- OSD function
- Built-in horizontal and vertical filters
- Micro controller interface : I<sup>2</sup>C bus
- +3.3V single power supply
- Package : QFP100-pin

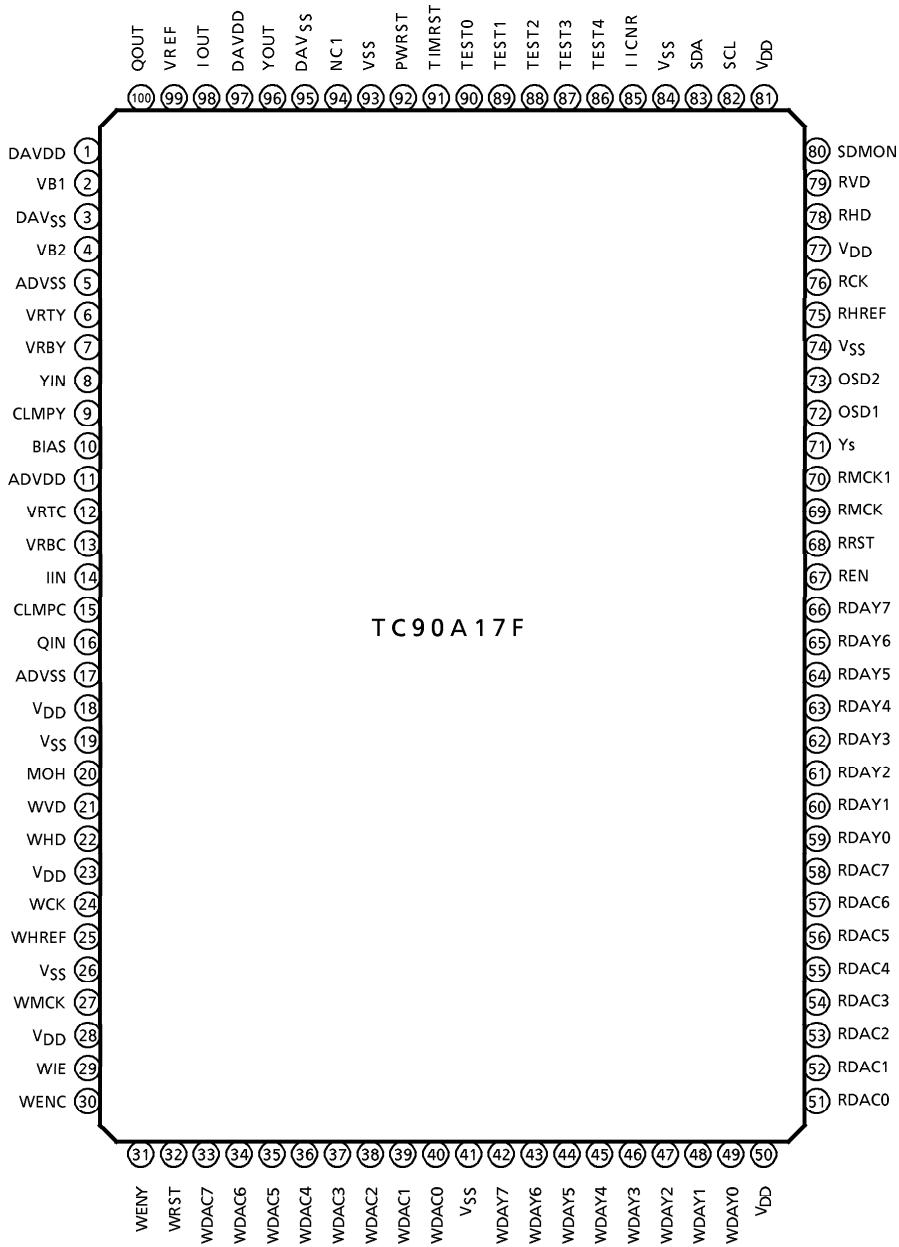


Weight : 1.6g (Typ.)

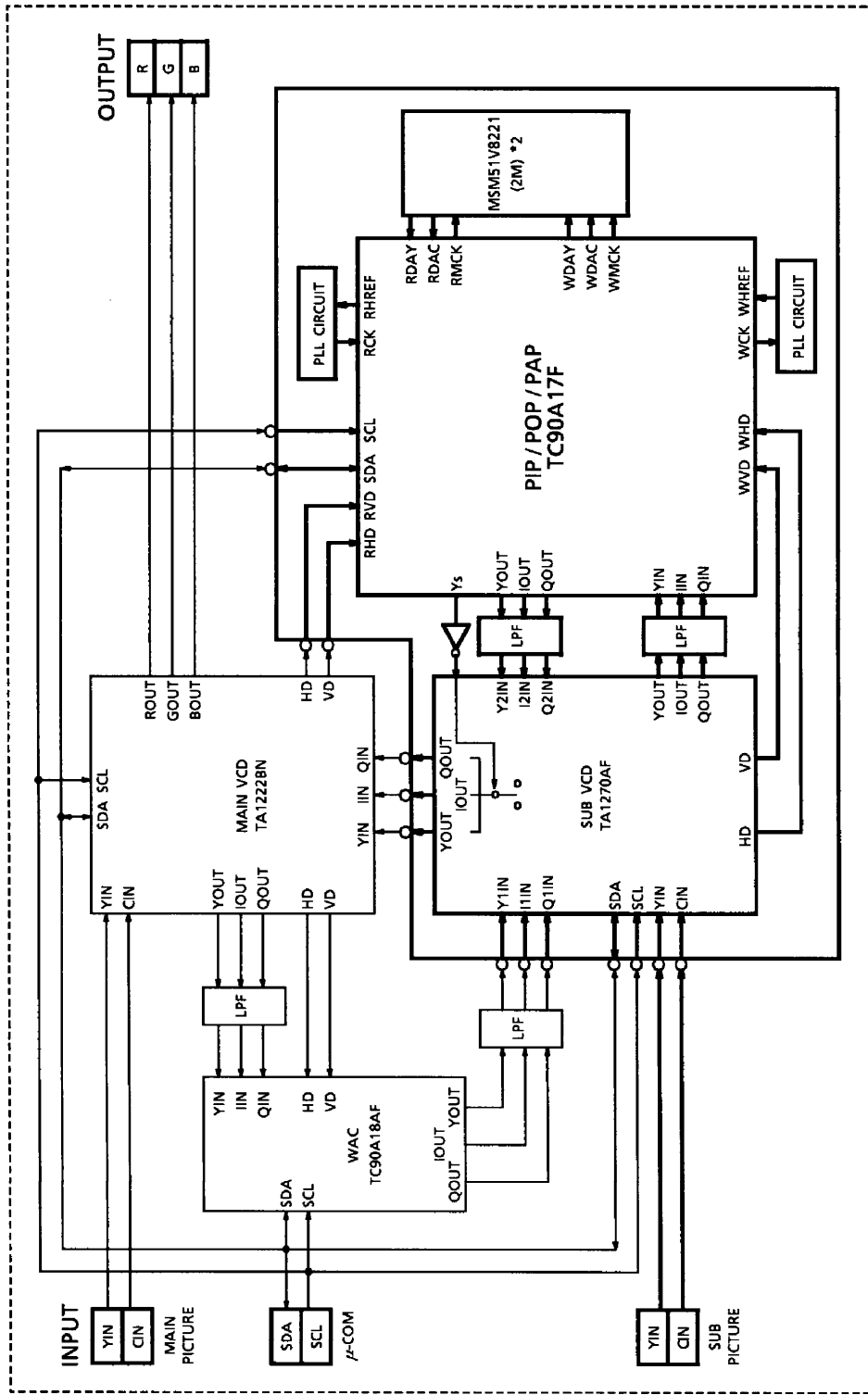


TC90A17F - 2

TERMINAL CONNECTION DIAGRAM



SYSTEM BLOCK DIAGRAM



## TERMINAL FUNCTIONS (QFP 100pin)

| PIN No. | PIN NAME | I/O | FUNCTION  | CONDITION                      |
|---------|----------|-----|---|--------------------------------|
| 1       | DAVDD    | —   | DAC $V_{DD}$                                      | $3.3V \pm 0.3$                 |
| 2       | VB1      | I   | DAC Bias  |                                |
| 3       | DAVSS    | —   | DAC $V_{SS}$                                      |                                |
| 4       | VB2      | I   | DAC Bias  |                                |
| 5       | ADVSS    | —   | ADC $V_{SS}$                                      |                                |
| 6       | VRTY     | —   | ADC Y signal reference input (TOP)                |                                |
| 7       | VRBY     | —   | ADC Y signal reference input (BOTTOM)             |                                |
| 8       | YIN      | I   | ADC Y signal input                                |                                |
| 9       | CLMPY    | —   | ADC Y signal clamp                                |                                |
| 10      | BIAS     | —   | ADC Bias  |                                |
| 11      | ADVDD    | —   | ADC $V_{DD}$                                      |                                |
| 12      | VRTC     | —   | ADC Chroma signal reference (TOP)                 |                                |
| 13      | VRBC     | —   | ADC Chroma signal reference (BOTTOM)              |                                |
| 14      | IIN      | I   | ADC I signal or R-Y signal input                  |                                |
| 15      | CLMPC    | —   | Chroma signal clamp                               |                                |
| 16      | QIN      | I   | ADC Q signal or B-Y signal input                  |                                |
| 17      | ADVSS    | —   | ADC $V_{SS}$                                      |                                |
| 18      | $V_{DD}$ | —   | Digital $V_{DD}$                                  | $3.3V \pm 0.3$                 |
| 19      | $V_{SS}$ | —   | Digital $V_{SS}$                                  |                                |
| 20      | MOH      | O   | Memory related signal output enable               |                                |
| 21      | WVD      | I   | Subscreen vertical synchronous signal output      | (Bus can handle polarity)      |
| 22      | WHD      | I   | Subscreen horizontal synchronous signal output    | (Bus can handle polarity)      |
| 23      | $V_{DD}$ | —   | Digital $V_{DD}$                                  | $3.3V \pm 0.3$                 |
| 24      | WCK      | I   | Subscreen system clock input                      |                                |
| 25      | WHREF    | O   | Subscreen PLL phase comparison output             |                                |
| 26      | $V_{SS}$ | —   | Digital $V_{SS}$                                  |                                |
| 27      | WMCK     | O   | Field memory write clock output                   |                                |
| 28      | $V_{DD}$ | —   | Digital $V_{DD}$                                  | $3.3V \pm 0.3$                 |
| 29      | WIE      | O   | Field memory input enable                         |                                |
| 30      | WENC     | O   | Field memory color write enable                   | 2M mode : open                 |
| 31      | WENY     | O   | Field memory intensity write enable               | (2M mode, for Y and C signals) |
| 32      | WRST     | O   | Field memory write reset                          |                                |
| 33      | WDAC7    | O   | C signal output (Field memory write signal / MSB) | 2M mode : open                 |
| 34      | WDAC6    | O   | C signal output (Field memory write signal)       | 2M mode : open                 |
| 35      | WDAC5    | O   | C signal output (Field memory write signal)       | 2M mode : open                 |
| 36      | WDAC4    | O   | C signal output (Field memory write signal)       | 2M mode : open                 |
| 37      | WDAC3    | O   | C signal output (Field memory write signal)       | 2M mode : open                 |
| 38      | WDAC2    | O   | C signal output (Field memory write signal)       | 2M mode : open                 |
| 39      | WDAC1    | O   | C signal output (Field memory write signal)       | 2M mode : open                 |
| 40      | WDAC0    | O   | C signal output (Field memory write signal / LSB) | 2M mode : open                 |

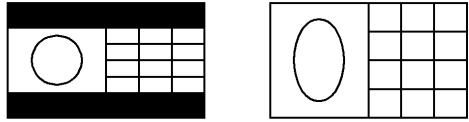
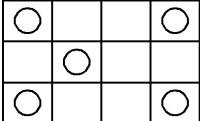
| PIN No. | PIN NAME        | I/O | FUNCTION  | CONDITION                 |
|---------|-----------------|-----|---|---------------------------|
| 41      | V <sub>SS</sub> | —   | Digital V <sub>SS</sub>   |                           |
| 42      | WDAY7           | O   | Y signal output (Field memory write signal / MSB)   |                           |
| 43      | WDAY6           | O   | Y signal output (Field memory write signal)   |                           |
| 44      | WDAY5           | O   | Y signal output (Field memory write signal)   |                           |
| 45      | WDAY4           | O   | Y signal output (Field memory write signal)   |                           |
| 46      | WDAY3           | O   | Y signal output (Field memory write signal)   |                           |
| 47      | WDAY2           | O   | Y signal output (Field memory write signal)   |                           |
| 48      | WDAY1           | O   | Y signal output (Field memory write signal)   |                           |
| 49      | WDAY0           | O   | Y signal output (Field memory write signal / LSB)   |                           |
| 50      | V <sub>DD</sub> | —   | Digital V <sub>DD</sub>   | 3.3V ± 0.3                |
| 51      | RDAC0           | I   | C signal input (Field memory read signal / LSB)   | 2M mode : Fixed to L      |
| 52      | RDAC1           | I   | C signal input (Field memory read signal)   | 2M mode : Fixed to L      |
| 53      | RDAC2           | I   | C signal input (Field memory read signal)   | 2M mode : Fixed to L      |
| 54      | RDAC3           | I   | C signal input (Field memory read signal)   | 2M mode : Fixed to L      |
| 55      | RDAC4           | I   | C signal input (Field memory read signal)   | 2M mode : Fixed to L      |
| 56      | RDAC5           | I   | C signal input (Field memory read signal)   | 2M mode : Fixed to L      |
| 57      | RDAC6           | I   | C signal input (Field memory read signal)   | 2M mode : Fixed to L      |
| 58      | RDAC7           | I   | C signal input (Field memory read signal / MSB)   | 2M mode : Fixed to L      |
| 59      | RDAY0           | I   | Y signal input (Field memory read signal / LSB)   |                           |
| 60      | RDAY1           | I   | Y signal input (Field memory read signal)   |                           |
| 61      | RDAY2           | I   | Y signal input (Field memory read signal)   |                           |
| 62      | RDAY3           | I   | Y signal input (Field memory read signal)   |                           |
| 63      | RDAY4           | I   | Y signal input (Field memory read signal)   |                           |
| 64      | RDAY5           | I   | Y signal input (Field memory read signal)   |                           |
| 65      | RDAY6           | I   | Y signal input (Field memory read signal)   |                           |
| 66      | RDAY7           | I   | Y signal input (Field memory read signal / MSB)   |                           |
| 67      | REN             | O   | Field memory read enable  |                           |
| 68      | RRST            | O   | Field memory read reset   |                           |
| 69      | RMCK            | O   | Filed memory read clock output  |                           |
| 70      | RMCKI           | I   | RMCK input (phase matching)   |                           |
| 71      | YS              | O   | Main screen/subscreen switching timing signal output  |                           |
| 72      | OSD1            | O   | OSD character signal output   |                           |
| 73      | OSD2            | O   | OSD character color Ys signal output  |                           |
| 74      | V <sub>SS</sub> | —   | Digital V <sub>SS</sub>   |                           |
| 75      | RHREF           | O   | Main screen PLL phase comparison output   |                           |
| 76      | RCK             | I   | Main screen system clock input  |                           |
| 77      | V <sub>DD</sub> | —   | Digital V <sub>DD</sub>   | 3.3V ± 0.3                |
| 78      | RHD             | I   | Main screen horizontal synchronous signal input   | (Bus can handle polarity) |
| 79      | RVD             | I   | Main screen vertical synchronous signal input   | (Bus can handle polarity) |
| 80      | SDMON           | O   | I <sup>2</sup> C BUS acknowledgement output/standard checking signal for micron controller 5V |                           |

| PIN No. | PIN NAME        | I/O | FUNCTION  | CONDITION                |
|---------|-----------------|-----|---|--------------------------|
| 81      | V <sub>DD</sub> | —   | Digital V <sub>DD</sub>                                       | 3.3V ± 0.3               |
| 82      | SCL             | I   | I <sup>2</sup> C BUS serial clock input                       |                          |
| 83      | SDA             | I/O | I <sup>2</sup> C BUS serial data input/acknowledgement output |                          |
| 84      | V <sub>SS</sub> | —   | Digital V <sub>SS</sub>                                       |                          |
| 85      | IICNR           | I   | I <sup>2</sup> C BUS noise removal circuit                    | (ON (H) / OFF (L))       |
| 86      | TEST4           | I   | Fixed to L  |                          |
| 87      | TEST3           | I   | Fixed to L  |                          |
| 88      | TEST2           | I   | Fixed to L  |                          |
| 89      | TEST1           | I   | Fixed to L  |                          |
| 90      | TEST0           | I   | L : 4M mode, H : 2M mode                                      |                          |
| 91      | TIMRST          | I   | Fixed to L  |                          |
| 92      | PWRST           | I   | System reset input  | L : Reset                |
| 93      | V <sub>SS</sub> | —   | Digital V <sub>SS</sub>                                       |                          |
| 94      | NC1             | —   |   |                          |
| 95      | DAVSS           | —   | DAC V <sub>SS</sub>   |                          |
| 96      | YOUT            | O   | DAC Y signal output   |                          |
| 97      | DAVDD           | —   | DAC V <sub>DD</sub>   |                          |
| 98      | IOUT            | O   | DAC I signal or R-Y signal output                             |                          |
| 99      | VREF            | —   | DAC Reference   | Reference voltage : 2.3V |
| 100     | QOUT            | O   | DAC Q signal or B-Y signal output                             |                          |

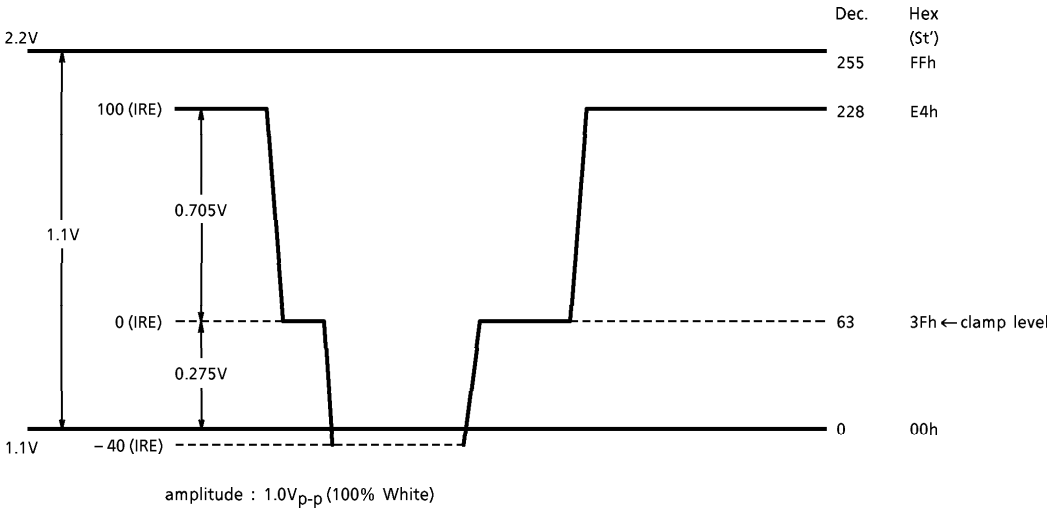
DISPLAY SCREEN FUNCTIONS

|   | FUNCTION   | DISPLAY SCREEN IMAGE |
|---|--|----------------------|
| 1 | <p>[PAP display screen (animation)]<br/>(using TC9097F)</p> <ul style="list-style-type: none"> <li>● 4 : 3 display<br/>Main screen-animation image /subscreen-animation image</li> <li>● Full screen display<br/>Main screen-animation image /subscreen-animation image</li> </ul>             |                      |
| 2 | <p>[PAP display screen (still image)]</p> <ul style="list-style-type: none"> <li>● 4 : 3 display<br/>Main screen-animation image /subscreen-still image</li> <li>● Full screen display<br/>Main screen-animation image /subscreen-still image</li> </ul>                                       |                      |
| 3 | <p>[9-screen search]</p> <ul style="list-style-type: none"> <li>● Main screen<br/>Animation image</li> <li>● Subscreen<br/>Display of 9-screen channel-select still image and strobe display<br/>Only one screen displays an animation image and other screens display stillimages.</li> </ul> |                      |
| 4 | <p>[PIP display]</p> <ul style="list-style-type: none"> <li>● Main screen<br/>16 : 9 animation image display</li> <li>● Subscreen<br/>Display of animation image or still image<br/>4 : 3 or 16 : 9 display</li> </ul>   |                      |
| 5 | <p>[3-screen POP display]</p> <ul style="list-style-type: none"> <li>● Main screen<br/>4 : 3 animation display</li> <li>● Subscreen<br/>4 : 3 animation display<br/>Display of still image, strobe, one animation image</li> </ul>   |                      |
| 6 | <p>[Multiple still image display]</p> <ul style="list-style-type: none"> <li>● Main screen<br/>16 : 9 animation image display</li> <li>● Subscreen<br/>Display of one screen of still image<br/>Up to 24 screens can be fetched.<br/>Frame forward playback is possible.</li> </ul>            |                      |

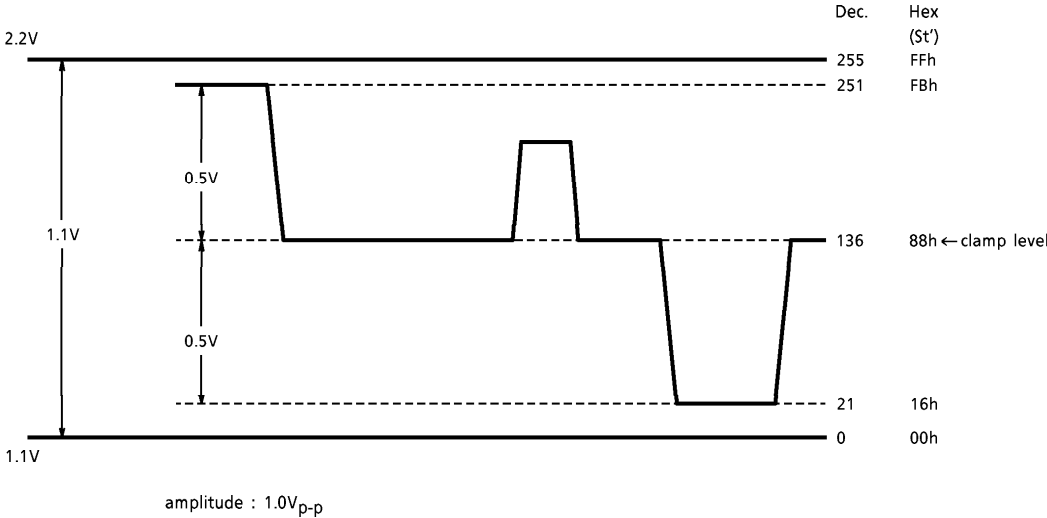


|   | FUNCTION   | DISPLAY SCREEN IMAGE  |
|---|--|---|
| 7 | <p>[12-screen search]</p> <ul style="list-style-type: none"><li>• Main screen animation</li><li>• Subscreen</li></ul> <p>Display of 12 screen channel-select still image and strobedisplay<br/>Only one animation screen is displayed and others are still images.</p> |   |
| 8 | <p>[12-screen search using full screen]</p> <ul style="list-style-type: none"><li>• Subscreen</li></ul> <p>Display of 12-screen channel-select still images and strobedisplay<br/>Only one animation image is displayed and others are still images.</p>               |  |

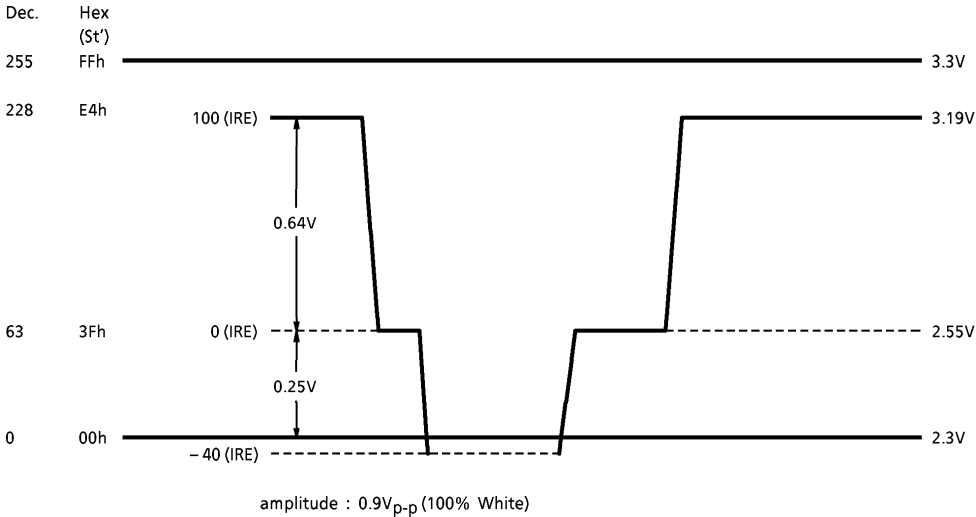
Standard signal input for ADC (luminance signal)



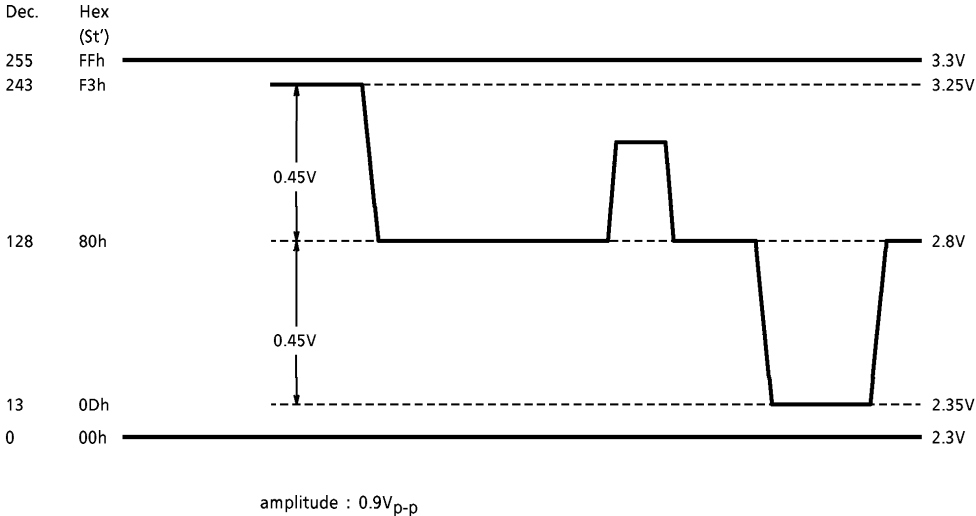
Standard signal input for ADC (color signal)



Standard signal output for DAC (luminance signal)



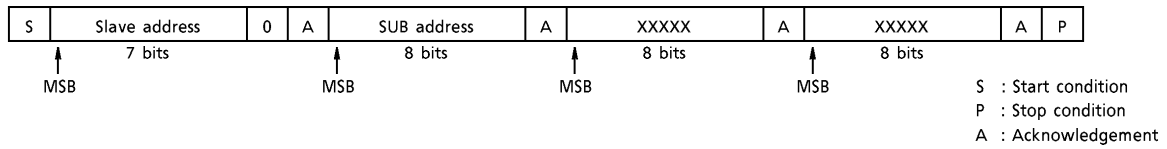
Standard signal output for DAC (color signal)



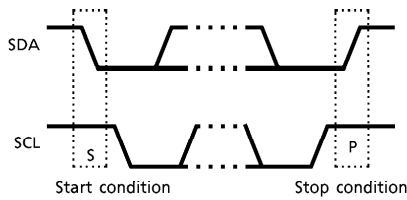
**OUTLINE OF I<sup>2</sup>C BUS CONTROL FORMAT**

The Bus control format of TC90A17F complies with the I<sup>2</sup>C bus control format of the PHILIPS Company.

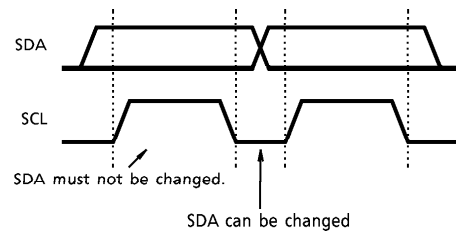
Data transfer format



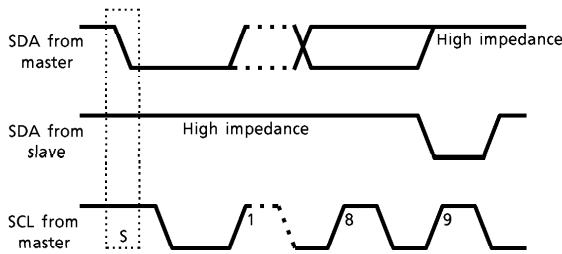
(1) Start condition and stop condition



(2) Bit transfer



(3) Acknowledgement



(4) Slave address

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0   |

Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

I<sup>2</sup>C-BUS ADDRESS SETTING TABLE

Slave address 26H (00100110)

Subaddress 00H (00000000) to 3FH (00111111)

| SUB-ADD-RESS | MSB 15  | 14     | 13     | 12     | 11      | 10     | 9      | 8      | 7      | 6      | 5     | 4      | 3       | 2      | 1     | LSB 0  |
|--------------|---------|--------|--------|--------|---------|--------|--------|--------|--------|--------|-------|--------|---------|--------|-------|--------|
| 00           | YCMF1   | YCMF0  | YCMN   | C2HFT  | Y2HFT   | WINSEL |        | KMODE  | YDL3   | →2     | →1    | →0     | KTC     | KTB    | KTA   |        |
| 01           | KD15    | →14    | →13    | →12    | →11     | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 02           | KD31    | →30    | →29    | →28    | →27     | →26    | →25    | →24    | →23    | →22    | →21   | →20    | →19     | →18    | →17   | →16    |
| 03           | HYPH2   | →1     | →0     | MIQPH1 | →0      |        |        |        | MOSY7  | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 04           | MOSIF3  | →2     | →1     | →0     | MOSQF3  | →2     | →1     | →0     | MOSIB3 | →2     | →1    | →0     | MOSQB3  | →2     | →1    | →0     |
| 05           | HFR13   | →2     | →1     | →0     | HFRQ3   | →2     | →1     | →0     | HFRY7  | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 06           | HWN13   | →2     | →1     | →0     | HWNQ3   | →2     | →1     | →0     | HWNY7  | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 07           | RF115   |        |        |        |         |        | RF119  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 08           | RF1215  |        |        |        |         |        | RF129  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 09           | RF1315  |        |        |        |         |        | RF139  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 0A           | RF1415  |        |        |        |         |        | RF149  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 0B           | RF1515  |        |        |        |         |        | RF159  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 0C           | RF1615  |        |        |        |         |        | RF169  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 0D           | RF1715  |        |        |        |         |        | RF179  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 0E           | RF1815  |        |        |        |         |        | RF189  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 0F           | RF1915  |        |        |        |         |        | RF199  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 10           | RF1A15  |        |        |        |         |        | RF1A9  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 11           | RHYSE11 | →10    | →9     | →8     | RHWIE11 | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 12           | →7      | →6     | →5     | →4     | RHWIS11 | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 13           | →3      | →2     | →1     | →0     |         |        | RVWIE9 | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 14           | RHYSS11 | →10    | →9     | →8     |         |        | RVWIS9 | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 15           | →7      | →6     | →5     | →4     | RHSIZ11 | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 16           | →3      | →2     | →1     | →0     |         |        | RVSIZ9 | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 17           |         |        |        |        | RRH11   | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 18           |         |        |        |        |         |        | RRV9   | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 19           |         |        |        |        |         |        | RWRN9  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 1A           |         |        |        |        |         |        | RWRA9  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 1B           | RHRFTH  | RHRF1V | RHINV2 |        | PRHP11  | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 1C           |         |        |        |        |         |        | RVPG9  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 1D           | NTPAL   |        | WCSEL1 | WCSEL0 | PAPFIL  | WHST10 | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 1E           | WHMOD3  | →2     | →1     | →0     | WCKINV  | WHED10 | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 1F           | WEYINV  | WEYDL2 | →1     | →0     | IENINV  | KWST10 | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 20           | WECINV  | WECDL2 | →1     | →0     |         | KWED10 | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 21           | WHRFTH  | WHRF1V | WHINV2 | MOH    | WHRST11 | →10    | →9     | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 22           | WKHYO   | WHINV1 | WVINV  | WS263  | HYJ3    | →2     | →1     | WFCMP8 | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 23           | RKHYO   | RHINV1 | RVINV  | RS263  | HIJ3    | →2     | →1     | RFCMP8 | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 24           | VFB47   | →46    | →45    | →44    | VFB43   | →42    | →41    | →40    | VFB39  | →38    | →37   | →36    | VFB35   | →34    | →33   | →32    |
| 25           | VFB31   | →30    | →29    | →28    | VFB27   | →26    | →25    | →24    | VFB23  | →22    | →21   | →20    | VFB19   | →18    | →17   | →16    |
| 26           | VFB15   | →14    | →13    | →12    | VFB11   | →10    | →9     | →8     | VFB7   | →6     | →5    | →4     | VFB3    | →2     | →1    | →0     |
| 27           | FMINT   | FMON   | PIP    |        | WXMCP2  | →1     | →0     | WVST8  | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 28           | WVMOD3  | →2     | →1     | →0     | WSYILL  | WXMCP4 | →3     | WVED8  | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 29           |         |        |        |        | VFTHR   | WXYFRM | MULT1  | →0     | AUTIIC | WXCP6  | →5    | →4     | →3      | →2     | →1    | →0     |
| 2A           |         |        |        | W9H82  | →1      | →0     | W9IE9  | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 2B           | WINT3   | →2     | →1     | →0     |         |        | W9H58  | →7     | →6     | →5     | →4    | →3     | →2      | →1     | →0    | →0     |
| 2C           |         |        |        | W9M4   | →3      | →2     | →1     | →0     | W9V57  | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 2D           |         |        |        |        |         |        |        |        |        |        |       |        |         |        |       |        |
| 2E           |         |        |        | RREINV | RRSTINV | RCKINV | RREP11 | →0     | RMUTE  | VSVOFF |       | PAPSW  | FRF1    | ROEALT | RFISW | RFIALT |
| 2F           |         |        |        |        |         |        |        |        | RF10_7 | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 30           |         | OSDYA1 | →0     | OSDYB1 | →0      | OSDXA1 | →0     | OSDXB1 | →0     | OSDXC1 | →0    | OSDXD1 | →0      | OSDXE1 | →0    | →0     |
| 31           | OSDDX7  | →6     | →5     | →4     | →3      | →2     | →1     | →0     | OSDX7  | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 32           | OSDDY7  | →6     | →5     | →4     | →3      | →2     | →1     | →0     | OSDY7  | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 33           |         |        |        |        |         |        |        |        |        |        |       |        |         |        |       |        |
| 34           |         |        |        | HYJMON |         |        | LMRST9 | →8     | →7     | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 35           | CLPST7  | →6     | →5     | →4     | →3      | →2     | →1     | →0     | CLPED7 | →6     | →5    | →4     | →3      | →2     | →1    | →0     |
| 36~3C        |         |        |        |        |         |        |        |        |        |        |       |        |         |        |       |        |
| 3F           |         |        |        |        |         |        |        |        |        | OKDSE  | OSDSE | OLSEL  | ON1BYTE | OWRSKC | OCRW  | OKRW   |

DESCRIPTION OF THE CONTENTS OF WRITE I<sup>2</sup>C-BUS DATA 1

| SUB-ADDRESS | DISPLAY NAME    | FUNCTION   |
|-------------|-----------------|--|
| 00H         | YCMF1           | Y/C MIX signal (M/N output) polarity switching<br>(L : Inversion, H : Non-inversion)   |
|             | YCMF0           | Y/C MIX signal (pre-multiplier) polarity switching<br>(L : Inversion, H : Non-inversion)   |
|             | YCMN            | Switching to fixed to Y or Y/C MIX (L : Fixed to Y, H : Y/C MIX)   |
|             | C2HFT           | Binary interpolation circuit of color signal (I/Q) (L : OFF, H : ON)   |
|             | Y2HFT           | Binary interpolation circuit of brightness signal (Y) (L : OFF, H : ON)<br>(Horizontal thinning mode : 3/8 [5H], 2/5 [6H] = H)   |
|             | W1NSEL          | Switching of thinning processing circuit<br>(L : M/N thinning, H : 1/N thinning)   |
|             | KMODE           | Horizontal filter coefficient mode switching<br>(l : L/N processing, H : M/N processing)   |
|             | YDL3-0<br>KTC-A | Brightness signal (Y) delay adjustment (0 to 10CK, 600fh units)<br>Filter coefficient count setting (0H = 1, 7H = 8)   |
| 01H         | KD3-0           | Horizontal filter 1st coefficient  |
|             | KD7-4           | Horizontal filter 2nd coefficient  |
|             | KD11-8          | Horizontal filter 3rd coefficient  |
|             | KD15-12         | Horizontal filter 4th coefficient  |
| 02H         | KD19-16         | Horizontal filter 5th coefficient  |
|             | KD23-20         | Horizontal filter 6th coefficient  |
|             | KD27-24         | Horizontal filter 7th coefficient  |
|             | KD31-28         | Horizontal filter 8th coefficient  |
| 1DH         | NTPAL           | NTSC/PAL (L : NTSC, H : PAL)   |
|             | WCSEL1, 0       | I/Q inversion (1=For SEL block, (0=ADIQ for multiplexer)   |
|             | PAPFIL          | PAP/filter processing switching (L : PAP, H : Filter processing)   |
|             | WHST10-0        | Specification of Write Enable Horizontal Gate Starting position<br>(setting an odd number value only)  |
| 1EH         | WHMOD3-0        | Setting thinning rate<br>0H = 1/16, 1H = 1/8, 2H = 1/5, 3H = 1/4, 4H = 1/3, 5H = 3/8, 6H = 2/5, 7H = 1/2, 8H = 3/5, 9H = 5/8, AH = 2/3, BH = 3/4, CH = 4/5, DH = 7/8, EH = 15/16, FH = 16/16 |
|             | WCKINV          | Inversion of field memory Write clock polarity (H : Sets inversion)  |
|             | WHED10-0        | Specification of an end position of Write Enable Horizontal Gate (Set an odd value only)   |

DESCRIPTION OF THE CONTENTS OF WRITE I<sup>2</sup>C-BUS DATA 2

| SUB-ADDRESS | DISPLAY NAME | FUNCTION  |
|-------------|--------------|---|
| 1FH         | WEYINV       | Polarity inversion of brightness field Memory Writer Enable signal (WENY)<br>(L : Sets non-inversion)   |
|             | WEYDL2-0     | WENY signal delay adjustment (Unit : 1200fh)<br>0H = +0, 1H = +1, 2H = +2, 3H = +3, 4H = +4, 5H = +6, 6H = -1, 7H = -2<br>(Set 0H = +0)                                 |
|             | IENINV       | Polarity inversion of field memory Input Enable signal<br>(L : Non-inversion, H : Inversion)<br>(Set according to the memory specification (fixed after determination)) |
|             | KWST10-0     | Specification of HFIL operation gate (WKWHY) start position<br>(set an odd number only)   |
| 20H         | WECINV       | Polarity inversion of color field memory Write Enable signal (WENC)<br>(L : Sets non-inversion)   |
|             | WECDL2-0     | WENY signal delay adjustment (unit : W2CK)  |
|             | KWED10-0     | 0H = +0, 1H = +1, 2H = +2, 3H = +3, 4H = +4, 5H = +6, 6H = -1, 7H = -2<br>Specification of end position of HFIL operation gate (WKWHT) (Set an odd value only)          |
| 21H         | WHRFTH       | PLL control signal (WHREF) forced output (H : Forced output)  |
|             | WHRFIV       | WHREF polarity inversion (L : Non-inversion, H : Inversion)   |
|             | WHINV2       | HD polarity inversion of WHREF output control<br>(L : Non-inversion, H : Inversion)   |
|             | MOH          | Field memory occupation signal (L : Other IC, H : PAP IC)   |
|             | WHRST11-0    | Write horizontal phase reference  |
| 22H         | WKHYO        | Write forced standard checking<br>(L : Standard / non-standard, H : Forced standard)  |
|             | WHINV1       | Subscreen-horizontal synchronous signal (WHD) polarity inversion<br>(L : Non-inversion, H : Inversion)  |
|             | WVINV        | Subscreen-vertical synchronous signal (WVD) polarity inversion<br>(L : Non-inversion, H : Inversion)  |
|             | WS263        | Inversion of Write field checking (L : 263, H : 262)  |
|             | HYJ3-1       | Non-standard checking circuit setting value   |
|             | WFCMP8-0     | Write forced non-standard setting value   |

DESCRIPTION OF THE CONTENTS OF WRITE I<sup>2</sup>C-BUS DATA 3

| SUB-ADDRESS | DISPLAY NAME | FUNCTION  |
|-------------|--------------|---|
| 23H         | RKHYO        | Read forced standard checking<br>(L : Standard / non-standard, H : Forced standard)   |
|             | RHINV1       | Main screen-horizontal synchronous signal (RHD) polarity inversion<br>(L : Non-inversion, H : Inversion)  |
|             | RVINV        | Main screen-vertical synchronous signal (RVD) polarity inversion<br>(L : Non-inversion, H : Inversion)  |
|             | RS263        | Inversion of Read field checking (L : 263, H : 262)   |
|             | HIJ3-1       | Non-standard checking circuit setting value   |
|             | RFCMP8-0     | Read forced non-standard setting value  |
| 24H         | VFB47-44     | Vertical filter 1st coefficient A   |
|             | VFB43-40     | Vertical filter 2nd coefficient A   |
|             | VFB39-36     | Vertical filter 3rd coefficient A   |
|             | VFB35-32     | Vertical filter 4th coefficient A   |
| 25H         | VFB31-32     | Vertical filter 5th coefficient A   |
|             | VFB27-24     | Vertical filter 6th coefficient A   |
|             | VFB23-20     | Vertical filter 7th coefficient A   |
|             | VFB19-16     | Vertical filter 8th coefficient A   |
| 26H         | VFB15-12     | Vertical filter 9th coefficient A   |
|             | VFB11-08     | Vertical filter 10th coefficient A  |
|             | VFB07-04     | Vertical filter 11th coefficient A / 1st coefficient B (VFB 7, 6), 2nd coefficient B (VFB 5, 4)   |
|             | VFB03-00     | Vertical filter 3rd coefficient B (VFB 3, 2), 4th coefficient B (VFB 1, 0)  |
| 27H         | FMINT        | Field memory initialization ON/OFF (for control by micro controller only)<br>(H : ON)   |
|             | FMON         | Fixed to H  |
|             | PIP          | Handles PIP display (frame display) (H : PIP)   |
|             | WXMCP2-0     | Setting horizontal block cycle of strobe display mode (0H : 1 to 7H : 8)  |
|             | WVST8-0      | Specification of start position of Write Enable Vertical Gate   |
| 28H         | WVMOD3-0     | Vertical thinning rate setting<br>0H = 1/16, 1H = 1/8, 2H = 1/5, 3H = 1/4, 4H = 1/3, 5H = 3/8, 6H = 2/5, 7H = 1/2, 8H = 3/5, 9H = 5/8, AH = 2/3, BH = 3/4, CH = 4/5, DH = 7/8, EH = 15/16, FH = 16/16 |
|             | WSTILL       | Field memory Write Halt (still regeneration) (H : Write Halt)<br>(Changing parameters after halt operation)   |
|             | WXMCP4, 3    | Setting vertical block cycle setting of a strobe display mode<br>(0H : 1 to 3H : 4)   |
|             | WVED8-0      | Specification of end position of Write Enable Vertical Gate   |
|             |              |   |



DESCRIPTION OF THE CONTENTS OF WRITE I<sup>2</sup>C-BUS DATA 4

| SUB-ADDRESS | DISPLAY NAME | FUNCTION   |
|-------------|--------------|--|
| 29H         | VFTHR        | Vertical filter ON/OFF (L : ON, H : OFF)   |
|             | WKYFRM       | Write forced frame processing (L : Normal, H : Forced frame)   |
|             | MULT1, 0     | Memory control signal mode switching<br>(00H : PAP, 11H : Multiple search, strobe)   |
|             | AUTIIC       | Switching split display Write position specification mode<br>(L : Bus setting, H : Automatic setting)  |
|             | WXCP6-0      | Specification of memory write interval (2, 4, 6, 8, to 512 fields)   |
| 2AH         | W9HB2-0      | Split screen control-setting the number of horizontal blocks<br>(number of horizontal blocks-1)  |
|             | W9IE9-0      | Split screen control-setting horizontal input enable period<br>Number of block picture elements × (number of horizontal blocks-1))   |
| 2BH         | WINT3-0      | Setting field memory initialization level (SEL block)  |
|             | W9HS8-0      | Split screen control-setting the number of block picture elements-3  |
| 2CH         | W9M4-3       | Split screen control-specification of Write position<br>(vertical, 0→3 : Top→bottom) (AUTIIC = L)  |
|             | W9M2-0       | Split screen control-specification of Write position<br>(horizontal, 0→7 : Left→right) (AUTIIC = L)  |
|             | W9VS7-0      | Split screen control-setting the number of block lines<br>(number of block lines-1)<br>[ Note : Subaddress 2CH is for transmission only in multiple search Write processing] |
| 34H         | HYJMON       | Fixed to L   |
|             | LMRST9-0     | Rest phase of vertical filter line memory  |
| 35H         | CLPST7-0     | Specification of clamp pulse start position  |
|             | CLPED7-0     | Specification of clamp pulse stop position   |

DESCRIPTION OF THE CONTENTS OF READ I<sup>2</sup>C-BUS DATA 5

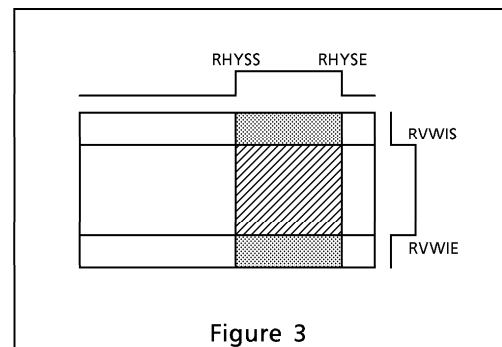
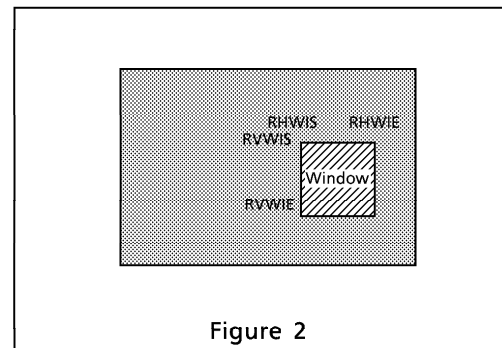
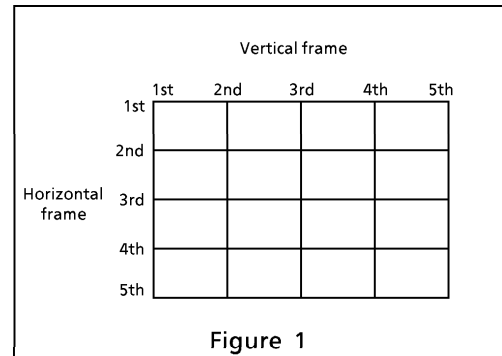
| SUB-ADDRESS | DISPLAY NAME                  | FUNCTION  |
|-------------|-------------------------------|---|
| 03H         | HYPH2-0<br>HIQPH10            | Read Y signal phase adjustment<br>Read I and QY signal phase adjustment                               |
| 05H         | HFR13-0<br>HFRQ3-0<br>HFRY7-0 | Frame I signal level<br>Frame Q signal level<br>Frame Y signal level                                  |
| 06H         | HWNI3-0<br>HWNQ3-0<br>HWN7-0  | I signal clamp level<br>Q signal clamp level<br>Y signal clamp level                                  |
| 07H         | RF1115<br>RF11 (9-0)          | 1st horizontal frame ON/OFF (0 : ON)<br>1st horizontal frame vertical phase                           |
| 08H         | RF1215<br>RF12 (9-0)          | 2nd horizontal frame ON/OFF (0 : ON)<br>2nd horizontal frame vertical phase                           |
| 09H         | RF1315<br>RF13 (9-0)          | 3rd horizontal frame ON/OFF (0 : ON)<br>3rd horizontal frame vertical phase                           |
| 0AH         | RF1415<br>RF14 (9-0)          | 4th horizontal frame ON/OFF (0 : ON)<br>4th horizontal frame vertical phase                           |
| 0BH         | RF1515<br>RF15 (9-0)          | 5th horizontal frame ON/OFF (0 : ON)<br>5th horizontal frame vertical phase                           |
| 0CH         | RF1615<br>RF16 (9-0)          | 1st vertical frame ON/OFF (0 : ON)<br>1st vertical frame horizontal phase                             |
| 0DH         | RF1715<br>RF17 (9-0)          | 2nd vertical frame ON/OFF (0 : ON)<br>2nd vertical frame horizontal phase                             |
| 0EH         | RF1815<br>RF18 (9-0)          | 3rd vertical frame ON/OFF (0 : ON)<br>3rd vertical frame horizontal phase                             |
| 0FH         | RF1915<br>RF19 (9-0)          | 4th vertical frame ON/OFF (0 : ON)<br>4th vertical frame horizontal phase                             |
| 10H         | RF1A15<br>RF1A (9-0)          | 5th vertical frame ON/OFF (0 : ON)<br>5th vertical frame horizontal phase                             |
| 11H         | RHYSE11-8<br>RHWIE11-0        | YS signal horizontal end phase (MSB)<br>Clamp window horizontal start phase                           |
| 12H         | RHYSE7-4<br>RHWIS11-0         | YS signal horizontal end phase<br>Clamp window horizontal start phase                                 |
| 13H         | RHYSE3-0<br>RVWIE9-0          | YS signal horizontal end phase (LSB)<br>Clamp window vertical end phase                               |
| 14H         | RHYSS11-8<br>RVWIS9-0         | YS signal horizontal start phase (MSB)<br>Clamp window vertical start phase                           |
| 15H         | RHYSS07-4<br>RHSIZ11-0        | YS signal horizontal start phase<br>Horizontal display size (number of horizontal picture elements-3) |
| 16H         | RHYSS03-0<br>RVSIZ9-0         | YS signal horizontal start phase (LSB)<br>Vertical display size (number of lines)                     |

DESCRIPTION OF THE CONTENTS OF READ I<sup>2</sup>C-BUS DATA 6

| SUB-ADDRESS | DISPLAY NAME | FUNCTION  |
|-------------|--------------|---|
| 17H         | RRF11-0      | Horizontal display start phase  |
| 18H         | RRV9-0       | Vertical display start phase  |
| 19H         | RWRN9-0      | Field memory Write/Read phase setting value 1   |
| 1AH         | RWRA9-0      | Field memory Write/Read phase setting value 2   |
| 1BH         | RHRFTH       | RHREF output control forced output mode setting (L : Normal, H : Forced output)                   |
|             | RHRFIV       | RHREF output polarity inversion (L : Non-inversion, H : Inversion)                                |
|             | RHINV2       | RHREF output control HD polarity inversion (L : Non-inversion, H : Inversion)                     |
|             | PRHP11-0     | Read processing, horizontal reference (PLL counter value decoding)                                |
| 1CH         | RVPG9-0      | Read processing, vertical reference<br>(input VD : vertical counter, reading initial value)       |
| 2EH         | RREINV       | Polarity inversion of field memory Read Enable (RRE) signal<br>(L : Non-inversion, H : Inversion) |
|             | RRSTINV      | Polarity inversion of field memory Read Reset (RRST) signal<br>(L : Non-inversion, H : Inversion) |
|             | RCKINV       | Polarity inversion of field memory Read Clock (RCK) signal<br>(L : Non-inversion, H : Inversion)  |
|             | RREPH1-0     | RRE signal phase adjustment   |
|             | RMUTE        | Read, Image muting (L : Without muting, H : Muting)   |
|             | YSVOFF       | YS signal vertical ON/OFF (L : ON, H : OFF)   |
|             | PAPSW        | ON in PAP mode (L : ON, H : OFF)  |
|             | FRFI         | Forced single field display ON/OFF (L : OFF, H : ON)  |
|             | ROEALT       | ODD/EVNE inversion (L : Normal, H : Inversion)  |
|             | RFISW        | Fixed to H  |
| RFIALT      | Fixed to L   |   |
| 2FH         | RF10 (7-4)   | Horizontal frame thickness adjustment (thick→fine, fine→thick)                                    |
|             | RF10 (3-0)   | Vertical frame thickness adjustment (thick→fine, fine→thick)                                      |

### DESCRIPTION OF THE CONTENTS OF READ I<sup>2</sup>C-BUS DATA 6 (contents supplement)

1. Frame display (see Figure 1)
  - (1) Up to five of each vertical and horizontal frames can be displayed in any positions.
  - (2) Any vertical and horizontal frames can be erased.
  - (3) Y signals can be set in 8-bit precision and I and Q signals can be set in 4-bit precision.
  - (4) The frame thickness can be set in 4-bit precision.
  - (5) Use the 1st and 5th vertical and horizontal frames for one-screen display such as PIP.
2. Display of a clamp window (see Figures 2 and 3)
  - (1) A clamp window can be set in any position with any size.
  - (2) Clamp level variable range of the shaded section  
Y signal : 0H to FFH  
I and Q signals: 78H to 87H
3. YS signal (See Figure 3)
  - (1) Set horizontal timing of YS signals according to the horizontal start position RHYSS and horizontal end position RHYSE.
  - (2) For vertical timing, the vertical start position RVWIS and vertical end position RVWIE of the clamp window are also used.
  - (3) When YS signal vertical ON/OFF (YSVOFF) is set to OFF, the is also set to the YS signal level.
4. Read phase adjustment  
4M mode  
The Y signal comprises 8 steps and the C signal comprises 4 steps in 26ns units.
5. PAPSW signal  
To set double-screen display (PAP), set the signal to 0.
6. FRFI signal  
To set forced single display, set the signal to 1.



DESCRIPTION OF THE CONTENTS OF READ I<sup>2</sup>C-BUS DATA 7 (OSD related data 1)

| SUB-ADDRESS | DISPLAY NAME | FUNCTION   |
|-------------|--------------|--|
| 03H         | MOSY7-0      | Brightness level setting of OSD display character                  |
| 04H         | MOSIF3-0     | Setting I level of OSD display character color 1 (OCOLR = 0)       |
|             | MOSQF3-0     | Setting Q level of OSD display character color 1 (OCOLR = 0)       |
|             | MOSIB3-0     | Setting I level of OSD display character color 2 (OCOLR = 1)       |
|             | MOSQB3-0     | Setting Q level of OSD display character color 2 (OCOLR = 1)       |
| 30H         | OSDYA1-0     | Screen start position micro adjustment A (vertical)                |
|             | OSDYB1-0     | Screen start position micro adjustment B (vertical)                |
|             | OSDXA1-0     | Screen start position micro adjustment A (horizontal)              |
|             | OSDXB1-0     | Screen start position micro adjustment B (horizontal)              |
|             | OSDXC1-0     | Screen start position micro adjustment C (horizontal)              |
|             | OSDXD1-0     | Screen start position micro adjustment D (horizontal)              |
|             | OSDXE1-0     | Screen start position micro adjustment E (horizontal)              |
| 31H         | OSDDX7-0     | Adjustment of width for OSD display (horizontal)                   |
|             | OSDX7-0      | Screen display start position (horizontal)                         |
| 32H         | OSDDY7-0     | Adjustment of width for OSD display (vertical)                     |
|             | OSDY7-0      | Screen display start position (vertical)                           |
| 3FH         | OKDSE        | Character shadow selection (L : 1 dot, H : 2 dots)                 |
|             | OSDSE        | Character display (L : OFF, H : ON)                                |
|             | OLSEL        | Screen display selection (L : Display mode 1, H : Display mode 2)* |
|             | ON1BYTE      | 1-byte Write selection (L : Normal, H : 1-byte Write)              |
|             | OWRSKC       | Write RAM selection (L : Character, H : Code)                      |
|             | OCRW         | Code RAM Write ON/OFF (L : ON, H : OFF)                            |
|             | OKRW         | Character RAM Write ON/OFF (L : ON, H : OFF)                       |

\* : See Page 22

DESCRIPTION OF THE CONTENTS OF READ I<sup>2</sup>C-BUS DATA 8 (OSC related data 2)

1. Display mode 1

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D |
| 1  |    |    |    |    | 2  |    |    |    |    | 3  |    |    |    |    | 4  |    |    |    |    | 5  |    |    |    |    | 6  |    |    |    |    |
| 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D |
| 7  |    |    |    |    | 8  |    |    |    |    | 9  |    |    |    |    | 10 |    |    |    |    | 11 |    |    |    |    | 12 |    |    |    |    |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D |
| 13 |    |    |    |    | 14 |    |    |    |    | 15 |    |    |    |    | 16 |    |    |    |    | 17 |    |    |    |    | 18 |    |    |    |    |

(Note 1) OSD display possible up to a vertical maximum 3 blocks x horizontal maximum 6 blocks.

(Note 2) The digits in one screen indicate the code RAM address.

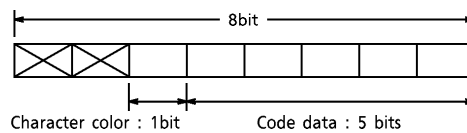
2. Display mode 2

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 |
| 1  |    |    |    |    | 2  |    |    |    |    | 3  |    |    |    |    | 4  |    |    |    |    |
| 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B |
| 5  |    |    |    |    | 6  |    |    |    |    | 7  |    |    |    |    | 8  |    |    |    |    |
| 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F | 40 | 41 | 42 | 43 |
| 9  |    |    |    |    | 10 |    |    |    |    | 11 |    |    |    |    | 12 |    |    |    |    |
| 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B |
| 13 |    |    |    |    | 14 |    |    |    |    | 15 |    |    |    |    | 16 |    |    |    |    |

(Note 1) OSD display possible up to a vertical maximum 4 blocks x horizontal maximum 4 blocks.

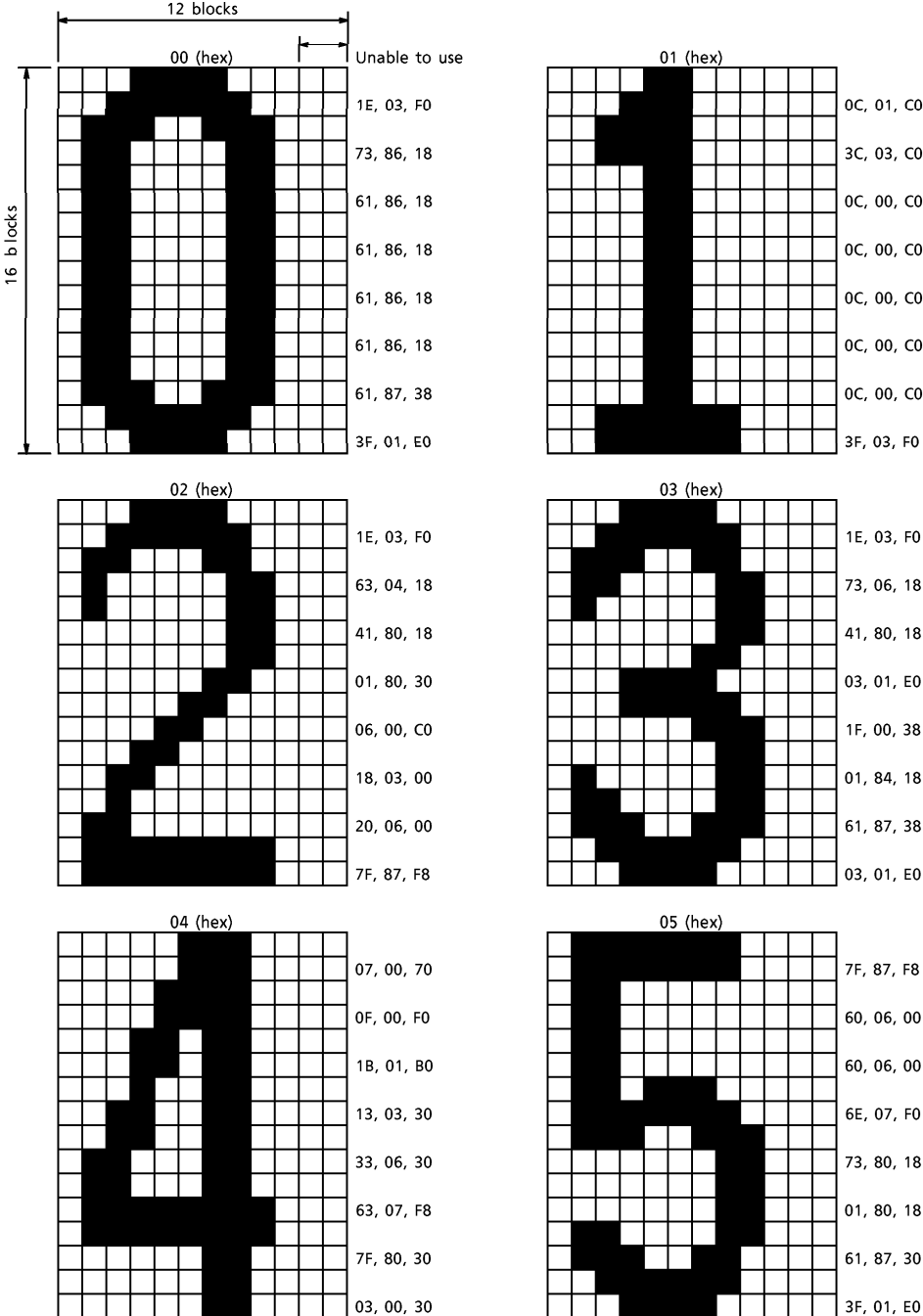
(Note 2) The digits in one screen indicate the code RAM address.

3. Example of code data



DESCRIPTION OF THE CONTENTS OF READ I<sup>2</sup>C-BUS DATA 8 (OSC related data 3)

Example of character data creation

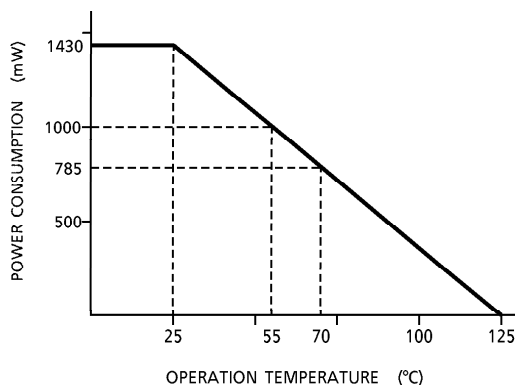


**MAXIMUM RATINGS** ( $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ )

| CHARACTERISTIC       | SYMBOL           | RATING                     | UNIT       |
|----------------------|------------------|----------------------------|------------|
| Power Supply Voltage | $V_{SS}, V_{DD}$ | $V_{SS} \sim V_{SS} + 4.0$ | V          |
| Input Voltage        | $V_{IN}$         | $-0.3 \sim V_{DD} + 0.3$   | V          |
| Power Dissipation    | $P_D$ (Note)     | 1430                       | mW         |
| Storage Temperature  | $T_{stg}$        | $-55 \sim 125$             | $^\circ C$ |

(Note) When using the controller under the temperature  $T_a = 25^\circ C$  or higher, reduce the acceptable loss by 14.3mW per  $1^\circ C$ .

**POWER CONSUMPTION TEMPERATURE DROP CURVE** (when substrate is installed)



**RECOMMENDED OPERATING RANGE** ( $V_{SS} = 0V$ )

| CHARACTERISTIC        | SYMBOL    | TEST CONDITION | MIN. | TYP. | MAX.     | UNIT       |
|-----------------------|-----------|----------------|------|------|----------|------------|
| Power Supply Voltage  | $V_{DD}$  | —              | 3.0  | 3.3  | 3.6      | V          |
| Input Voltage         | $V_{IN}$  | —              | 0    | —    | $V_{DD}$ | V          |
| Operation Temperature | $T_{opr}$ | —              | -20  | —    | 70       | $^\circ C$ |



## ELECTRICAL CHARACTERISTICS

## DC CHARACTERISTICS

(Operation conditions :  $V_{DD} = 3.0 \sim 3.6V$ ,  $V_{IN} = 0 \sim V_{DD}$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$ )

| CHARACTERISTIC                         |                       | SYMBOL    | TEST CIR-CUIT | TEST CONDITION    | MIN.                | TYP. | MAX.                | UNIT    | APPLICABLE TERMINALS |      |
|--|-----------------------|-----------|---------------|-------------------|---------------------|------|---------------------|---------|----------------------|------|
| Current Consumption                    |                       | $I_{DD1}$ | —             | NTSC              |                     |      | 180                 | mA      |                      |      |
| High Level Input Voltage               | CMOS Input            | $V_{IH}$  | —             |                   | $V_{DD} \times 0.8$ |      |                     | V       | (*1)                 |      |
|  | Shumitt Trigger Input |           |               |                   |                     |      |                     |         | $V_{DD} \times 0.8$  |      |
| Low Level Input Voltage                | CMOS Input            | $V_{IL}$  | —             |                   |                     |      | $V_{DD} \times 0.2$ | V       | (*1)                 |      |
|  | Shumitt Trigger Input |           |               |                   |                     |      |                     |         | $V_{DD} \times 0.2$  |      |
| Input Current                          | High Level            | $I_{IH}$  | —             | $V_{IN} = V_{DD}$ | -10                 |      | 10                  | $\mu A$ | (*3)                 |      |
|  | Low Level             | $I_{IL}$  |               | $V_{IN} = V_{SS}$ | -10                 |      | 10                  |         |                      |      |
| Output Voltage                         | High Level            | VOH1      | —             | IOH1 = 4mA        | 2.4                 |      |                     | V       | (*4)                 |      |
|  |                       | VOH2      |               | IOH2 = 8mA        | 2.4                 |      |                     |         | (*5)                 |      |
|  | Low Level             | VOL1      |               | IOL1 = 4mA        |                     |      | 0.4                 |         |                      | (*4) |
|  |                       | VOL2      |               | IOL2 = 8mA        |                     |      | 0.4                 |         |                      | (*5) |
| Shumitt Trigger And Hysteresis Voltage |                       | VH        | —             |                   |                     | 0.5  |                     |         | (*2)                 |      |

(\*1) WCK, RDAC7~0, RDAY7~0, RMCKI, RCK, SDA, IICNR, TEST3~0, TIMRST, PWRST

(\*2) WVD, WHD, RHD, RVD, SCL

(\*3) WVD, WHD, WCK, RDAC7~0, RDAY7~0, RMCKI, RCK, RHD, RVD, SCL, SDA, IICNR, TEST3~0, TIMRST, PWRST

(\*4) MOH, WHREF, WIE, WENC, WENY, WRST, WDAC7~0, WDAY7~0, REN, RRST, YS, OSD1, OSD2, RHREF, SDMON, SDA

(\*5) WMCK, RMCK

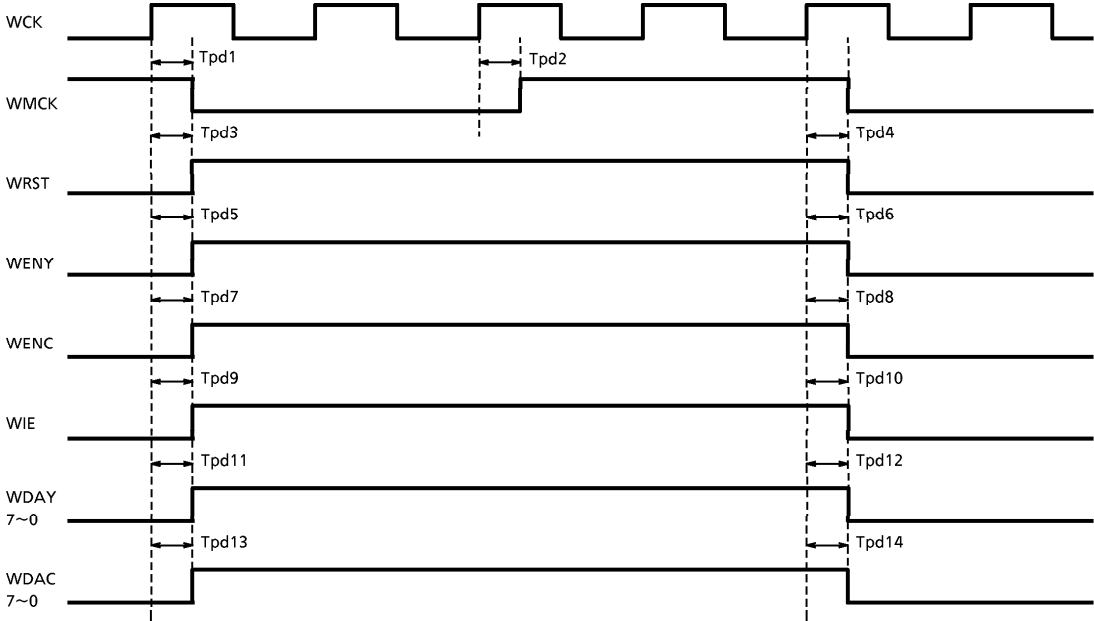
AC CHARACTERISTICS

(Operation conditions :  $V_{DD} = 3.0 \sim 3.6V$ ,  $V_{IN} = 0 \sim V_{DD}$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$ )

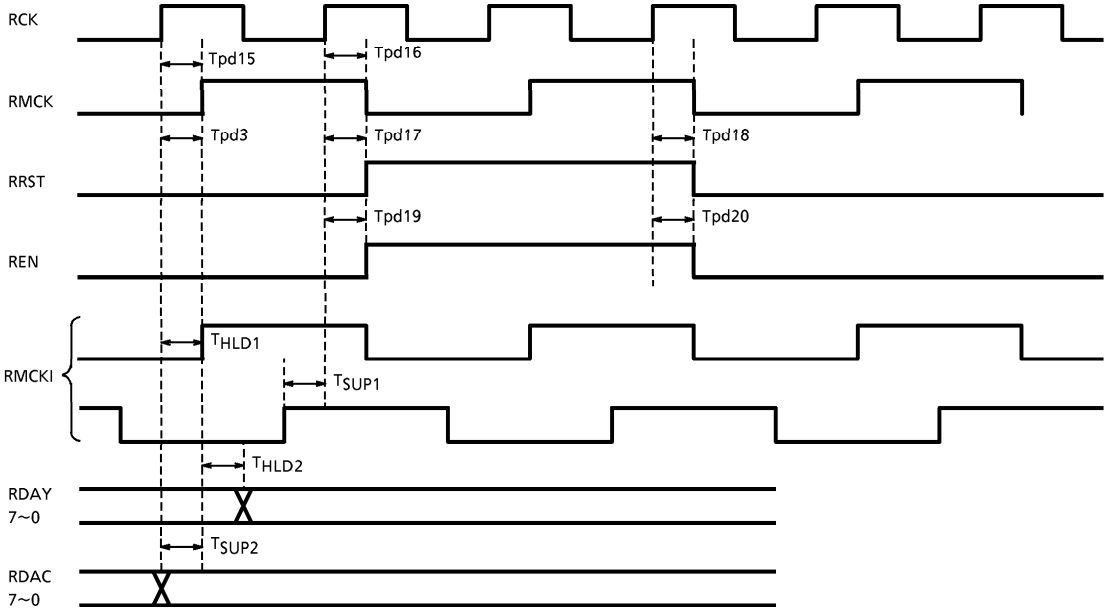
| CHARACTERISTIC                | SYMBOL | TEST CIR-CUIT | TEST CONDITION          | MIN. | TYP. | MAX. | UNIT | REMARKS |
|-------------------------------|--------|---------------|-------------------------|------|------|------|------|---------|
| Operation Frequency Condition |        | —             | NTSC mode               |      | 20   |      | MHz  |         |
| Input Setup Time              | TSUP1  | —             | Operation frequency MHz | 5    | —    | —    | ns   |         |
|                               | TSUP2  |               |                         | 5    | —    | —    |      |         |
| Input Hold Time               | THLD1  | —             | Operation frequency MHz | 3    | —    | —    | ns   |         |
|                               | THLD2  |               |                         | 5    | —    | —    |      |         |
| Output Propagation Delay Time | Tpd1   | —             |                         | 5    | —    | 14   | ns   |         |
|                               | Tpd2   |               |                         | 4    | —    | 11   |      |         |
|                               | Tpd3   |               |                         | 6    | —    | 19   |      |         |
|                               | Tpd4   |               |                         | 6    | —    | 15   |      |         |
|                               | Tpd5   |               |                         | 6    | —    | 19   |      |         |
|                               | Tpd6   |               |                         | 6    | —    | 15   |      |         |
|                               | Tpd7   |               |                         | 6    | —    | 19   |      |         |
|                               | Tpd8   |               |                         | 6    | —    | 15   |      |         |
|                               | Tpd9   |               |                         | 7    | —    | 21   |      |         |
|                               | Tpd10  |               |                         | 6    | —    | 16   |      |         |
|                               | Tpd11  |               |                         | 6    | —    | 18   |      |         |
|                               | Tpd12  |               |                         | 6    | —    | 15   |      |         |
|                               | Tpd13  |               |                         | 6    | —    | 18   |      |         |
|                               | Tpd14  |               |                         | 5    | —    | 15   |      |         |
|                               | Tpd15  |               |                         | 4    | —    | 13   |      |         |
|                               | Tpd16  |               |                         | 4    | —    | 10   |      |         |
|                               | Tpd17  |               |                         | 6    | —    | 18   |      |         |
|                               | Tpd18  |               |                         | 5    | —    | 14   |      |         |
|                               | Tpd19  |               |                         | 6    | —    | 18   |      |         |
|                               | Tpd20  |               |                         | 6    | —    | 13   |      |         |

SETUP-HOLD TIME & OUTPUT DELAY TIME

WRITE



READ



## ADC CHARACTERISTICS

(Operation conditions :  $V_{DD} = 3.3V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$ )

| CHARACTERISTIC                |          | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX.      | UNIT |
|-------------------------------|----------|--------|---------------|----------------|------|------|-----------|------|
| Non-linear Error              |          | ILE    | —             |                |      |      | $\pm 1$   | LSB  |
| Differential Non-linear Error |          | DLE    | —             |                |      |      | $\pm 0.5$ | LSB  |
| Analog Input Voltage          | FULL SCA | VIFS   | —             |                |      | 2.2  |           | V    |
|                               | ZERO SCA | VIZS   | —             |                |      | 1.1  |           |      |

## CLAMPING AND MULTIPLEXER

(Operation conditions :  $V_{DD} = 3.3V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$ )

| CHARACTERISTIC |  | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|----------------|--|--------|---------------|----------------|------|------|------|------|
| Clamping Y     |  |        | —             |                |      | 63   |      | LSB  |
| Clamping C     |  |        | —             |                |      | 136  |      | LSB  |
| Multiplexer    |  |        | —             |                |      | 5    |      | MHz  |

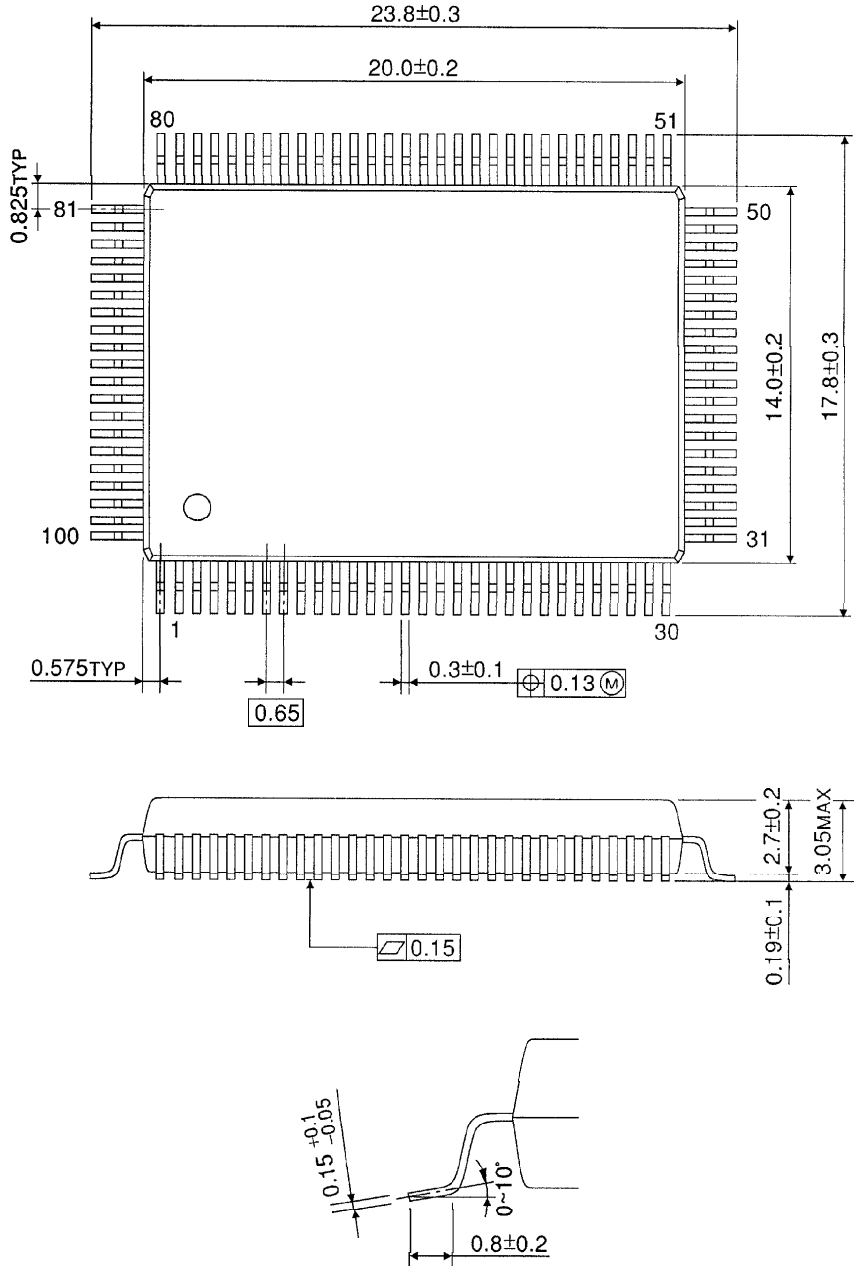
## DAC CHARACTERISTICS

(Operation conditions :  $V_{DD} = 3.3V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$ )

| CHARACTERISTIC                |          | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX.     | UNIT |
|-------------------------------|----------|--------|---------------|----------------|------|------|----------|------|
| Non-linear Error              |          | ILE    | —             |                |      |      | $\pm 1$  | LSB  |
| Differential Non-linear Error |          | DLE    | —             |                |      |      | $\pm 1$  | LSB  |
| Analog Output Voltage         | FULL SCA | VIFS   | —             |                |      |      | $V_{DD}$ | V    |
|                               | ZERO SCA | VIZS   | —             |                | VREF |      |          |      |

PACKAGE DIMENSIONS  
QFP100-P-1420-0.65A

Unit : mm



Weight : 1.6g (Typ.)

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000707EBA

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