December 1995, Rev. E FN7033

730MHz Closed Loop Buffer

The EL2072 is a wide bandwidth, fast settling monolithic buffer built using an advanced complementary bipolar process. This buffer is closed loop to achieve lower output impedance and higher gain accuracy. Designed for closed-loop unity gain, the EL2072 has a 730MHz -3dB bandwidth and 5ns settling to 0.2% while consuming only 15mA of supply current.

The EL2072 is an obvious high-performance solution for video distribution and line-driving applications. With low 15mA supply current and a 70mA output drive, performance in these areas is assured.

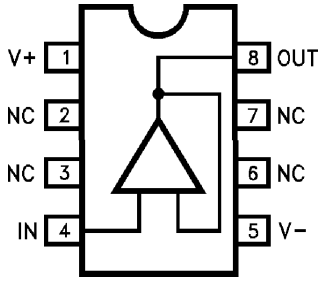
The EL2072's settling to 0.2% in 5ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 730MHz bandwidth and extremely linear phase allow unmatched signal fidelity.

The EL2072 can be used inside an amplifier loop or PLL as its wide bandwidth and fast rise time have minimal effect on loop dynamics.

Elantec products and facilities comply with MIL-I-45028A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

Pinout

EL2072
(8-PIN PDIP SO)
TOP VIEW



Manufactured under U.S. Patent No. 4,893,091

Features

- 730MHz -3dB bandwidth ($0.5V_{PP}$)
- 5ns settling to 0.2%
- V_S = ±5V @ 15mA
- Low distortion: HD2, HD3 of -65dBc at 20MHz
- Overload/short-circuit protected
- Closed-loop, unity gain
- Low cost
- Direct replacement for CLC110

Applications

- Video buffer
- Video distribution
- HDTV buffer
- High-speed A/D buffer
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2072CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL2072CS	-40°C to +85°C	8-Pin SO	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S) . . . . . ±7V
Output Current
Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70mA.

Input Voltage . . . . . ±V_S
Operating Temperature . . . . . -40°C to +85° C

Junction Temperature . . . . . 175°C
Storage Temperature . . . . . -60°C to +150°C
Thermal Resistance . . . . . θ_{JA} = 95°C/W PDIP
. . . . . θ_{JA} = 175°C /W SO
Note: See EL2071/EL2171 for Thermal Impedance curves.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
V_{OS}	Output Offset Voltage		25° C		2.0	8.0	mV
			T_{MIN}			16.0	mV
			T_{MAX}			13.0	mV
TCV_{OS}	Average Offset Voltage Drift		25°C - T_{MAX}		20.0	50.0	µV/°C
			25°C - T_{MIN}		20.0	100.0	
I_B	Input Bias Current		25°C, T_{MAX}		10.0	50.0	µA
			T_{MIN}			100.0	µA
TCI_B	Average Input Bias Current Drift		25°C - T_{MAX}		200.0	300.0	nA/°C
			25°C - T_{MIN}		200.0	700.0	
A_V	Small Signal Gain	R_L = 100Ω	25° C	0.96	0.98		V/V
			T_{MIN}, T_{MAX}	0.95			V/V
ILIN	Integral End Point linearity	±2V F.S.	25° C		0.2	0.4	%F.S.
			T_{MIN}			0.8	%F.S.
			T_{MAX}			0.3	%F.S.
PSRR	Power Supply Rejection Ratio		All	45.0	65.0		dB
I_S	Supply Current—Quiescent	No Load	All		15.0	20.0	mA
R_{IN}	Input Resistance		25° C	100.0	160.0		kΩ
			T_{MIN}	50.0			kΩ
			T_{MAX}	200.0			kΩ
C_{IN}	Input Capacitance		25° C		1.6	2.2	pF
			T_{MIN}, T_{MAX}			2.5	pF
R_{OUT}	Output Impedance (DC)		25° C		2.0	3.0	Ω
			T_{MIN}, T_{MAX}			3.5	Ω
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		mA
			T_{MIN}	45.0			mA
V_{OUT}	Output Voltage Swing	R_L = 100Ω	25°C, T_{MAX}	±3.2	±4.0		V
			T_{MIN}	±3.0			V

AC Electrical Specifications

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

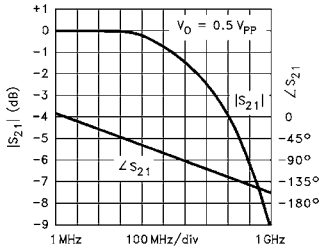
PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE							
SSBW	-3dB Bandwidth (V_{OUT} < 0.5V_{PP})		25°C	400.0	730.0		MHz
			T_{MIN}	400.0			MHz
			T_{MAX}	300.0			MHz
LSBW	-3dB Bandwidth (V_{OUT} = 5.0V_{PP})		25°C	55.0	90.0		MHz
			T_{MIN}, T_{MAX}	50.0			MHz
GAIN FLATNESS							
GFPL	Peaking V_{OUT} < 0.5V_{PP}	< 200MHz	25°C		0.0	0.5	dB
			T_{MAX}			0.6	dB
			T_{MIN}			0.8	dB
GFR	Rolloff V_{OUT} < 0.5V_{PP}	< 200MHz	25°C		0.0	0.8	dB
			T_{MIN}			1.0	dB
			T_{MAX}			1.2	dB
GDL	Group Delay	< 200MHz	25°C , T_{MIN}		0.75	1.0	ns
			T_{MAX}			1.2	ns
LPD	Linear Phase Deviation V_{OUT} < 0.5V_{PP}	< 200MHz	25°C , T_{MIN}		0.7	1.5	°
			T_{MAX}			2.0	°
TIME-DOMAIN RESPONSE							
TR1, TF1	Rise Time, Fall Time Input Signal Rise/Fall = 300ps	0.5V Step	25°C , T_{MIN}		0.4	1.0	ns
			T_{MAX}			1.4	ns
TR2, TF2	Rise Time, Fall Time Input Signal Rise/Fall ð 1ns	5.0V Step	25°C		4.5	7.5	ns
			T_{MIN}, T_{MAX}			8.5	ns
TS1	Settling Time to 0.2% Input Signal Rise/Fall ð 1ns	2.0V Step	All		5.0	10.0	ns
OS	Overshoot Input Signal Rise/Fall = 300ps	0.5V Step	25°C		0.0	10.0	%
			T_{MIN}, T_{MAX}			15.0	%
SR	Slew Rate		25°C	500.0	800.0		V/µs
			T_{MIN}, T_{MAX}	450.0			V/µs
DISTORTION							
HD2	2nd Harmonic Distortion at 20MHz	2V_{PP}	25°C		-55.0	-50.0	dBc
			T_{MIN}			-48.0	dBc
			T_{MAX}			-55.0	dBc
HD2A	2nd Harmonic Distortion at 50MHz	2V_{PP}	25°C , T_{MAX}		-50.0	-45.0	dBc
			T_{MIN}			-40.0	dBc
HD3	3rd Harmonic Distortion at 20MHz	2V_{PP}	25°C		-65.0	-55.0	dBc
			T_{MIN}, T_{MAX}			-55.0	dBc
HD3A	3rd Harmonic Distortion at 50MHz	2V_{PP}	25°C , T_{MIN}		-60.0	-50.0	dBc
			T_{MAX}			-45.0	dBc

AC Electrical Specifications V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified **(Continued)**

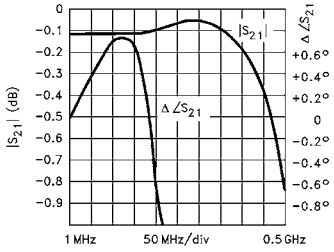
PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
EQUIVALENT INPUT NOISE							
NF	Noise Floor > 100kHz		25° C, T_{MIN}		-158.0	-155.0	dBm (1Hz)
			T_{MAX}			-154.0	dBm (1Hz)
INV	Integrated Noise 100kHz to 200MHz		25° C, T_{MIN}		40.0	57.0	µV
			T_{MAX}			63.0	µV

Typical Performance Curves

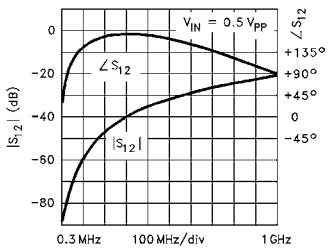
Forward Gain and Phase



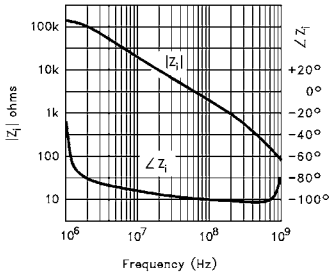
Gain Flatness & Deviation from Linear Phase



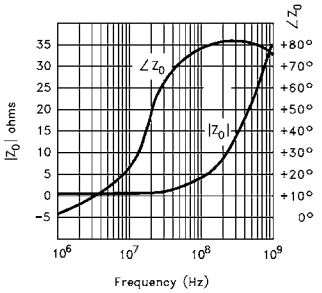
Reverse Gain and phase



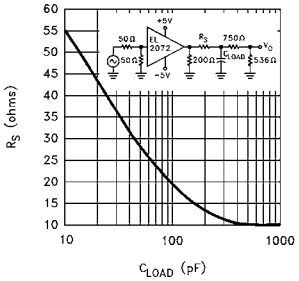
Input Impedance



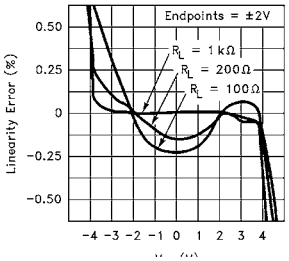
Output Impedance



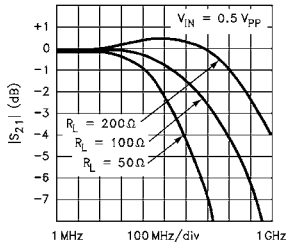
Recommended R_S vs Load Capacitance



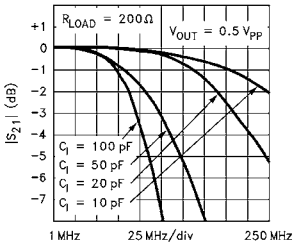
Integral Linearity Error



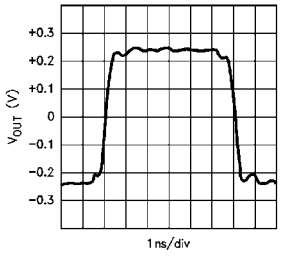
Frequency Response vs R_{LOAD}



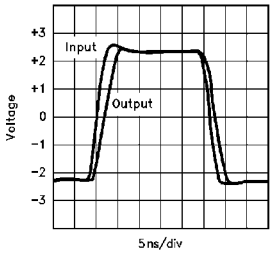
$|S_{21}|$ vs C_{LOAD} with Recommended R_S



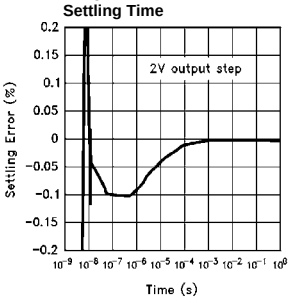
Small Signal Pulse Response



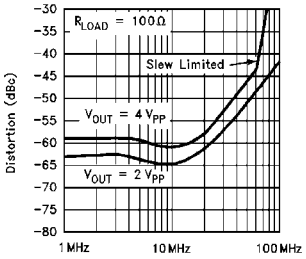
Large Signal Pulse Response



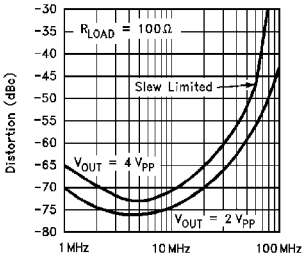
Long-Term Settling Time



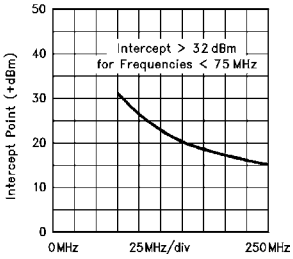
2nd Harmonic Distortion



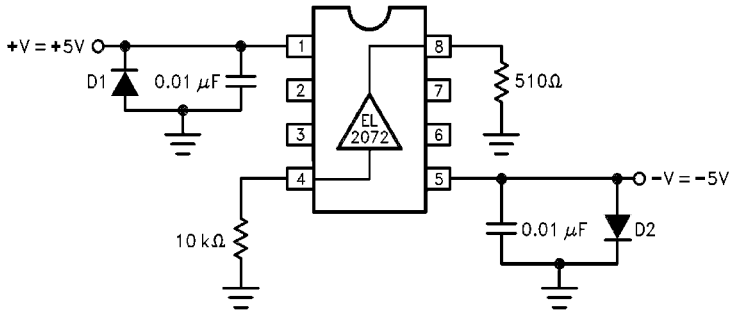
3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



Burn-In Circuit



Printed Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. This is especially important for the EL2072, which has a typical bandwidth of 730MHz. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. A closely-placed 0.01µF ceramic capacitor between each supply pin and the ground plane is usually sufficient decoupling.

Pins 2, 3, 6, and 7 should be connected to the ground-plane to minimize capacitive feedthrough, and all input and output traces should be laid out as transmission lines and terminated as close to the EL2072 package as possible.

Increasing capacitance on the output of the EL2072 will add phase shift, decreasing phase margin and increasing frequency-response peaking. A small series resistor before the capacitance decouples this effect, and should be used for large capacitance values. Please refer to the graphs for the appropriate resistor value to be used.