December 1995, Rev. E FN7032

150MHz Current Feedback Amplifier

The EL2071 and EL2171 are wide bandwidth, fast settling monolithic amplifiers built using an advanced complementary bipolar process. The EL2071 has a disable/enable feature which allows power down and analog multiplexing. These amplifiers use current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±7 to ±50, the EL2071 and EL2171 have a 150MHz - 3dB bandwidth (A_V = +20), and 2.5ns rise/fall time, while consuming only 15mA of supply current. The EL2071 consumes only 1.5mA when disabled.

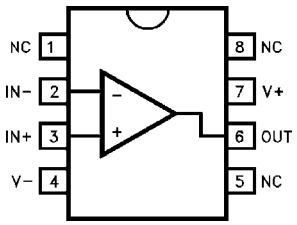
The wide 150MHz bandwidth and extremely linear phase (0.2dB deviation from linear at 50MHz) allow superior signal fidelity. These features make the EL2071 and EL2171 especially suited for many digital communication system applications.

The EL2071's and EL2171's settling to 0.1% in 10ns and ability to drive capacitive loads make them ideal in flash A/D applications. D/A systems can also benefit from the EL2071 and EL2171, especially if linearity and drive levels are important.

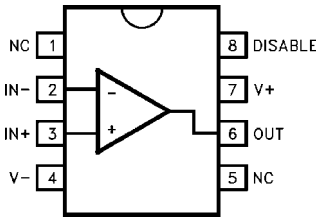
Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

Pinout

EL2171
(8-PIN PDIP, SO)
TOP VIEW



EL2071
(8-PIN PDIP, SO)
TOP VIEW



Manufactured under U.S. Patent No. 4,893,091

Features

- 150MHz - 3dB bandwidth, A_V = 20
- 10ns settling to 0.1%
- V_S = ±5V @ 15mA
- 2.5ns rise/fall times (2V step)
- Overload/short-circuit protected
- ±7 to ±50 closed-loop gain range
- Low cost
- EL2171 is direct replacement for CLC401
- Disable capability on EL2071

Applications

- Line drivers
- DC-coupled log amplifiers
- High-speed modems, radios
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications
- Analog multiplexing (using disable—EL2071)
- Power down mode (using disable—EL2071)

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2171CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL2171CS	-40°C to +85°C	8-Pin SO	MDP0027
EL2071CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL2071CS	-40°C to +85°C	8-Pin SO	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S) . . . . . ±7V
(Output Current Output is short-circuit protected to ground, however,maximum reliability is obtained if I_{OUT} does not exceed 70mA.)

Common Mode Input Voltage . . . . . ±V_S
Differential Input Voltage 5V
Power Dissipation . . . . . See Curves

Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature
Ceramic Packages . . . . . 175°C
Plastic Packages . . . . . 150°C
Storage Temperature . . . . . -60°C to +15 0°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

V_S = ±5V, R_L = 100Ω, unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		25°C		3	6	mV
			T_{MIN}, T_{MAX}			10	mV
TC V_{OS}	Average Offset Voltage Drift	(Note 1)	All		20	50	µV/°C
$+I_{IN}$	+Input Current		25°C , T_{MAX}		10	20	µA
			T_{MIN}			36	µA
TC ($+I_{IN}$)	Average +Input Current Drift	(Note 1)	All		100	200	nA/° C
$-I_{IN}$	-Input Current		25°C		10	30	µA
			T_{MIN}			46	µA
			T_{MAX}			40	µA
TC ($-I_{IN}$)	Average -Input Current Drift	(Note 1)	All		100	200	nA/° C
PSRR	Power Supply Rejection Ratio	(Note 2)	All	50	55		dB
CMRR	Common-Mode Rejection Ratio		All	40	50		dB
I_S	Supply Current—Quiescent	No Load	All		15	21	mA
I_{SOFF}	Supply Current—Disabled	EL2071 (Note 3)	All		1.5	3.0	mA
$+R_{IN}$	+Input Resistance		25°C , T_{MAX}	100	200		kΩ
			T_{MIN}	50			kΩ
C_{IN}	Input Capacitance		All		0.5	2.5	pF
R_{OUT}	Output Resistance (DC)		All		0.2	0.3	Ω
R_{OUTD}	Output Resistance (DC)	EL2071 Disabled	All	100	200		kΩ
C_{OUTD}	Output Capacitance (DC)	EL2071 Disabled	All		0.5	2.0	pF
CMIR	Common-Mode Input Range	(Note 4)	25°C , T_{MAX}	±2.5	±2.8		V
			T_{MIN}	±2			V
I_{OUT}	Output Current		25°C , T_{MAX}	50	70		mA
			T_{MIN}	35			mA
V_{OUT}	Output Voltage Swing	No Load	25°C , T_{MAX}	3.2	3.5		V
			T_{MIN}	3			V

Open-Loop DC Electrical Specifications

V_S = ±5V, R_L = 100Ω, unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
V_{OUTL}	Output Voltage Swing	R_L = 100Ω	25°C	3.2	3.4		V
R_{OL}	Transimpedance		25°C	250	1000		V/mA
I_{LOGIC}	Pin 8 Current @+5V	EL2071	All		500	750	µA
V_{DIS}	Minimum Pin 8 V to Disable	EL2071	25°C	4.3			
			T_{MIN}	4.0			V
			T_{MAX}	4.6			
V_{EN}	Maximum Pin 8 V to Enable	EL2071	All			0.7	V
I_{DIS}	Minimum Pin 8 I to Disable	EL2071	All	750			µA
I_{EN}	Maximum Pin 8 I to Enable	EL2071	All			35	µA

NOTES:

1. Measured from T_{MIN} to T_{MAX}.
2. PSRR is measured at V_S = ±4.5V and V_S = ±5.5V. Both supplies are changed simultaneously.
3. Supply current when disabled is measured at the negative supply.
4. Common-Mode Input Range for Rated Performance.

Closed-Loop AC Electrical Specifications

V_S = ±5V, R_F = 1.5kΩ, A_V = +20, R_L = 100Ω unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE							
SSBW	-3dB Bandwidth (V_{OUT} < 2.0 V_{PP})		25° C	100	150		MHz
			T_{MIN}	100			MHZ
			T_{MAX}	70			MHz
LSBW	-3dB Bandwidth (V_{OUT} < 5.0 V_{PP})		25°C, T_{MIN}	65	100		MHz
			T_{MAX}	55			MHz
GAIN FLATNESS							
GFPL	Peaking V_{OUT} < 2.0 V_{PP}	< 25MHz	25° C		0.0	0.1	dB
			T_{MIN}, T_{MAX}			0.1	dB
GFPH	Peaking V_{OUT} < 2.0 V_{PP}	> 25MHz	25° C		0.0	0.2	dB
			T_{MIN}, T_{MAX}			0.2	dB
GFR	Rolloff V_{OUT} < 2.0 V_{PP}	< 50MHz	25° C		0.2	1.0	dB
			T_{MIN}			1.0	dB
			T_{MAX}			1.3	dB
LPD	Linear Phase Deviation V_{OUT} < 2.0 V_{PP}	< 50MHz	25°C, T_{MIN}		0.2	1.0	°
			T_{MAX}			1.5	°
TIME-DOMAIN RESPONSE							
t_{R1}, t_{F1}	Rise Time, Fall Time	2.0V Step	25°C, T_{MIN}		2.5	3.5	ns
			T_{MAX}			5	ns
t_{R2}, t_{F2}	Rise Time, Fall Time	5.0V Step	25°C, T_{MIN}		5	7	ns
			T_{MAX}			8	ns
t_S	Settling Time to 0.1%	2.0V Step	All		10	15	ns

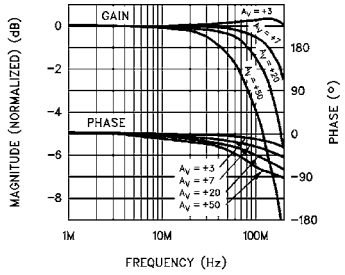
Closed-Loop AC Electrical Specifications

V_S = ±5V, R_F = 1.5kΩ, A_V = +20, R_L = 100Ω unless otherwise specified **(Continued)**

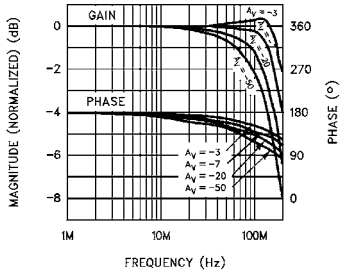
PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
OS	Overshoot	2.0V Step	All		0	10	%
SR	Slew Rate		25°C, T_{MIN}	800	1200		V/µs
			T_{MAX}	700			V/µs
DISTORTION							
HD2	2nd Harmonic Distortion @20MHz	$2V_{PP}$	25° C		-45	-35	dBc
			T_{MIN}, T_{MAX}			-35	dBc
HD3	3rd Harmonic Distortion @20MHz	$2V_{PP}$	25° C		-60	-50	dBc
			T_{MIN}			-50	dBc
			T_{MAX}			-45	dBc
EQUIVALENT INPUT NOISE							
NF	Noise Floor >100kHz		25° C		-158	-155	dBm (1Hz)
			T_{MIN}			-155	dBm (1Hz)
			T_{MAX}			-154	dBm (1Hz)
INV	Integrated Noise 100kHz to 200MHz		25° C		35	50	µV
			T_{MIN}			50	µV
			T_{MAX}			55	µV
DISABLE/ENABLE PERFORMANCE—EL2071C							
T_{OFF}	V_{OUT} = 2 V_{PP} Disable Time to >40dB	20MHz	All		70	200	ns
T_{ON}	Enable Time		All		40	100	ns
ISO	Off Isolation	20MHz	All	50	55		dB

Typical Performance Curves

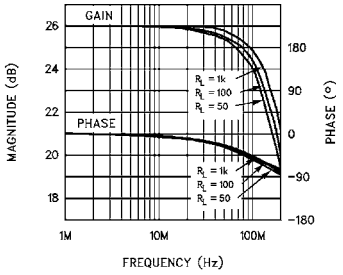
Non-Inverting Frequency Response



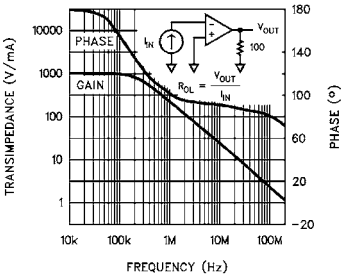
Inverting Frequency Response



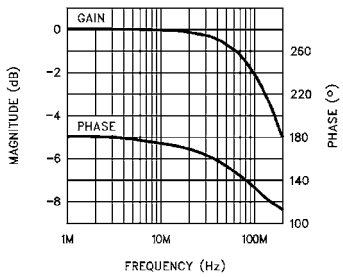
Frequency Response for Various R_Ls



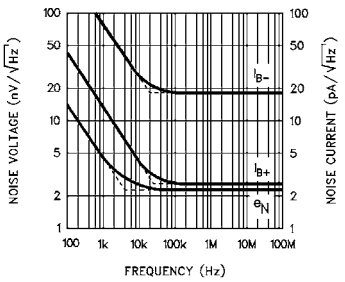
Open-Loop Transimpedance Gain and Phase



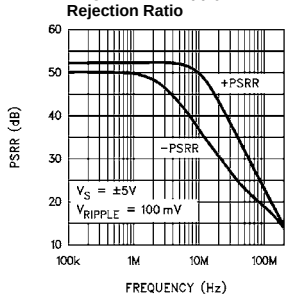
Frequency Response, A_V = -1, R_F = 2.5kΩ



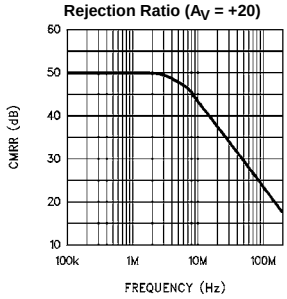
Equivalent Input Noise



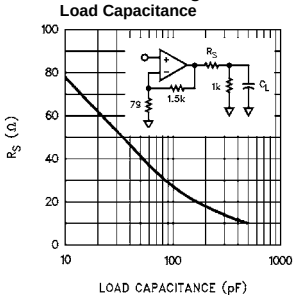
Single Power Supply Rejection Ratio



Common Mode Rejection Ratio (A_V = +20)

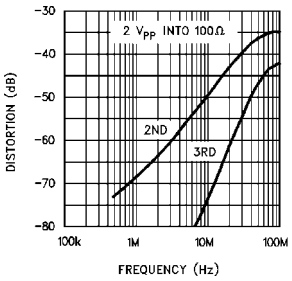


Recommended R_S vs Load Capacitance

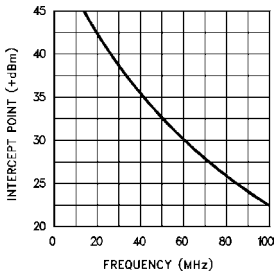


Typical Performance Curves (Continued)

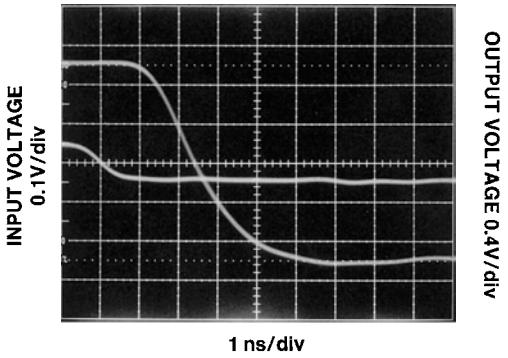
2nd and 3rd Harmonic Distortion



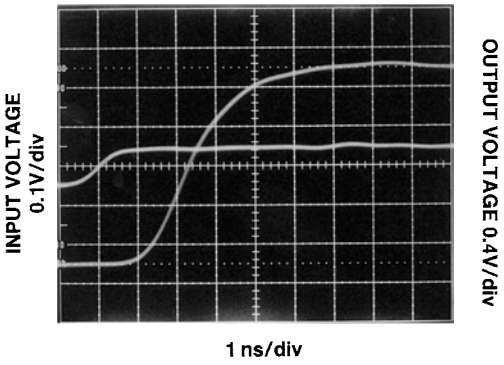
2-Tone 3rd Order Intermodulation Intercept



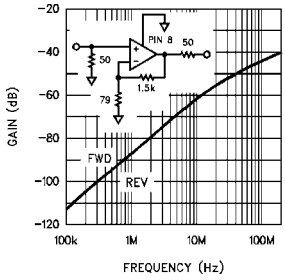
Pulse Response A_V = +20



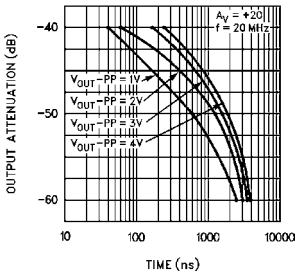
Pulse Response A_V = +20



Forward and Reverse Gain during Disable—EL2071

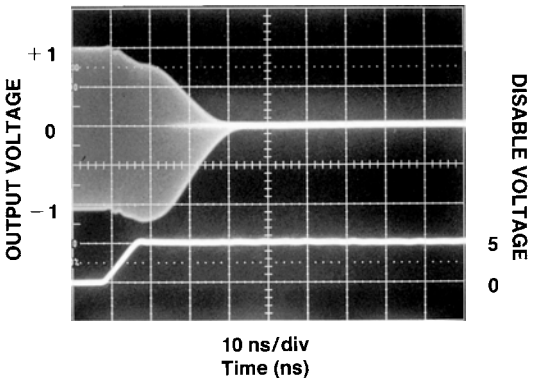


Disabled Attenuation vs Time for Various Output Levels—EL2071

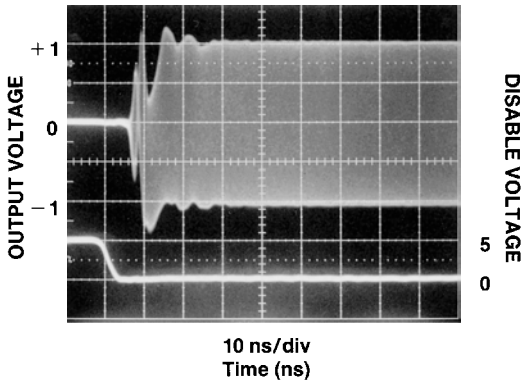


Typical Performance Curves (Continued)

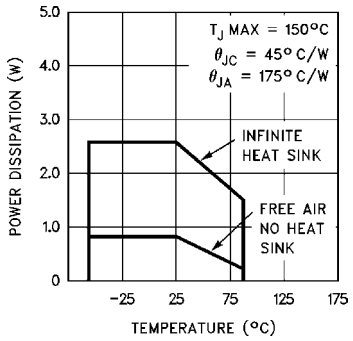
Disable Response—EL2071



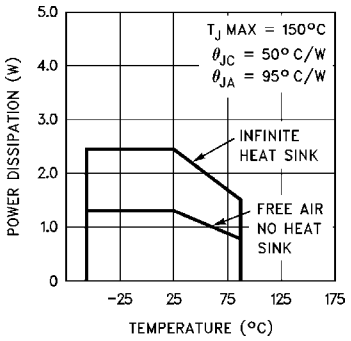
Enable Response—EL2071



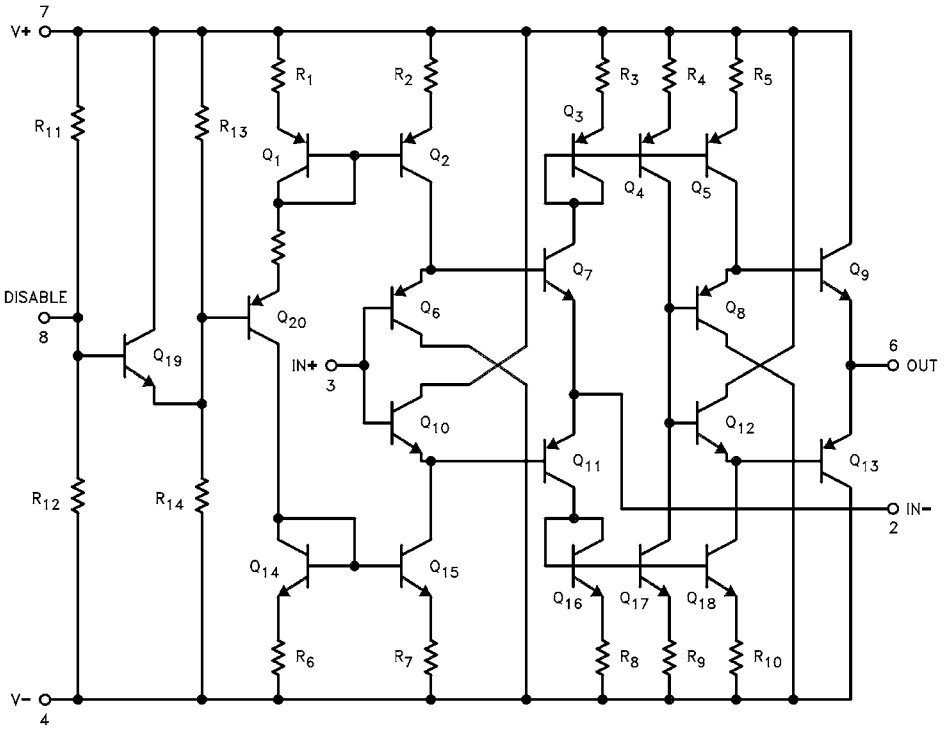
8-Pin SO
Maximum Power Dissipation
vs Ambient Temperature



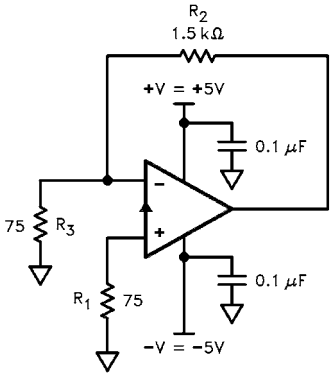
8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



Equivalent Circuit



Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL2071/EL2171 have a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2071/EL2171 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL2071/EL2171 [$V_{OUT} = (R_{OL}) * (-I_{IN})$]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1.The voltage across the inputs is approximately 0V.

2.The current into the inputs is approximately 0mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2071/EL2171. The nominal value for the feedback resistor is 1.5kΩ, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower -3dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Capacitive Feedback

The EL2071/EL2171 rely on their feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

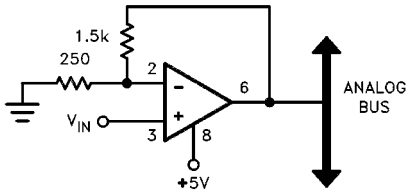
Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2071/EL2171 allow a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation for EL2071

The EL2071 has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to ground. When the voltage at pin 8 is brought to within 0.4V of pin 7 (V_S+), the EL2071 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced to less than 2.2.mA. There are internal resistors which limit the current at pin 8 to a safe level (~ ±500µA) if pin 8 is shorted to either supply.

Typically, analog and digital circuits should have separate power supplies. This usually leads to slight differences between the power supply voltages. The EL2071's disable feature is dependent on the voltage at pins 8 and 7. Therefore, to operate the disable feature of the EL2071 dependably over temperature, it is recommended that the logic circuitry which drives pin 8 of the EL2071 operate from the same +5V supply as the EL2071 to avoid voltage differences between the digital and analog power supplies. Since V_{DIS} is temperature dependent, it is recommended that 5V CMOS logic (with a V_{OH} > 4.6V sourcing > 750µA over temperature) be used to drive the disable pin of the EL2071.

When disabled, (as well as in enabled mode), care must be taken to prevent a differential voltage between the + and - inputs greater than 5.0V. For example, in the figure below, the EL2071 is connected in a gain of +7 configuration and is disabled while the analog bus is driven externally to +5V. Pin 2 is consequently at +0.71V, and if V_{IN} is driven to -5V, then 5.71V appears between pins 3 and 2. Internally, this voltage appears across a forward biased V_{BE} in series with a reverse biased V_{BE} and is past the threshold for zenering the reverse biased V_{BE}. In a typical application, a 50Ω or 75Ω terminating resistor from pin 3 to ground will prevent pin 3 from approaching -5V.

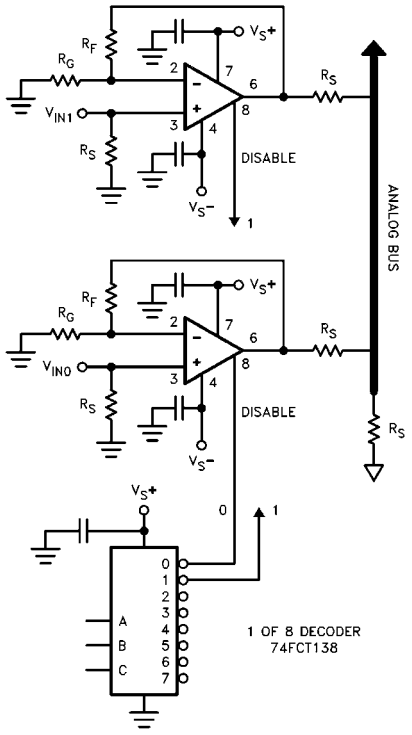


Using the EL2071 as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs in common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown. The series resistance at each output helps to further increase isolation between amplifiers.

When the EL2071 is disabled, the DC output impedance is > 100kΩ in parallel with 2pF capacitance.

To operate properly, the decoder that is used must have a V_{OH} > (V_S+) - 0.4V with I_{OH} = 750µA, and should be connected to the same power supply as the EL2071.



EL2071 Macromodel

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* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:   +input
*                |    -input
*                |    |    +Vsupply
*                |    |    |    -Vsupply
*                |    |    |    |    output
*                |    |    |    |    |
.subckt M2071   3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 2
l1 11 12 1nH
iinp 3 0 10µA
iinm 2 0 10µA
*
* Slew Rate Limiting
*
*h1 13 0 vis 1K
h1 13 0 vis 600
r2 13 14 100
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
e2 30 0 14 0 0.001
13 30 17 1.0µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 1Meg
cdp 18 0 0.88pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
```

EL2071 Macromodel (Continued)

```
ivos 0 23 3mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 316
r10 25 23 562
r11 26 23 562
*
* Models
*
.model qn npn (is=5e-15 bf=500 tf=0.05nS)
.model qp pnp (is=5e-15 bf=500 tf=0.05nS)
.model dclamp d(is=1e-30 ibv=1pA bv=3.5  n=4)
.ends
```